

## P-Channel 200V (D-S) MOSFET

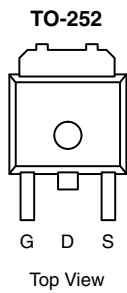
PRODUCT SUMMARY		
V <sub>DS</sub> (V)	-200	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = -10 V	2.0
Q <sub>g</sub> max. (nC)	29	
Q <sub>gs</sub> (nC)	5.4	
Q <sub>gd</sub> (nC)	15	
Configuration	Single	

### FEATURES

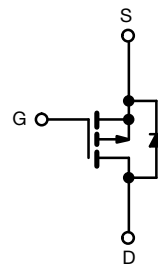
- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available



Drain Connected to Tab



P-Channel MOSFET

VBsemi @6688

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	-200	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at -10 V	T <sub>C</sub> = 25 °C	-3.6
		T <sub>C</sub> = 100 °C	-2.5
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	-12	A
Linear Derating Factor		0.59	W/°C
Linear Derating Factor (PCB mount) <sup>e</sup>		0.025	
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	500	mJ
Avalanche Current <sup>a</sup>	I <sub>AR</sub>	-6.4	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	7.4	mJ
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	74
Maximum Power Dissipation (PCB mount) <sup>e</sup>		T <sub>A</sub> = 25 °C	3.0
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	-5.0	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s	300	

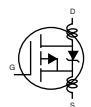

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = -50 V, starting T<sub>J</sub> = 25 °C, L = 17 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = -6.5 A (see fig. 12).
- I<sub>SD</sub> ≤ -6.5 A, di/dt ≤ 120 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

**Note**

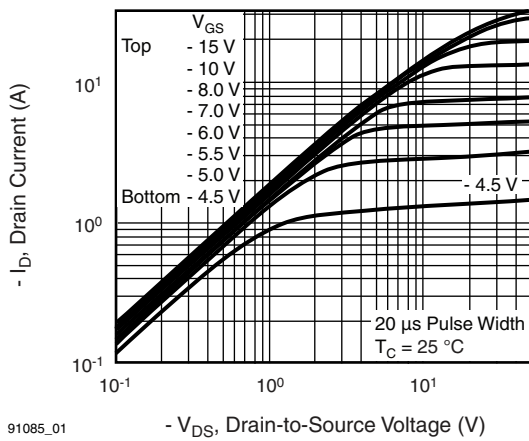
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = -250\ \mu\text{A}$	-200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\ \text{mA}$	-	-0.24	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.5	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\ \text{V}$	-	-	$\pm 10$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -200\ \text{V}, V_{GS} = 0\ \text{V}$	-	-	-100	$\mu\text{A}$
		$V_{DS} = -160\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	-	-	-500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -1.0\ \text{A}^b$	-	2.00	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\ \text{V}, I_D = -1.0\ \text{A}^b$	2.8	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\ \text{V}, V_{DS} = -25\ \text{V}, f = 1.0\ \text{MHz}$ , see fig. 5	-	700	-	pF
Output Capacitance	$C_{oss}$		-	200	-	
Reverse Transfer Capacitance	$C_{rss}$		-	40	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\ \text{V}, I_D = -3.5\ \text{A}, V_{DS} = -160\ \text{V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	29	nC
Gate-Source Charge	$Q_{gs}$		-	-	5.4	
Gate-Drain Charge	$Q_{gd}$		-	-	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100\ \text{V}, I_D = -3.5\ \text{A}, R_g = 12\ \Omega, R_D = 15\ \Omega$ , see fig. 10 <sup>b</sup>	-	12	-	ns
Rise Time	$t_r$		-	27	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28	-	
Fall Time	$t_f$		-	24	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
Gate Input Resistance	$R_g$	$f = 1\ \text{MHz}$ , open drain	0.6	-	3.7	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	-3 .5	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	-6	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -3.5\ \text{A}, V_{GS} = 0\ \text{V}^b$	-	-	-6.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -3.5\ \text{A}, dI/dt = 100\ \text{A}/\mu\text{s}^b$	-	200	300	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	1.9	2.9	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

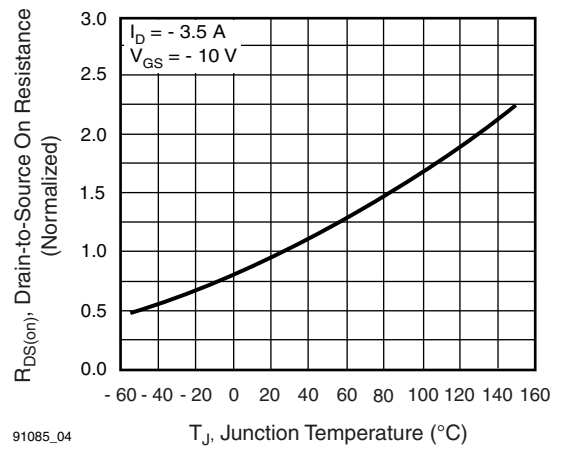
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\ \%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



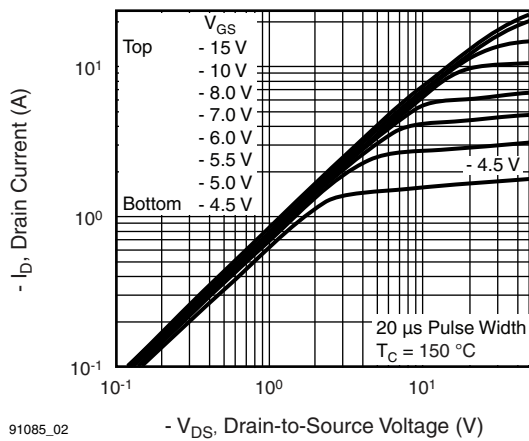
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**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



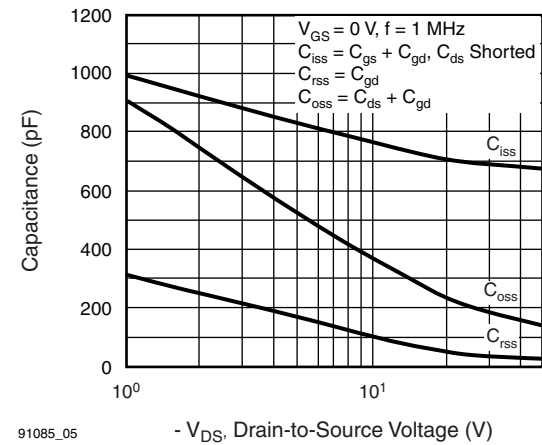
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**Fig. 4 - Normalized On-Resistance vs. Temperature**



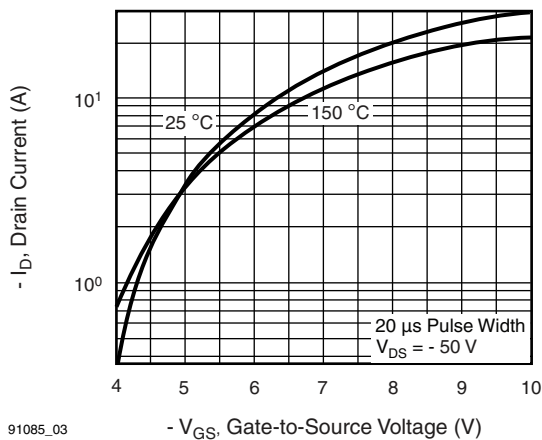
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**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



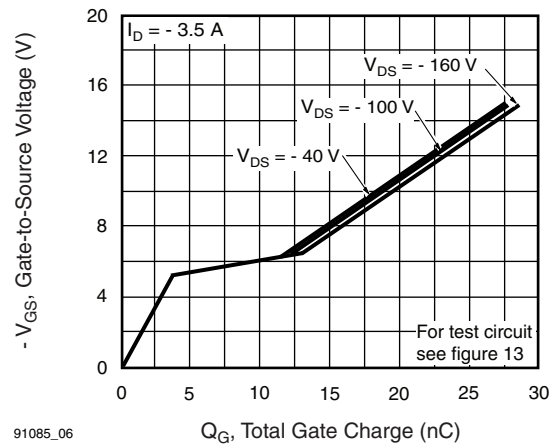
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**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



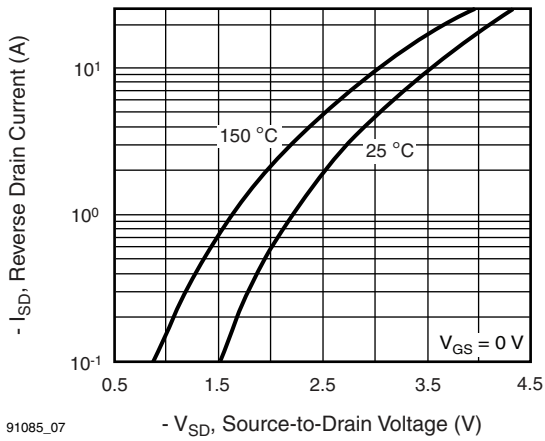
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**Fig. 3 - Typical Transfer Characteristics**



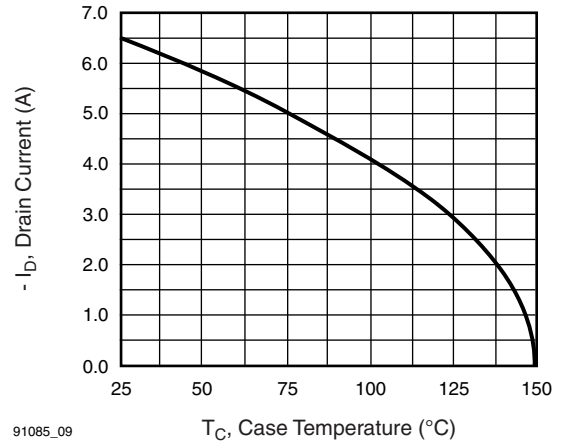
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**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



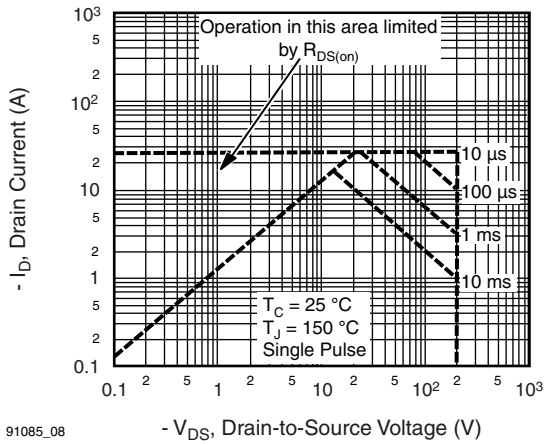
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



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Fig. 9 - Maximum Drain Current vs. Case Temperature



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Fig. 8 - Maximum Safe Operating Area

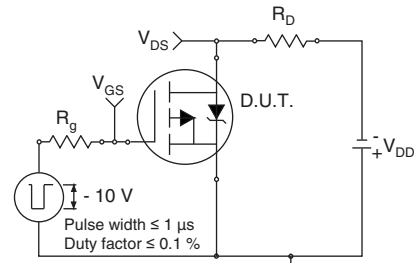


Fig. 10a - Switching Time Test Circuit

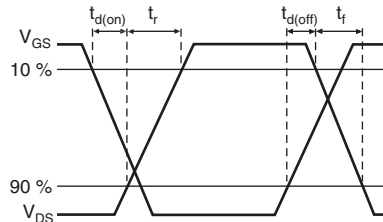
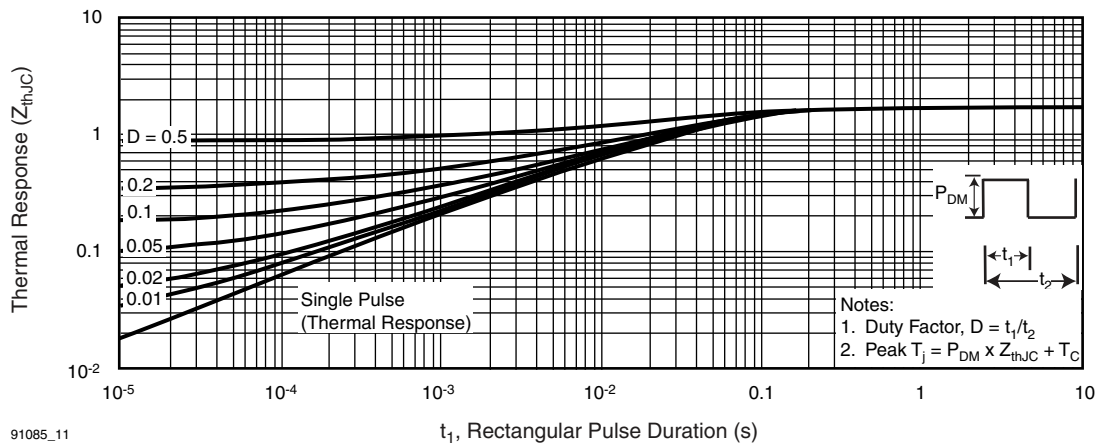


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

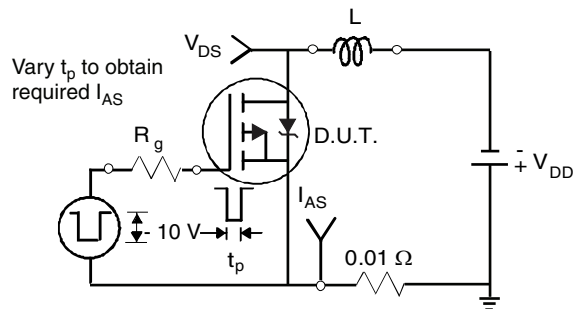


Fig. 12a - Unclamped Inductive Test Circuit

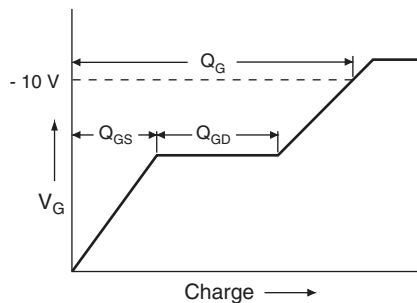


Fig. 13a - Basic Gate Charge Waveform

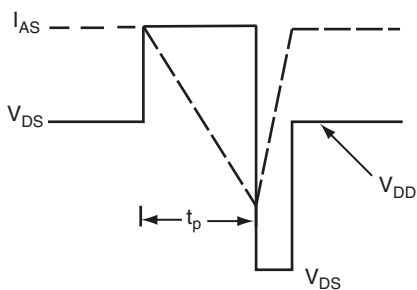


Fig. 12b - Unclamped Inductive Waveforms

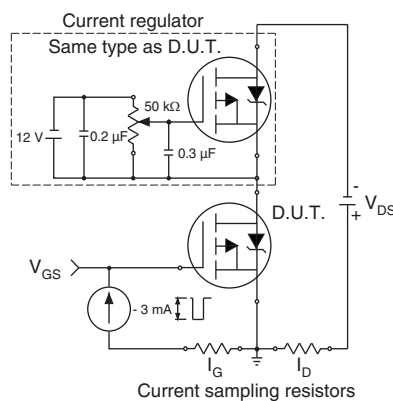


Fig. 13b - Gate Charge Test Circuit

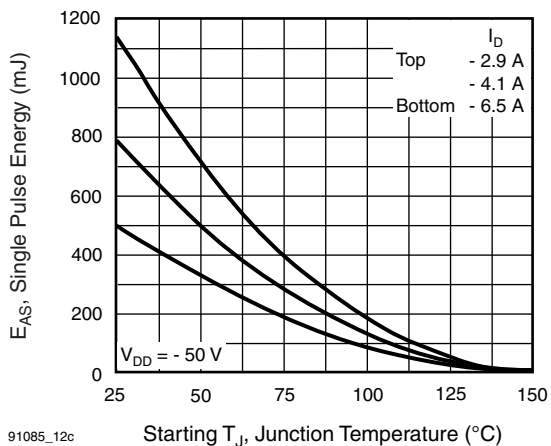
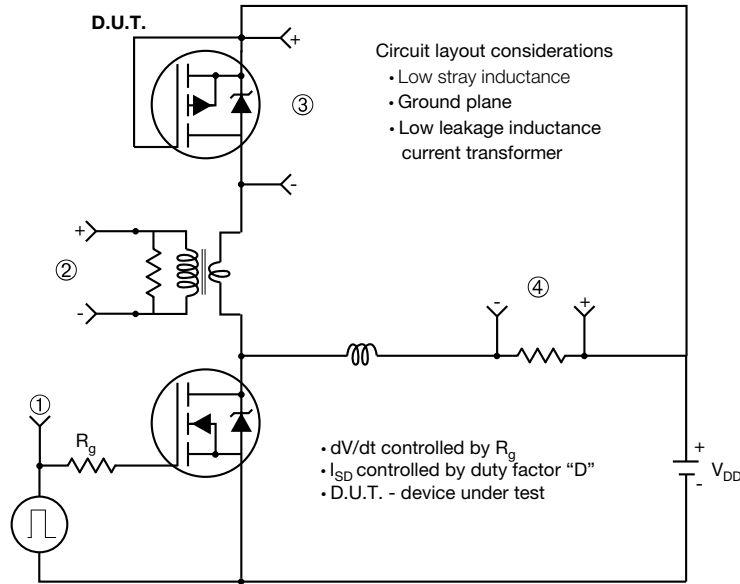
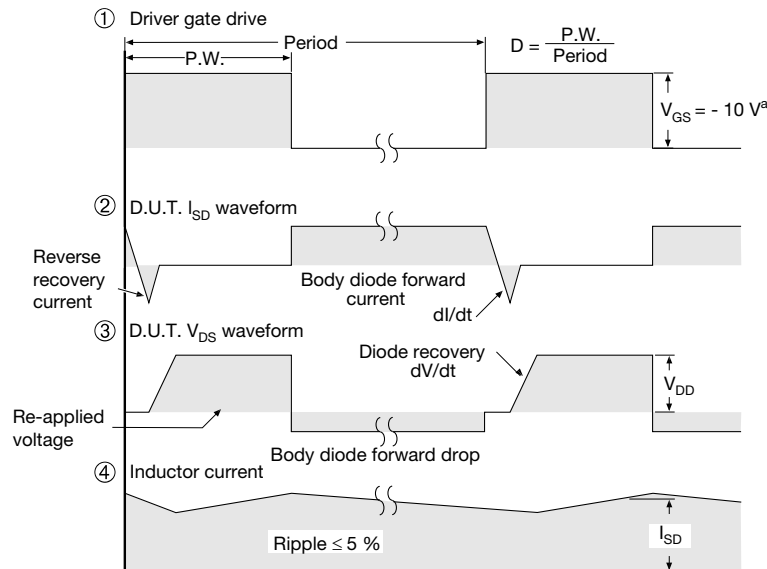


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

**Peak Diode Recovery dV/dt Test Circuit**



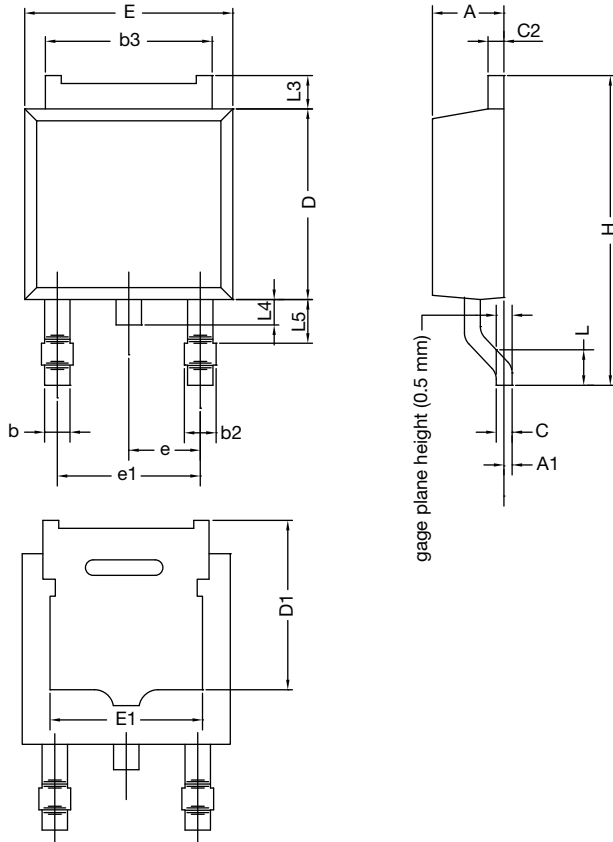
**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 14 - For P-Channel**

## TO-252AA CASE OUTLINE

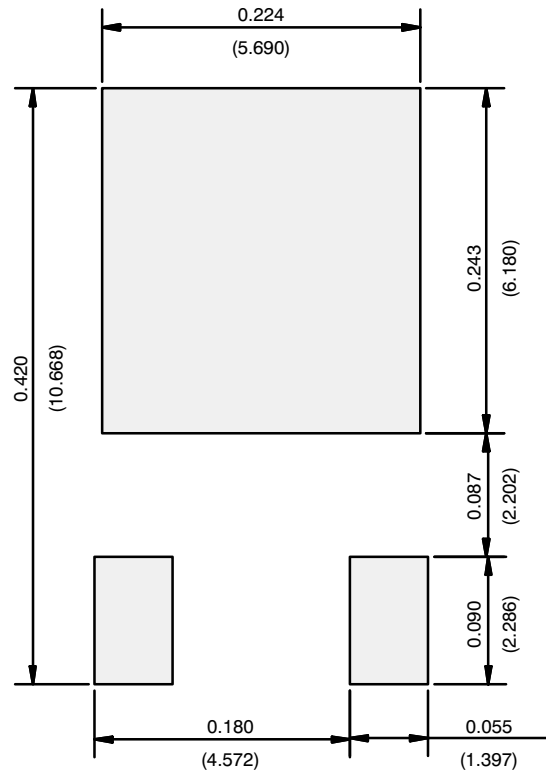


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

**Note**

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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