

## N-Channel 100-V (D-S) MOSFET

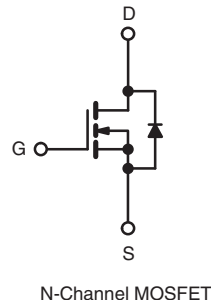
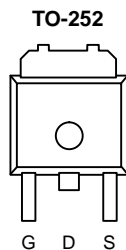
PRODUCT SUMMARY		
$V_{DS}$ (V)	100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.20
$Q_g$ (Max.) (nC)	16	
$Q_{gs}$ (nC)	4.4	
$Q_{gd}$ (nC)	7.7	
Configuration	Single	

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling



**RoHS\***  
Available  
**HALOGEN**  
**FREE**  
Available

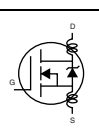



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	100	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	12	A
		$T_C = 100\text{ }^\circ\text{C}$	7.5	
Pulsed Drain Current <sup>a</sup>		37	W/°C	
Linear Derating Factor		0.40		
Linear Derating Factor (PCB Mount)		0.025		
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	200	mJ	
Avalanche Currenta	$I_{AR}$	9.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	6.0	mJ	
Maximum Power Dissipation		$T_C = 25\text{ }^\circ\text{C}$	60	W
		$T_A = 25\text{ }^\circ\text{C}$	3.7	
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)	For 10 s	300 <sup>d</sup>		

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3.5\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 9.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$ ,  $dI/dt \leq 110\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .

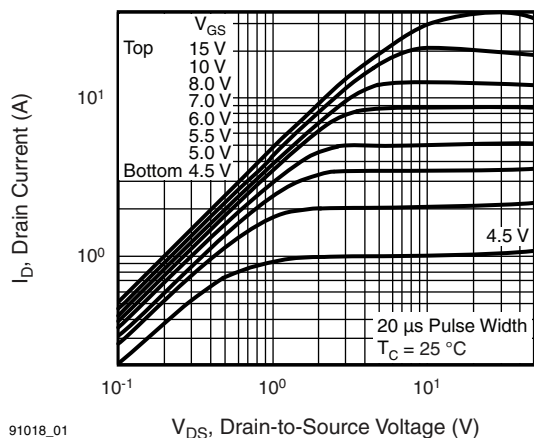
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	40	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.5	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.5	-	3.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 5.5\text{ A}^b$	-	0.20	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 5.5\text{ A}^b$		2.7	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	360	-	pF
Output Capacitance	$C_{oss}$			-	150	-	
Reverse Transfer Capacitance	$C_{riss}$			-	34	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	16	nC
Gate-Source Charge	$Q_{gs}$			-	-	4.4	
Gate-Drain Charge	$Q_{gd}$			-	-	7.7	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}, R_g = 18\text{ }\Omega, R_D = 5.2\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	8.8	-	ns
Rise Time	$t_r$			-	30	-	
Turn-Off Delay Time	$t_{d(off)}$			-	19	-	
Fall Time	$t_f$			-	20	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	9.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	37	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	110	260	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.53	1.3	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

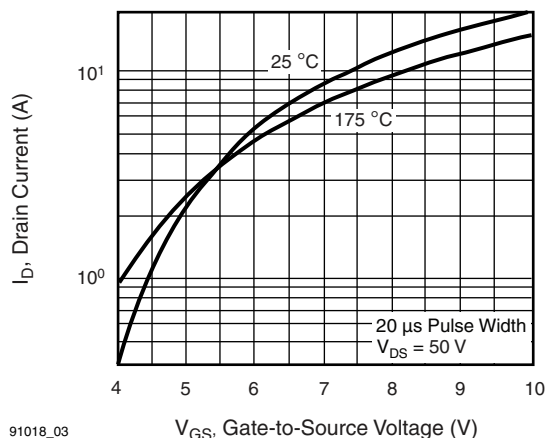
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

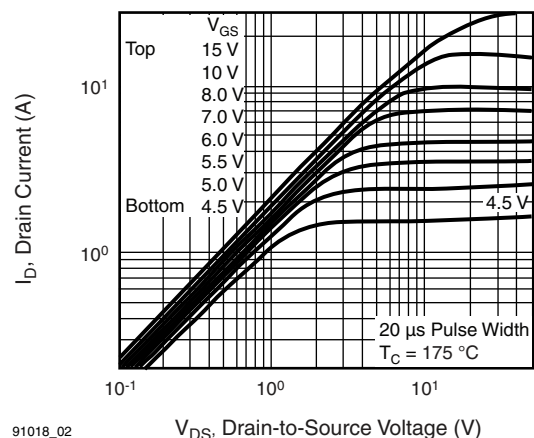
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



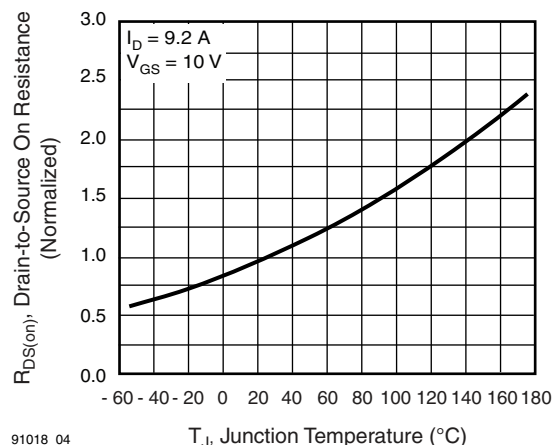
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



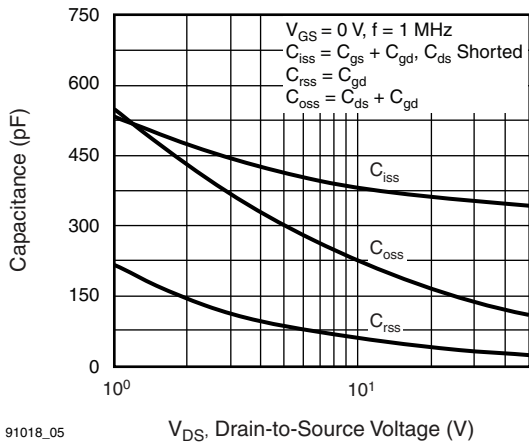
**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^\circ\text{C}$**

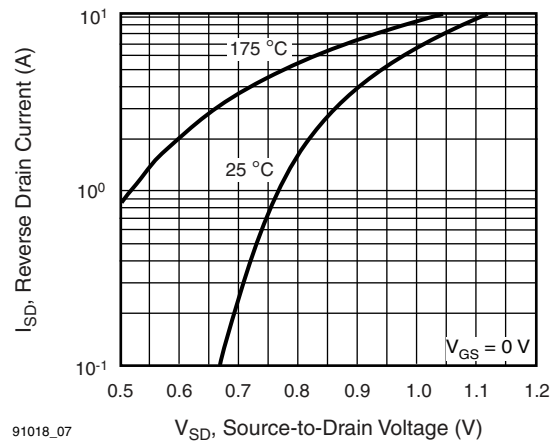


**Fig. 4 - Normalized On-Resistance vs. Temperature**



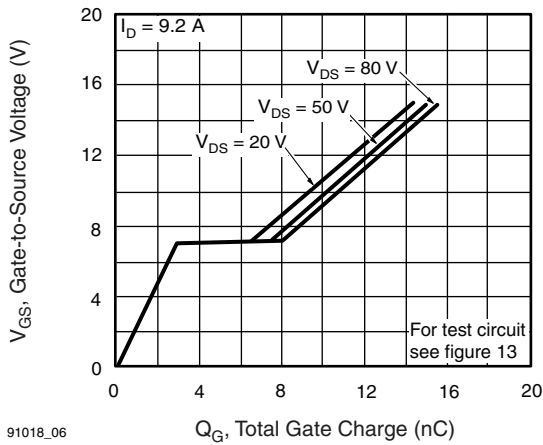
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



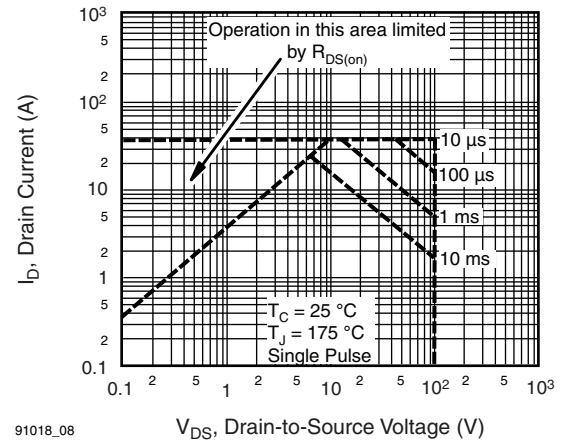
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



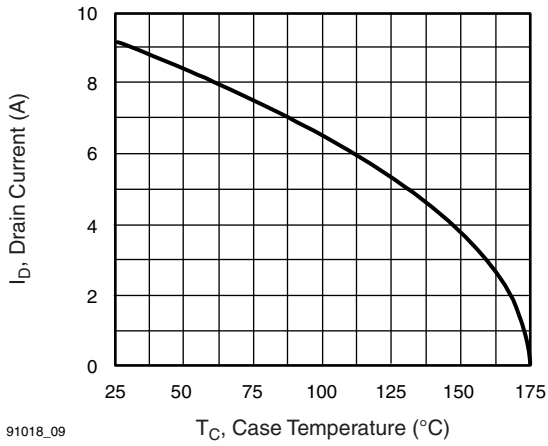
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Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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Fig. 8 - Maximum Safe Operating Area



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Fig. 9 - Maximum Drain Current vs. Case Temperature

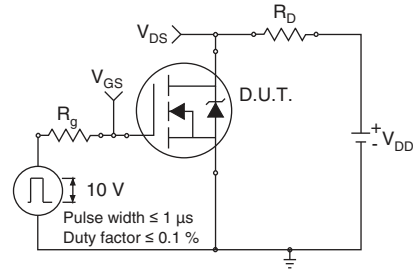


Fig. 10a - Switching Time Test Circuit

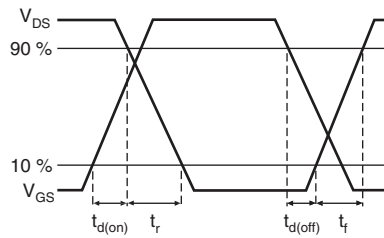
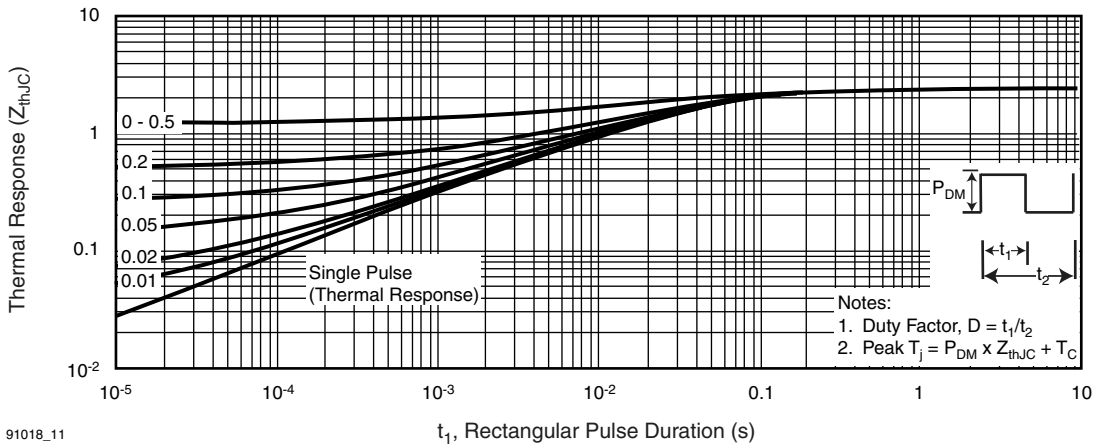


Fig. 10b - Switching Time Waveforms



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Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

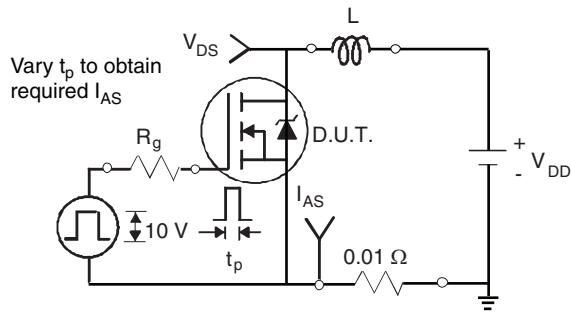


Fig. 12a - Unclamped Inductive Test Circuit

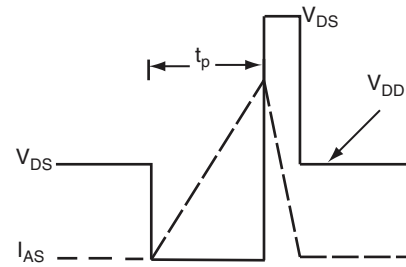
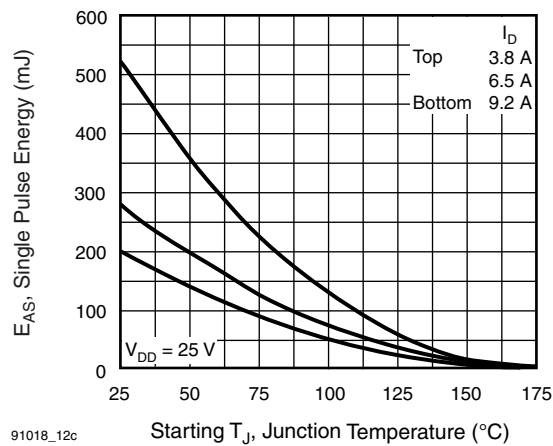


Fig. 12b - Unclamped Inductive Waveforms



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Fig. 12c - Maximum Avalanche Energy vs. Drain Current

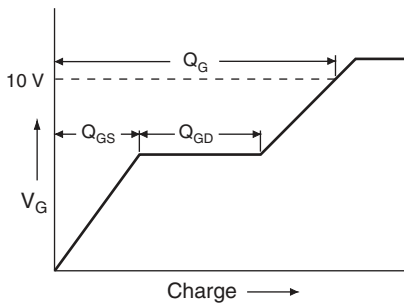


Fig. 13a - Basic Gate Charge Waveform

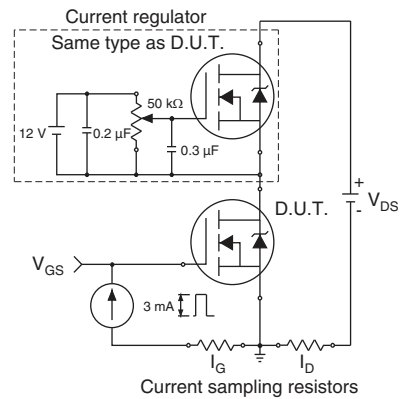
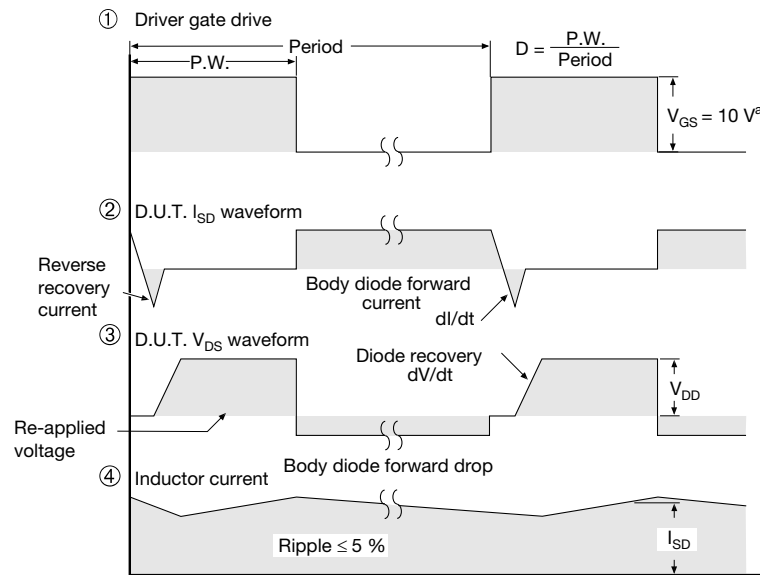
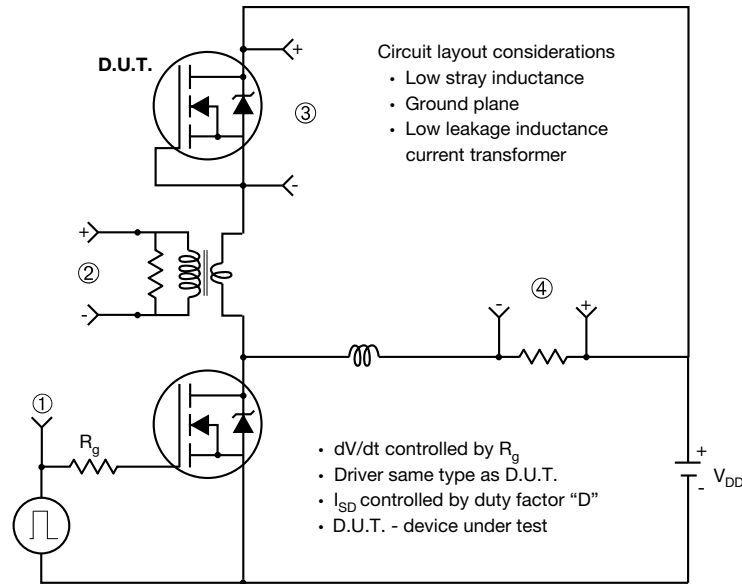


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

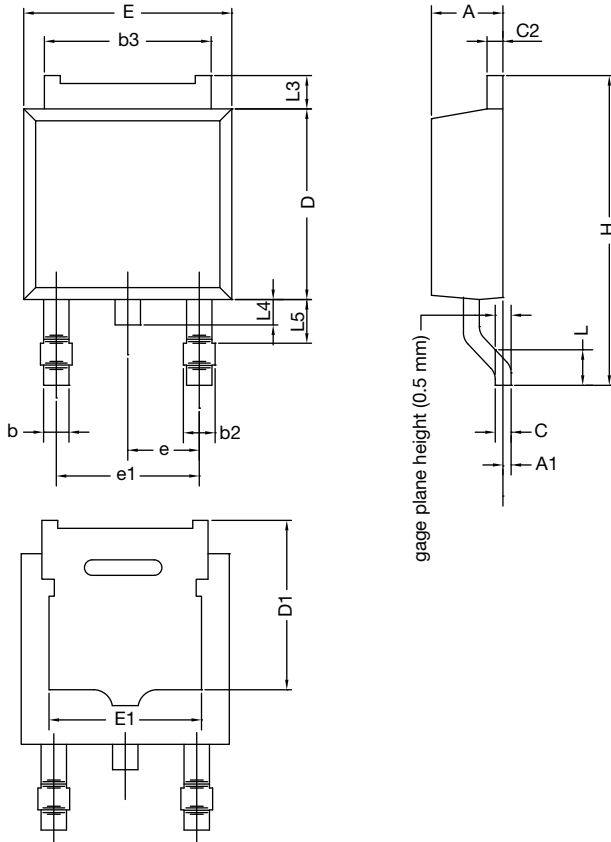


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

## TO-252AA CASE OUTLINE



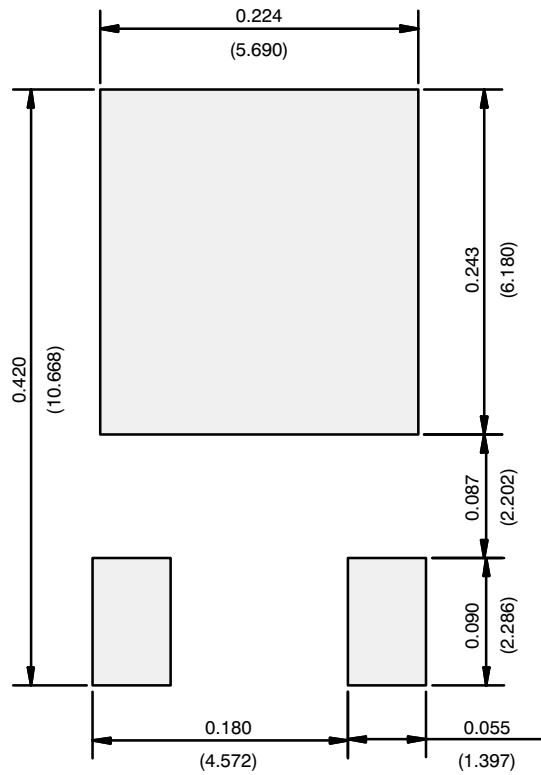
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

**Note**

- Dimension L3 is for reference only.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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