16-channel Analog Multiplexer/Demultiplexer

Features:

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +105°C
- Packaging information:SOP-24/TSSOP-24

SOP-24

TSSOP-24

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4067BM/TR	SOP-24	CD4067B	REEL	2000pcs/Reel
CD4067BMT/TR	TSSOP-24	CD4067B	REEL	2000pcs/Reel

General Description

The CD4067B is a 16-channel analog multiplexer/demultiplexer with four address inputs (A0 to A3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y0 to Y15) and a common input/output (Z). The device contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y15) and the other side connected to the common input/output (Z). With $\overline{E}$ LOW, one of the sixteen switches is selected (low-impedance ON-state) by A0 to A3. All unselected switches are in the high-impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high-impedance OFF-state, independent of A0 to A3. The analog inputs/outputs (Y0 to Y15 and Z) can swing between V_{DD} as a positive limit and VSS as a negative limit. V_{DD} to V_{SS} may not exceed 9V.

Block Diagram And Pin Description

Block Diagram

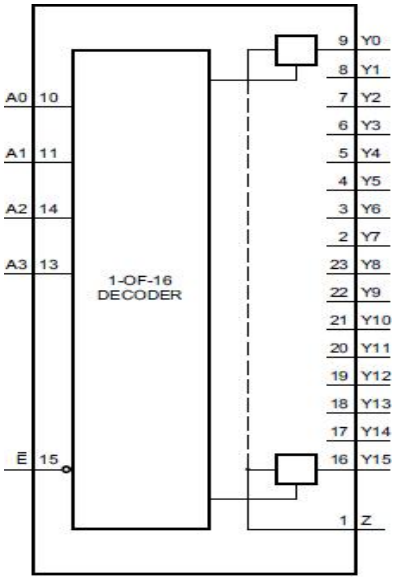


Figure 1. Functional diagram

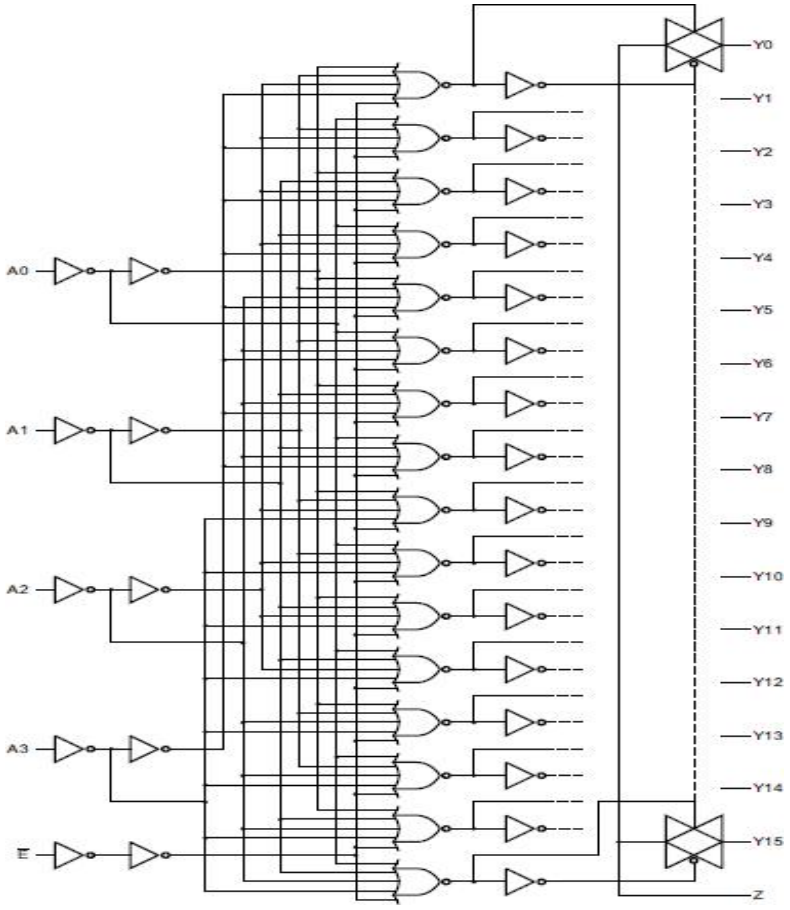


Figure 2. Logic diagram

Block Diagram

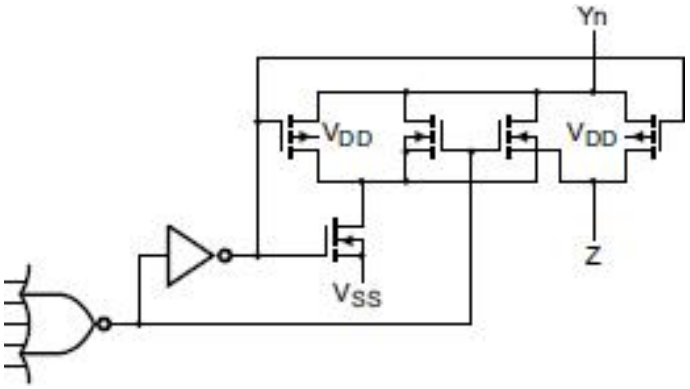
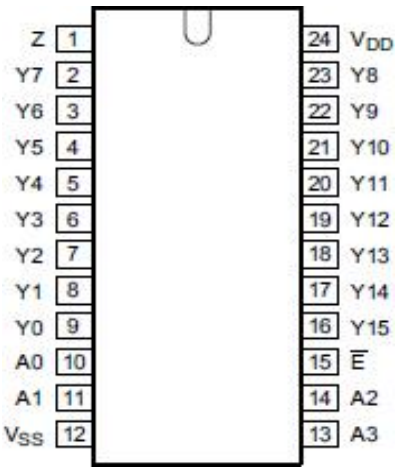


Figure 3. Schematic diagram (one switch)

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	Z	common input/output
2	Y7	independent input/output
3	Y6	independent input/output
4	Y5	independent input/output
5	Y4	independent input/output
6	Y3	independent input/output
7	Y2	independent input/output
8	Y1	independent input/output
9	Y0	independent input/output
10	A0	address input
11	A1	address input
12	VSS	ground (0V)
13	A3	address input
14	A2	address input
15	$\overline{E}$	enable input (active LOW)
16	Y15	independent input/output
17	Y14	independent input/output
18	Y13	independent input/output
19	Y12	independent input/output
20	Y11	independent input/output
21	Y10	independent input/output
22	Y9	independent input/output
23	Y8	independent input/output

Function Table

Input					Channel ON
$\overline{E}$	A3	A2	A1	A0	
L	L	L	L	L	Y0=Z
L	L	L	L	H	Y1=Z
L	L	L	H	L	Y2=Z
L	L	L	H	H	Y3=Z
L	L	H	L	L	Y4=Z
L	L	H	L	H	Y5=Z
L	L	H	H	L	Y6=Z
L	L	H	H	H	Y7=Z
L	H	L	L	L	Y8=Z
L	H	L	L	H	Y9=Z
L	H	L	H	L	Y10=Z
L	H	L	H	H	Y11=Z
L	H	H	L	L	Y12=Z
L	H	H	L	H	Y13=Z
L	H	H	H	L	Y14=Z
L	H	H	H	H	Y15=Z
H	X	X	X	X	none

Note: H=HIGH voltage level; L=LOW voltage level; X=don’t care.

Absolute Maximum Ratings

(Voltages are referenced to VSS (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+12	V
input clamping current	I_{IK}	V_I<0.5V or V_I>V_{DD}+0.5V	-	±10	mA
switch current	I	-	-	±10	mA
input voltage	V_I	all inputs	-0.5	V_{DD}+0.5	V
storage temperature	Tstg	-	-65	+150	°C
total power dissipation	Ptot	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
Soldering temperature	T_L	10s	245		°C

Note:

For SOP24 packages: above 70°C the value of Ptot derates linearly with 8mW/K.

For TSSOP24 packages: above 60°C the value of Ptot derates linearly with 5.5mW/K.

Recommended Operating Conditions

(Tamb=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	Tamb	in free air	-40	-	+105	°C
input voltage	VI	-	0	-	V_{DD}	V
multiplexer switch input current capability	-	-	-	-	25	mA
output load resistance	-	-	100	-	-	Ω

Electrical Characteristics

DC Characteristics 1

(Tamb=25°C, voltages are referenced to VSS (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		Tamb=25°C			Unit
				Min.	Typ.	Max.	
LOW-level input voltage	V_{IL}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	-	1.5	V
			V_{DD}=9V, V_O=1.0V or 9V	-	-	3	V
HIGH-level input voltage	V_{IH}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	-	V
			V_{DD}=9V, V_O=1.0V or 9V	7	-	-	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	$\pm10^{-5}$	±0.1	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{SS}=0V; V_{DD}=9V		-	±0.1	±100	nA
supply current	I_{DD}	all valid input combinations; I_O=0A	V_{DD}=5V	-	0.04	5	uA
			V_{DD}=9V	-	0.04	10	uA
input capacitance	C_I	any address or inhibit input		-	5	7.5	pF
ON resistance	R_{ON}	V_{SS}≤Vis≤V_{DD}	V_{DD}=5V	-	470	1050	Ω
			V_{DD}=9V	-	180	400	Ω
change in on-state resistance between channels	ΔR_{ON}	-	V_{DD}=5V	-	15	-	Ω
			V_{DD}=9V	-	10	-	Ω

DC Characteristics 2

(Tamb=-40℃ to +105℃, voltages are referenced to VSS (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		Tamb=-40℃		Tamb=+85℃		Tamb=+105℃		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
LOW-level input voltage	V_{IL}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	1.5	-	1.5	-	1.5	V
			V_{DD}=9V, V_O=1.0V or 9V	-	3	-	3	-	3	V
HIGH-level input voltage	V_{IH}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	3.5	-	3.5	-	V
			V_{DD}=9V, V_O=1.0V or 9V	7	-	7	-	7	-	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	±0.1	-	±1	-	±1	uA
OFF-state leakage current	$I_{S(OFF)}$	V_{SS}=0V; V_{DD}=9V		-	±100	-	±1000	-	±1000	nA
supply current	I_{DD}	all valid input combinations; I_O=0A	V_{DD}=5V	-	5	-	150	-	150	uA
			V_{DD}=9V	-	10	-	300	-	300	uA
ON resistance	R_{ON}	V_{SS}≤Vis≤V_{DD}	V_{DD}=5V	-	850	-	1200	-	1300	Ω
			V_{DD}=9V	-	330	-	520	-	550	Ω

AC Characteristics 1

(Tamb=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay time	t_{PHL}	Yn, Z to Z, Yn; see Figure 5	V_{DD}=5V	-	30	60	ns
			V_{DD}=9V	-	15	30	ns
LOW to HIGH propagation delay	t_{PLH}	Yn, Z to Z, Yn; see Figure 5	V_{DD}=5V	-	30	60	ns
			V_{DD}=9V	-	15	30	ns
HIGH to OFF-state propagation delay	t_{PHZ}	$\overline{E}$ to Yn, Z; see Figure 7	V_{DD}=5V	-	325	650	ns
			V_{DD}=9V	-	135	270	ns
LOW to OFF-state propagation delay	t_{PLZ}	$\overline{E}$ to Yn, Z; see Figure 7	V_{DD}=5V	-	325	650	ns
			V_{DD}=9V	-	135	270	ns
OFF-state to HIGH propagation delay	t_{PZH}	$\overline{E}$ to Yn, Z; see Figure 7	V_{DD}D=5V	-	220	440	ns
			V_{DD}=9V	-	90	180	ns
OFF-state to LOW propagation delay	t_{PZL}	$\overline{E}$ to Yn, Z; see Figure 7	V_{DD}=5V	-	220	440	ns
			V_{DD}=9V	-	90	180	ns

AC Characteristics 2

(Tamb=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
-3dB frequency response	$f_{(-3dB)}$	Vis=5V; V_{DD}=9V; RL=1kΩ; see Figure 9	Vos at Z	-	14	-	MHz
			Vos at any channel	-	60	-	MHz
total harmonic distortion	THD	fis=1kHz sine wave; see Figure 8	Vis=2V; V_{DD}=5V; R_L=10kΩ	-	0.3	-	%
			Vis=3V; V_{DD}=9V; R_L=10kΩ	-	0.2	-	%
-40dB feed through frequency	$f_{(-40dB)}$	Vis=5V; VDD=9V; RL=1kΩ; all channel off	Vos at Z	-	20	-	MHz
			Vos at any channel	-	8	-	MHz
crosstalk	X_{talk}	Vis=5V; V_{DD}=9V; R_L=1kΩ; frequency at -40dB; between any 2 channels; see Figure 11		-	1	-	MHz
crosstalk voltage	V_{ct}	V_{DD}=9V; R_L=10kΩ; V_C=V_{DD-VSS} (square wave); see Figure 10		-	75	-	mV

Note:

1. 20log (Vos/Vis) =-3dB.
2. 20log (Vos/Vis) =-40dB.
3. Peak-to-peak voltage symmetrical about (V_{DD}-V_{SS})/2.

Testing Circuit

AC Testing Circuit 1

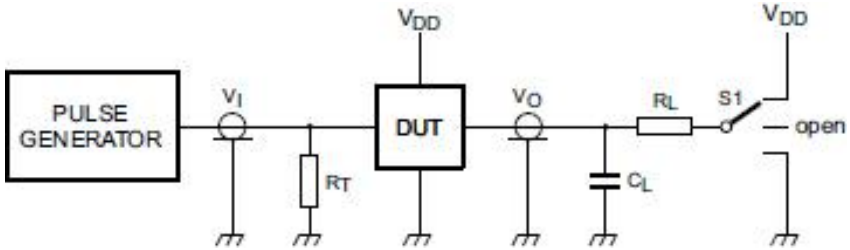


Figure 4. Test circuit for switching times

Definitions for test circuit:
C_L=Load capacitance including jig and probe capacitance.
R_T=Termination resistance should be equal to the output impedance Zo of the pulse generator.
R_L=Load resistance.
S_1=Test selection switch.

AC Testing Waveforms

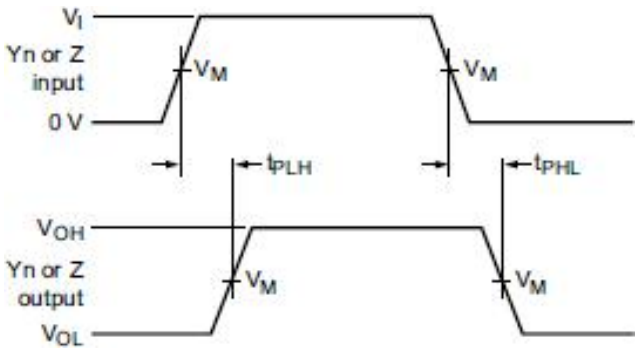


Figure 5. Yn, Z to Z, Yn propagation delays

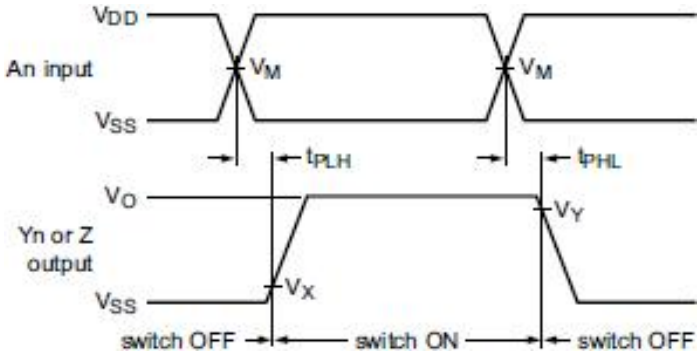


Figure 6. An to Yn, Z propagation delays

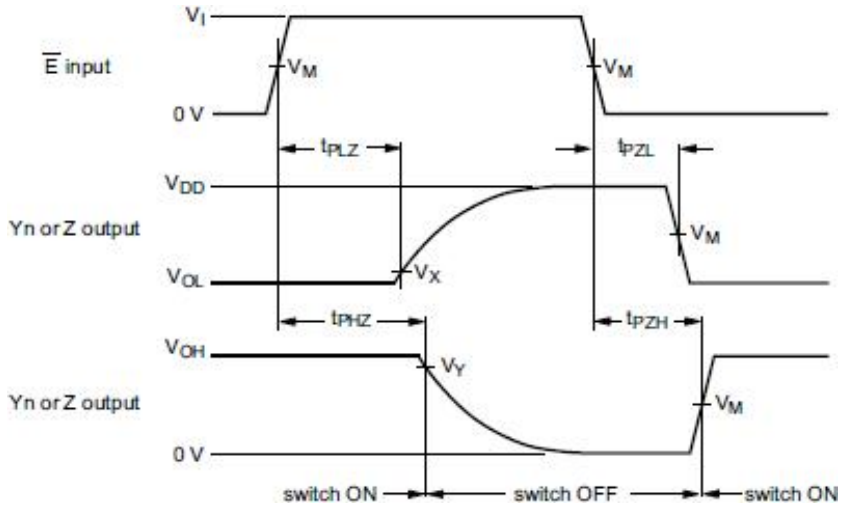


Figure 7. Enable and disable times

AC Testing Circuit 2

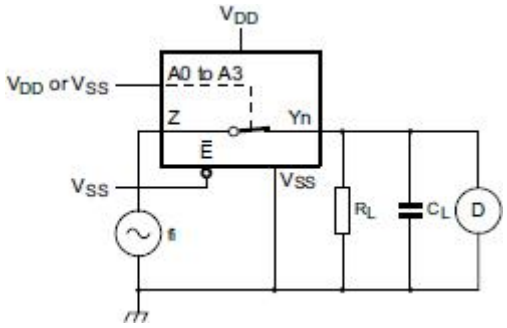


Figure 8. Test circuit for measuring total harmonic distortion

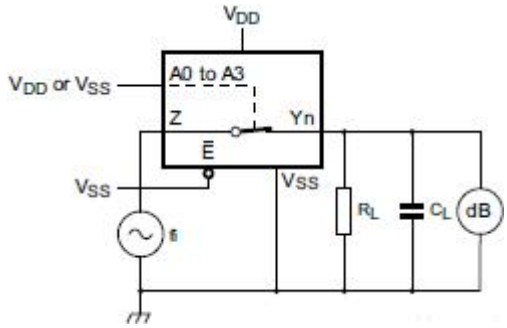


Figure 9. Test circuit for measuring frequency response

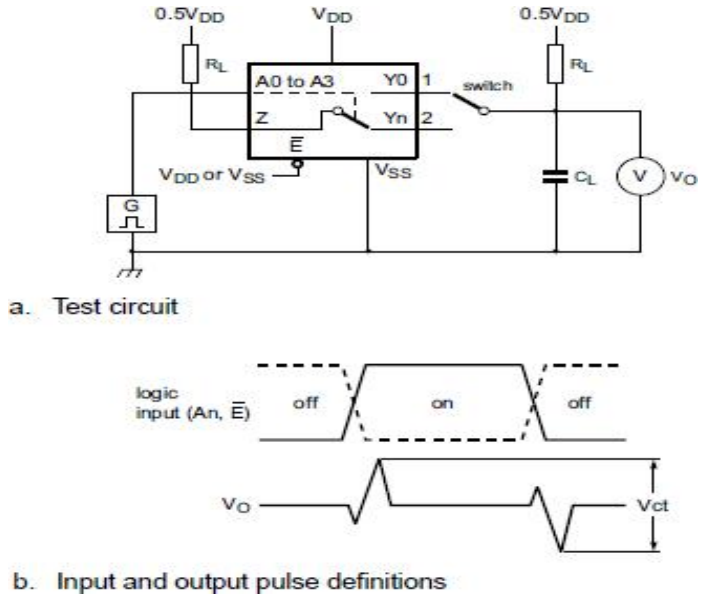


Figure 10. Test circuit for measuring crosstalk voltage between digital inputs and switch

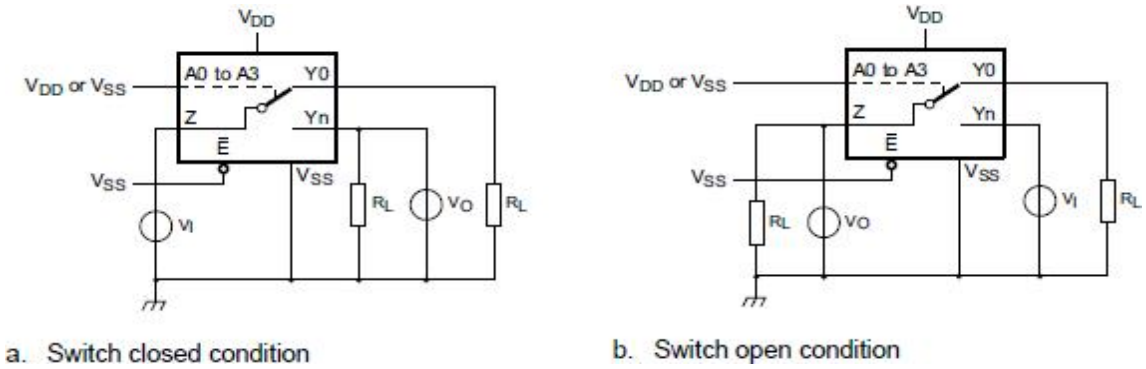


Figure 11. Test circuit for measuring crosstalk between switches

Measurement Points

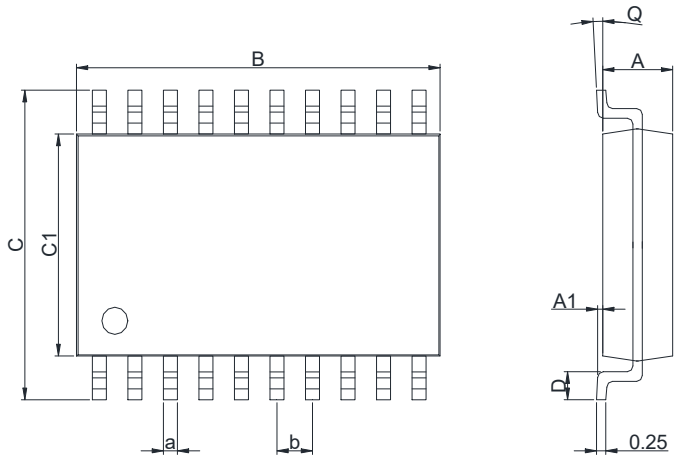
Supply voltage	Input	Output
VDD	VM	VM
3V to 9V	0.5×VDD	0.5×VDD

Test Data

Test	Input		Load		S1 position
	V_M	tr, tf	C_L	R_L	
t_{PHL}	0.5×V_{DD}	≤ 20ns	50pF	10kΩ	V_{DD} or V_{SS}
t_{PLH}	0.5×V_{DD}	≤ 20ns	50pF	10kΩ	V_{SS}
t_{PZH}, t_{PHZ}	0.5×V_{DD}	≤ 20ns	50pF	10kΩ	V_{SS}
t_{PZL}, t_{PLZ}	0.5×V_{DD}	≤ 20ns	50pF	10kΩ	V_{DD}
other	0.5×V_{DD}	≤ 20ns	50pF	10kΩ	V_{SS}

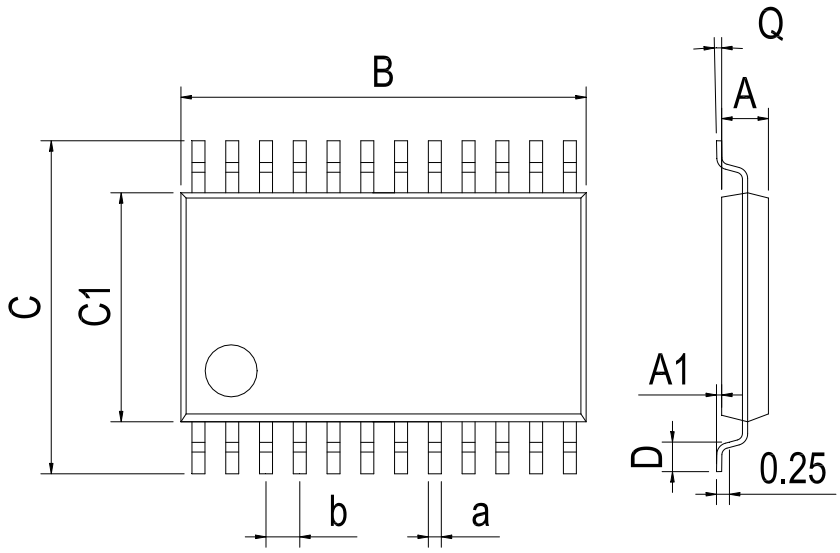
Physical Dimensions

SOP-24



Dimensions In Millimeters(SOP-24)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.26	0.1	15.3	10.10	7.4	0.7	0°	0.39	1.27 BSC
Max:	2.35	0.3	15.5	10.50	7.6	1	8°	0.47	

TSSOP-24



Dimensions In Millimeters(TSSOP-24)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	7.70	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	1.00	0.20	7.90	6.60	4.50	0.80	8°	0.25	

Revision History

DATE	REVISION	PAGE
2017-6-8	New	1-16
2023-7-21	Update encapsulation type、Update Lead Temperature	1、6

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