Dual Channel High Speed Low Side Driver with Negative Input Capability (24V Supply, 5A peak source and sink)

1 FEATURES

- 5A Peak Source Current and 5A Peak Sink Current
- 4.5V - 24V Wide Supply Voltage Range
- Down to -5V Negative Input Voltage Capability
- Fast Propagation Delay: 14ns
- Fast Rising and Falling Time: 8ns and 6ns
- TTL Input-Logic Threshold
- Under Voltage Lock Out Protection
- Low Quiescent Current: 64uA
- Output Low When Input Floating
- Independent Enable logic for Each Channel
- Available in SOIC-8L, DFN-8L, eMSOP-8L Package

2 APPLICATIONS

- Power MOSFET Gate Driver
- IGBT Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

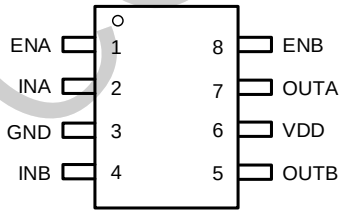
3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE
GBI7254SMBR	7254	SOIC-8L
GBI7254NMCR	7254	DFN-8L
GBI7254MMAR	7254	eMSOP-8L

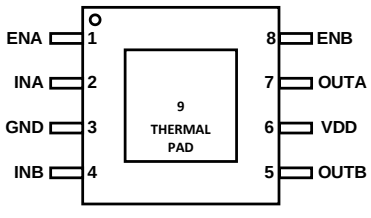
4 DISCRIPTION

The GBI7254, dual channel high speed low side gate driver, provides 5A peak source and sink current along with rail-to-rail driving capability for MOSFET, IGBT, and GaN power device. The device features a minimum 14ns input to output propagation delay and 24V power supply rail makes it suitable for high frequency power converter application. The negative input is acceptable down to -5V for enhancing the input noise immunity. The wide input hysteresis is compatible for both TTL and CMOS low voltage logic. Each channel of the device adopts non-overlap driver design to avoid the shoot-through of output stage. It operates over a wide temperature range -40°C to 150°C. The GBI7254 is available in SOIC-8L, DFN-8L, eMSOP-8L Packages.

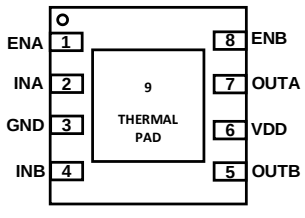
5 PIN CONFIGURATION



Top View (SOIC-8)



Top View (eMSOP-8)



Top View (QFN-8)

Table 1. GBI7254 PIN CONFIGURATION

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
ENA	1	I	Channel A Enable Input. ENA biased low disables Channel A output regardless of INA state. ENA biased high or floating enables Channel A output.
INA	2	I	Channel A Input
GND	3	-	Power Ground
INB	4	I	Channel B Input
OUTB	5	O	Channel B Output
VDD	6	I	System Power Supply.
OUTA	7	O	Channel A Output
ENB	8	I	Channel B Enable Input. ENB biased low disables Channel B output regardless of INA state. ENB biased high or floating enables Channel B output.
THERMAL PAD	9	-	Thermal dissipation soldering pad, suggest to connect to GND

6 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Logic Input & Input Enable	INA, INB, ENA, ENB	-5	26	V
Gate Driver Output	OUTA, OUTB	-0.3	26	V
Supply Voltage	VDD	-0.3	26	V
Operating junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

6.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

6.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	24	V
$V_{INA, INB, ENA, ENB}$	Input & Enable voltage range	-5	24	V
T_J	Operating junction temperature	-40	150	°C

6.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	SOIC-8	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	130.9	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	80	°C/W
ψ_{JT}	Junction to top characterization parameter	21.9	°C/W
ψ_{JB}	Junction to board characterization parameter	70.9	°C/W

6.5 ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{DD}	Operating supply voltage		4.5		24	V
V_{DD_UVLO}	Input UVLO	V_{DD} rising		4.2	4.5	V
	Hysteresis			300		mV
I_Q	Quiescent current	INA=INB=GND,		64		uA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		V_{DD}=3.5V, ENA=ENB= Floating				
		INA=INB=GND, V_{DD}=12V, ENA=ENB= Floating		124		uA
INPUTS						
$V_{INA, INB}$	Input+ logic high threshold			2.1		V
$V_{INA, INB}$	Input+ logic low threshold			1		
$V_{IN\ Hys}$	Hysteresis			1.1		V
V_{ENA_H, ENB_H}	Enable logic high threshold			2.1		V
V_{ENA_L, ENB_L}	Enable logic low threshold			1.2		V
V_{EN-_Hys}	Hysteresis			0.9		V
OUTPUT						
$I_{SINK/SRC}$	Output Sink/Source peak current	C_{Load}=10nF, F_{sw}=1kHz		5		A
R_{OH}	Output pull high resistance	I_{OUT}= - 10mA		10		Ω
R_{OL}	Output pull low resistance	I_{OUT}= 10mA		0.6		Ω
Timing						
T_R	Output rising time	C_{Load}=1nF		8		ns
T_F	Output falling time	C_{Load}=1nF		6		ns
T_{D_IN}	IN to output propagation delay, Rising edge	C_{Load}=1nF		14		ns
	IN to output propagation delay, Falling edge	C_{Load}=1nF		15		ns
T_{D_EN}	Enable to output propagation delay, Rising	C_{Load}=1nF		16		ns
	Enable to output propagation delay, Falling	C_{Load}=1nF		17		ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		15		ns

7 TYPICAL CHARACTERISTICS

V_{DD}=12V, T_A= 25°C.

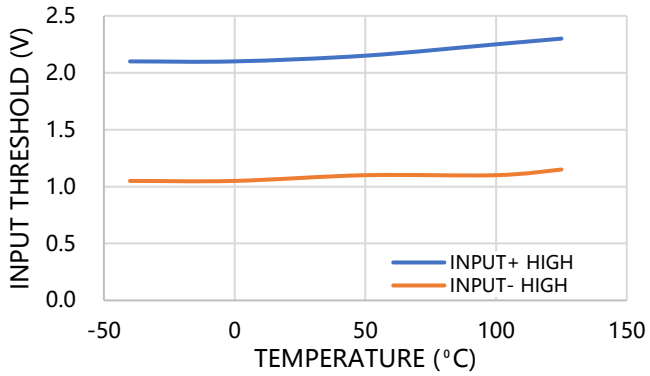


Figure 1. Input Threshold Vs Temperature

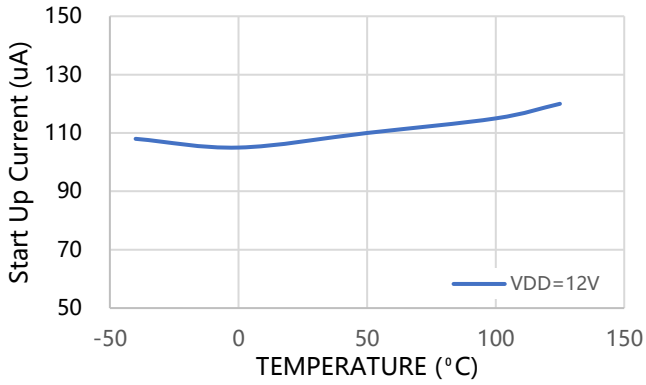


Figure 2.Start-up current Vs Temperature

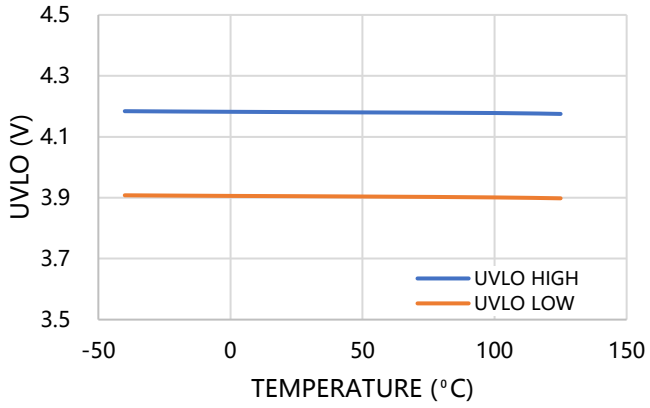


Figure 3.UVLO Vs Temperature

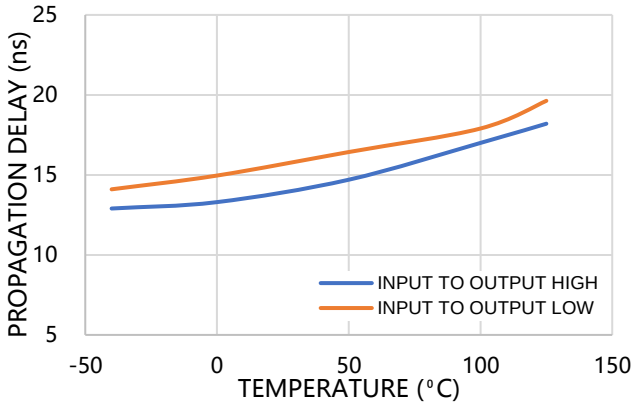


Figure 4. Input to Output Propagation Delay vs Temperature

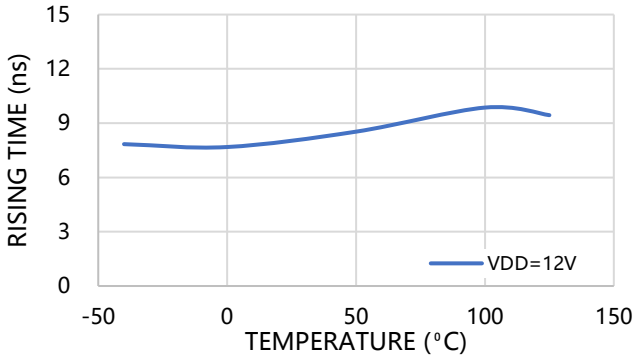


Figure 5.Output Rising Time Vs Temperature

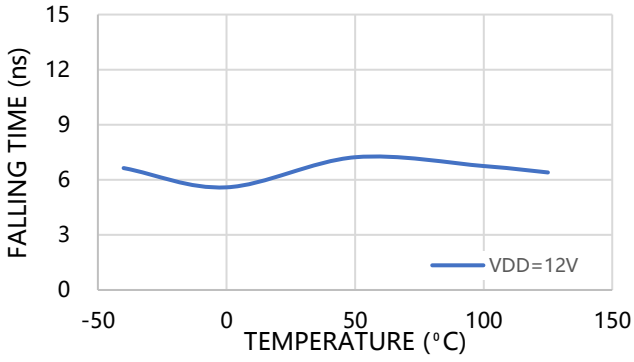


Figure 6.Output Falling Time Vs Temperature

8 FUNCTIONAL BLOCK DIAGRAM

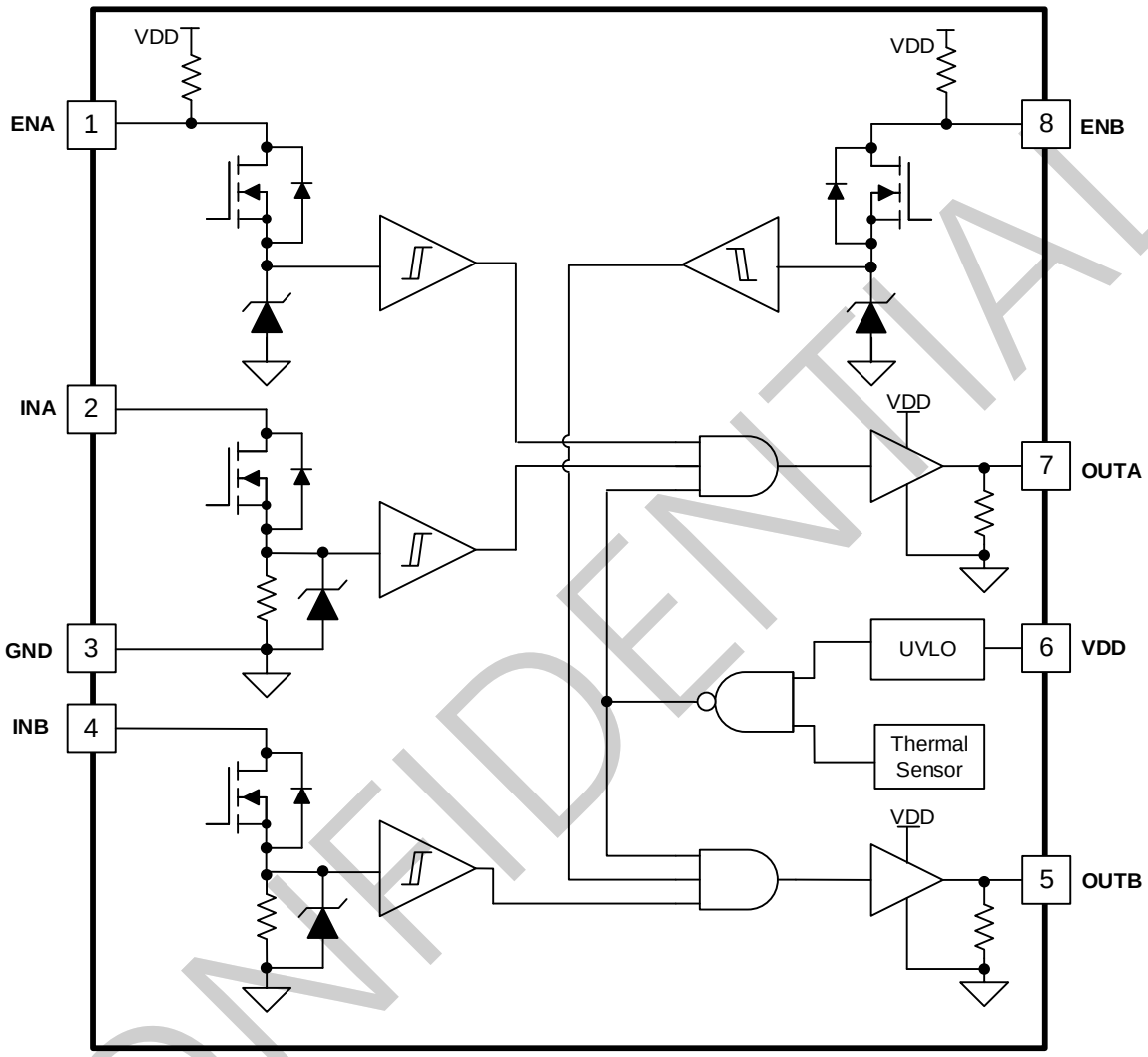


Figure 7. GBI7254 Block Diagram

9 DISCRIPTION

9.1 Overview

The GBI7254 is a dual channel, high speed, low side gate driver for power MOSFET, IGBT and GaN HMET with up to 24V wide supply and 5A source/sink peak current each channel along with the minimum input to output propagation delay of 14ns. The GBI7254 supports non-invertible outputs. The input is able to be down to -5V DC which enhances the driver input stage noise immunity.

The 24V rail-to-rail output improves the GBI7254 output stage robustness during the switching load fast transition.

9.2 VDD Power Supply

The GBI7254 operates under a supply voltage range between 4.5V to 24V. It' s recommended to put two VDD bypass capacitor in parallel to prevent noise problems on supply VDD. It has to put a 0.1uF SMT ceramic capacitor as close as possible between the VDD pin to the GND pin. To avoid the unexpected VDD glitch, a large capacitor (ex. 1uF or 10uF) with relatively low ESR must be connected in parallel with that 0.1uF capacitor. This parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

9.3 VDD Under Voltage Lock Out (UVLO)

The GBI7254 implements the Under Voltage Lock Out (UVLO) with rising threshold of typically 4.2 V along with 300mV typical hysteresis. The VDD voltage which is able to down to 4.5V is especially suitable for driving wide band gap power device, like GaN.

The UVLO holds the output low regardless of the input status when VDD is rising but the level is below the UVLO threshold. The hysteresis prevents output bouncing caused by the noise impact on the power supply. During power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD till VDD steady state reached.

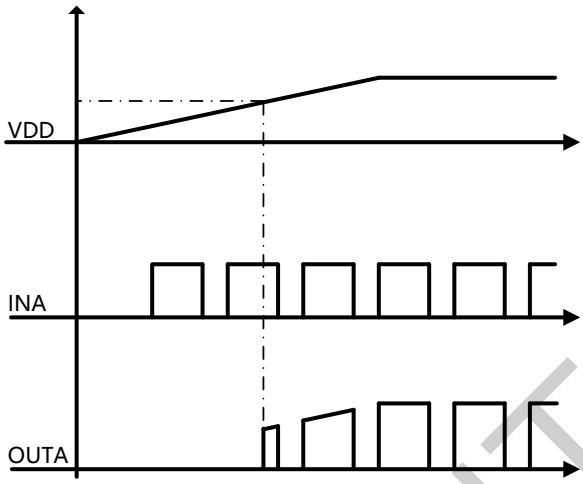


Figure 8. GBI7254 Output Vs VDD

9.4 Input Stage

The GBI7254 input is compatible on TTL logic which is independent of the VDD supply voltage. The typical threshold is 2.1-V (high) and 1.0-V (low), which make the device easily driven by PWM control signals derived from 3.3-V and 5-V digital power-controller devices. The device features wider hysteresis compared to typical threshold of 0.5V which offers enhanced noise immunity. It also implements tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

9.5 Enable Function

The GBI7254 features dedicated enable pins ENA and ENB for independent external control of each channel. The device will be enabled when the Enable signal voltage level is higher than its Enable logic high threshold, and it will be disabled when the Enable signal is lower than its Enable logic low threshold.

The enable input is compatible with TTL and CMOS logic adaptive with 3.3V or 5V microcontrollers. The GBI7254 enables all functions and starts gate driver operation when the EN input voltage is higher than the EN threshold (typical 2.1V). The enable pins are pulled up to the VDD internally with pull up resistors, thus allow the device enabled in the default state. In application without any enable feature, the enable pins could be left floating or disconnected.

9.6 Device Logic

The GBI7254 operates properly with different logic combination. The device logic is easily checked with following device logic table.

Table 2. GBI7254 Device Logic

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	Floating	Floating	L	L
Floating	Floating	L	L	L	L
Floating	Floating	L	H	L	H
Floating	Floating	H	L	H	L
Floating	Floating	H	H	H	H

10 APPLICATION INFORMATION

Typical Application

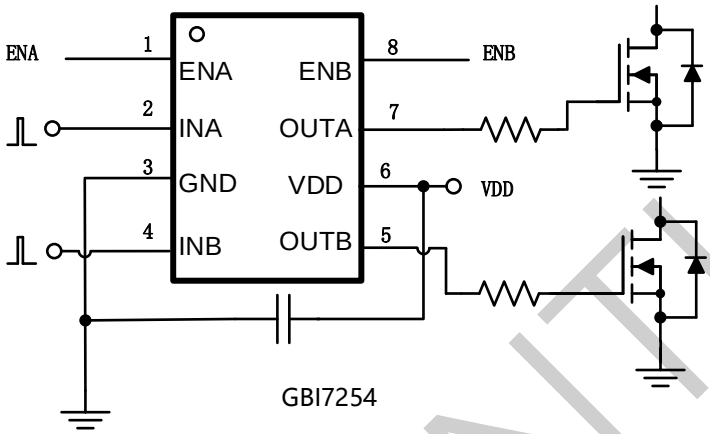


Figure 9. Typical Application Diagram

Driver Power Dissipation

Generally, the power dissipation depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The GBI7254 is designed with very low quiescent currents and internal logic to eliminate any output-stage shoot-through.

The power loss of GBI7254 caused by pure capacitive load is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \quad (1)$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

This equation (1) is also able to be adopted to calculate the switching load of power MOSFET, where gate charge Qg determines the capacitor charges.

$$Q_g = C_{LOAD} \times V_{DD} \quad (2)$$

Normally power device Manufacturers provide specifications with the typical and maximum Qg, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \quad (3)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

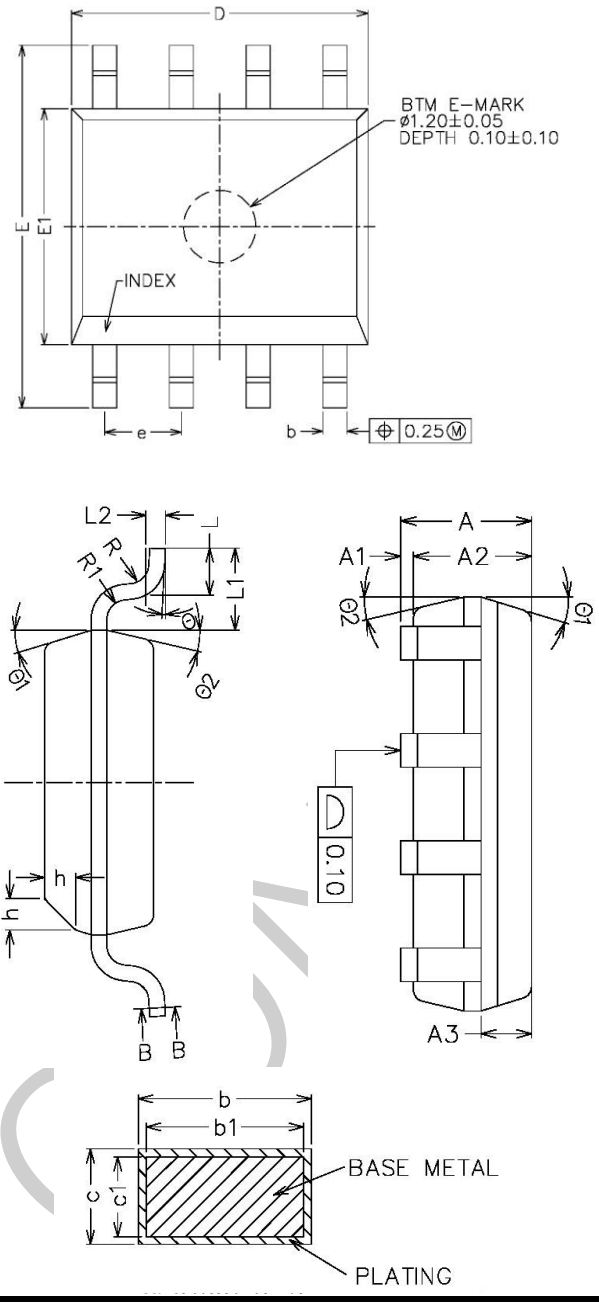
Sometimes, circuit designers put a resistor R_{GATE} between the driver output pin and the gate terminal of power device to slow down the power device transition. The power dissipation of the driver shows as below:

$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_L}{R_L + R_{GATE}} + \frac{R_H}{R_H + R_{GATE}}\right) \quad (3)$$

Where

- R_H is the equivalent pull up resistance of GBI7254
- R_L is the pull-down resistance of GBI7254
- R_{GATE} is the gate resistance between driver output and gate of power device.

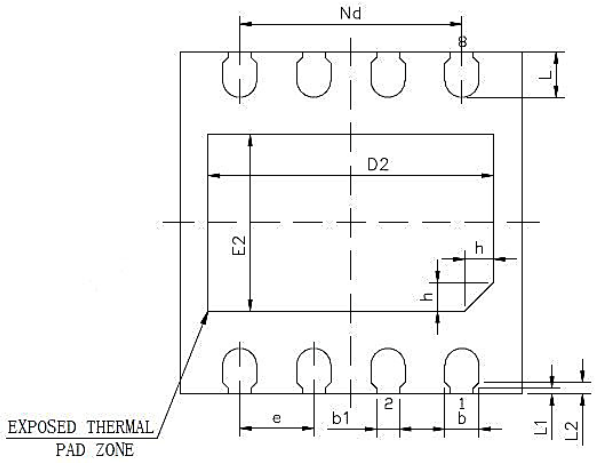
PACKAGE INFORMATION SOIC-8L

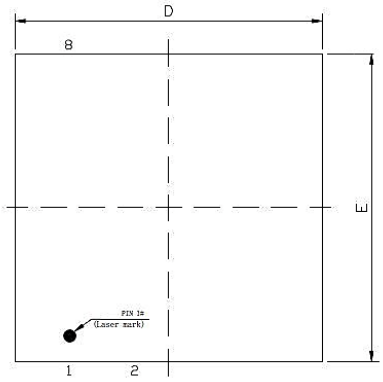


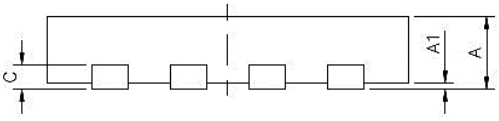
SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	15°	17°	19°
θ2	11°	13°	15°

- Units of measurement is millimeter

PACKAGE INFORMATION DFN-8L

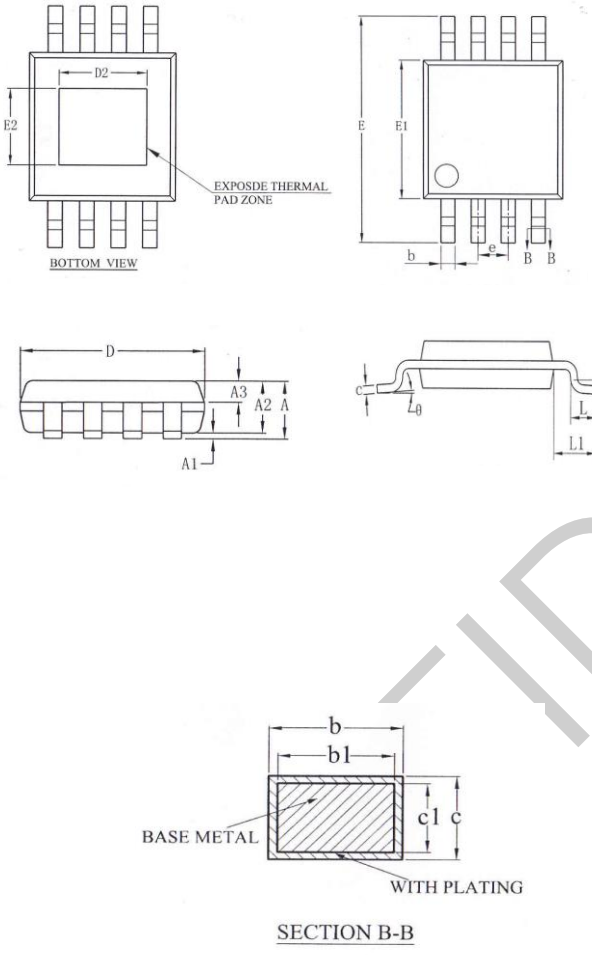






SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 85	0.90	0. 95
	0. 70	0.75	0. 80
A1	0.00	0.02	0. 05
b	0. 25	0.30	0. 35
b1	0.20REF		
c	0. 18	0.20	0. 25
D	2. 90	3. 00	3. 10
D2	2. 40	2. 50	2. 60
e	0. 65BSC		
Nd	1. 95BSC		
E	2. 90	3. 00	3. 10
E2	1. 45	1. 55	1. 65
L	0. 30	0.40	0. 50
L1	0.05REF		
L2	0.10REF		
h	0. 20	0. 25	0. 30

PACKAGE INFORMATION eMSOP-8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D2	E2
71*71	1.80REF	1.55REF