4.5V-60V Vin, 5A, High Efficiency Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 4.5V-60V
- Up to 5A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 80mΩ High-Side MOSFET
- Pulse Skipping Mode (PSM) in light load
- Low Quiescent Current: 175uA
- 130ns Minimum On-time
- 4ms Internal Soft-start Time
- External Clock Synchronization
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Adjustable Frequency 100KHz to 1.2MHz
- Low Dropout Mode Operation
- Derivable Inverting Voltage Regulator
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

DESCRIPTION

The TPS54560D is 5A buck converter with wide input voltage, ranging from 4.5V to 60V, which integrates an 80mΩ high-side MOSFET. The TPS54560D , adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load or standby condition.

The TPS54560D features programmable switching frequency from 100kHz to 1.2MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 1.2MHz. The TPS54560D allows power conversion from high input voltage to low output voltage with a minimum 130ns on-time of highside MOSFET.

The device offers fixed 4ms soft start to prevent inrush current during the startup of output voltage ramping. The TPS54560D features external loop compensation to provide the flexibility to optimize either loop stability or loop response.

The TPS54560D provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin ESOP-8 package.

FUNCTIONAL BLOCK DIAGRAM

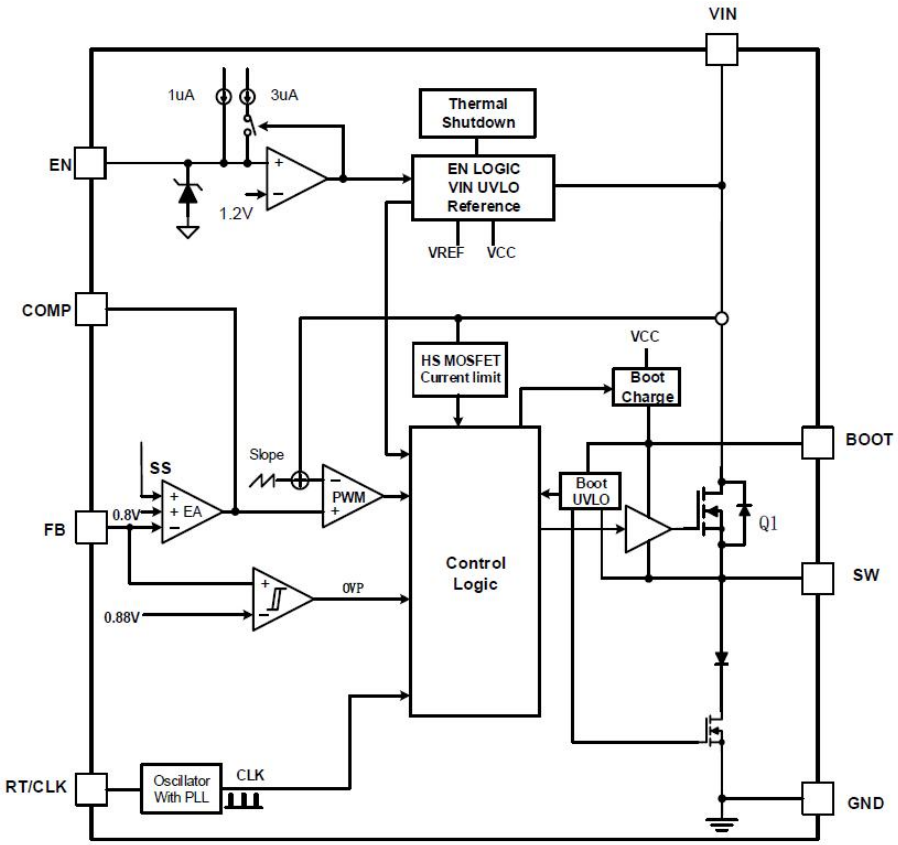


Figure 1. Functional Block Diagram

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40 ~ +125℃, typical value is tested under 25℃

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		4.5		60	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		4.2	4.4	V
	Hysteresis			320		mV
I_{SHDN}	Shutdown current from V_{IN} pin	EN=0V, No Load		2	5	μA
I_Q	Quiescent current from V_{IN} pin	EN floating, no load, V_{BST}-V_{SW}=5V		175		μA
R_{DSON_H}	High-side MOSFET on-resistance	V_{BST}-V_{SW}=5V		80		mΩ
V_{REF}	Reference voltage of FB		0.792	0.80	0.808	V
G_{EA}	Error amplifier trans-conductance	2μA<I_{COMP}<2μA, V_{COMP}=1V		300		uS
I_{COMP_SRC}	EA maximum source current	V_{FB}=V_{REF}-100mV, V_{COMP}=1V		30		μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=V_{REF}+100mV, V_{COMP}=1V		30		μA
V_{COMP_H}	COMP high clamp			2.25		V
V_{COMP_L}	COMP low clamp			0.47		V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		6.8	8	9.2	A
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.05		V

I_{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		4		μA
t_{ss}	Internal soft start time			4		ms
F_{RANGE_RT}	Frequency range using RT mode		100		1200	KHz
F_{SW}	Switching frequency	R_{RT}=200KΩ(1%)	400	450	500	KHz
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		130		ns
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	BOOT-SW UVLO threshold	V_{BST}-V_{SW} rising		2.52		V
	Hysteresis	V_{BST}-V_{SW} falling		230		mV
T_{SD}	Thermal shutdown threshold	T_J rising		172		℃
	Hysteresis			12		℃

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	VALUE	UNIT
V_{IN} ,V_{EN}	65	V
V_{BOOT}	71	V
V_{SW}	65	V
V_{FB}、V_{COMP}、$V_{RT/CLK}$	6	V
V_{BOOT}-V_{SW}	6	V
Operating junction temperature T_J	-40 ~ +150	℃
Storage temperature T_S	-65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS

DESCRIPTION	VALUE	UNIT
Input voltage range V_{IN}	4.5~60	V
Output voltage range V_{OUT}	0.8~57	V
Operating junction temperature T_J	-40 ~ +125	℃

ESD RATINGS

DESCRIPTION	VALUE	UNIT
Human Body Model(HBM), ANSI-JEDEC-JS-001-2014	-1~+1	KV
Charged Device Model(CDM), ANSI-JEDEC-JS-002-2014	-0.5~+0.5	KV

TYPICAL CHARACTERISTICS

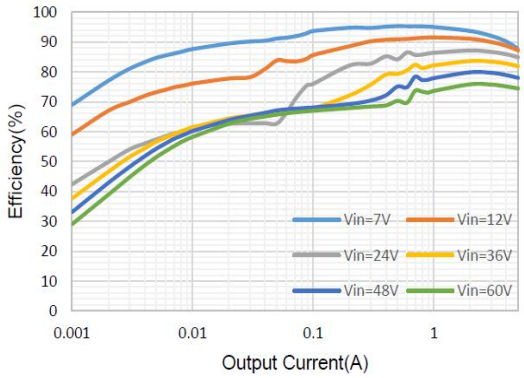


Figure 2. Efficiency vs Load Current, V_{OUT}=5V

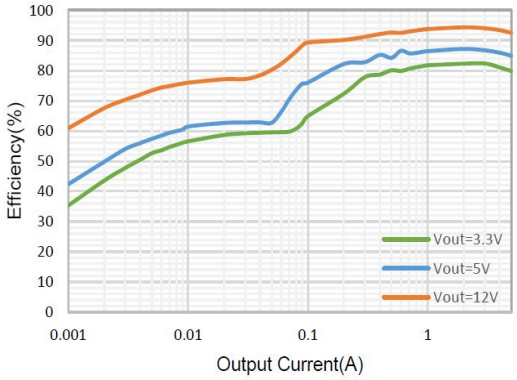


Figure 3. Efficiency vs Load Current, Vin=24V

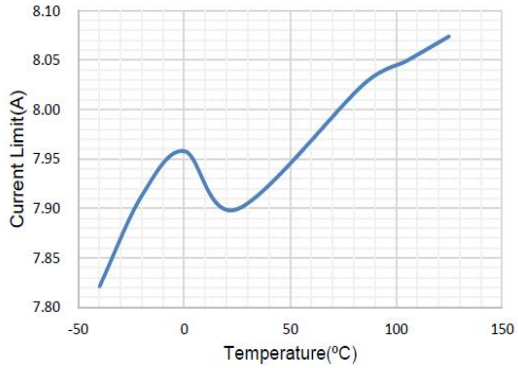


Figure 4. Current Limit VS Temperature

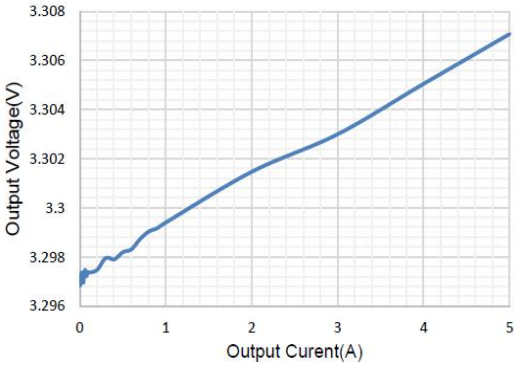


Figure 5. Load Regulation, Vin=24V, Vout=3.3V

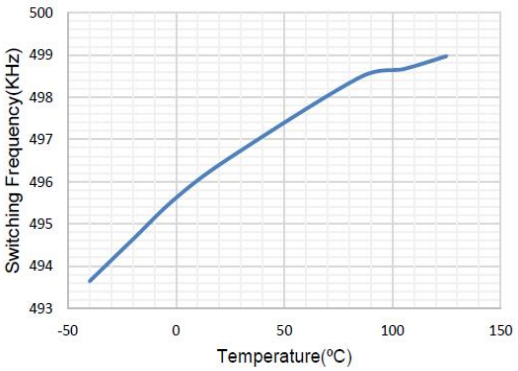


Figure 6. Switching Frequency VS Temperature

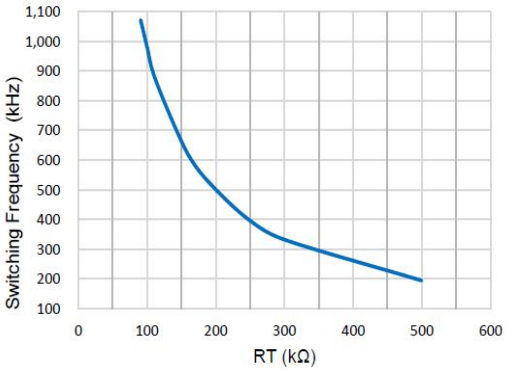


Figure 7. Switching Frequency vs RT Resistor

PIN CONFIGURATION

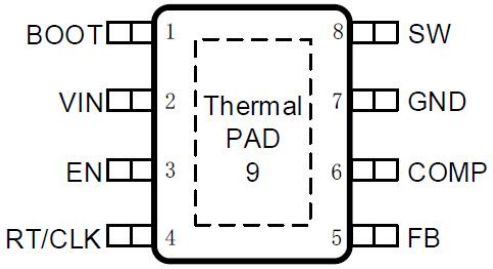


Figure 8. 8-Lead Plastic E-SOP

NO.	NAME	PIN FUNCTION
1	BOOT	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
2	VIN	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
3	EN	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
4	RT/CLK	Set the 20internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
5	FB	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
6	COMP	Error amplifier output. Connect to frequency loop compensation network.
7	GND	Ground.
8	SW	Regulator switching output. Connect SW to an external power inductor.
9	Thermal Pad	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

TYPICAL APPLICATION

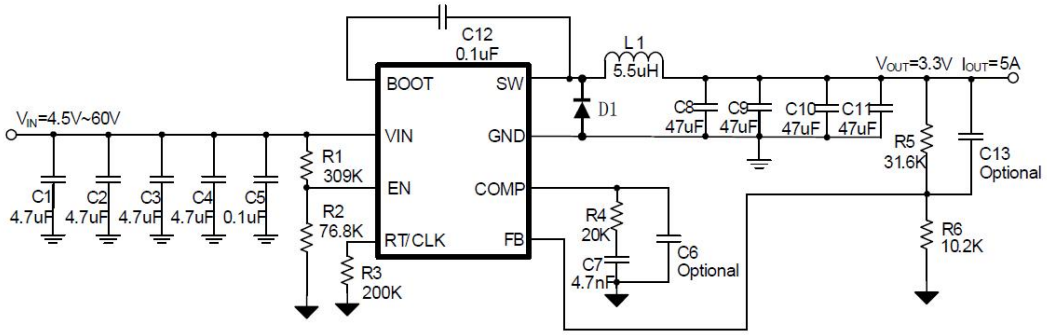


Figure9. TPS54560D Design Example, 3.3V Output with Programmable UVLO

Output Voltage:

$$V_{OUT} = 0.8 \bullet \frac{R_5 + R_6}{R_6}$$

Switching Frequency:

$$f_{SW}(KHz) = \frac{100000}{R_3(K\Omega)}$$

Under Voltage Lock-Out:

$$V_{rise} = 1.2 \times \left(1 + \frac{R_1}{R_2}\right) - 1uA \times R_1$$

$$V_{fall} = 1.05 \times \left(1 + \frac{R_1}{R_2}\right) - 4uA \times R_1$$

Compensation Values for Typical Output Voltage/Capacitor Combinations at fsw=500KHz:

Vout	L1	COUT	R4	C7	C6
2.5V	4.7uH	4*47uF	16.9K	4.7nF	68pF (optional)
3.3V	5.5uH	4*47uF	20K	4.7 nF	47pF (optional)
5V	7.8uH	4*47uF	33.2K	3.3nF	22pF (optional)
12V	10uH	4*47uF	53.6K	1nF	220pF
24V	15uH	4*47uF	105k	1nF	220pF

Inverting Power application

The TPS54560D can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.

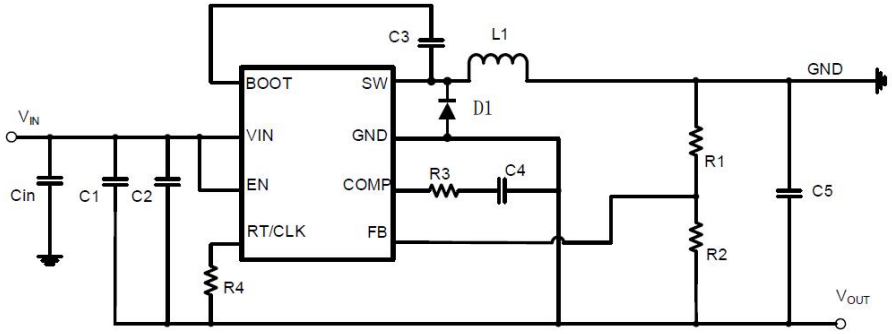
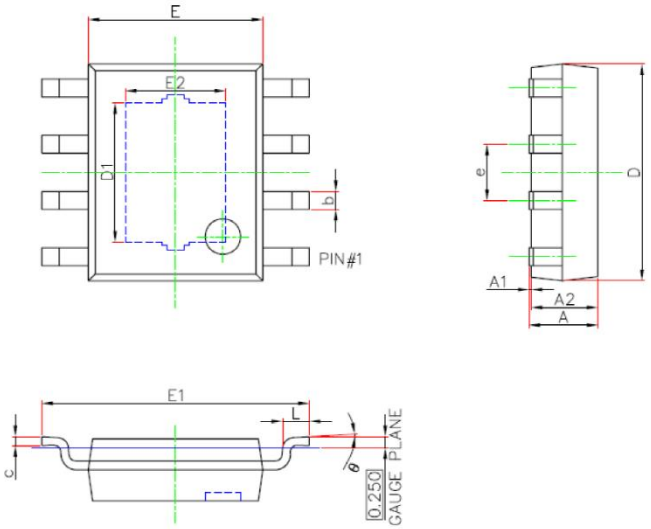


Figure 10. TPS54560D Inverting Power Supply

PACKAGE INFORMATION



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

Figure 11. Package Outline Dimensions Of TPS54560D