

3.8V-40V Vin, 3.5A, High Efficiency Synchronous Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 3.8V-40V
- Integrated 80mΩ High-Side and 50mΩ Low-Side Power MOSFETs
- Up to 3.5A Continuous Output Current
- Feedback Reference Voltage: 0.8V±1%
- Pulse Skipping Mode (PSM) with 25uA Quiescent Current in Sleep Mode
- Minimum On-time: 100ns
- Internal Soft-start Time: 2ms
- Adjustable Frequency 100KHz to 2.2MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for Programmable Input Voltage Under-voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout Mode Operation

- Derivable Inverting Voltage Regulator
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- Optical Communication and Networking System
- Automotive System
- Cigarette Lighter Adapters, Chargers
- LCD Display
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies
- Battery Pack Powered System - Cordless Power Tools, Cordless Home Appliance, Drone, Aero Modeling, GPS Tracker etc.

DESCRIPTION

The TPS54340DDAR is 3.5A synchronous buck converters with wide input voltage, ranging from 3.8V to 40V, which integrates an 80mΩ high-side MOSFET and a 50mΩ low-side MOSFET. The TPS54340DDAR, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 25uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The TPS54340DDAR features programmable switching frequency from 100 kHz to 2.2MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 2.2MHz. The TPS54340DDAR allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET.

The TPS54340DDAR is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction.

The TPS54340DDAR features Frequency Spread Spectrum FSS with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI. The TPS54340DDAR offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced SOP-8 package.

FUNCTIONAL BLOCK DIAGRAM

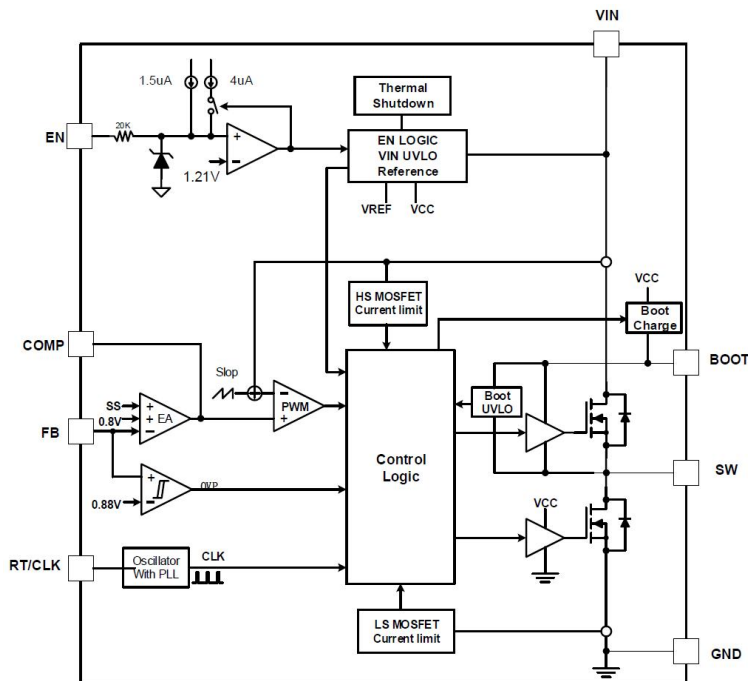


Figure 1. Functional Block Diagram

ELECTRICAL CHARACTERISTICS

$V_{IN}=24V$, $T_J=-40^{\circ}C\sim 125^{\circ}C$, typical value is tested under $25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		3.8		40	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		3.5	3.7	V
	Hysteresis			400		mV
I_{SD}	Shutdown current from VIN pin	EN=0V, No Load		1	3	μA
I_Q	Quiescent current from VIN pin	EN floating, No Load, No switching, $V_{BST}-V_{SW}=5V$		25		μA
$R_{DS(on)_H}$	High-side MOSFET on-resistance	$V_{BST}-V_{SW}=5V$		80		m Ω
$R_{DS(on)_L}$	Low-side MOSFET on-resistance			50		m Ω
V_{REF}	Reference voltage of FB		0.792	0.80	0.808	V
G_{EA}	Error amplifier trans-conductance	$2\mu A < I_{COMP} < 2\mu A$, $V_{COMP}=1V$		300		μS
I_{COMP_SRC}	EA maximum source current	$V_{FB}=V_{REF}-100mV$, $V_{COMP}=1V$		30		μA
I_{COMP_SNK}	EA maximum sink current	$V_{FB}=V_{REF}+100mV$, $V_{COMP}=1V$		30		μA
V_{COMP_H}	COMP high clamp			3		V
V_{COMP_L}	COMP low clamp			0.4		V
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		4.25	5	5.75	A
I_{LIM_LSSRC}	Low-side power MOSFET sourcing current limit threshold			5.5		A
t_{HIC_W}	Over current protection hiccup wait time			512		cycles

t_{HIC_R}	Over current protection hiccup restart time			8192		cycles
V_{EN_H}	Enable high threshold			1.18	1.25	V
V_{EN_L}	Enable low threshold		1.03	1.1		V
I_{EN_L}	Enable pin pull-up current	EN=1V	1	1.5	2	μ A
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		μ A
t_{ss}	Internal soft start time			2		ms
F_{RANGE_RT}	Frequency range using RT mode		100		2200	KHz
F_{SW}	Switching frequency	$R_{RT}=200\text{ k}\Omega(1\%)$	400	450	500	KHz
F_{RANGE_CLK}	Frequency range using CLK mode		100		2200	KHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			± 6		%
t_{ON_MIN}	Minimum on-time	$V_{IN}=24V$		100		ns
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling		2.36		V
		Hysteresis		300		mV
T_{SD}	Thermal shutdown threshold	T_J rising		170		$^{\circ}$ C
		Hysteresis		25		$^{\circ}$ C

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	VALUE	UNIT
V_{IN}, V_{EN}	42	V
V_{BOOT}	48	V
V_{SW}	42	V
$V_{FB}, V_{COMP}, V_{RT/CLK}$	6	V
$V_{BOOT}-V_{SW}$	6	V
Operating junction temperature T_J	-40 ~ +150	$^{\circ}$ C
Storage temperature T_S	-65 ~ +150	$^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

DESCRIPTION	VALUE	UNIT
Input voltage range V_{IN}	3.8~40	V
Output voltage range V_{OUT}	0.8~39	V
Operating junction temperature T_J	-40 ~ +125	$^{\circ}$ C

ESD RATINGS

DESCRIPTION	VALUE	UNIT
Human Body Model(HBM), ANSI-JEDEC-JS-001-2014	-2~+2	KV
Charged Device Model(CDM), ANSI-JEDEC-JS-002-2014	-0.5~+0.5	KV

TYPICAL CHARACTERISTICS

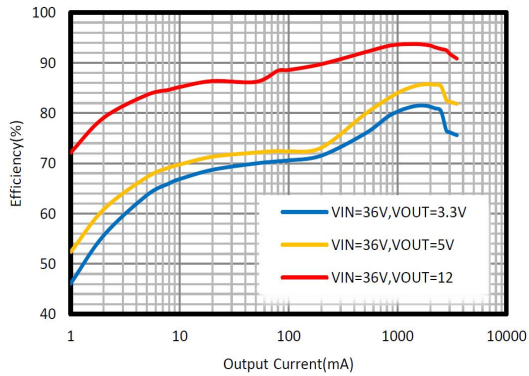


Figure 2. Efficiency vs Load Current, Vin=36V

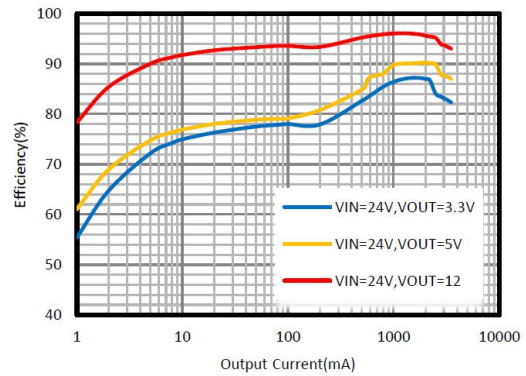


Figure 3. Efficiency vs Load Current, Vin=24V

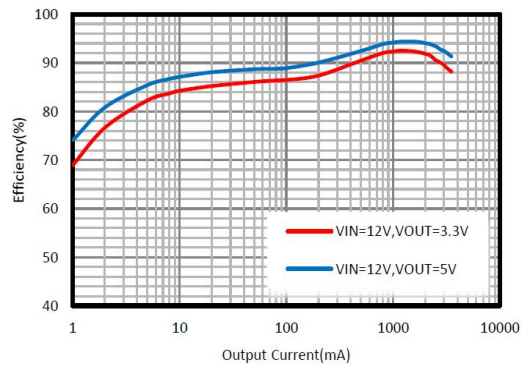


Figure 4. Efficiency vs Load Current, Vin=12V

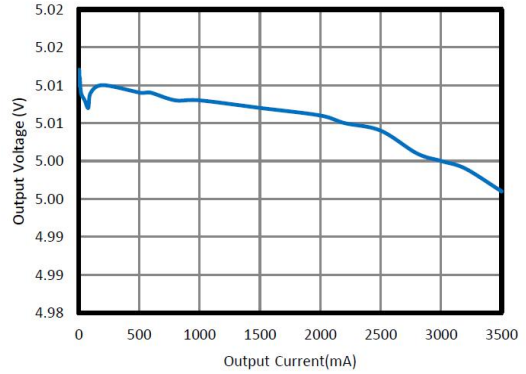


Figure 5. Load Regulation (Vout=5V)

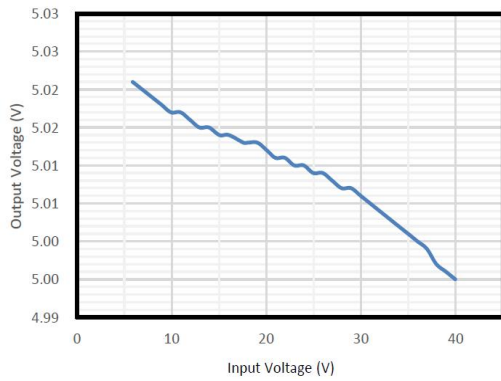


Figure 6. Line Regulation (Iout=3.5A)

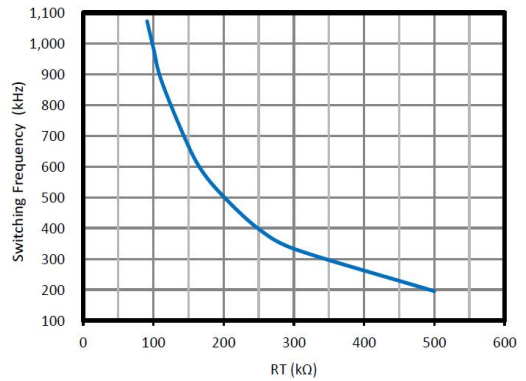


Figure 7. Clock Frequency vs RT/CLK Resistor

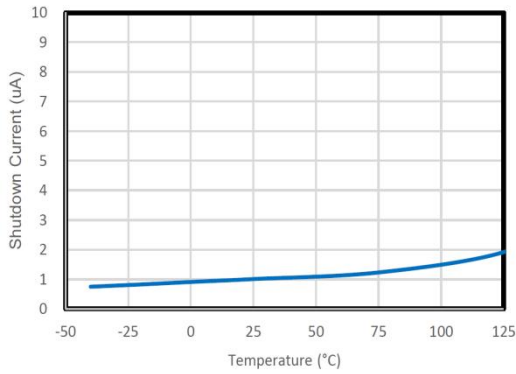


Figure 8. Shutdown Current vs Temperature

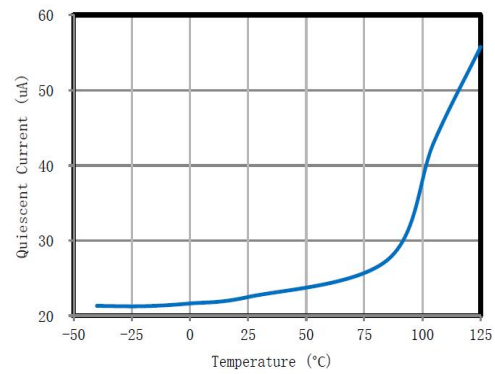


Figure 9. Quiescent Current vs Temperature

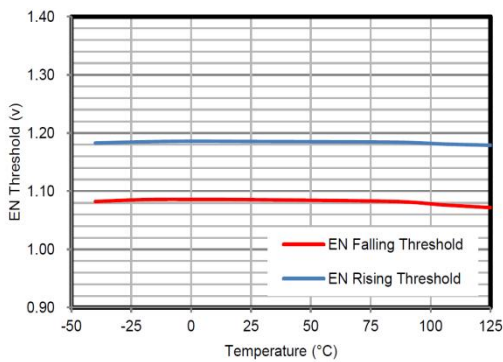


Figure 10. EN Threshold vs Temperature

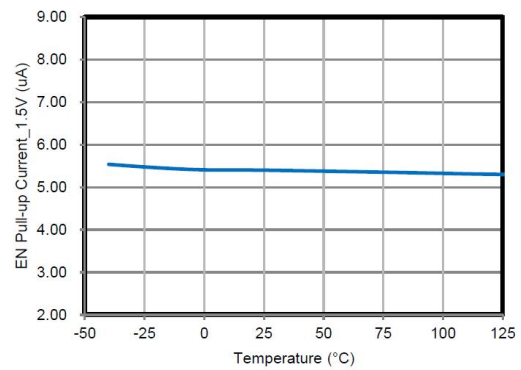


Figure 11. EN Pull-up Current vs Temperature

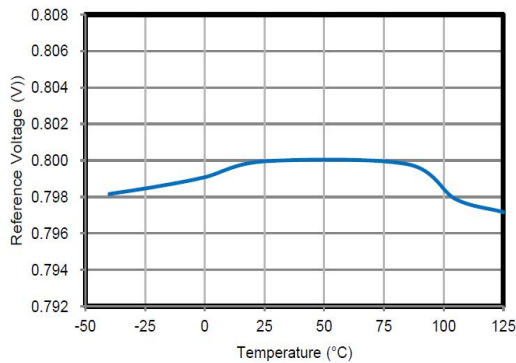


Figure 12. Reference Voltage vs Temperature

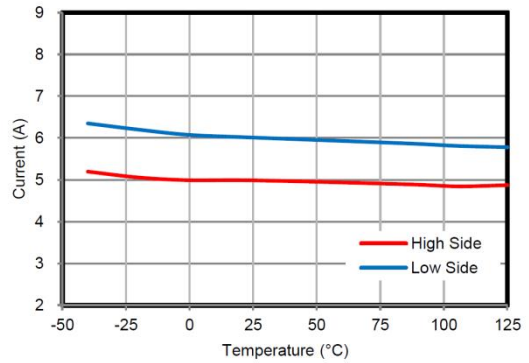


Figure 13. Peak Current Limit vs Temperature

PIN CONFIGURATION

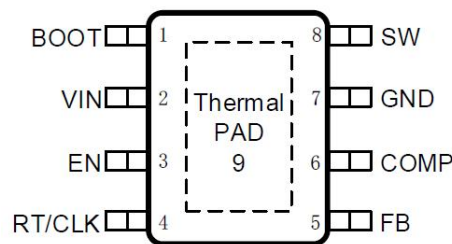


Figure 14. 8-Lead Plastic E-SOP

NO.	NAME	PIN FUNCTION
1	BOOT	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
2	VIN	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
3	EN	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
4	RT/CLK	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
5	FB	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
6	COMP	Error amplifier output. Connect to frequency loop compensation network.
7	GND	Ground
8	SW	Regulator switching output. Connect SW to an external power inductor.
9	Thermal Pad	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

TYPICAL APPLICATION

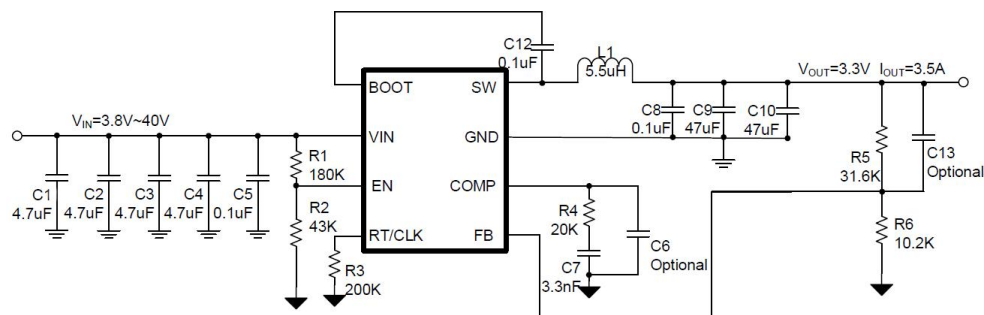


Figure 15. TPS54340DDAR Design Example, 3.3V Output with Programmable UVLO

Output Voltage:

$$V_{OUT} = 0.8 \cdot \frac{R_5 + R_6}{R_6}$$

Switching Frequency:

$$f_{SW} (kHz) = \frac{100000}{R_3 (k\Omega)}$$

Under Voltage Lock-Out:

$$V_{rise} = 1.18 \times \left(1 + \frac{R_1}{R_2} \right) - 1.5 \mu A \times R_1$$

$$V_{fall} = 1.10 \times \left(1 + \frac{R_1}{R_2} \right) - 5.5 \mu A \times R_1$$

Compensation Values for Typical Output Voltage/Capacitor Combinations at fsw=500KHz:

Vout	L1	COUT	R4	C7	C6
1.8V	3.3uH	2*47uF	12.1K	6.8nF	100pF(optional)
2.5V	4.7uH	2*47uF	16.9K	4.7nF	68pF(optional)
3.3V	5.5uH	2*47uF	20K	4.7 nF	47pF(optional)
5V	7.8uH	2*47uF	33.2K	3.3nF	22pF(optional)
12V	10uH	2*47uF	53.6K	1nF	220pF

Inverting Power application

The TPS54340DDAR can be used to convert a positive input voltage to a negative output voltage. Typical applications are amplifiers requiring a negative power supply.

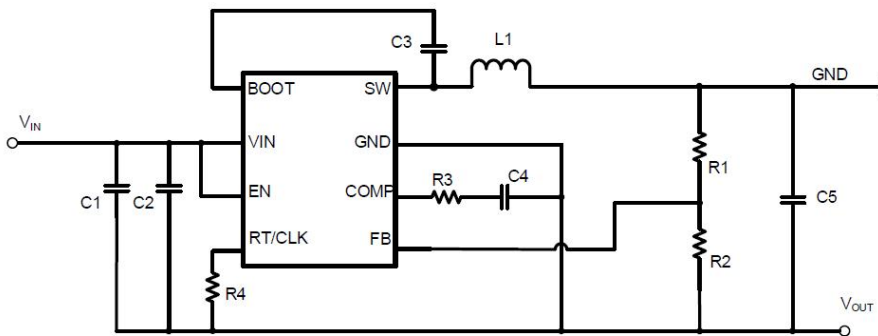
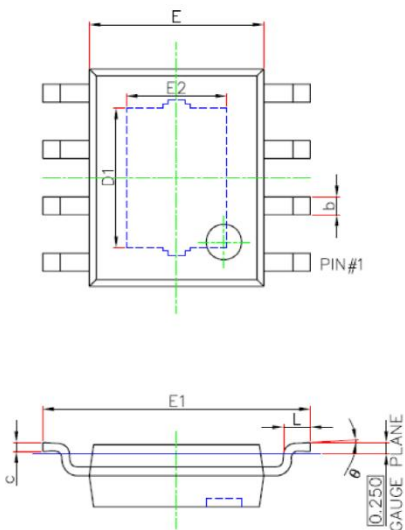


Figure 16. TPS54340DDAR Inverting Power Supply

PACKAGE INFORMATION



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.050	3.250
E	3.800	4.000
E1	5.800	6.200
E2	2.160	2.360
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

Figure 17. Package Outline Dimensions Of TPS54340DDAR