NCF29A1 / NCF29A2

NCF29A1 (TOKEN 3D) / NCF29A2 (TOKEN 1D)

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Product data sheet
CONFIDENTIAL

Document information

Info	Content
Keywords	Car key, Vehicle Immobilization (IMMO), Passive Keyless Entry (PKE), Remote Keyless Entry (RKE), RF transceiver, ISM band, FSK, ASK, MRK III
Abstract	The NCF29A1 / NCF29A2 is a fully integrated single-chip solution combining RKE, PKE and IMMO functionality designed for use in automotive environments.

1. General information

1.1 General description

The NCF29A1 / NCF29A2 is an extremely compact single chip solution, ideally suited for automotive applications with combined vehicle immobilization and keyless entry / start functions. The device incorporates a Security Transponder, UHF Transmitter and RISC Controller on the same chip and requires only a few external components.

The RISC Controller is powered by NXP's low power hardware extended (MUL/DIV) 16-Bit MICRO RISC KERNEL (MRK IIIe) employing a 2- stage pipeline architecture in order to improve performance. The device features 10 I/O ports allowing for up to 10 command button inputs. For transponder, keyless entry and go operations, the on-chip hardware Calculation Unit or any user-defined software based algorithm can be employed for data communication.

The device provides up to 2048 Byte of EEPROM for data storage with access control as defined by the application. In addition, the device supports a sophisticated EEPROM access scheme when operating as Security Transponder during immobilizer operation.

The on-chip multi-channel UHF Transmitter requires no external components to operate except for the reference crystal and the loop antenna matching circuitry. The device is specified to operate in the frequency bands 310-447MHz. The frequency bands 868 MHz and 915 MHz can be supported on request. The device features a uniform reference frequency (27.6 MHz) for all bands. The UHF Transmitter is directly controlled by the RISC Controller and supports FSK, ASK, OOK modulation of the carrier with data rates up to 25 kbit/s (Manchester). The programmable power amplifier regulates the antenna pin voltage in order to minimize carrier variations over temperature and battery voltage variations.

The device provides a motion detection function that detects state changes on the motion sensor pin and may wake-up the CPU core if needed. The device can be configured to automatically disable the LF Active receiver block for saving power when key-fob still (no motion) is detected, and also, to automatically enable the LF Active receiver when key-fob in motion is detected.

The device provides means for capacitive tuning for maintaining an optimal resonance frequency and optimize reception of an incoming LF signal in order to save cost in the bill of material.

Unused RSSI channels can be attenuated in order to acquire precise single channel RSSI measurements.

LF Active channel polling enables battery supply current reductions depending on the protocol length and this extend the battery lifetime significantly.

The device comes in a tiny 32 pin HVQFN Package demanding minimal board space (5 mm x 5 mm).

1.2 Features and benefits

1.2.1 General

- Single chip security transponder and keyless entry solution
- On-chip UHF transmitter (310 MHz to 447 MHz)
- 868 MHz and 915 MHz on-chip UHF transmitter available on request
- Up to 10 command buttons with wake-up function
- Current source option for direct LED drive
- RISC programmable device operation
- 32 bit quasi unique device and product type identification
- Single Lithium cell operation, 2.0 V to 3.6 V
- C-Compiler supported software development
- 32-pin compact HVQFN package (5 mm x 5 mm)
- On-chip temperature sensor
- Motion sensor interface

1.2.2 Security Transponder

- Operating frequency 125 kHz
- 3D LF transponder operation (NCF29A1 only)
- LF capacitive antenna tuning
- Customer programmable transponder operation
- Fast mutual authentication
- Built-in HT2-E, HT3, HT-AES or HT-Pro2 based transponder emulations
- Data rate (tag to base station) 4 kbit/s
- 2 ms detection unit
- EEPROM read/write protection capability

1.2.3 3D LF active interface

- Operating frequency 125 kHz
- Boost mode for long range receive applications
- LF active capacitive antenna tuning
- Adjustable Q-factor with resistive LF active channel tuning
- Low power LF wake-up and data processing
  - Single-bit fault tolerant wake-up option
  - Polling option
  - Options for LF Active receiver control (ON and OFF) coupled to key-fob motion (STILL or MOVING)
- Three axis (3D) LF signal strength measurement and indication (RSSI)
- High receiver sensitivity
- 2 kbit/s PKE data rate (high-Q mode), 4 and 8 kbit/s Manchester
- Fast A/D conversion for RSSI measurement
- LF active telegram organization like PCF795x, NCF295x and NCF297x

1.2.4 UHF Transmitter

- Multi Channel Fractional-N PLL
- One reference frequency (XTAL) for all bands
- Programmable RF-output power, stabilized over temperature and voltage level
- Programmable ASK/FSK modulation characteristics
  - OOK ASK option with higher than 30dB dynamic range
- Low power consumption:
  - 12.5 mA @10 dBm (434 MHz)
  - 7 mA @ 0 dBm (434 MHz)

1.2.5 Calculation Unit

- Multimode hardware security algorithm
- HT2-E with 48 bit Secret Key
- HT3 with 96 bit Secret Key
- AES128 with 128 bit Secret Key
- CRC hardware co-processor unit
- True hardware and Pseudo Random Number Generator (16 bit)

1.2.6 RISC Controller

- 16 Bit Harvard Architecture (RISC)
- Hardware supported MUL/DIV instructions
- Two CPU clock cycles per instruction (2-stage instruction pipeline)
- System ROM for NXP firmware
- Up to 32 kByte user EROM for application (code and data space)
- Up to 2048 Byte Ultra Low Power (ULP) Serial EEPROM for extended user data
- 2 kByte RAM (1792 bytes USER RAM and 256 bytes used for SYSTEM RAM)
- Single level interrupt architecture
- On-chip low tolerance RC Oscillator (< +/- 10%)
- Short instruction execution time (0.125 µs @ 16 MHz CPU clock)
- Three 16-Bit Timer/Counter
- Watchdog
- Low operational power consumption

1.2.7 Peripherals

- Up to 10 general purpose I/Os
- Up to 10 wake-up / button inputs
- One I/O with LED drive capability
- Software configurable pull-up or pull-down resistor
- Software configurable pull-up strength: strong (27 kΩ) or weak pull up (115 kΩ)
- Software configurable wake-up either on high to low or low to high transition
- Optional clock/event input for Timer/Counter
- General purpose ADC supporting various analogue sources (incl. external source)
- Two synchronous serial peripheral interfaces SPI 0 and SPI 1 with a baud rate selectable between 125 kHz and 4 MHz
- Battery Voltage Sensor with programmable battery low threshold

1.3 Applications

The NCF29A1 / NCF29A2 is a compact single chip solution, ideally suited for automotive applications with combined vehicle immobilization and keyless entry / start functions. The device incorporates a Security Transponder, a UHF Transmitter and a RISC Controller on the same chip and requires only a few external components.

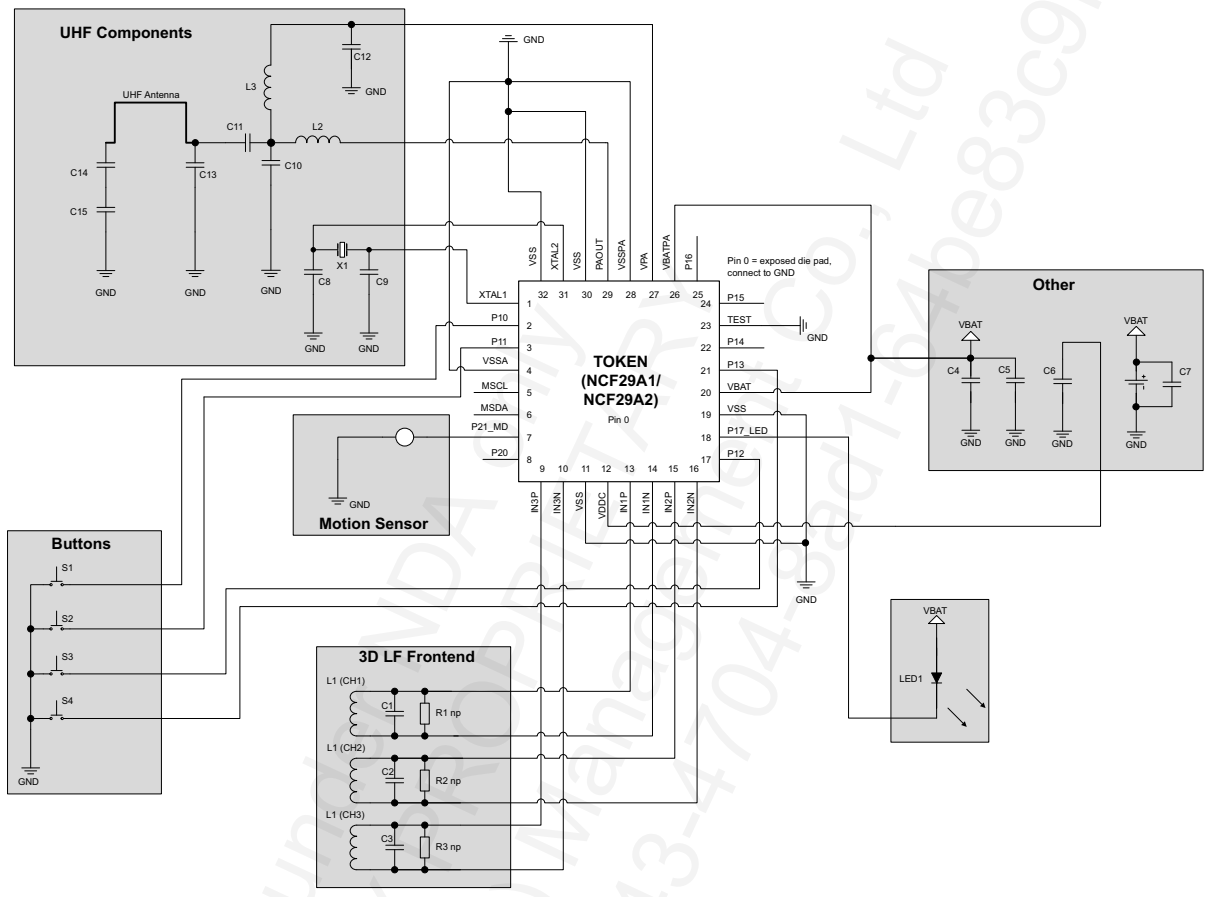


Fig 1. Typical application schematic

1.3.1 Application areas

- Remote Keyless Entry (RKE)
- Passive Keyless Entry (PKE) and/or Passive Keyless Go (PKG)
- Immobilization

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery supply voltage		1.8	3.0	3.6	V
T_{amb}	Operating temperature		-40		+85	°C
ULP-serial EEPROM						
t_{ULPRET}	Data retention time	T_{amb} = 50 °C	20			years
$N_{ULPWR-CYL}$	Write endurance ULP EEPROM	T_{amb} = 25 °C [1]	100 k			cycles

[1] The activation energy equals 0.15 eV. According to Arhennius' Law, the number of useful cycles at room temperature is about 2.5 times higher than at 85 °C.

1.5 NCF29A1 / NCF29A2 type naming conventions

The following table explains the naming conventions for the commercial product name of the NCF29A1 / NCF29A2 products. Every NCF29A1 / NCF29A2 product gets assigned a commercial type name, which includes also customer and application specific data.

The NCF29A1 / NCF29A2 commercial type names have the following format.

NCF29xxtHN/vrffmn

'**NCF29**' and 'HN' are constants, all other letters are variables, which are explained in the following Table 2.

Table 2. NCF29A1 / NCF29A2 type name format

Variable	Meaning	Values	Description
xx	Product Basic Type Name	A2	NCF29A2
		A1	NCF29A1
t	supported transponder emulation	E	HT2-E based transponder emulation
		X	HT3 based transponder emulation
		M	HT-AES based transponder emulation
		V	HT-Pro2 based transponder emulation
v	Product Version Code		
r	ROM Code ID		
ff	FabKey ID		
m	code for available amount of EROM and EEPROM	[1]	The available amount of EROM and EEPROM is adoptable on request. Up to 32 kByte user EROM and up to 2048 Byte EEPROM is supported.
n	code for available feature set	[1]	Some product features are optional and only available on request: Support for frequency bands 868 MHz and 915 MHz

[1] For details regarding the coding of the available amount of EROM and EEPROM and the available features please contact the local NXP sales representative.

1.6 Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NCF29A1EHN[1]	HVQFN32	Plastic thermal enhanced very thin quad flat package; 32 terminals; body 5 x 5 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT617-3
NCF29A1XHN[2]			
NCF29A1MHN[3]			
NCF29A1VHN[4]			
NCF29A2EHN[1]	HVQFN32	Plastic thermal enhanced very thin quad flat package; 32 terminals; body 5 x 5 x 0.85 mm; terminal pitch 0.5 mm; wettable flanks	SOT617-3
NCF29A2XHN[2]			
NCF29A2MHN[3]			
NCF29A2VHN[4]			

[1] EHN version contains a HT2-Extended based transponder emulation (legacy support, not recommended for future design in)

[2] XHN version contains a HT3 based transponder emulation

[3] MHN version contains a HT-AES based transponder emulation

[4] VHN version contains a HT-Pro2 based transponder emulation

1.7 Marking

Table 4. NCF29A1 / NCF29A2 marking codes

Type number	Marking code
NCF29A1xHN[1]	Line A: A1xnn[1][2] Line B: db_as[3] Line C: ZSywwrs[4]
NCF29A2xHN[1]	Line A: A2xnn[1][2] Line B: db_as[3] Line C: ZSywwrs[4]

[1] “x” is a code in the product type name indicating the supported transponder emulation:

E: HT2-E based transponder emulation, legacy support, not recommended for future design in

X: HT3 based transponder emulation

M: HT-AES based transponder emulation

V: HT-Pro2 based transponder emulation

[2] “nn” is a two digit code referring to a specific rom code version, to a specific fabkey data image and the supported feature set. For details contact your local NXP sales representative.

[3] ‘db_as’ is a five digit batch code: first two digits for DBSN followed by ‘_’ and last two digits for ASID

The Assembly Sequence ID (ASID) is a 2-digit indicator that counts the number of assembly batches (transport lots) within one diffusion batch id and one weekly date code. The week start and end dates are defined by the assembly center algorithm. The ASID is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero ‘0’ is only allowed within the sequence of 01 to 99. The alphabet letter ‘O’ is not allowed to avoid confusion with numeric ‘0’.

The Diffusion Batch Sequence Number (DBSN) is a 2-digit indicator that counts the number of diffusion batches (DBID) within one Package Type (i.e. HVQFN32) and one weekly date code. The DBSN is assigned sequentially starting with 01 and ranging through 99, then each digit ranges upper case alphabet letters in combination with numeric, then numeric in combination with upper case alphabet letters, then upper case alphabet letters in combination with upper case alphabet letters providing 1175 possible values within a week-code. The numeric zero ‘0’ is only allowed within the sequence of 01 to 99. The alphabet letter ‘O’ is not allowed to avoid confusion with numeric ‘0’.

[4] yww is a three digit Date code: “YWW”, ** refers to a two digit arbitrary character

“Y” is a code indicating the year in which the IC is assembled. Examples: for year 1999 is Y = 9, for year 2000 is Y = 0, for year 2001 is Y = 1. ”WW” is a code indicating the week in which the IC is assembled. It is determined from the date the assembly transport lot is created or alternately the date die is issued from die stores to assembly start or the date die attach (Diebond) occurs or the date encapsulation occurs. Examples: for week 01 is WW = 01, for week 52 is WW = 52, for week 53 is WW = 53.

“r” is the product version code referring to the fab indicator, mask versions and package versions.

“s” is the memory size code referring to the available amount of EROM and EEPROM.
For details contact your local NXP sales representative.

1.8 Block diagram

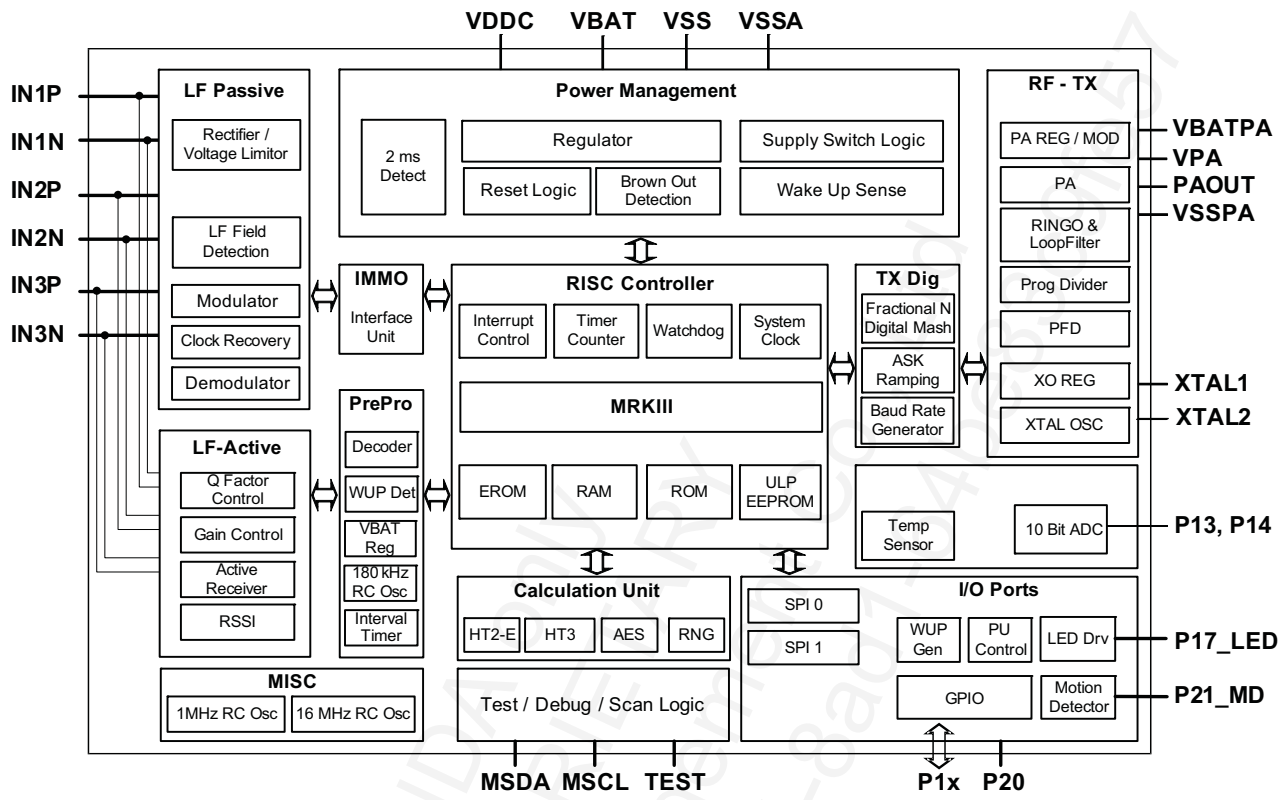
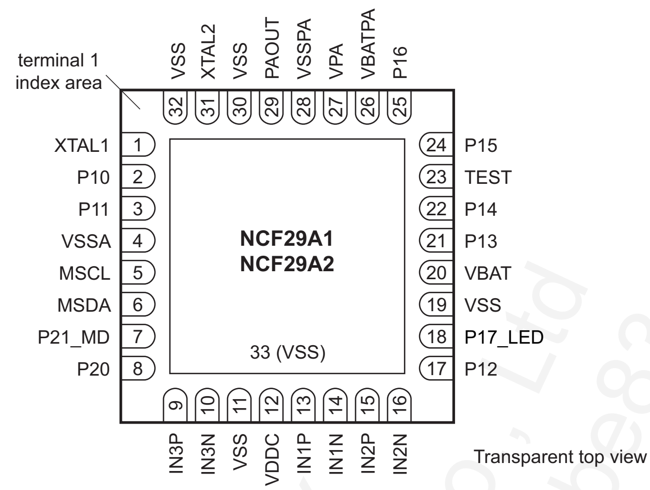


Fig 2. NCF29A1 / NCF29A2 block diagram

1.9 Pinning information

1.9.1 Pinning

The pin configuration of the NCF29A1 / NCF29A2 in HVQFN32 package is shown in Figure 3.



(1) Pinning in Top View

Fig 3. Pin configuration HVQFN32 (SOT617-3)

1.9.2 Pin description

Table 5. Pin description

Symbol	Pin	Description
XTAL1	1	crystal oscillator interface
P10	2	general purpose digital IO
P11	3	general purpose digital IO
VSSA	4	common ground
MSCL	5	debug interface. MSCL is an output and shall be unconnected in the application.
MSDA	6	debug interface. MSDA features an on-chip pull-up to VBAT and may be left open or terminated to VBAT.
P21_MD	7	general purpose digital IO, Motion Sensor Interface
P20	8	general purpose digital IO
IN3P	9	LF input, transponder and active interface (LF antenna)[2]
IN3N	10	LF input, transponder and active interface (LF antenna)[2]
VSS	11	common ground
VDDC	12	device LF field supply voltage
IN1P	13	LF input, transponder and active interface (LF antenna)[2]
IN1N	14	LF input, transponder and active interface (LF antenna)[2]
IN2P	15	LF input, transponder and active interface (LF antenna)[2]
IN2N	16	LF input, transponder and active interface (LF antenna)[2]
P12	17	general purpose digital IO
P17_LED	18	general purpose digital IO, LED driver pin
VSS	19	common ground
VBAT	20	battery supply
P13	21	general purpose digital IO

Table 5. Pin description

Symbol	Pin	Description
P14	22	general purpose digital IO
TEST[1]	23	test terminal - not used in application
P15	24	general purpose digital IO
P16	25	general purpose digital IO
VBATPA	26	battery supply
VPA	27	choke supply
VSSPA	28	ground power amplifier
PAOUT	29	power amplifier output
VSS	30	common ground
XTAL2	31	crystal oscillator interface
VSS	32	common ground
EP[1]	33	exposed die pad

[1] Terminal must be connected to VSS

[2] NCF29A2 (1D) supports only one LF antenna input for the transponder on IN1P and IN1N

2. Design information

2.1 Special function register set

Table 6 summarizes the device Special Function Register (SFR) set. It comprises registers containing configuration bits, status bits, control bits and data bits that serve to operate the device. The detailed bit descriptions are given in the corresponding sections.

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
CPU/MMU Exceptions [6]	CXPC	0014h	CPU Exception PC value	VDD
	CXSW	0016h	CPU Exception code	
Port 1/2 [4]	P1INS	0019h	Port 1 input sense register	VDD
	P1OUT	001Ah	Port 1 output control register	
	P1DIR	001Bh	Port 1 direction control register	
	P2INS[5]	001Ch	Port 2 input sense register	
	P2OUT[5]	001Dh	Port 2 output control register	
	P2DIR[5]	001Eh	Port 2 direction control register	
	P1INTDIS	001Fh	Port 1 Interrupt Disable	
	P2INTDIS[5]	0020h	Port 2 Interrupt Disable	
	P1ALTF[5]	00ECh	Port 1 alternative digital functions register	
	P2ALTF[5]	00EEh	Port 2 alternative digital functions register	
	P1WRES[2]	00C8h	Port 1 Pull-up Resistor Configuration	VBAT
	P2WRES[3]	00C9h	Port 2 Pull-up Resistor Configuration	
	PRESWUP0	00C2h	Port 1 Wake-up Configuration P12-P15	
	PRESWUP1	00C4h	Port 1 Wake-up Configuration P16-P21	
	PRESWUP2[5]	00C6h	Port 2 Wake-up Configuration, reserved for future use	
IIU [2]	IIUDAT	0025h	IIU data register	VDD
	IIUCON0	0022h	IIU control register 0	
	IIUCON1	0024h	IIU control register 1	
	IIUCON2 [6]	0021h	IIU control register 2	
	IIUSTAT	0023h	IIU status register	
	IIUSTATE	0026h	IIU state register	
HT calculation unit[2]	HTCON	0027h	HT control register	VDD
AES [2]	AESDAT	0028h	AES data register	VDD
	AESCON	002Ah	AES control register	
Watchdog timer[2]	WDCON	0037h	Watchdog timer control register	VDD
Clock Control[2]	CLKCON0[3]	0038h	Clock Control register 0	VDD
	CLKCON1	0039h	Clock Control register 1	
	CLKCON2	003Ah	Clock Control register 2	
	CLKCON4[6]	003Fh	Clock Control register 4	
Timer Clocks[4]	CLKCON3	003Dh	Timer multiplexors control register	VDD

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
LF Active Preprocessor, Interval Timer, Real-time Clock [4]	PREDAT	0040h	Pre-processor data register	VBATREG
	RTCCON	0041h	Real-time clock control register 1	
	PRECON2[5]	0042h	Pre-processor control register 2	
	PRECON3	0043h	Pre-processor control register 3	
	PRECON4	0044h	Pre-processor control register 4	
	PRECON5	0045h	Pre-processor control register 5	
	PRECON6[5]	0046h	Pre-processor control register 6	
	PRECON7	0047h	Pre-processor control register 7	
	PRECON8[5]	0048h	Pre-processor control register 8	
	PRECON9[5]	0049h	Pre-processor control register 9	
	PRECON10[5]	006Eh	Pre-processor control register 10	
	PRECON11[6]	006Fh	Pre-processor control register 11	
	PRECON12[6]	00F9h	Pre-processor control register 12, reserved for future use	
	PREPD[5]	004Ah	Pre-processor control power down	
	PRESTAT[5]	005Ch	Pre-processor status register	
	WUP1W0	005Eh	Pre-processor wake-up pattern register 1	
	WUP1W1	0060h	Pre-processor wake-up pattern register 1	
	WUP2W0	0062h	Pre-processor wake-up pattern register 2	
	WUP2W1	0064h	Pre-processor wake-up pattern register 2	
	WUP3W0	0066h	Pre-processor wake-up pattern register 3	
	PRET	0068h	Pre-processor T timing calibration register	
	PRE3T	006Ah	Pre-processor 3T timing calibration register	
	RTCDAT	006Ch	Pre-processor Real Time Clock register	
Polling Configuration[6]	PREPOLL0	00F7h	Pre-processor polling control register 0	VBATREG
	PREPOLL1	00F8h	Pre-processor polling control register 1	
Motion Sensor Interface[6]	MSICON0	00FAh	Motion sensor control register 0	VBATREG
	MSICON1	00FBh	Motion sensor control register 1	
	MSISTAT0	00FCh	Motion sensor status register 0	
	MSISTAT1	00FDh	Motion sensor status register 1	
ADC[2]	ADCDAT	0072h	ADC data register	VDD
	ADCCON[3]	0074h	ADC control register	
RSSI[4]	RSSICON[5]	007Ch	RSSI control register	VDD
ULP EEPROM [2]	ULPDAT	0085h	ULP EEPROM data register	VDD
	ULPCON0	0084h	ULP EEPROM control register 0	
	ULPCON1	008Ah	ULP EEPROM control register 1	
	ULPSEL	0082h	ULP EEPROM selection register	
	ULPADDR	0080h	ULP EEPROM address register	

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
Timer 0 [2]	T0REG	0096h	Timer 0 register	VDD
	T0CON0	0094h	Timer 0 control register 0	
	T0CON1	0095h	Timer 0 control register 1	
	T0RLD	0098h	Timer 0 reload register	
Timer 1 [2]	T1REG	009Eh	Timer 1 register	VDD
	T1CON0	009Ah	Timer 1 control register 0	
	T1CON1	009Bh	Timer 1 control register 1	
	T1CON2	009Ch	Timer 1 control register 2	
	T1CMP	00A2h	Timer 1 compare register	
	T1CAP	00A0h	Timer 1 capture register	
Timer 2 [2]	T2REG	00A6h	Timer 2 register	VDD
	T2CON0	00A4h	Timer 2 control register 0	
	T2CON1	00A5h	Timer 2 control register 1	
	T2RLD	00A8h	Timer 2 reload register	
RNG[2]	RNGDAT	00AAh	Random number generator data register	VDD
	RNGCON	00ACh	Random number generator control register	
Interrupt system[2]	INTEN0	00B3h	User interrupt enable register 0	VDD
	INTEN1	00B4h	User interrupt enable register 1	
	INTEN2	00B5h	User interrupt enable register 2	
	INTEN3[6]	0101h	User interrupt enable register 3	
	INTCON	00AFh	Interrupt control register	
	SYSINTEN0	00B6h	System interrupt enable register 0	
	SYSINTEN1	00B7h	System interrupt enable register 1	
	INTFLAG0	00B0h	Interrupt request flag register 0	
	INTFLAG1	00B1h	Interrupt request flag register 1	
	INTFLAG2	00B2h	Interrupt request flag register 2	
	INTFLAG3[6]	0100h	Interrupt request flag register 3	
	INTSET0	00B8h	Interrupt set register 0	
	INTSET1	00B9h	Interrupt set register 1	
	INTSET2	00BAh	Interrupt set register 2	
	INTSET3[6]	0102h	Interrupt set register 3	
	INTCLR0	00BBh	Interrupt clear register 0	
	INTCLR1	00BCh	Interrupt clear register 1	
	INTCLR2	00BDh	Interrupt clear register 2	
	INTCLR3[6]	0103h	Interrupt clear register 3	
	INTVEC	00BEh	User interrupt vector address	
Battery Control[4]	BATSYS0[5]	00C0h	Battery domain system control register 0	VBAT
	BATSYS1	00C1h	Battery domain system control register 1	

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
Regulated Battery Domain user registers [4]	USRBATRGL0	004Ch	Pre-processor user register 0	VBATREG
	USRBATRGL1	004Dh	Pre-processor user register 1	
	USRBATRGL2	004Eh	Pre-processor user register 2	
	USRBATRGL3	004Fh	Pre-processor user register 3	
	USRBATRGL4	0050h	Pre-processor user register 4	
	USRBATRGL5	0051h	Pre-processor user register 5	
	USRBATRGL6	0052h	Pre-processor user register 6	
	USRBATRGL7	0053h	Pre-processor user register 7	
Battery Domain user registers[4]	USRBAT0	00CAh	Battery domain user register 0	VBAT
	USRBAT1	00CBh	Battery domain user register 1	
	USRBAT2	00CCh	Battery domain user register 2	
	USRBAT3	00CDh	Battery domain user register 3	
	USRBAT4	00CEh	Battery domain user register 4	
	USRBAT5	00CFh	Battery domain user register 5	
	USRBAT6	00D0h	Battery domain user register 6	
	USRBAT7	00D1h	Battery domain user register 7	
LF Tune [6]	LFTUNEVBAT	00D2h	Battery domain LF tuning register	VBAT
LF Tune [6]	LFTUNEVDD	00D4h	Vdd domain LF tuning register	VDD
LF Short [6]	LFSHCON	00D6h	LF Channels short control register	VDD
Power management [4]	PCON0[5]	00D8h	Power control register 0	VDD
	PCON1[5]	00D9h	Power control register 1	
	PCON2[5]	00DAh	Power control register 2	
SPI0[4]	SPI0CON0	00E0h	SPI0 control register 0	VDD
	SPI0CON1	00E1h	SPI0 control register 1	
	SPI0DAT	00E2h	SPI0 data register	
	SPI0STAT	00E3h	SPI0 status register	
SPI1[4]	SPI1CON0	00E4h	SPI1 control register 0	VDD
	SPI1CON1	00E5h	SPI1 control register 1	
	SPI1DAT	00E6h	SPI1 data register	
	SPI1STAT	00E7h	SPI1 status register	
Mathematical/ logical registers [4]	BITSWAP	00F2h	Bit swap register	VDD
	BITCNT	00F0h	Bit count register	
	CRCDAT	002Ch	CRC data register	
	CRC8DIN	002Eh	CRC data input register	
TX Power Control[2]	TXPCON	0104h	TX Power Control register	VDD
TX Clock Reset Control [2]	CLKRSTCON	0105h	TX Clock and Reset Control register	VDD
VCO Calibration Control [2]	VCOCALCON	0106h	VCO Calibration Control register	VDD
TX PLL Control [2]	PLLCON	0107h	PLL Control register	VDD

Table 6. Device register set

Peripheral	Register name[1]	Address	Description	Supply domain
TX Data Encoder [2]	TXDAT	0108h	TX Data register	VDD
	TXSPC	010Ah	Transmission space masking register	
	ENCCON0	010Ch	TX Encoder control register 0	
	ENCCON1	010Eh	TX Encoder control register 1	
TX Frequency Control [2]	FREQCON0	0110h	Frequency control register 0	VDD
	FREQCON1	0112h	Frequency control register 1	
TX Baud Rate Control [2]	BRGCON	0114h	Baud Rate control register	VDD
TX Modulation Control [2]	FSKCON	0116h	FSK control register	VDD
	FSKRMP	0117h	FSK ramp control register	
	ASKCON	0118h	ASK control register	
	ASKRMP	011Ah	ASK ramp control register	
TX PA control [2]	PACON [3]	011Bh	PA control register	VDD
	PAPWR [3]	011Ch	PA power control register	
	PATRIM [6]	011Dh	PA reference trimming register	
	PALIMIT[6]	011Eh	PA current limiter control register	

[1] In the detailed register descriptions, bits marked 'RFU' are reserved for future use. Note that read operation to 'RFU' bits may return an undefined result. For future compatibility, a write operation shall assign a '0'.

[2] Register group as in predecessor device, NCF2960

[3] Register differs from the predecessor device, NCF2960

[4] Register group as in predecessor devices, NCF2971, NCF2950, NCF2951, NCF2952

[5] Register differs from the predecessor devices, NCF2971, NCF2950, NCF2951, NCF2952

[6] New register in NCF29A1 / NCF29A2

[7] Under normal operating conditions all registers belonging to VBAT domain keep their content as long as VBAT power supply is maintained and BATPOR is not asserted. Its recommended that the application software refreshes these registers to improve the system robustness in case of ESD stress conditions.

[8] Under normal operating conditions all registers belonging to VBATREG domain keep their content as long as VBATREG power supply is maintained. Its recommended that the application software refreshes these registers to improve the system robustness in case of ESD stress conditions.

2.2 Power management

2.2.1 Power supply domains

The NCF29A1 / NCF29A2 features several power supply domains (see Figure 4). A versatile power management (see Figure 5) enables the device to derive its power supply from two different energy sources

- External battery (VBAT, VBATPA)
- Low frequency field (VFLDLF)

The two corresponding power supply domains VBAT (VBATPA) and VFLDLF are unregulated. The device is able to operate when any of the energy sources is available regardless the presence or absence of the other.

Derived from either of the two unregulated domains are the regulated power supply domains:

- Digital core supply (VDD)
- Analogue core supply (VDDA)

Derived from the unregulated battery domain are the regulated power supply domains:

- Digital battery supply (VBATREG)
- Analogue battery supply (VBATAREG)
- Crystal oscillator supply (VDDXO)
- Analogue PLL supply (VDDPLL)
- Digital PLL supply (VDDHS)
- Power amplifier internal supplies (VDDPA)

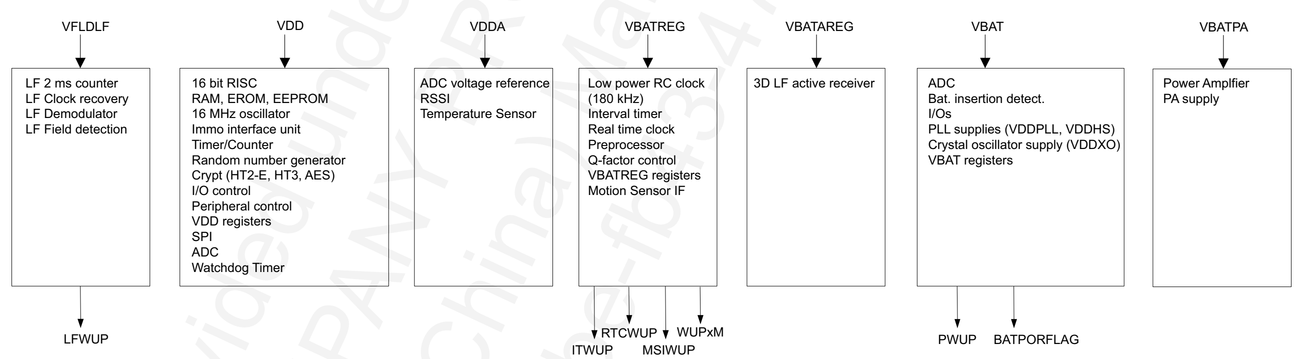


Fig 4. Power Supply Domains

The Digital core supply (VDD) can be derived from the two unregulated domains VBAT and VFLDLF. The regulated analogue core supply (VDDA) supplies the RSSI and ADC bandgap for supply voltage measurements.

The crystal oscillator, PLL, PA, LF active supplies (VDDXO, VDDPLL, VDDHS, VDDPA, VBATREG, VBATAREG) can only be derived from battery pin (VBAT, VBATPA).

Except VDD, the voltage regulators for the digital and analogue supplies are turned off after device start-up. In order to employ the blocks supplied with these voltages, the respective dedicated voltage regulators have to be activated first.

Determining the appropriate supply configuration is accomplished by means of the power supply control (Figure 5).

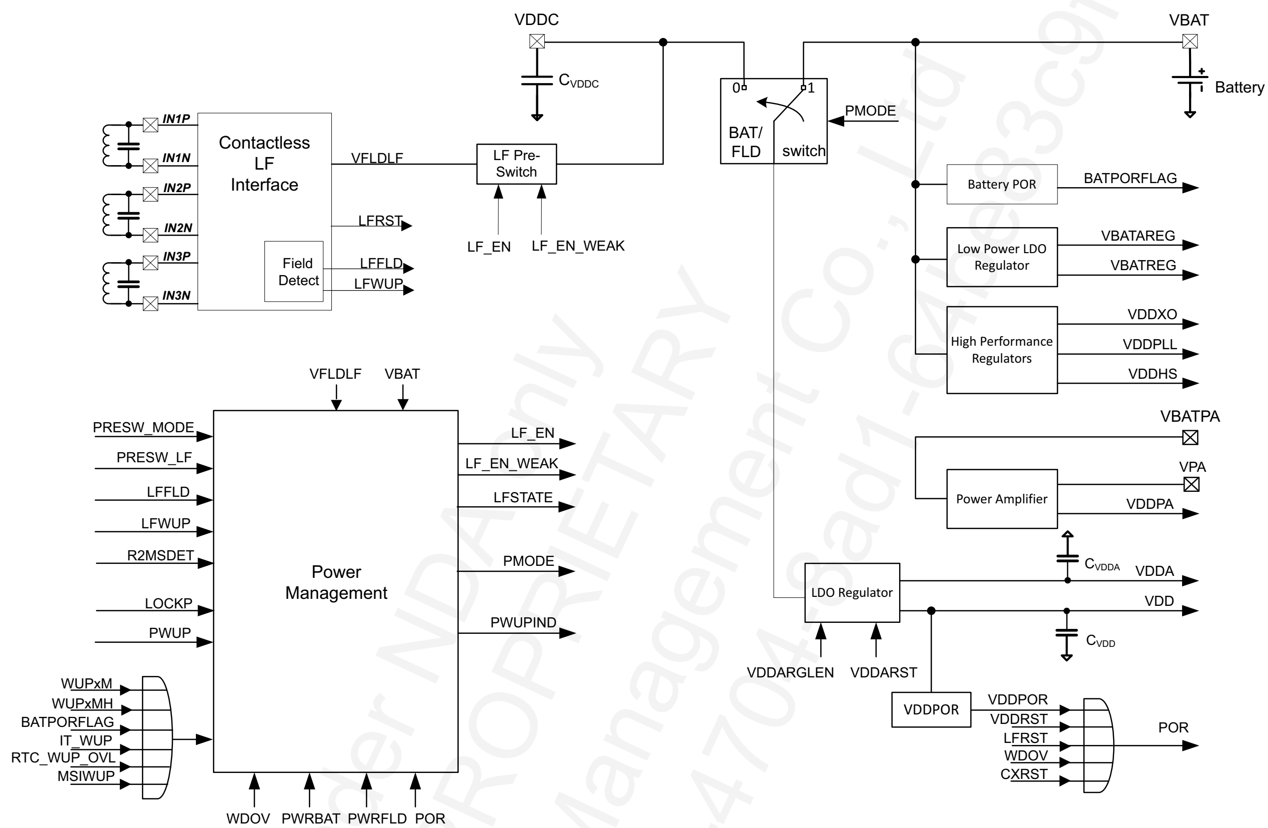


Fig 5. Power supply control

2.2.2 Power supply control

2.2.2.1 Power supply switch

The NCF29A1 / NCF29A2 provides several switches for power supply selection of the core. The main supply switch selects between battery and field supply (set by PWRBAT and PWRFLD).

The field supply is based on one pre-switch for the LF. The pre-switch consist of a weak and a strong part. It can be activated either in one or two stages. The weak pre-switch features a current limitation in order to limit the energy transferred from the field into the blocking capacitor at VDDC. This avoids deep dips in the field supply, which might be erroneously interpreted as a load modulation by the base station.

When the power supply state is changed the device supply switch opens the existing connection before connecting the new supply. The device is powered for a short period of time from the internal blocking capacitor. Therefore, the application shall minimize the current consumption when changing the supply state to prevent an accidental power-on reset.

2.2.2.2 Device wake up

The following wake up events terminate the POWER OFF state:

- Presence of LF field
- Port wake-up (button press)
- Motion sensor wake-up
- Detection of valid LF active wake-up pattern
- Interval counter or real time clock wake-up
- Battery insertion

If a wake-up event emerges, the power management selects the corresponding power supply. If more than one wake-up event is pending at the same time, the power management automatically selects the strongest available supply source related to the wake-up event.

Once the supply voltage (VDD) exceeds the power on reset threshold voltage (V_{POR}), the power management state is locked and the power on reset comparator output signal (VDDPOR) becomes low. After a short delay (t_{POR_HLD}), the RISC becomes operational and the device enters RUN mode (Figure 6). All further supply state changes are under control of the application.

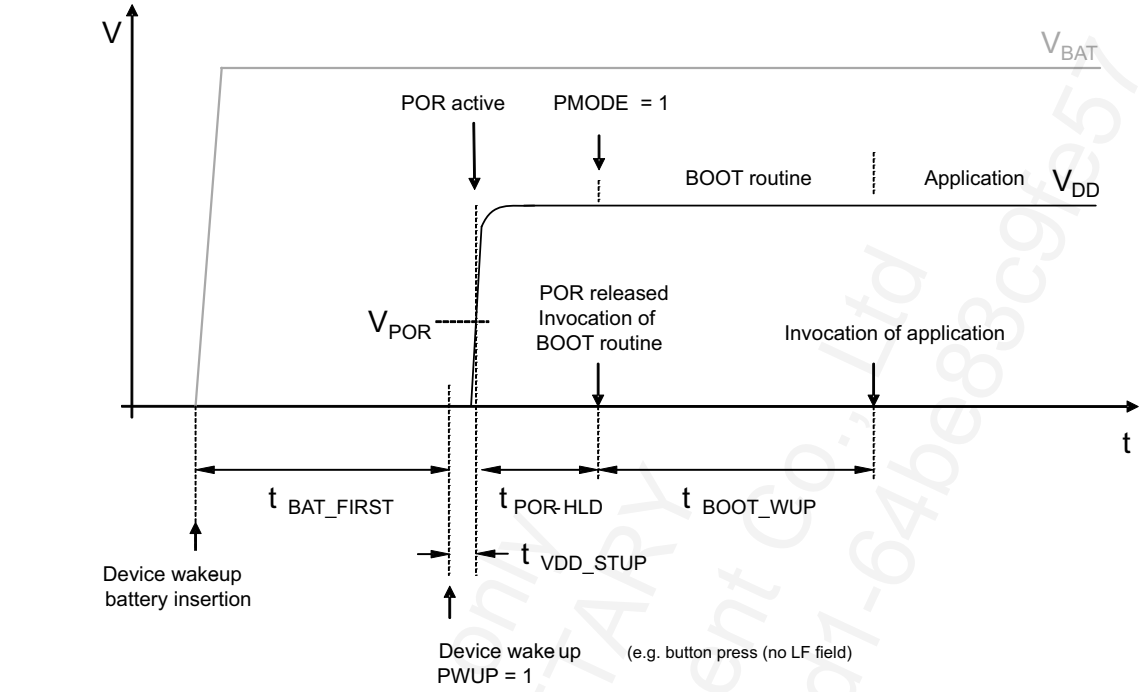
Starting with the BOOT sequence, the power supply state of the VDD supplied part can be monitored and influenced via the power control registers. A change of the supply configuration may apply e.g. in case an LF Field and button press is detected at the same time or in case an LF Field is being detected while battery supply has been utilized. If an LF field and button press event are detected at the same time, then the LF field wake up has precedence and will commence.

2.2.2.3 Device reset

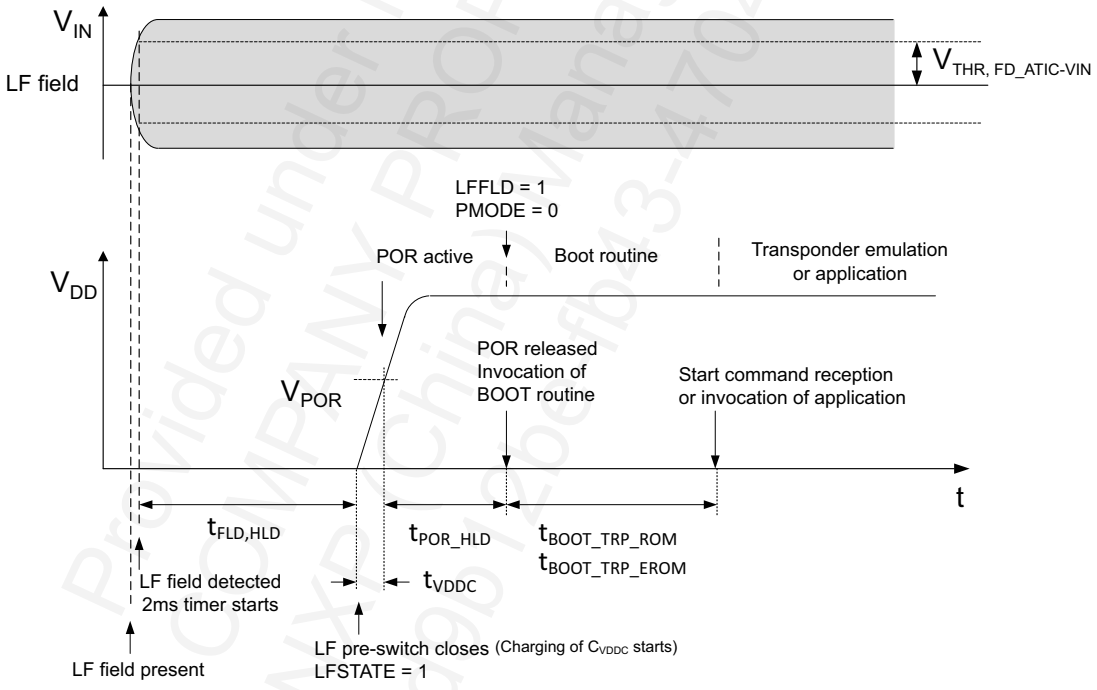
The device supply voltage (VDD) is monitored by a power on reset circuitry. A reset (POR) is generated under the following conditions:

- The device leaves the POWER-OFF state
- VDD brown out is detected and code is executed from EROM or a VDD brown out is detected and the CPU clock source is set to a frequency greater than 8MHz.
- Voltage level at VDD falls below power-on reset threshold (VDDPOR)
- LF field emerges and LFNMIEN bit is '0' (LFRST)
- Watchdog overflow (WDOV)
- VDDRST is set by the application (Software reset)
- CPU/MMU exception occurs and CXNMIEN bit is '0' (CXRST)

Upon a device reset the power management logic is released and starts with a new evaluation of the supply condition.



a) Battery supplied application



b) LF field supplied application

Fig 6. Power up timing

2.2.2.4 Power supply states

Dependent on whether the device power is derived from an external battery or from either the LF field, the device supports two different core supply states:

- Battery supply (BATTERY)
- LF field supply (LF FIELD)

These two supply states are CPU active states. In POWER OFF state, the device remains in a third very low power state (see Figure 7).

Determining the appropriate supply configuration is accomplished by means of the ROM implemented device BOOT sequence called by the RISC controller during device power-up.

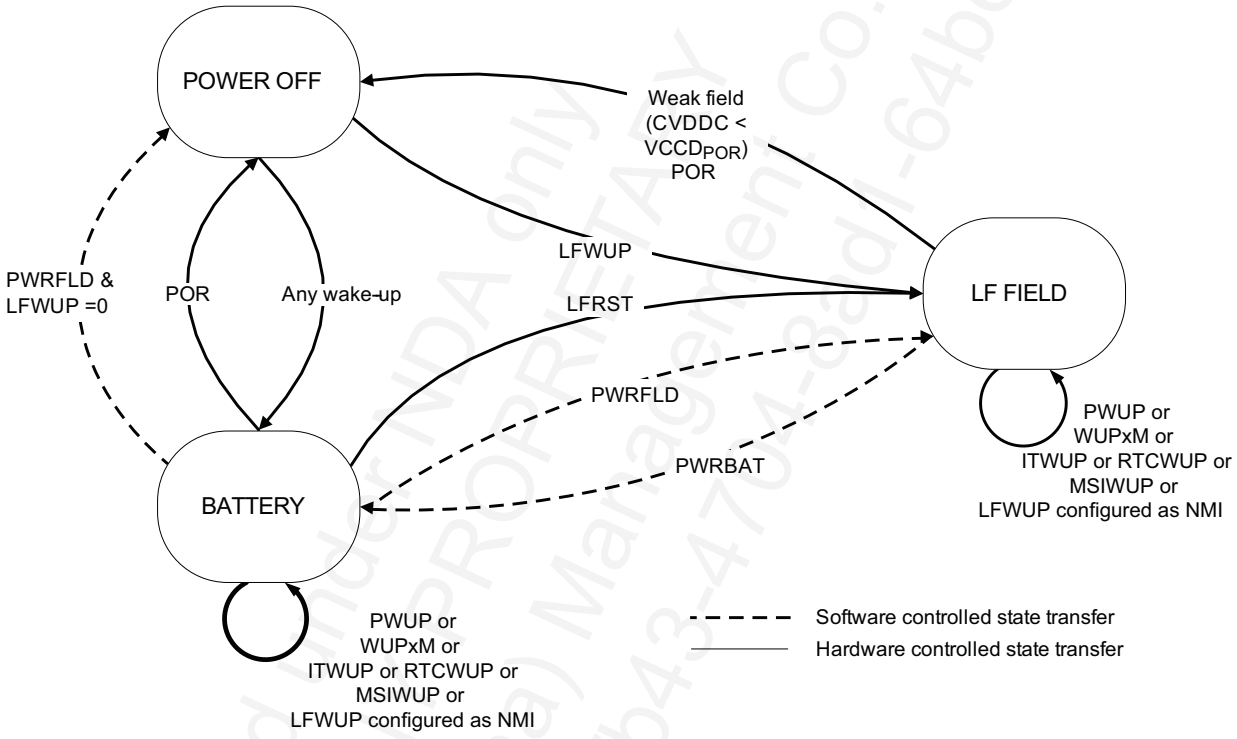


Fig 7. Power Supply States

2.2.2.5 POWER OFF state

In POWER OFF state, most blocks of the device are internally disconnected from the battery supply, resulting in a very low current consumption. The internal device supply voltage (VDD) stays below the Power On Reset threshold voltage and device operation is halted. Only a minimum of circuitry remains operational, like the power management and I/O ports (configured as input).

The device resides in POWER OFF state any time a Power On Reset comparator output (VDDPOR) condition is applicable because of a weak supply condition. The POWER OFF state is terminated by a Wake Up event, like the presence of an LF Field (LFWUP) or a Port Wake Up (PWUP).

Once the supply condition is evaluated during device power-up and the BOOT sequence is completed, the device will start execution of the application program in either BATTERY state or LF FIELD state.

2.2.2.6 BATTERY state

In BATTERY state, the device is powered from the external battery. After execution of the BOOT sequence, device operation is controlled by the RISC and the program code starts at the BATTERY WARM BOOT vector. The application code can terminate the BATTERY state.

In case an LF field is detected, the device behavior depends on the configuration. If according to the configuration an NMI is caused after field detection, the state is kept and control is still with the RISC. If according to the configuration a reset is caused by field detection, the boot routine is invoked again and the state is changed to LF FIELD, dependent on whether the LF Field has been detected. Activating the LF Field switches also provokes a state change to LF FIELD.

Button events do not cause a state change and have to be handled via the RISC. In case no LF Field is present, and the device supply drops below the Power On Reset threshold voltage, the device enters POWER OFF state.

2.2.2.7 LF FIELD state

In LF FIELD state the device supply is derived from the LF Interface.

After execution of the BOOT sequence, device operation is controlled by the RISC and the program code starts at the LF FIELD WARM BOOT vector (unless a built-in LF transponder emulation is selected in the boot routine).

The LF FIELD state is left either in case of a weak LF Field supply condition, branching to POWER OFF state, or forced by the application program when activating the Battery Supply switch. The state changes to BATTERY state.

2.2.3 Battery supply states

The battery supply domains VBATREG and VBATAREG supports the two supply states ON and OFF. A state change can be initiated via the control bits BATRGLEN and BATRGLRST.

The battery supply states are independent of the power supply states which are related to the core.

2.2.4 Registers

2.2.4.1 Battery system register BATSYS0

The battery system register BATSYS0 controls the VBAT regulator. The VBAT regulator shall be turned on in order to get access to the blocks supplied by the regulated battery supplies VBATREG and VBATAREG, like the interval timer and LF active preprocessor.

BATSYS0 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 7. Battery system register BATSYS0 (reset value xxxx_x101b)

Bit	Symbol	Access	Value	Description
7 to 3	RFU	R		Reserved for future use
2	BATRGLRST	R		Static reset of VBATREG supplied part
			0	Release reset
			1	Reset
1	BATRGLEN	R		VBAT regulator enable
			0	Disable
			1	Enable
0	BATPORFLAG	R		VBAT power-on reset flag
			0	Clear
			1	Set

BATRGLRST, static reset of VBATREG supplied part

Setting BATRGLRST resets the battery powered registers in the VBATREG domain.

BATRGLEN, VBAT regulator enable

BATRGLEN turns on and off the VBAT regulator.

BATPORFLAG, VBAT power-on reset flag

Sets or clears the Battery Power On Reset (BATPOR) flag. If BATPOR is low and BATPORFLAG is high a battery insertion device wake-up occurs.

2.2.4.2 Battery system register BATSYS1

The battery system register BATSYS1 controls the battery reset.

BATSYS1 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 8. Battery system register BATSYS1 (reset value xxxx_xxx0b)

Bit	Symbol	Access	Value	Description
7 to 1	RDT	R		Reserved for device test
0	BATRST	R		Reset of VBAT supplied part
			0	No effect
			1	Reset

BATRST, reset of VBAT supplied part

Setting this bit has the same effect as a battery reset caused by a battery insertion. All registers supplied with VBAT are initialized to their default states. The VBAT regulator is turned off and BATRGLRST is set.

2.2.4.3 Power control register PCON0

The power control register PCON0 provides means to select the supply state of the device and the behavior of the LF passive mode.

Table 9. Power control register PCON0 (reset value 0100_x000b)

Bit	Symbol	Access	Value	Description
7	VDDRST	R0[1]/W		Reset of VDD supplied part
			0	No effect
			1	Reset
6	VDDARST	R/W		Static reset of VDDA supplied part
			0	Release reset
			1	Reset
5	VDDARGLEN	R/W		Enable VDD regulator for battery and die temperature measurement
			0	Disable
			1	Enable
4	PRESW_MODE	R/W		Pre-switch mode
			0	see Table 10
			1	see Table 10
3	VBATBRNIND	R		2.4 V VBAT brown-out indicator flag
			0	The voltage level at VBAT is above the brown-out indicator threshold $V_{VBATIND}$ (typ. 2.4 V)
			1	The voltage level at VBAT is below the brown-out indicator threshold
2	PRESW_LF	R/W		Pre-switch for LF supply
			0	see Table 10
			1	see Table 10
1	PWRBAT[2]	R0/W		Activate power supply from battery
			0	No effect
			1	Activate
0	PWRFLD[2]	R0/W		Activate power supply from field
			0	No effect
			1	Activate

[1] R0 means the return value is always 0

[2] If PWRBAT and PWRFLD are set to '1' at the same time, PWRFLD has priority.

VDDRST, Reset of VDD supplied part

Setting VDDRST triggers a reset (POR) and sets the device in POWER OFF state, a reset of the entire VDD supplied part is executed, the VDDA regulator will be turned off and the bit VDDARST is set. VDDRST reads always ‘0’. A pending wake-up triggers an immediate re-boot of the device.

VDDARST, static reset of VDDA supplied part

VDDARST is a static reset signal for the VDDA supplied part. If the VDDA regulator is turned off (VDDARGLEN = '0'), VDDARST is always active.

Setting VDDARST to '0' releases the reset of the VDDA supplied part and is only possible when the VDDA regulator is turned on (VDDARGLEN = '1'). Before VDDARST can be released, the VDDA regulator start-up time $t_{VDDA,PON}$ must be considered.

VDDARGLEN, VDDA regulator enable

The VDDA regulator is turned on and off by setting and resetting VDDARGLEN, respectively. For VDDARGLEN = '0', VDDARST will become '1' automatically.

Example: In order to turn on the VDDA regulator, execute the following steps:

- Set VDDARGLEN to '1': This activates the VDDA regulator.
- Wait the time $t_{VDDA,PON}$ until the voltage at VDDA has stabilized (do not use the VDDA brown-out detector flag VDDABRNFLAG to determine this time).
- Reset VDDARST to release the static reset and to activate the VDDA domain.

The application shall only enable the VDDA regulator, if the voltage at VDD is sufficiently large, i.e. the VDD brown-out flag VDDBRNFLAG is '0'. Otherwise the activation of the VDDA regulator can generate a VDD reset.

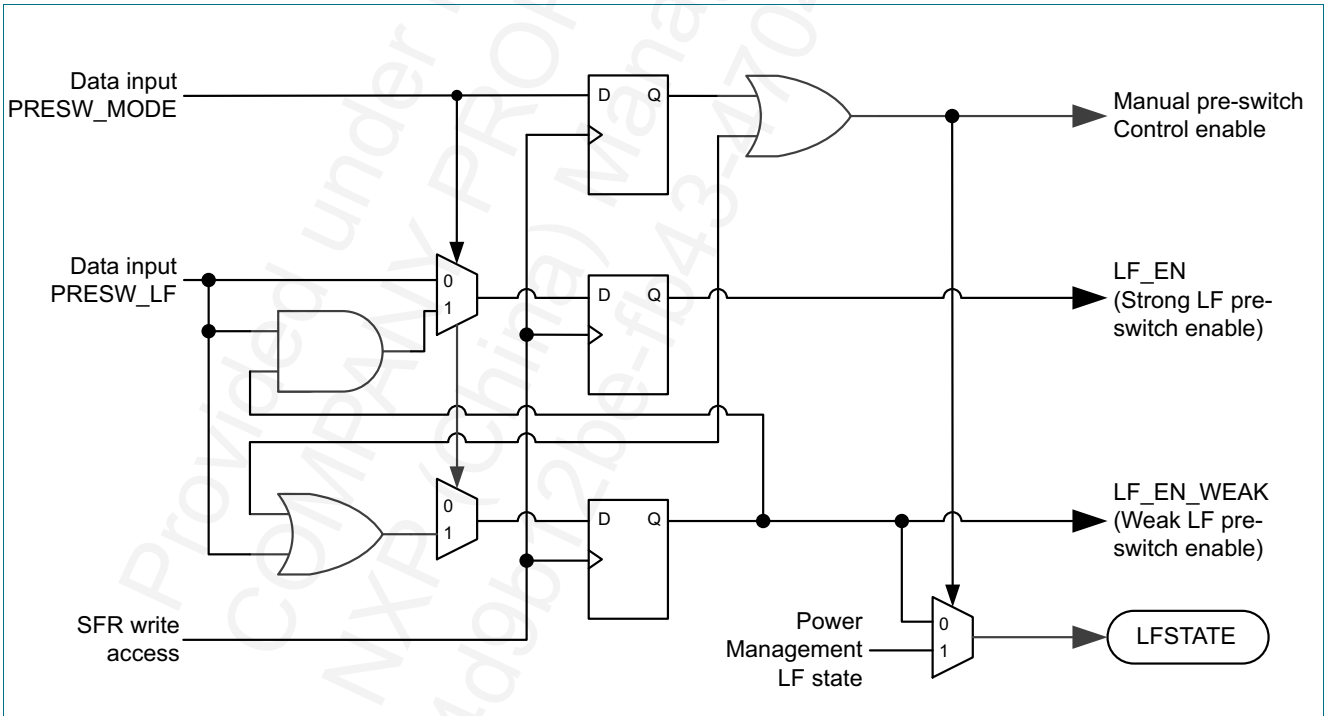


Fig 8. Manual LF pre-switch control

PRESW_MODE, PRESW_LF, Activate LF field pre-switch

These two control bits are used to activate the pre-switch for LF field supply (Figure 8). If at least one of these bits is set, the LF pre-switch is controlled manually by the application and the state of the power management field selection after device start-up is ignored.

The control of PRESW_MODE and PRESW_LF is organized in a state machine, which valid state transitions are given in Table 10.

Table 10. Valid state transitions for PRESW_MODE, PRESW_LF and LFSTATE

Previous state			New data		Next state		
PRESW _MODE	PRESW_LF	LFSTATE	PRESW_ MODE	PRESW_LF	PRESW _MODE	PRESW_LF	LFSTATE
X	X	X	0	0	0	0	0
X	X	X	0	1	0	1	1
X	0	0	1	0	1	0	0
X	0	0	1	1	1	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	1	1
X	1	1	1	0	1	0	1
X	1	1	1	1	1	1	1

If PRESW_MODE is equal to '0' the bit PRESW_LF controls the weak and the strong pre-switches directly. It is possible to activate and deactivate the pre-switches with one write access.

If the bit PRESW_MODE is equal to '1' the weak and the strong pre-switch can be activated and deactivated in a sequence. If a '1' is written to PRESW_LF the weak pre-switch is activated, while the register bit PRESW_LF is not yet set. Instead a shadow flag is set, which activates the weak pre-switch. The state of the weak pre-switch can be observed via the control bit LFSTATE in this case. The strong pre-switch is finally activated, if the application writes another '1' to register PRESW_LF. The de-activation follows the same procedure: The first '0' deactivates the strong pre-switch and the second '0' the weak one.

The value, which is written to PRESW_MODE at the same time when PRESW_LF is written, determines the mode rather than the stored value in the register. The register content of PRESW_MODE is required to ensure the manual pre-switch control in case no strong pre-switch is activated.

Example: In order to switch power supply from battery to LF field, execute the following steps:

- Close the pre-switch of the LF supply by writing a '1' to PRESW_LF. The blocking capacitor at pin VDDC gets charged (if the activation of the strong pre-switch causes a too deep dip in the field supply it is also possible to close only the weak pre-switch prior to the strong one).
- Wait until the voltage at VDDC has settled. The waiting time shall be properly determined for specific capacitance values and field strengths by the user.
- Set the bit PWRFLD to '1' to commutate from battery supply to field supply.

VBATBRNIND, Weak battery indicator

Battery monitoring used to identify battery end of life (approximately 2.4V), VBATBRNINDEN bit must be set to '1'. The battery indicator connects a resistor load (100 to 300 kΩ) across the VBAT supply.

PWRBAT, Activate power supply from battery

If the device is supplied by field and a '1' is written to register bit PWRBAT the main supply switch commutates to battery supply. If the device is already supplied by battery writing a '1' has no effect. The bit reads always '0'.

The application shall reduce the power consumption as much as possible when changing the supply condition. Moreover, the CPU shall not run at a clock speed of more than 250 kHz when PWRBAT is set to '1'. These measures avoid an unintentional reset caused by the "break-before-make" mechanism of the supply switches.

If PWRFLD and PWRBAT are set to '1' at the same time, PWRFLD has priority.

In order to enter POWER-OFF state when the device is running with battery supply, set VDDRST to one.

PWRFLD, Activate power supply from field

If the device is supplied by the battery and a '1' is written to register bit PWRFLD the main supply switch commutates to field supply. If the device is already supplied by field, writing a '1' has no effect. The bit reads always '0'.

PWRFLD does not influence the LF field pre-switch.

The application shall reduce the power consumption as much as possible when changing the supply condition. Moreover, the CPU shall not run at a CPU clock speed of more than 250 kHz when PWRFLD is set to '1'. These measures avoid an unintentional reset caused by the "break-before-make" mechanism of the supply switches.

If PWRFLD and PWRBAT are set to '1' at the same time, PWRFLD has priority.

2.2.4.4 Power control register PCON1

The power control register PCON1 provides flags to monitor the current state of the power management, battery voltage and the field supply.

Table 11. Power control register PCON1 (reset value xx0xxxxxb)

Bit	Symbol	Access	Value	Description
7	VDDBRNFLAG	R		VDD brown-out detector flag
			0	VDD voltage level is above brown-out threshold
			1	VDD voltage level is below brown-out threshold
6	VDDABRNFLAG	R		VDDA brown-out detector flag
			0	VDDA voltage level is above brown-out threshold
			1	VDDA voltage level is below brown-out threshold
5	VBATMONEN	R/W		Battery monitoring control
			0	Battery brownout disabled
			1	Battery brownout enable

Table 11. Power control register PCON1 (reset value xx0xxxxxb)

Bit	Symbol	Access	Value	Description
4	PWRMANLFSTATE	R		LF field supply state
			0	Device start-up: LF pre-switch open (insufficient LF field) Manual control: LF pre-switch is turned off
			1	Device start-up: LF pre-switch selected by power management Manual control: Weak LF pre-switch is turned on
3	VBATBRNFLAG	R		VBAT brown-out detector flag
			0	VBAT voltage level is above brown-out threshold
			1	VBAT voltage level is below brown-out threshold
2	LFFLD	R		LF field detection
			0	LF field does not exceed detection threshold for > $t_{FLD,HLD}$ (2ms)
			1	LF field exceeds detection threshold for > $t_{FLD,HLD}$ (2ms)
1	PMODE	R		Power mode
			0	Device is powered with field supply
			1	Device is powered with battery supply
0	PWUPIND	R		Port wake-up indicator
			0	Battery supply: No effect Field supply: No port wake-up request detected
			1	Battery supply: N.A. Field supply: Port wake-up request detected

VDDBRNFLAG, VDD brown-out detector flag

The brown-out detector at VDD monitors the supply voltage level continuously and it checks, whether VDD is above or below a certain threshold that is necessary for proper read operation of the ULP EEPROM and the EROM as well a programming of all EEPROM modules. The brown-out detector uses a hysteresis, thus the activation threshold can be slightly higher than the deactivation threshold.

VDDBRNFLAG influences the bit VDDBRNREG.

A device reset is generated only, if the voltage at VDD drops below the brown-out threshold and one of the following conditions are given:

- Code is executed from the EROM

  Note: Any other read/write/program access to the EROM or EEPROM does not generate a device reset. It is up to the application to verify the brown-out flag and discard read or programmed data, if the voltage dropped below the brown-out threshold.
- A CPU clock source with a frequency greater than 8 MHz is selected (CPUCLKSEL[0] = 1b).

VDDABRNFLAG, VDDA brown-out detector flag

The brown-out detector at VDDA monitors the supply voltage level continuously and it checks, whether VDDA is above VBO,VDDA that is necessary for proper operation of all VDDA supplied parts. The brown-out detector uses a hysteresis, thus the activation threshold can be slightly higher than the deactivation threshold.

The bit VDDABRNFLAG only influences the bit VDDABRNREG but does not generate any reset or interrupt.

VBATMONEN, Battery brown-out enabled

The battery brownout detector is enabled when VBATMONEN is set to '1' and after the settling time $t_{VBATMON\_SETT}$ the battery brownout detector is operational. If the battery brownout detector is disabled by clearing the VBATMONEN bit, then VBATBRNFLAG (VBAT brown-out detector flag) and VBATBRNREG (VBAT brown-out detector register) can not be used by the application software.

PWRMANLFSTATE, power management field supply states

This bit has different meaning dependent on whether manual pre-switch control is assumed (at least one of the bits PRESW_MODE and PRESW_LF is set) or not.

In the first case this flag shows the state of the weak pre-switch, in the latter one the state of the field selection of the power management after device start-up.

VBATBRNFLAG, VBAT brown-out detector flag

The brown-out detector at VBAT monitors the supply voltage level continuously only if VBATMONEN is set to '1'. It checks whether VBAT is above or below a certain threshold that is necessary for proper operation of all VBAT supplied parts, especially the UHF transmitter. Before starting a UHF transmission, the user should have a careful look on this flag in order to guarantee correct data transmission.

LFFLD, LF field detection

This flag signals the presence of an LF Field by monitoring the rectified LF field supply. If this exceeds the LF field detection threshold voltage $V_{THR,FDLF-VIN}$ LFFLD is set, otherwise it is cleared.

PMODE, Power mode

This flag signals the current state of the main supply switch (battery supply switch).

PWUPIND, Port wake-up indicator

The port wake-up indicator flag indicates that a port wake-up request was detected while the device is powered with field supply. The port wake-up indicator flag is active only if the battery supply switch is turned off (PMODE = 0).

The information is used in the boot routine in order to select the correct supply condition. When the battery switch is turned on, the flag is cleared automatically.

If the application program wants to monitor a port wake-up event in LF FIELD state it is recommended to check the port interrupt flag rather than the port wake-up indicator flag.

2.2.4.5 Power control register PCON2

The power control register PCON2 accommodates additional power supply state registers plus influences the behavior of the LF active and LF passive mode.

Table 12. Power control register PCON2 (reset value xx00_x000b)

Bit	Symbol	Access	Value	Description
7	VDDBRNREG	R/W		VDD brown-out detector register
			0	VDDBRNFLAG is / was not set
			1	VDDBRNFLAG is / was set
6	VDDABRNREG	R/W		VDDA brown-out detector register
			0	VDDABRNFLAG is/was not set
			1	VDDABRNFLAG is/was set
5	RDT	R/W		Reserved for device test
4	VBATBRNINDEN	R/W		Battery indication control
			0	2.4 V sense disabled
			1	2.4 V sense enabled
3	VBATBRNREG	R/W		VBAT brown-out detector register
			0	VBATBRNFLAG is / was not set
			1	VBATBRNFLAG is / was set
2	VBATBRNEXT	R/W		Extended battery brownout range
			0	Standard battery brownout falling threshold
			1	Extended battery brownout falling threshold
1	R2MSDET	R0/W		Reset 2ms detection
			0	No effect
			1	Dynamic reset of the 2ms detection
0	LOCKP	R/W		Lock passive mode
			0	Release passive mode lock
			1	Keep analogue frontend in passive (transponder) mode

VDDBRNREG, VDD brown-out detector register

The VDD brown-out detector register is a registered version of the corresponding brown-out detector flag. It is set as soon as VDDBRNFLAG becomes '1' and keeps its state, even if VDDBRNFLAG becomes '0' afterwards.

The bit VDDBRNREG can be set and cleared by the application only if the flag VDDBRNFLAG is '0'.

VDDBRNREG can be used to monitor the supply voltage level at VDD over a long period, e.g. to check whether the supply voltage at VDD was sufficient during EEPROM programming.

VDDABRNREG, VDDA brown-out detector register

The VDDA brown-out detector register is a registered version of the corresponding brown-out detector flag. It is set as soon as VDDABRNFLAG becomes '1' and keeps it state, even if VDDABRNFLAG becomes '0' afterwards. The bit VDDABRNREG can be set and cleared by the application only if the flag VDDABRNFLAG is '0'.

VDDABRNREG can be used to monitor the supply voltage level at VDDA over a long period, e.g. to check whether the supply voltage at VDDA was sufficient during a complete ADC conversion.

Battery brownout extended range, VBATBRNEXT

The battery brownout extended range allows the brownout threshold for VBAT to be extended from V_{BO}, V_{BAT_STD} falling to V_{BO}, V_{BAT_EXT} falling.

The extended battery brownout range allows for possible UHF transmitter trim adjustment when the battery falls below V_{BO}, V_{BAT_STD}. e.g. trimming of the power amplifier settings / power.

VBATBRNINDEN, Battery indicator monitor enable register

The battery indicator monitor is enabled when VBATBRNINDEN is set to '1'. This powers the VBAT monitoring circuitry in the analogue and connects a resistive load across the battery (VBAT). Battery monitoring is used to identify battery end of life (approximately 2.4V). The status of the battery indicator monitor can be obtained by reading the bit VBATBRNIND (Weak battery indicator).

VBATBRNREG, VBAT brown-out detector register

The VBAT brown-out detector register is a registered version of the corresponding brown-out detector flag. It is set as soon as VBATBRNFLAG becomes '1' and keeps its state, even if VABTBRNFLAG becomes '0' afterwards.

The bit VBATBRNREG can be set and cleared by the application, only if the flag VBATBRNFLAG is '0'.

VBATBRNREG can be used to monitor the supply voltage level at VBAT over a long period, e.g. to check whether the supply voltage at VBAT was sufficient during a complete ADC conversion.

Reset 2ms detection, R2MSDET

The application can manually reset the 2 ms ($t_{FLD,HLD}$) detection to avoid unintended activation of the LF passive mode. This feature can be used in LF active mode for example during the RSSI measurement when a constant carrier is required.

If a '1' is written to bit R2MSDET a dynamic reset of the 2 ms detection is triggered. The reset request is synchronized to the correct clock automatically without any further interaction by the application. Writing a '0' has no effect and reading of bit R2MSDET always yields '0'.

The reset of the 2 ms detection is generated temporarily when a '1' is written to bit R2MSDET and the 2 ms detection starts again immediately thereafter. A static reset is not supported in order to avoid unintentional blocking of the LF passive mode. If a constant carrier is applied in LF active mode for more than 2 ms, the application shall reset the 2 ms detection regularly.

Lock passive mode, LOCKP

This control bit overrides the 2 ms detection circuit and keeps the analogue frontend in passive (transponder) configuration. Long modulation pauses during a passive communication might reset the 2 ms detection unit and disturb the passive protocol. It is strongly recommended to set the bit LOCKP after recognition of a passive protocol (un-modulated field > 2 ms) and to release the bit again after the passive protocol is finished.

2.3 System clock

The clock generation unit provides versatile means to select the clock source and the clock speed for the CPU and the peripheral components.

2.3.1 Clock sources

The NCF29A1 / NCF29A2 provides several clock sources, which are summarized in Table 13. Four of these clock sources (RCCLK, AUXCLK, XODIV2CLK, LPRCCLK) are based on internal oscillators.

Table 13. Clock sources

Symbol	Description
RCCLK	Clock from 16 MHz main RC oscillator
AUXCLK	Clock from 1 MHz auxiliary RC oscillator
LFCLK	Clock from 125 kHz LF field
XODIV2CLK	Divided clock from 27.6 MHz crystal oscillator
LPRCCLK	Clock from 180 kHz low power RC oscillator
XCLK	External clock at P15

2.3.1.1 RCCLK, clock from 16 MHz main RC oscillator

The 16 MHz main RC oscillator is the main clock source for high speed CPU and peripheral operation. The oscillator starts up when it is activated and can be selected independently of the available core supply state.

The main RC oscillator is activated automatically under the following circumstances:

- RCCLK is selected as the CPU clock source
- RCCLK is required for EROM programming
- RCCLK is selected as the ADC clock source and a conversion is running
- RCCLK is selected as the AES calculation unit clock source and the calculation unit is running
- RCCLK is required for the monitor and debug interface

The application has the possibility to activate the main RC oscillator unconditionally, if the clock is needed for any other reason (e.g. timer 0, timer 1 and timer 2).

2.3.1.2 AUXCLK, clock from 1 MHz auxiliary RC oscillator

The 1 MHz auxiliary RC oscillator is intended for auxiliary tasks and low speed CPU and peripheral operation. The oscillator is used by several peripherals and requires a start-up time $t_{AUXCLK,PON}$.

The auxiliary RC oscillator is always running unless the LF clock is selected. The auxiliary RC oscillator is automatically activated under the following circumstances:

- Read/write access to the ULP EEPROM interface
- Device is powered with the battery (then the clock from the RC oscillator is used to operate the watchdog)
- AUXCLK is required for the monitor and debug interface
- AUXCLK is selected for the AES calculation unit and the calculation unit is running

The application has the possibility to activate the auxiliary RC oscillator unconditionally, if the clock is needed for any other reason (e.g. timer 0, timer 1 and timer 2).

2.3.1.3 LFCLK, clock from 125 kHz LF field

The selection of the 125 kHz clock (LFCLK) is intended for transponder applications with ultra low current consumption, where even the current consumption of the auxiliary RC oscillator shall be avoided.

Although the LF field has a frequency of 125 kHz, twice the frequency (250 kHz) can be generated with a clock doubler (LFCLKX2). LFCLKX2 shall only be used when the LF field is unmodulated.

2.3.1.4 XODIV2CLK, clock from 27.6 MHz crystal oscillator divided by 2

The XODIV2CLK is primarily intended for the UHF data transmission. When data transmission is enabled, it is recommended that XODIV2CLK is also used to clock the CPU. XODIV2CLK can also be selected as the clock source for the ADC, AES calculation unit and timers.

2.3.1.5 LPRCCLK, clock from 180 kHz low power RC oscillator

The clock of the low power RC oscillator is intended for low power applications like the LF active preprocessor, the interval timer and the motion sensor interface. As these blocks shall be operated even in POWER OFF state the supply is derived from the battery supply. The oscillator has a nominal frequency of 180 kHz.

The oscillator has to be enabled, before it can be used, and the oscillator start-up time $t_{LPRCCLK,PON}$ shall be considered. When the oscillator is not used, it should be set to power-down mode in order to reduce power consumption.

Using the low power RC oscillator, trimming capabilities allow compensation of short term deviations, e.g. caused by supply voltage or temperature.

2.3.1.6 XCLK, external clock at P15

An external clock XCLK with a frequency of f_{XCLK} can be connected at P15. This clock is intended as external clock source for timer 0, timer 1 and timer 2 as well as for the monitor and debug interface.

P15 port wake-ups and interrupts can be disabled if these events are unwanted when XCLK is driving P15. The bits P15C in the PRESWUP0 register configure the P15 port wake-up. The bit P15INTDIS in the P1INTDIS register configures the P15 port interrupts.

2.3.2 Clock domains

Based on the clock sources, clock domains are derived to provide the clock for the CPU and the peripheral components.

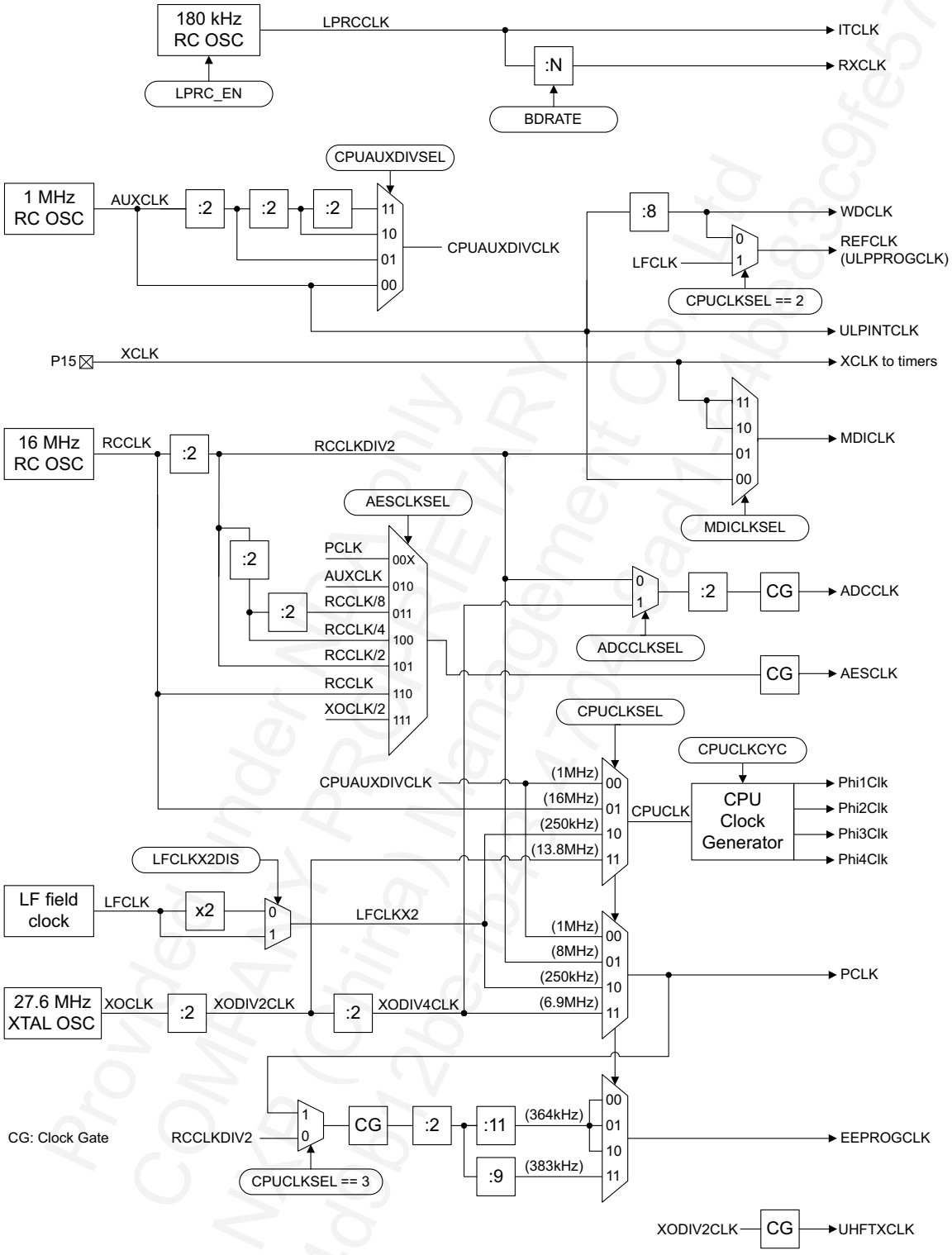


Fig 9. Clock domains for CPU and peripherals

Further clock domains are provided for timer 0, timer 1 and timer 2, based on two central timer clock multiplexers.

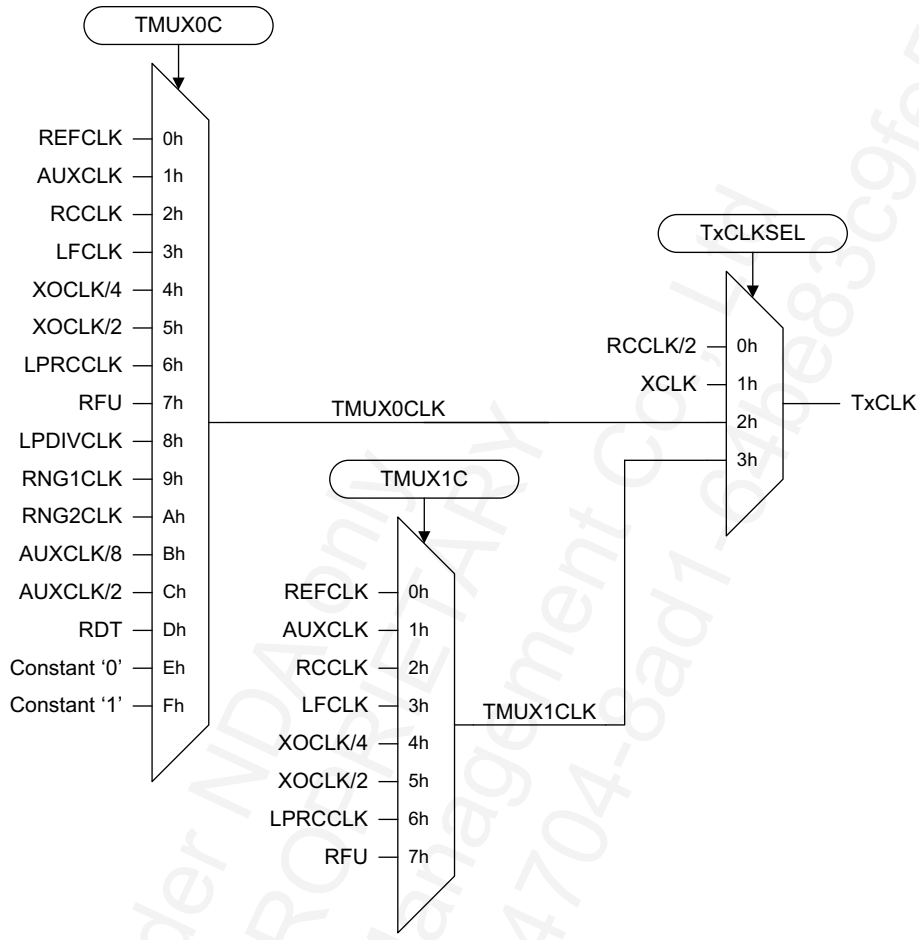


Fig 10. Clock domains for timer 0, timer 1 and timer 2

2.3.2.1 CPUCLK, CPU clock

Four clock sources are selectable for the CPU via system calls, the 16 MHz main RC oscillator RCCLK, the 1 MHz auxiliary RC oscillator AUXCLK, the clock can be derived from the LF Field LFCLK and the divided 27.6 MHz crystal oscillator XODIV2CLK. The main and the auxiliary RC clock are always selectable, even for LF field supplied operation.

The CPU clock domain has interfaces to the ROM, RAM, EROM and ULP EEPROM. The clocks for all these modules are generated by a central CPU clock generation unit. The actual execution speed of the CPU is controlled by insertion of additional wait states, dependent on the accessed memories.

Some standard peripherals use the same clock source as the CPU whereas others have only a limited selection of clock sources.

The boot routine always starts with using the auxiliary RC clock. After completion of the boot routine, all other available clock sources can be selected by the application via system calls in order to balance CPU speed and power consumption.

The CPU speed can be chosen dependent on the used clock source. Using the main RC oscillator, the CPU speed can be configured from approximately 485 kHz (16 MHz / 33) to 4 MHz (16 MHz / 4). In high performance mode, a CPU speed of up to 8 MHz is possible when code is executed from the ROM. In this mode, wait states for EROM access and VBATREG supply domain SFR read access are necessary. These wait states are inserted automatically, resulting in an average CPU speed of up to 5.3 MHz (16 MHz / 3 for 16 bit instructions) when executing code from the EROM and not reading VBATREG supply domain SFRs.

The device supports a ROM/EROM timing compatibility mode in order to allow application code transfer from an EROM version to a ROM coded product version with identical timing behavior even in high performance mode. If the compatibility mode is active in the ROM product version wait states are inserted at the same positions where they would be inserted in an EROM version. The application program can disable the timing compatibility mode feature in order to get the maximum performance in a ROM version.

By using the auxiliary RC oscillator as clock source, the CPU speed can be set from approximately 3.8 kHz (1 MHz / 264) to 500 kHz (1 MHz / 2).

In case the clock source is derived from the LF field, the CPU speed is selectable between 3.8 kHz (125 kHz / 33) to 125 kHz (250 kHz / 2 when LFCLKX2 is enabled).

Using the 27.6 MHz crystal oscillator as the clock source, the CPU speed can be set from 418 kHz (27.6 MHz / 66) to 3.45 MHz (27.6 MHz / 8).

2.3.2.2 PCLK, peripheral clock

The PCLK domain is used by peripherals like the SPI interface and the random number generator. These peripherals usually run with the same clock source as the CPU.

2.3.2.3 AESCLK, AES clock

The AES calculation unit operates either with the same source as the CPU, the auxiliary RC oscillator, a (divided) clock of the main RC oscillator, or the divided crystal oscillator clock. The faster main RC oscillator clock speed can be used to speed up the calculation time for the LF transponder without the necessity to switch to a faster CPU clock.

2.3.2.4 ADCCLK, ADC clock

The ADC operates either on the clock sourced by the Main RC Oscillator, RCCLK/2, or on the crystal oscillator, XOCLK/4. It is advised to use the crystal oscillator as clock source when an ADC measurement is triggered during RF transmission to maintain the UHF harmonics. In any other case, the Main RC oscillator is preferred as it consumes less power and performs faster conversion.Note that the actual ADC clock is divided by two after clock source selection, thus actual ADC clock is either RCCLK/4 or XOCLK/8, see also Figure 9.

2.3.2.5 WDCLK, watchdog clock

The watchdog uses the clock from the auxiliary RC oscillator independent of the selected CPU clock source. When the watchdog is enabled, the auxiliary RC oscillator is conditionally enabled too.

2.3.2.6 REFCLK, reference clock

The reference clock is a 125 kHz clock source (clock period $T_{REF,LF}$) which is intended for the timers, either derived from the auxiliary RC oscillator or from the LFCLK.

2.3.2.7 ULPINTCLK, ULP EEPROM interface clock

The clock for the ULP EEPROM interface (read/write access) is derived from the auxiliary RC oscillator independent of the selected CPU clock source.

2.3.2.8 ULPPROGCLK, ULP EEPROM programming clock

The 125 kHz ULP EEPROM programming clock is either derived from the auxiliary RC oscillator or from the LF clock. The correct clock source is always selected automatically, based on CPU clock source selection, CPUCLKSEL.

2.3.2.9 EEPROGCLK, EROM programming clock

The programming clock for the EROM is derived from the main RC oscillator, 364 kHz (16 MHz / 44), or from the divided crystal oscillator clock, 383 kHz (27.6 MHz / 72).

2.3.2.10 MDICLK, monitor and download interface clock

Clock sources for the monitor and debug interface are the auxiliary RC clock, the main RC clock and the external clock XCLK. The MDI clock is independent of the selected CPU clock source.

2.3.2.11 IIUCLK, immobilizer interface unit clock

Clock sources for the immobilizer interface unit are the LF clock for the immobilizer, the PCLK for standalone operation of the HT calculation unit and the overflow of timer 0 for the modulator operation. The IIU has a local clock selection unit independent of the selected CPU clock source.

2.3.2.12 RXCLK, LF active preprocessor clock

RXCLK is the clock domain of the LF active preprocessor. Using the LPRC oscillator as the clock source, a configurable divider adapts RXCLK to the bit rate of 2, 4 or 8 kbit/s that has been chosen using bits in PRECON2.

2.3.2.13 ITCLK, interval timer clock

ITCLK is the clock source for the interval timer, real time clock and motion sensor interface.

2.3.2.14 XCLK, external clock

The external clock XCLK is provided to timers 0, 1 and 2.

2.3.2.15 TMUX0CLK, timer multiplexer 0 clock

The timer multiplexer 0 clock, TMUX0CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

2.3.2.16 TMUX1CLK, timer multiplexer 1 clock

The timer multiplexer 1 clock, TMUX1CLK, is provided to timers 0, 1 and 2. The multiplexer concept allows these timers to operate with and to synchronize to several clock sources.

2.3.2.17 XODIV2CLK

The clock is divided by 2 from the 27.6 MHz crystal oscillator. The XODIV2CLK is available on request (VDDXOEN = '1' and XOEN = '1' in the TXPCON register), after the crystal oscillator start-up time.

2.3.3 Registers

The bit LPRC_EN that is used to enable the low power RC oscillator for the LF active preprocessor, interval timer, real time clock and the motion sensor interface is located in register PRECON2. The bits LPRC_CAL (available for improving the timing accuracy of the interval timer, real time clock and motion sensor interface) can be accessed in register PRECON6. The bit IIU_CLKSEL selecting the clock for the immobilizer interface unit is located in register IIUCON0. The bits TxCLKSEL for timers 0, 1 and 2 clock source selection are located in the registers T0CON1, T1CON1 and T2CON1 respectively.

2.3.3.1 Clock control register CLKCON0

The clock control register CLKCON0 selects the CPU clock source and speed.

CLKCON0 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 14. Clock control register CLKCON0 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	RDT	R/W	R		Reserved for device test
6 and 5	CPUCLKSEL[1:0]	R/W	R		CPU clock source selection
				00	Auxiliary RC oscillator division, CPUAUXDIVCLK, see also CPUAUXDIVSEL in Table 19
				01	Main RC oscillator, RCCLK
				10	Clock from LF field, LFCLK or LFCLKX2
				11	Divided clock from the crystal oscillator, XODIV2CLK
4 to 0	CPUCLKCYC[4:0]	R/W	R		See Table 15

CPUCLKSEL[1:0], CPU clock source selection

CPUCLKSEL determines the used clock source for the CPU and the standard peripherals.

CPUCLKCYC[4:0], number of CPUCLK periods per machine cycle

CPUCLKCYC is used to adjust the CPU speed by setting the number of CPU clock periods (T_{CPUCLK}) per command. Normally, one command is executed in CPUCLKCYC + 2 periods of CPUCLK.

In high performance timing mode, CPU wait states are inserted automatically at every command executing an EROM access, independent of whether code or data is accessed, or a VBATREG supply domain SFR read access. The effective number of periods for high performance timing mode is given in Table 15.

Table 15. Effective periods of CPUCLK in case of EROM access or VBATREG supply domain SFR read access

CPUCLKSEL[1:0]	CPUCLKCYC	Effective value of CPUCLKCYC
00	0 … 31	CPUCLKCYC + 2 (2 … 33)
01	0 … 1	4
	2 … 31	CPUCLKCYC + 2 (4 … 33)
10	0 … 31	CPUCLKCYC + 2 (2 … 33)
11	0 … 1	4
	2 … 31	CPUCLKCYC + 2 (4 … 33)

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 0

- The application executes (16 or 32 bit commands) from System ROM. Every command needs 2 T_{CPUCLK}, so the average CPU speed is 8 MHz.
- The application executes code from the EROM. It is assumed that every command is a 32 bit command. Every command shall read 32 bit from the EROM, which needs 4 T_{CPUCLK}. The average speed is 4 MHz.
- The application executes code from the EROM. It is assumed that every command is a 16 bit command. The first command fetches 32 bits from the EROM, which needs 4 T_{CPUCLK}. The second command can execute from the code buffer and, therefore, needs only 2 T_{CPUCLK}. The average speed is 5.3 MHz.

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 2

- The application executes code from the EROM. Since one 32 bit word is read from the EROM per 4 MHz cycle, the instruction rate (for non-branching instructions) is 4 MHz, independent of the command length. Additional read cycles may be inserted in case of branch instructions or interrupts.

Example: Application with 16 MHz RCCLK and CPUCLKCYC = 6

- The instruction rate (for non-branching instructions) is 2 MHz.

2.3.3.2 Clock control register CLKCON1

CLKCON1 selects the clock source for several peripherals and contains the settings for using an external clock.

CLKCON1 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 16. Clock control register CLKCON1 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	RDT	R0/W	R		Reserved for device test
6	LFCLKX2DIS	R/W	R		LF clock doubler disable
				0	Clock doubler on, LFCLKX2 = 250 kHz
				1	Clock doubler off, LFCLKX2 = 125 kHz
5 and 4	MDICLKSEL[1:0]	R/W	R		Monitor and download interface clock selection
				00	1 MHz AUXCLK
				01	8 MHz RCCLK
				10, 11	External clock XCLK
3 to 1	RDT	R/W	R		Reserved for device test
0	RER_COMP	R/W	R		ROM/EROM timing compatibility mode
				0	Disabled
				1	Enabled

LFCLKX2DIS, LF clock doubler disable

This bit disables the LF clock doubler. If the clock doubler is disabled and the clock from the LF field is selected as CPU clock, the CPU operates at half the clock speed. This bit can be used to reduce the current consumption when the device is clocked from the LF field.

MDICLKSEL[1:0], monitor and download interface clock selection

In general the MDI operates with the clock from the auxiliary RC oscillator. For high speed communication it is possible to switch to 8 MHz of the main RC oscillator.

The setting MDICLKSEL = 1Xb is intended for general applications that want to use a (synchronous) external clock. For example this allows for the parallel initialization of several devices with an external clock.

RER_COMP, ROM/EROM timing compatibility mode

This bit is functional only in the ROM version although for compatibility reasons it is also implemented in the EROM version. It controls the activation of the ROM/EROM timing compatibility mode.

If RER_COMP = ‘0’, any read access to the ROM is accomplished at the maximum possible speed. This setting is provided to benefit from the speed advantage of the ROM version compared to the EROM version.

If RER_COMP is set, any read access to the User ROM area is accomplished with the same timing as if the EROM is present, i.e. the same amount of WAIT CPU clock cycles are inserted as in the EROM version. This setting is provided for 1:1 timing compatibility between EROM and ROM version.

RER_COMP only influences the behavior of the User ROM. This bit does not influence the execution speed of the System ROM.

2.3.3.3 Clock control register CLKCON2

CLKCON2 selects the clock source for the ADC and the AES calculation unit. Control bits for the main RC oscillator and the auxiliary RC oscillator are also included.

Table 17. Clock control register CLKCON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	ADCCLKSEL	R/W		ADC clock selection
			0	clock source from the Main RC oscillator, RCCLK/2 further divided by 2 (16 MHz / 4 = 4 MHz)
			1	clock source from 27.6 MHz crystal oscillator, XODIV2CLK/2 further divided by 2 (27.6 MHz / 8 = 3.45 MHz)
6 to 4	AESCLKSEL[2:0]	R/W		AES calculation unit clock selection
			000	PCLK
			001	Reserved for future use
			010	AUXCLK
			011	Reserved for future use
			100	4 MHz RCCLK
			101	8 MHz RCCLK
			110	16 MHz RCCLK
			111	13.8 MHz XODIV2CLK
3	RDT	R/W0[1]		Reserved for device test
2	AUXRCOSC_OUTDIS	R/W		Auxiliary RC oscillator clock output disable
			0	Normal operation
			1	Output of auxiliary oscillator is gated to ‘0’ unless it is used as CPU clock source or any automated event requires the auxiliary clock
1	AUXRCOSC_EN	R/W		Auxiliary RC oscillator enable, see also Section 2.3.1.2
			0	Activate oscillator conditionally dependent on selected CPU clock source and peripherals
			1	Activate oscillator unconditionally
0	MRCOSC_EN	R/W		Main RC oscillator enable, see also Section 2.3.1.1
			0	Activate main RC oscillator if used as CPU clock or peripheral clock (PCLK)
			1	Activate main RC oscillator unconditionally

[1] W0 means value 0 can be written only

AESCLKSEL[2:0], AES clock selection

In general the clock for the AES calculation unit is derived from the peripheral clock PCLK. If the device is running with a slow clock source (AUXCLK or LFCLK), the available speed of PCLK might not be sufficient. Hence, it is possible to select other clock sources like the main or auxiliary RC clock for the AES calculation unit.

If the RC oscillator is not started up, selecting an RCCLK source for the AESCLK may cause that the RC oscillator does not start up and the AES calculation does not terminate. To prevent such situation, it is recommended to explicitly enable the RCCLK by setting bit MRCOSC_EN to 1 prior to running the AES with RCCLK.

AUXRCOSC_OUTDIS, auxiliary RC oscillator clock output disable

The clock output of the auxiliary oscillator is turned off by setting the bit AUXRCOSC_OUTDIS to '1'. The clock output is gated to '0' in this case. The oscillator cell itself is not influenced and keeps on running. The value of bit AUXRCOSC_OUTDIS is ignored, if the auxiliary oscillator is used as CPU clock source or if it is activated automatically.

AUXRCOSC_OUTDIS is suitable if the application operates with the clock derived from the LF field but the auxiliary clock is used for certain operations (e.g. ULP EEPROM access). If the start-up time of the auxiliary oscillator is not fast enough the oscillator can stay turned on but the output can be disabled in order to reduce the current consumption when the clock is not needed. An automated event (e.g. ULP EEPROM access) will enable the clock output when required.

AUXRCOSC_EN, Auxiliary RC oscillator enable

Usually the auxiliary RC oscillator is turned off, if the CPU clock is derived from the LF field. If AUXRCOSC_EN is set, the auxiliary RC oscillator is activated independent of the selected clock source for the CPU and the peripherals.

MRCOSC_EN, Main RC oscillator enable

If MRCOSC_EN is set, the main RC oscillator is activated independent of the selected clock source for the CPU and the peripherals.

2.3.3.4 Clock control register CLKCON3

CLKCON3 selects the clock sources for the two central timer clock multiplexers, the output of which can be used as clock source for timer 0, timer 1 and timer 2.

Table 18. Clock control register CLKCON3 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	R0/W0		Reserved for future use
6 to 4	TMUX1C[2:0]	R/W		Timer clock source multiplexer 1 control
			000	REFCLK (nominally 125 kHz)
			001	AUXCLK (nominally 1 MHz)
			010	RCCLK (nominally 16 MHz)
			011	LFCLK (nominally 125 kHz)
			100	XOCLK/4 (nominally 6.9 MHz)
			101	XOCLK/2 (nominally 13.8 MHz)
			110	LPRCCLK (nominally 180 kHz)
			111	Reserved for future use
3 to 0	TMUX0C[3:0]	R/W		Timer clock source multiplexer 0 control
			0000	REFCLK (nominally 125 kHz)
			0001	AUXCLK (nominally 1 MHz)
			0010	RCCLK (nominally 16 MHz)
			0011	LFCLK (nominally 125 kHz)
			0100	XOCLK/4 (nominally 6.9 MHz)
			0101	XOCLK/2 (nominally 13.8 MHz)
			0110	LPRCCLK (nominally 180 kHz)
			0111	Reserved for future use
			1000	LPDIVCLK (nominally 2 kHz)
			1001	RNG1CLK
			1010	RNG2CLK
			1011	AUXCLK/8 (nominally 125 kHz)
			1100	AUXCLK/2 (nominally 500 kHz)
			1101	Reserved for device test
			1110	Constant ‘0’
			1111	Constant ‘1

TMUX0C[3:0], Timer clock source multiplexer 0 control

TMUX0CLK[3:0] defines which clock source is provided to timers 0, 1 and 2. Note that RNG1CLK and RNG2CLK are the ring oscillators used by the Random Number Generator for entropy generation. They are made available as timer clock source for test purposes only and shall not be used by the application.

2.3.3.5 Clock control register CLKCON4

CLKCON4 selects the auxiliary RC oscillator division for CPUCLK and PCLK. A clock tree root disable for the AESCLK is also included.

CLKCON4 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 19. Clock control register CLKCON4 (reset value 0000_0x00b)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7 to 3	RFU	R0/W0	R		Reserved for future use
2	CGAESDIS[1]	R/W	R		AESCLK clock tree root disable
				0	AESCLK enabled
				1	AESCLK disabled at
1 and 0	CPUAUXDIVSEL[1:0]	R/W	R		CPUCLK/PCLK auxiliary RC oscillator division selection
				00	1 MHz AUXCLK
				01	500 kHz AUXCLK/2
				10	250 kHz AUXCLK/4
				11	125 kHz AUXCLK/8

[1] The reset value of CGAESDIS is undefined at the beginning of the EROM application. Please see application note for detailed information.

CGAESDIS, AESCLK clock tree root disable

This bit disables the AESCLK clock tree at its root. This will result in a small power saving even when the AES calculation unit is not being used. This bit must be set to ‘0’ to use the AES calculation unit.

CPUAUXDIVSEL[1:0], CPUCLK/PCLK auxiliary RC oscillator division selection

These bits select the auxiliary RC oscillator division for CPUCLK and PCLK when bits CPUCLKSEL in the CLKCON0 register are set to 0.

2.4 LF Passive interface (Immobilizer)

The contactless passive LF interface provides means to utilize the NCF29A1 / NCF29A2 as a contactless transponder, capable to derive its power supply and system clock by inductive coupling to an LF field generated by a corresponding base station. The same LF field is used to receive data from and transmit data to the base station under control of the RISC controller. An external LC resonant circuit needs to be connected to the coil inputs (INxP and INxN) of the contactless interface (Figure 11).

The NCF29A1 features a 3D contactless transponder.

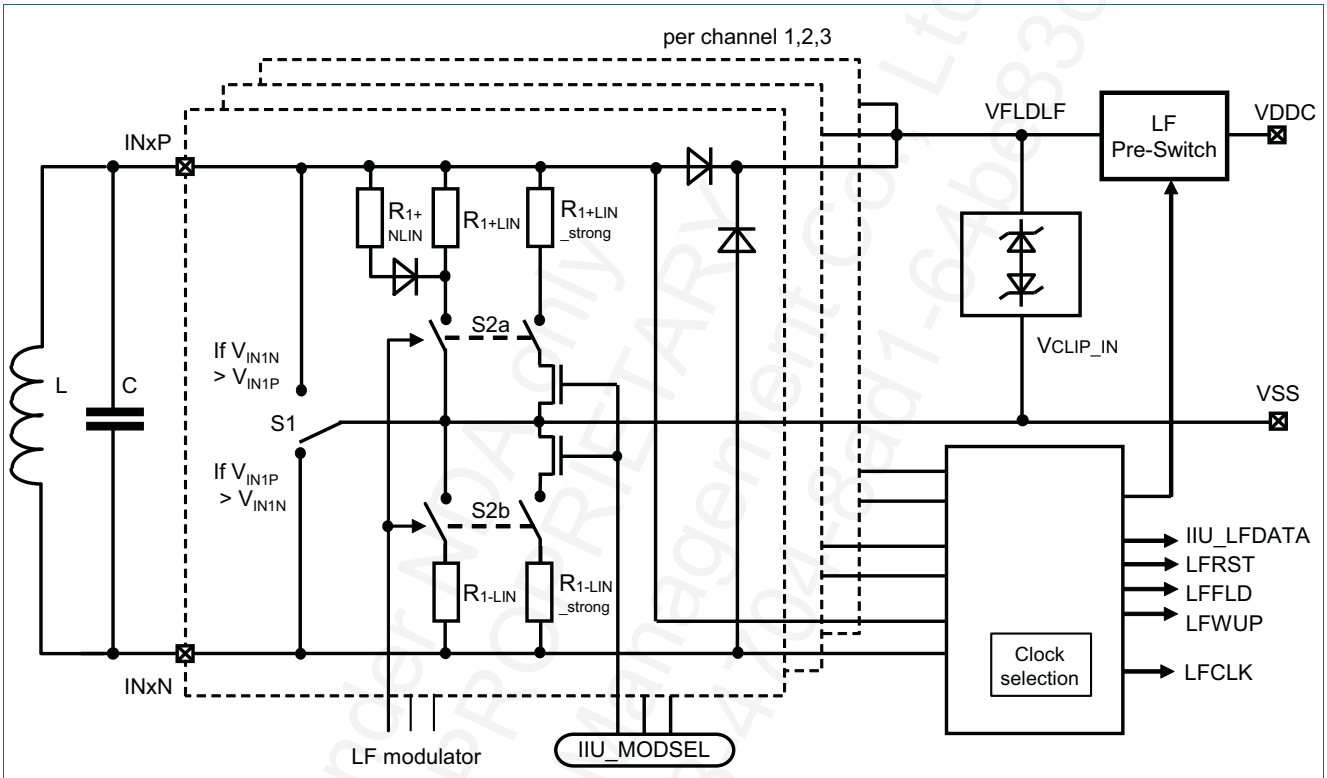


Fig 11. 3D contactless interface front end circuitry

Independent of the device operating mode, the contactless interface is capable to detect the presence of an LF field at any channel and to provide a corresponding signal to wake-up the device from POWER OFF state or to interrupt device operation.

2.4.1 Rectifier and limiter

The NCF29A1 front end features three independent LF rectifier circuits, one per channel.

The NCF29A2 uses only one LF rectifier circuit. Each rectifier operates in full-bridge configuration, the outputs of the rectifiers are shorted and charge an external capacitor connected to the common pin VDDC. A single shunt voltage limiter connected to the output of the rectifiers is provided to ensure that the voltage at pin VDDC does not exceed the specification. The interface input current shall not exceed the specified limits.

The data communication with the device employs amplitude shift keying (ASK) of the LF field. The modulation duration and LF field strength shall be chosen such that the rectified supply voltage stays above the power-on reset threshold V_{POR} during the LF field low condition (see Figure 12).

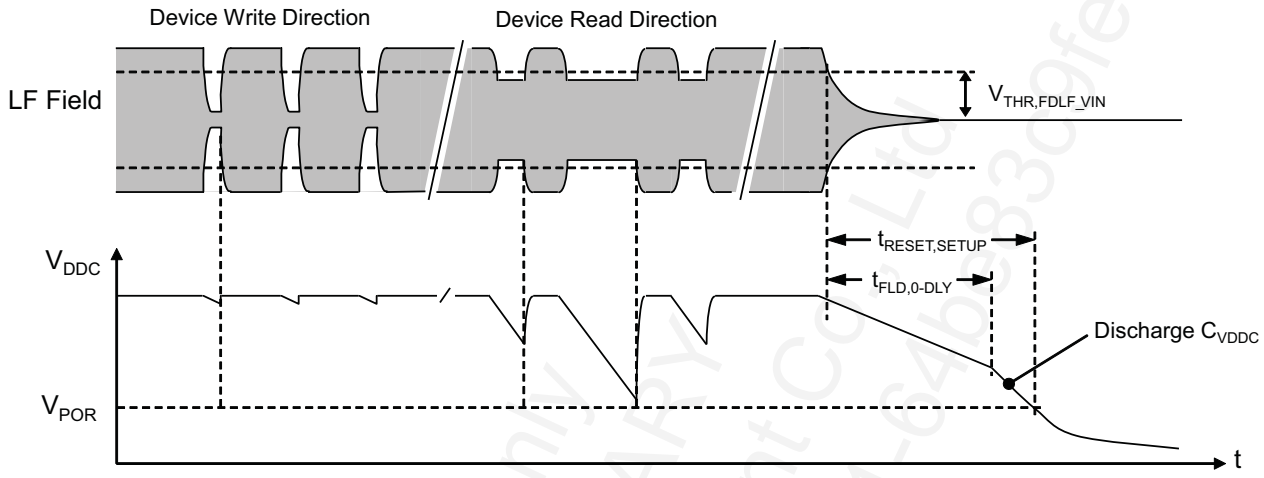


Fig 12. LF Field Reset Timing

A power on reset is triggered if all 3 channels are low for the specified time $t_{RESET,SETUP}$.

2.4.2 Modulator

The contactless interface utilizes absorption modulation of the LF Field on all three channels simultaneously to send data to the base station. The modulation timing is determined by the RISC controller.

Absorption modulation is accomplished by applying an additional load (S2 closed, see Figure 11) across the coil inputs. The LF field modulator contains a standard modulator and a strong modulator. If the standard modulator is selected, the high ohmic path (Rx+LIN, Rx+NLIN and Rx-LIN) is turned on (weak modulation), while selecting the strong modulator, both the low-ohmic path (Rx+LIN_strong and Rx-LIN_strong) and the high ohmic path are enabled (strong modulation).

Besides the modulation load impedance, the absorption modulation characteristics depend on the source impedance of the external resonance circuit, the voltage limiter and the internal power consumption of the device. The applied load (S2) is different for each of the two half waves of the carrier, to support clock recovery. The resistors Rx and the switches S1, S2 are implemented for each channel.

2.4.3 Demodulator

The front end features an envelope ASK demodulator able to detect the on-off keying (OOK) signal provided by the base station. The envelope is tracked on all three channels simultaneously and derived from the three channel demodulation signals a single demodulated signal is provided to the IIU. The demodulator circuitry (Figure 13) has been designed to fit the modulation characteristics as implemented by the NXP transponder families.

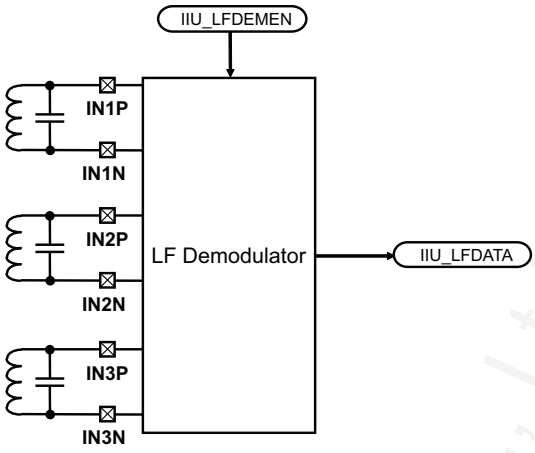


Fig 13. Demodulator Block Diagram

Once enabled, the demodulator freezes the internal demodulator threshold individually for the three channels and after the settling time t_{ADLY} the demodulator is operational for the duration t_{IDLE}. After that, it needs to be disabled for a certain time (t_{DSETUP}) before it is enabled again, in order to refresh the demodulator thresholds (Figure 14). Refreshing the demodulator references guarantees reliable sensitivity especially for high Q factors.

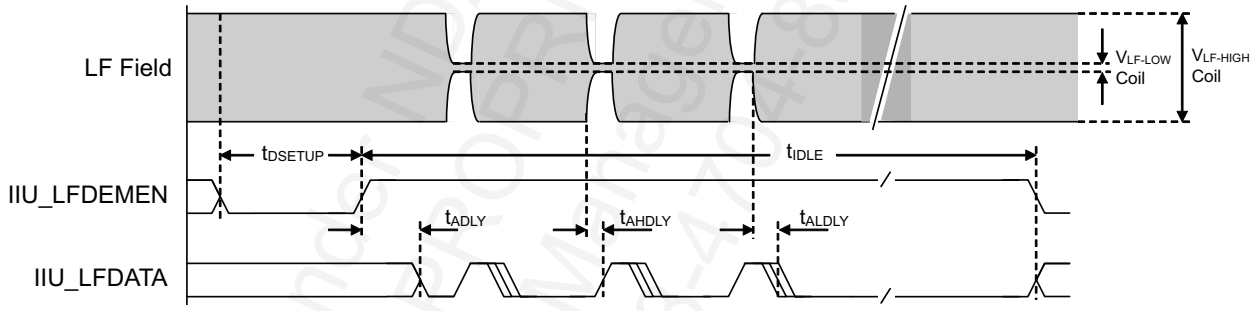


Fig 14. Demodulator Timing

The demodulator sensitivity applicable in write direction is illustrated in Figure 15.

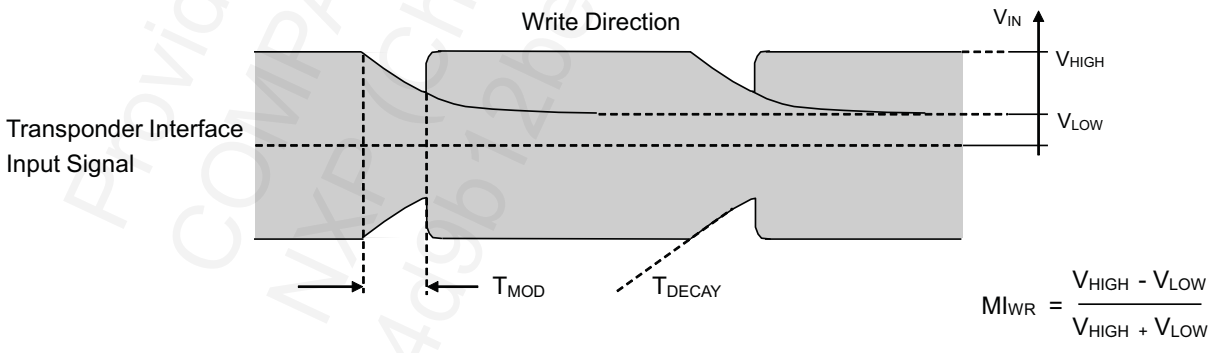


Fig 15. Demodulator Specification

During an LF Field modulation phase the demodulator shall be disabled. The immobilizer interface unit performs serial to parallel conversion of the demodulator output signal, which is then provided to the CPU.

2.4.4 Field detection

Independent of the actual device operating state, the contactless interface is able to detect the presence of an LF field at any channel, in order to wake-up the device from POWER OFF state or to interrupt device operation (see Figure 16).

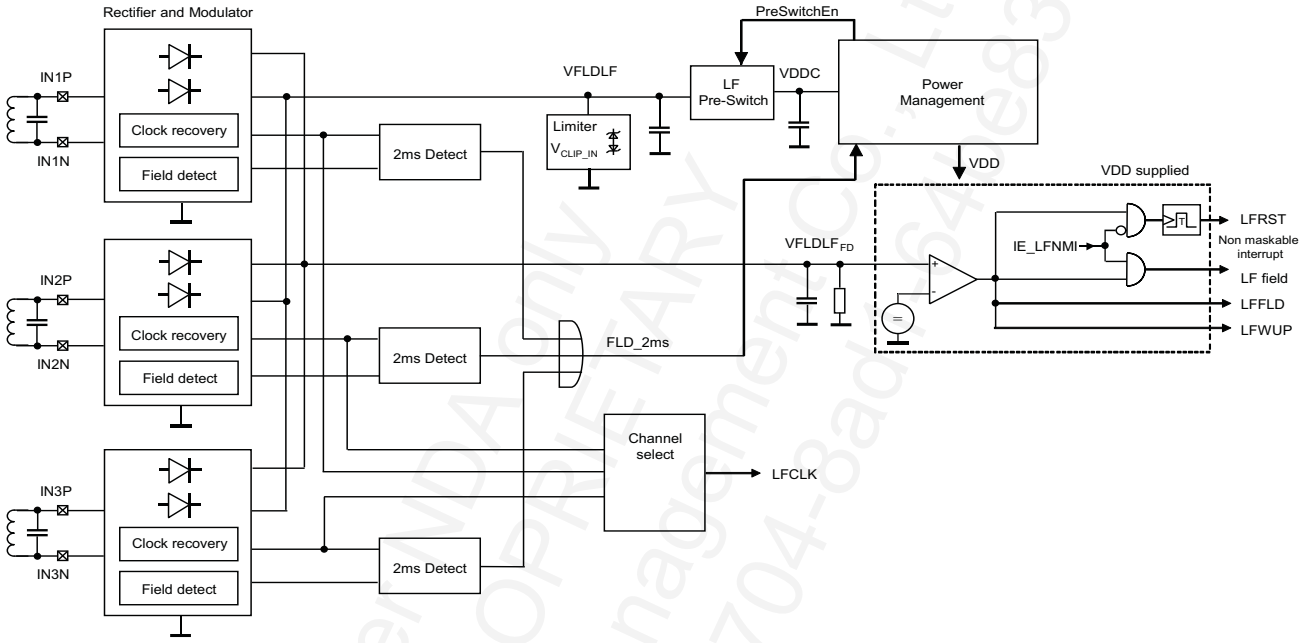


Fig 16. LF field detection circuitry

Once a constant carrier ($t_{FLD,HLD}$) is detected at any channel and the pre-switch between V_{FLDLF} and VDDC is closed, the field detection circuitry gets activated. It features an independent envelope detector that senses the differential voltage across the coil inputs (pins INxP and INxN) followed by a comparator. The LF field envelope is compared with a certain threshold, which is greater than the power-on reset threshold, forming the field detect flag (LFFLD). LFFLD turns high, when the LF field on at least one channel exceeds the field detection threshold ($V_{THR,FDLF-VIN}$). LFFLD may be tested by the RISC controller when desired.

The output signal of the field detection circuit can be configured as reset or interrupt source (non maskable interrupt).

In case the non maskable interrupt is selected and considered operating from battery supply (BATTERY state) it is up to the application whether to force an LF field supply condition (LF FIELD state) or not. However, LFFLD being set is no guarantee that the available LF field is sufficient to power the device. A device power-on reset may occur in case of a weak LF field, which needs to be taken into account once the LF field supply condition is forced.

LFFLD turns low, if the input voltage on all three channels is below the field detect threshold for at least $t_{FLD,0\text{-}DLY}$ and triggers an active discharge of the capacitor connected to VDDC to safely generate a device reset.

2.4.5 Detection of 2 ms constant carrier

In order to activate the immobilizer state, a 256 LF clock cycles constant carrier has to be applied to the input pins. The internal rectified supply voltage V_{FLDLF} has to exceed the 'active' field detection threshold. After valid 256 LF clock cycles detection, the pre-switch is activated. The pre-switch incorporates a current-control that limits the charging-current flowing into the capacitor connected to pin VDDC, until the device POR state is exited. Thereafter, the pre-switch is configured in fast-charging mode.

2.4.6 Immobilizer interface unit (IIU)

The immobilizer interface unit (IIU) allows convenient buffered read and write access to the immobilizer LF demodulator and LF modulator. With its various data path selection capabilities the IIU minimizes the CPU load for most power efficient immobilizer implementations.

The IIU allows an autonomous bit handling for transmission/reception/shifting of 1 to 8 bit and provides a dedicated transponder mode compatible to the HT2-E and HT3 transponder families as well as a general purpose mode. The HT calculation unit can be inserted in all data flow combinations for enciphering. The controlling of the data transfer is supported by the generation of an interrupt or wake-up event (see Figure 17).

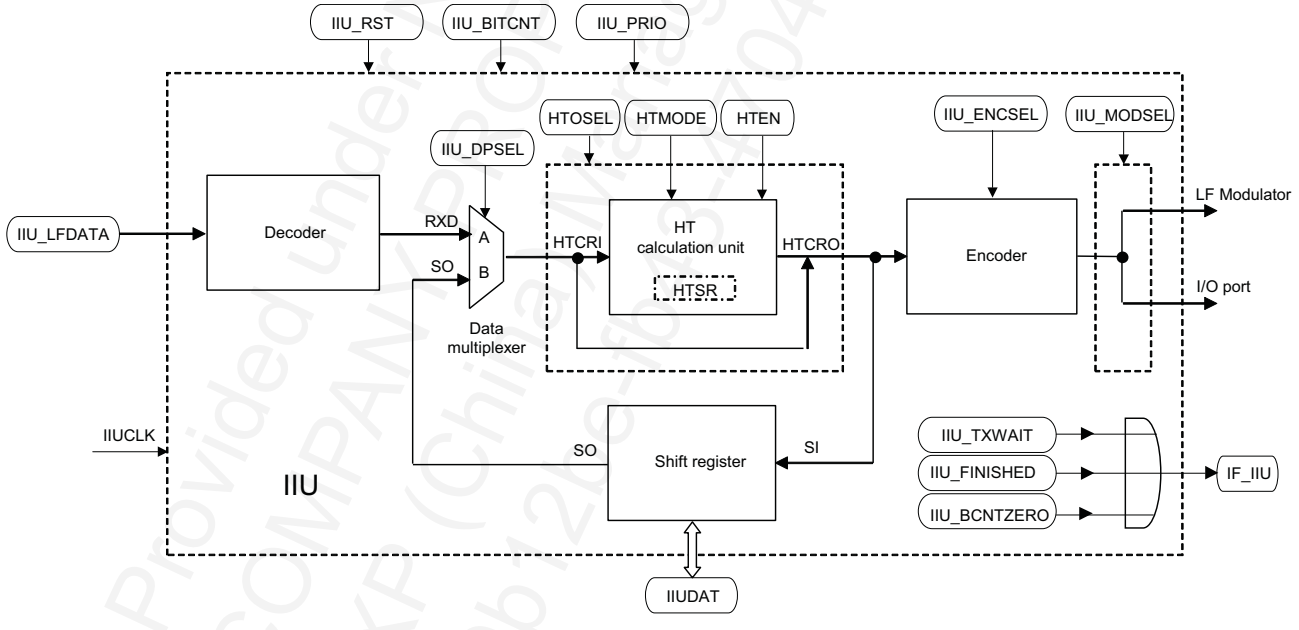


Fig 17. IIU block diagram

Several IIU clock sources can be selected. For HT2-E and HT3 compatible timing either the LFCLK or a 125 kHz clock source shall be selected.

With the help of an integrated timer, the time base for the LF demodulator (zero bit, one bit, stop bit) is controlled. The timer is also responsible to generate the LF modulator baudrate and to control the timing between data reception and transmission ($t_{WAIT,TR}$).

The encoded IIU output signal can be selected to modulate the LF field or to be directed to a port pin for general purpose use.

2.4.6.1 IIU

For data reception the IIU applies binary pulse length modulation (BPLM) decoding (Figure 18) and converts the decoded bits via the 8 bit shift-register into byte format.

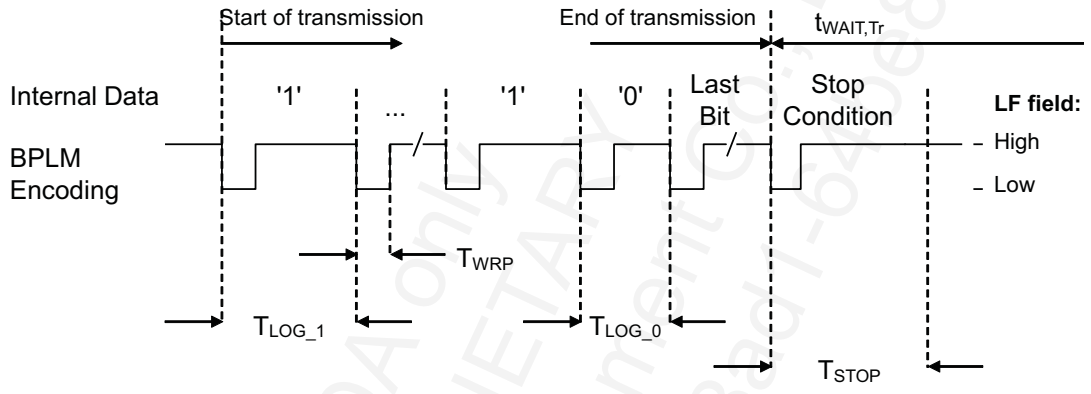


Fig 18. Data encoding - base station to NCF29A1 / NCF29A2

For data transmission the IIU converts the bytes via the shift-register into a bit stream and applies Manchester or CDP encoding (Figure 19). Since the encoding scheme can be selected via IIU_ENCSEL, the encoder also supports plain transmission (NRZ).

The encoded output signal can modulate the LF field or can be directed to a port pin (via IIU_MODSEL).

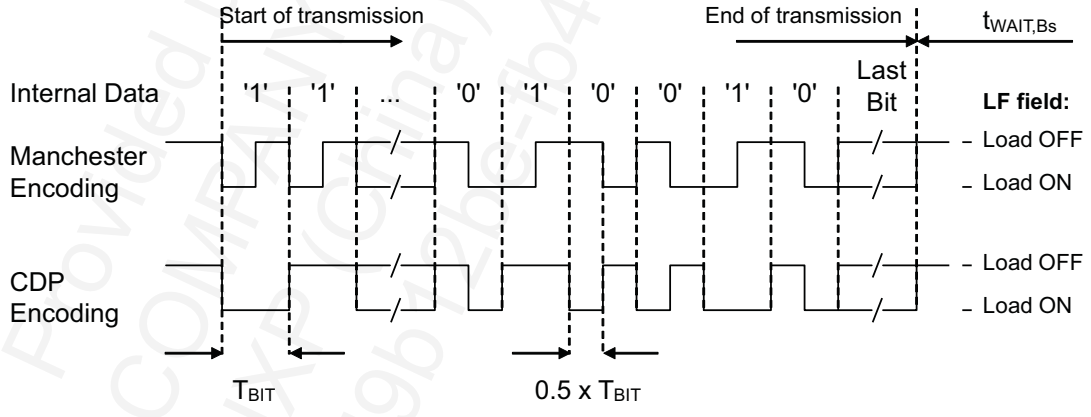


Fig 19. Data encoding - NCF29A1 / NCF29A2 to base station

2.4.6.2 IIU general purpose mode

If not occupied by the immobilizer application, the IIU can be used for general purpose applications like implementation of a custom LF protocol. The shift register allows byte-wise control of transmitted data. When Manchester and CDP encoding is selected, the encoder runs with the chip clock whereas it runs with the bit clock for NRZ encoding. This allows for convenient four state Manchester generation (Manchester zero and one with Manchester encoding, Manchester mark and space with NRZ encoding) with a constant baudrate.

Access to the demodulated data line is given via the dedicated register bit IIU_LFDATA. The timer capture function can be used for demodulation. Besides the LF field clock and the peripheral clock a general purpose timer can be used for baudrate generation.

In order to implement variable transponder wait times $t_{WAIT,TR}$, transmission can be started on user request.

Enciphering can be realized with the HT calculation unit, which provides stand-alone access.

2.4.6.3 IIU states

The IIU state diagram is shown in Figure 20. The states RXWAIT, RXFIRST, RXDATA, TXWAIT and TXDATA are used in LF transponder mode, while the states SHIFT and SHIFTCONT are intended for general purpose applications.

The CPU can control the IIU states by reading from and writing to the state register IIUSTATE. The application has to select any state except IDLE to initiate an automated action. Every action can be interrupted by switching back to IDLE state.

Direct state changes from transponder mode states to general purpose application states and vice versa should be avoided. Instead, IDLE mode shall be selected before such a state change is executed.

IDLE state

In IDLE state all IIU modules are disabled and the IIU clock is turned off. The IIU leaves the IDLE state only if the CPU selects a new IIU state by updating the state register.

RXWAIT

Switching to RXWAIT state initiates the transponder mode. In RX WAIT state the IIU waits for a first rising edge of the demodulated LF data.

RXFIRST and RXDATA

In transponder mode, the IIU is receiving data in RXFIRST and RXDATA states. The decoder is enabled automatically and can be disabled in case custom protocol / general purpose modulation will be implemented.

The RXFIRST state is only used for the first bit received and only if clear text one bit command support is enabled (bit IIU_OBCSEN is set to ‘1’ in register IIUCON2).

The IIU switches to TXWAIT state when a stop condition is received. In this case, a TXWAIT interrupt is generated.

In case the bit counter becomes 0 but no stop condition is received, the IIU switches back to IDLE state as soon as a new rising edge of the demodulated LF data is detected. This indicates that more bits were received than it was expected by the application.

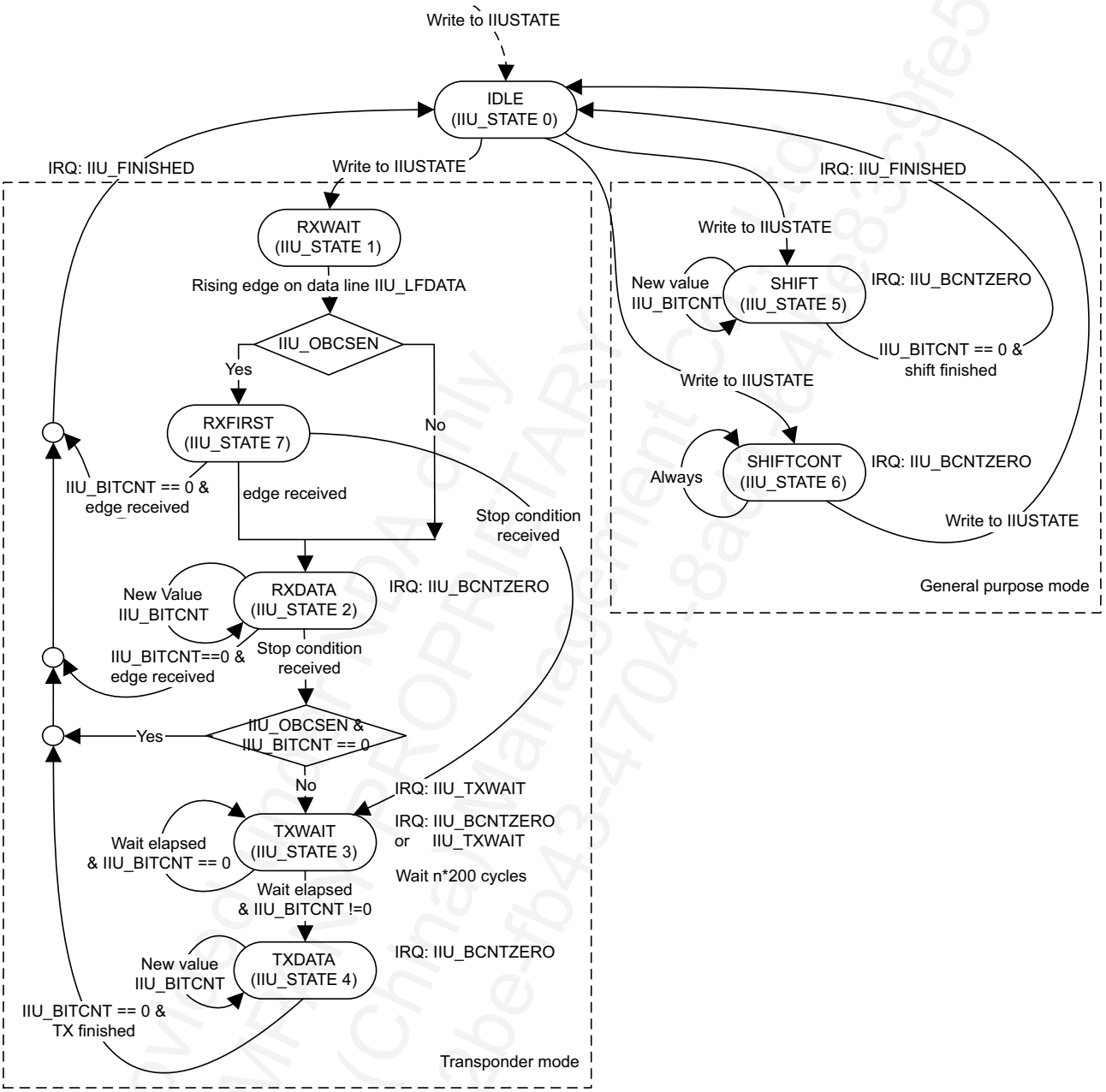


Fig 20. IIU state diagram

TXWAIT

The TXWAIT state is used for implementing the wait time according to the transponder protocol before switching to transmission mode. The wait time is a multiple of 200 cycles and derived from the period counter. Every time the wait time elapses and the IIU does not switch to TXDATA state, the CPU receives an IF_IIU interrupt request (flag IIU_TXWAIT set).

The IIU stays in TXWAIT state until the bit counter has a non-zero value when the respective 200 cycle wait time has elapsed. Hence, the application can control the length of the wait time in multiples of 200 cycles by writing a non-zero value to the bit counter in the desired time frame.

TXDATA

In transponder mode, the IIU is transmitting data in TXDATA state (depending on the settings for encoder and modulator selection). The encoder is enabled automatically.

The CPU receives an IF_IIU interrupt request (flag IIU_BCNTZERO set) when the bit counter becomes zero. If the application does not load new data and a new bit counter value before the transmission of the current bit has finished, the IIU switches back to IDLE state and signals the end of transmission at the same time with an IF_IIU interrupt request (flag IIU_FINISHED set).

SHIFT and SHIFTCONT state

Both states SHIFT and SHIFTCONT are used for general purpose modulation tasks and for stand-alone usage of the HT calculation unit. In both states the following blocks are enabled automatically:

- shift register
- bit counter
- encoder (enabling depends on IIU_ENCSEL)
- HT calculation unit (enabling depends on HTEN)

When the bit counter reaches the value 0, an IF_IIU interrupt request (flag IIU_BCNTZERO set) is generated. In this case, in SHIFT state the IIU switches back to IDLE state, while in SHIFTCONT state the IIU keeps the state until the CPU changes the state setting.

The SHIFT state is convenient when the HT calculation unit is operated in stand-alone mode or the last byte of a general purpose modulation is processed. The SHIFTCONT state is helpful when implementing general purpose modulation and the CPU requires some time after processing to load new data.

2.4.6.4 IIU wake-up

The IIU provides a signal to wake-up or interrupt the application. Hence, the CPU can enter IDLE mode while the IIU operates autonomously until the desired operation has been finished.

The wake-up or interrupt signal is generated in three cases:

- Bit counter zero: the required number of bits was received / transmitted / shifted.
- Enter/keep TXWAIT state: a stop condition was recognized and the IIU advances to TXWAIT state or the 200 cycle wait time has elapsed without switching to TXDATA state.
- IIU operation finished: the automated IIU operation has been finished and the state machine enters IDLE state automatically.

2.4.7 Registers

2.4.7.1 IIU data register IIUDAT

The IIU data register provides access to the 8 bit shift register, which gives byte-wise access (Table 20) to the received and transmitted data as well as to the HT calculation unit.

While accessing IIUDAT by the CPU it has to be ensured that the register content is stable, otherwise the data may be invalid. IIUDAT is not buffered. Every read or write access is directly accomplished to the internal shift register.

Table 20. IIU data register IIUDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	IIUDATA[7:0]	R/W		Rx/Tx Buffer

Typically during transmission, the MSB (bit 7) of the shift register is shifted out first. In case the number of bits to be transmitted is less than 8, the data bits should be aligned to bit 7. In case of reception of data consisting of less than 8 bits, the LSB is aligned to bit 0 (Table 21). The transmission bit order can be changed to LSB first by setting bit IIU_LSBF to ‘1’ in register IIUCON0.

Table 21. IIU data transfer examples with 3 bits, alignment of transmit and receive data

Transfer bit order	Transfer direction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB first (IIU_LSBF = ‘0’)	Transmit data	T2 (1st)	T1	T0	X	X	X	X	X
	Receive data	X	X	X	X	X	R2 (1st)	R1	R0
LSB first (IIU_LSBF = ‘1’)	Transmit data	X	X	X	X	X	T2	T1	T0 (1st)
	Receive data	R2	R1	R0 (1st)	X	X	X	X	X

2.4.7.2 IIU control register IIUCON0

The IIU Control Register IIUCON0 provides bits to control the selection of data transfer order, modulator, data out and clock. Please note that CPU and IIU shall use the same clock source and IIU clock selection must be set accordingly.

Table 22. IIU control register IIUCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IIU_LSBF	R/W		IIU data transfer order
			0	MSB first
			1	LSB first
6 and 5	IIU_MODSEL[1:0]	R/W		IIU modulator selection
			00	Port pins Inactive output level: 0
			01	Port pins Inactive output level: 1
			10	Port pins + standard LF modulator (high-ohmic) Inactive output level: 0
			11	Port pins + strong LF modulator (high-ohmic + low-ohmic) Inactive output level: 0

Table 22. IIU control register IIUCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
4 to 2	IIU_DPSEL[2:0]	R/W		IIU data path selection
			000	RXD (received data)
			001	RXD inverted
			010	SO (shift register serial output)
			011	SO inverted
			100	RXD XOR SO
			101	RXD XNOR SO
			110	Reserved for future use
			111	Reserved for future use
1 and 0	IIU_CLKSEL[1:0]	R/W		IIU clock selection
			00	Field clock
			01	Timer 0 overflow
			10	Peripheral clock (PCLK)
			11	No clock

IIU_MODSEL[1:0], IIU modulator selection

The encoded data stream can be provided to the LF field modulator or to a dedicated port pin.

In case the signal is provided to the LF modulator, the LF field can be modulated by switching on/off additional load in the analog front-end. The LF field modulator contains a standard modulator and a strong modulator. If the standard modulator is selected, the high ohmic path is turned on (weak modulation), while selecting the strong modulator, both the low-ohmic path and the high ohmic path are enabled (strong modulation). If the strong modulator is selected, the low-ohmic path is turned on with a delay of 1 clock cycle to ensure seamless operation of the LF clock recovery.

Selecting the LF modulator, the inactive IIU output level at the end of the encoding is set to 0, independent whether a port pin is selected additionally or not. In case the signal is provided only to a port pin, the inactive IIU output level can be chosen. The inactive IIU level is also used in IIU IDLE mode or in case the encoder is disabled (IIU_ENCSEL = 00b).

Writing IIU_MODSEL changes the inactive IIU output level immediately unless the IIU is running. The application shall not modify these bits if the IIU is running to avoid any unintentional behavior.

IIU_DPSEL[2:0], IIU data path selection

The IIU data path can be configured to have different input sources for the HT calculation unit and for the shift register:

- Received data bit RXD (plain or inverted)
- Shift register output SO (plain or inverted)
- RXD xor SO
- RXD inverted xor SO

IIU_CLKSEL[1:0], IIU clock select

Different clock sources can be selected by IIU_CLKSEL to be used for the shift register / encoder / bit counter / HT calculation unit. The peripheral clock (PCLK) is mainly intended for stand-alone operation of the calculation unit, while using Timer 0 overflow supports flexible baud rate generation for custom protocol implementations.

The application shall change the setting of IIU_CLKSEL only, if the IIU is in IDLE state (IIU_STATE[2:0] = 000b). A change of IIU_CLKSEL when the IIU is running can cause unpredictable behavior.

2.4.7.3 IIU control register IIUCON1

The IIU Control Register IIUCON1 provides bits for immediate execution and for the number of bits to be send or received.

Table 23. IIU control register IIUCON1 (reset value 0xh)

Bit	Symbol	Access	Value	Description
7	IIU_PRIO	R/W		Priority for immediate execution
			0	No bit processing during TXWAIT
			1	Immediate bit processing during TXWAIT
6 to 4	RFU	R0/W0		Reserved for future use
3 to 0	IIU_BITCNT[3:0]	R/W		Number of bits to be received/transmitted/shifted
			0000	Read access: 0 bit Write access: Invalid
			0001	1 bit
			0010	2 bit
			0011	3 bit
			0100	4 bit
			0101	5 bit
			0110	6 bit
			0111	7 bit
			1000	8 bit
			1001 - 1111	Invalid

IIU_PRIO, IIU priority for immediate execution

IIU_PRIO has only effect in TXWAIT state. With IIU_PRIO it can be specified whether the value written to IIU_BITCNT[3:0] shall be processed immediately or not.

Setting IIU_PRIO to '0' corresponds to "normal" operation, hence in TXWAIT state the shift register and HT calculation unit is not clocked and no shift or load operation is performed.

Setting IIU_PRIO to '1' performs the shift or load operation immediately. In this case, the bit counter content will not be interpreted as state exit condition, but will be used to process immediately the number of specified shifting steps written to the counter. This feature enables the application to use the shift register and/or HT calculation unit in TXWAIT state and is useful e.g. when the HT calculation unit needs to be pre-loaded with a value before the TXDATA state is entered.

The IIU and CPU shall use the same clock source and the same clock speed when setting IIU_PRIO.

IIU_BITCNT[3:0], IIU number of bits received/transmitted/shifted

IIU_BITCNT[3:0] provides access to the IIU bit counter. The value written to the register corresponds to the number of bits to be received/transmitted/shifted. The bit counter counts downwards from the written value to 0. Writing '8' to IIU_BITCNT causes to receive/transmit/shift 8 bits. Once 0 is reached, an IF_IIU interrupt request (flag IIU_BCNTZERO set) is generated.

It has to be considered that the register content can be unstable if IIU_BITCNT is accessed when the IIU is processing data. Hence, the application shall check the flag IBCNTZERO rather than the content of IIU_BITCNT to determine the status of the bit counter.

2.4.7.4 IIU control register IIUCON2

The IIU Control Register IIUCON2 provides a bit to enable clear text one bit command support.

Table 24. IIU control register IIUCON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 1	RFU	R0/W0		Reserved for future use
0	IIU_OBCSEN	R/W		Enable clear text one bit command support
			0	All received data passes through the normal data path
			1	Received data consisting of a single bit is passed directly from the data path selection multiplexor output to the data shift register input without passing through, or shifting, the HT calculation unit.

IIU_OBCSEN, enable clear text one bit command support

IIU_OBCSEN provides a means of bypassing the HT calculation unit for received data that consists of a single bit. When IIU_OBCSEN is set to ‘1’, one bit received data is passed directly from the data path selection multiplexor output to the data shift register input without passing through, or shifting, the HT calculation unit. If the HT calculation unit is disabled (HTEN set to ‘0’ in HTCON), IIU_OBCSEN has no effect on the IIUDATA.

An example application for this data path mode is in the HT2-E and HT3 transponder protocols where the one bit commands, REFRESH and SOFT_RESET, are always sent in clear text (information that is not encrypted) whereas the multi-bit commands may be in cipher text (information that is encrypted).

2.4.7.5 IIU status register IIUSTAT

The status of the IIU can be monitored via the IIU Status Register.

Table 25. IIU status register IIUSTAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IIU_LFDATA	R		LF data
			0	LF field unmodulated
			1	LF field LOW modulation
6	IIU_LFDEMEN	R/W		Analog LF demodulator enable
			0	Disable
			1	Enable
5	IIU_RST	R0/W		IIU reset
			0	No effect
			1	Execute reset
4 and 3	IIU_ENCSEL[1:0]	R/W		IIU encoding selection
			00	Disable encoder
			01	NRZ encoding
			10	Manchester encoding
			11	CDP encoding
2	IIU_TXWAIT	R/W1->0		IIU TXWAIT interrupt flag
			0	No interrupt request
			1	Interrupt request
1	IIU_FINISHED	R/W1->0		IIU finished interrupt flag
			0	No interrupt request
			1	Interrupt request
0	IIU_BCNTZERO	R/W1->0		IIU bit counter zero interrupt flag
			0	No interrupt request
			1	Interrupt request

IIU_LFDATA, LF data

IIU_LFDATA allows direct read access to the demodulated data signal coming from the analog LF demodulator.

The analog LF demodulator senses the differential voltage across the coil inputs (pin IN1P and IN1N). When the demodulator detects a LF field LOW modulation, IIU_LFDATA is set, otherwise cleared. While the LF demodulator is disabled, IIU_LFDATA yields a one.

IIU_LFDEMEN, analog LF demodulator enable

IIU_LFDEMEN enables or disables the analog LF demodulator.

After activation the signal IIU_LFDATA is undefined until the LF demodulator settling time $t_{LFDSETUP}$ is elapsed. The application shall reset the LF decoder with bit IRST thereafter to clear any latched spurious event at IIU_LFDATA, which might occur during start-up of the LF demodulator.

IIU_RST, IIU reset

The reset bit IIU_RST can be used to generate an asynchronous reset of the IIU comprising the state machine, the LF decoder with the internal counters, the IIU output signal and the interrupt request flags.

Launching a reset when the IIU is running causes an immediate stop. The IIU enters IDLE state and the IIU output switches to the specified inactive level.

The bit counter value IIU_BITCNT is not influenced by the reset operation as a new value for IIU_BITCNT shall be written anyway in order to start a subsequent operation.

IIU_ENCSEL[1:0], IIU encoding selection

The data encoder can be configured to operate in different encoding modes.

IIU_TXWAIT, IIU TX wait interrupt flag

The IIU_TXWAIT interrupt flag is set under the following two conditions:

- The IIU changes from RXFIRST or RXDATA to TXWAIT state since an LF stop condition is detected
- The IIU stays in TXWAIT state after the TX wait period (200 cycles) has elapsed and the exit condition is not true

IIU_TXWAIT can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_TXWAIT is not supported. Writing a zero has no effect and does not alter the stored value.

IIU_FINISHED, IIU finished interrupt flag

The IIU_FINISHED interrupt flag is set if the IIU operation is finished and IDLE state is entered, which occurs under the following two conditions.

- Unexpected end of receive: The IIU is in RXFIRST or RXDATA state, the bit counter IIU_BITCNT is equal to 0 and a LF LOW modulation is again received (stop condition not met).
- End of transmission/shift operation: The bit counter IIU_BITCNT is equal to 0 and the last bit was transmitted (state TXDATA) or shifted (state SHIFT) completely

IIU_FINISHED can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_FINISHED is not supported. Writing a zero has no effect and does not alter the stored value.

IIU_BCNTZERO, IIU bit counter zero interrupt flag

The IIU_BCNTZERO interrupt flag indicates that the bit counter has reached the value 0, hence the instructed number of bits was received/transmitted/shifted.

IIU_BCNTZERO can be cleared either manually by writing a '1' or automatically by writing to register IIU_BITCNT. Manual setting of IIU_BCNTZERO is not supported. Writing a zero has no effect and does not alter the stored value.

2.4.7.6 IIU state register IIUSTATE

The IIU state can be monitored and controlled via the IIU state register IIUSTATE. Reading IIUSTATE reflects the actual IIU state, while a value written to IIUSTATE has an immediate effect on the IIU state.

Table 26. IIU state register IIUSTATE (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 3	RFU	R0/W0		Reserved for future use
2 to 0	IIU_STATE[2:0]	R/W		IIU state
			000	IDLE
			001	RXWAIT
			010	RXDATA
			011	TXWAIT
			100	TXDATA
			101	SHIFT
			110	SHIFTCONT
			111	RXFIRST

2.5 LF Active interface (PKE receiver)

The device supports communication for passive keyless entry (PKE) applications by a high sensitive 3D LF active interface that receives data over a wide input range.

The 3D LF active interface consists of a 3D LF receiver and a preprocessor. The LF interface autonomously monitors the coil inputs for a modulated LF carrier and, in case a pre-defined LF telegram is detected, a device wake-up is caused and the Manchester decoded data will be buffered for post-processing with the RISC. Figure 21 shows a general block diagram of the LF active interface.

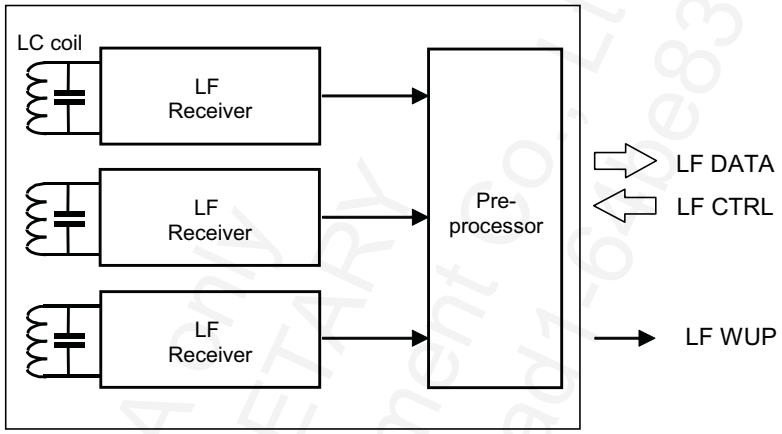


Fig 21. LF Active interface, block diagram

2.5.1 Receiver

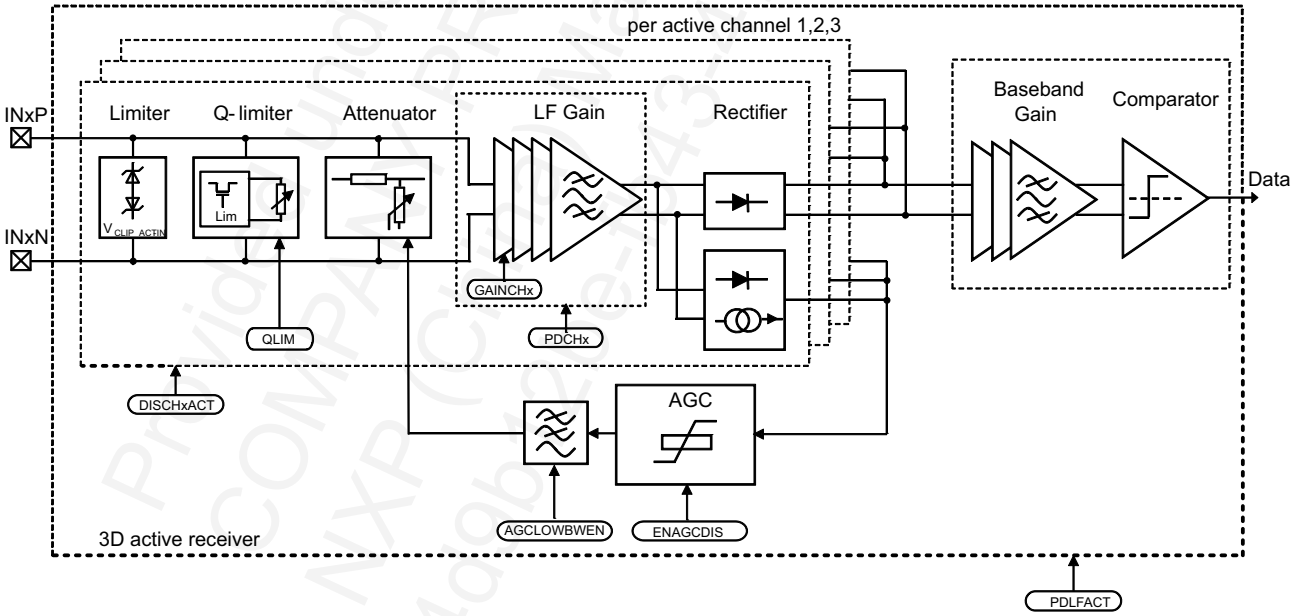


Fig 22. Active LF receiver block diagram

The configurable 3D LF active receiver consists of three active channels and one baseband amplifier (Figure 22). The LF active receiver monitors the three coils for amplitude modulation of the field from the base station and converts the modulation into a serial data stream. The LF active receiver is powered from the regulated battery domain VBATAREG and has ultra low power consumption.

Each of the three coils is connected to its own active channel, comprising of:

- Q-factor limiter
- Attenuator
- Preamplifier
- Rectifier

2.5.1.1 Q-factor limiter

The Q-factor limiter limits the system Q factor of the LF active interface during LF data reception dynamically. For this, different input resistors can be selected and are applied in parallel to the external resonant circuit.

For high input voltages, a current limiter becomes active in parallel to the selected resistance and increases the differential input resistance. The resulting non-linear resistance behavior is advantageous compared to a fixed value e.g. for the immobilizer application.

2.5.1.2 Preamplifier

The preamplifier contains four gain stages (LF Gain, in Figure 22) in each of the three channels. Each gain stage is band limited to minimize noise. Second to fourth gain stages have fixed gains, while the first gain stage is configurable to activate a high sensitivity modes where the gain is increased by 6 dB or 12 dB by means of GAINCHx[1:0] bits (Table 37).

The overall gain of the preamplifier is controlled by an automatic gain control (AGC) circuit. A common AGC is used to make equal the gain for all three active channels. The AGC loop is controlled by a DC level derived from the rectified voltages at the output of the 3 channel Rectifier blocks. The AGC sources the feedback signals to the preamplifier's Attenuator block.

The signal outputs of the three active channels are summed before being passed to the baseband amplifier (Baseband Gain, in Figure 22).

2.5.1.3 Baseband Amplifier

The baseband block comprises three bandwidth limited gain blocks and a comparator. The comparator at the output of the baseband amplifiers converts the demodulated signal into a digital data stream as input to the preprocessor unit.

2.5.2 Preprocessor

The preprocessor works independently of the RISC core and autonomously monitors the demodulated, digitized signal coming from the LF receiver for a distinct LF telegram. The preprocessor supports byte wise data reception. Command or data handling is determined by the application program.

Figure 23 shows the block diagram of the preprocessor. The digital filter removes possible spikes from the data signal. The code violation detector detects a code violation pattern and activates the Manchester decoder, which decodes the received data which can be a wake-up ID or data.

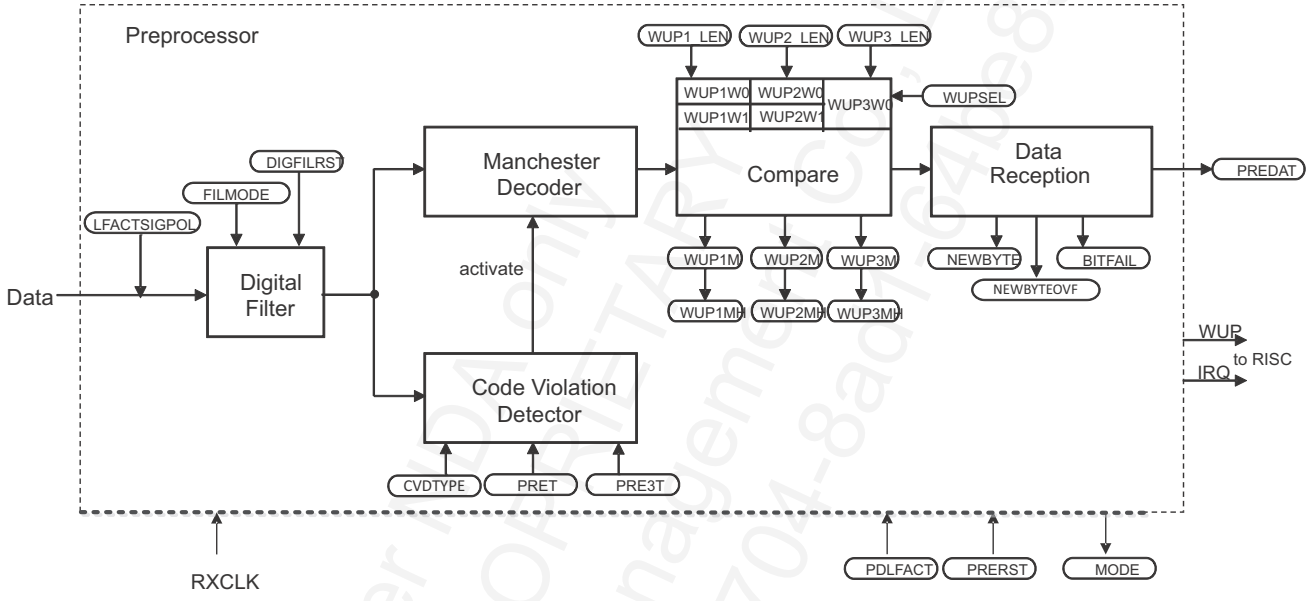


Fig 23. Preprocessor block diagram

In case a wake-up ID is detected a wake-up event or interrupt is generated, dependent on the configuration. When data bits are received they are shifted to the internal data register (PREDAT) to be accessed via the RISC core. The preprocessor is supplied via VBATREG.

While the LF interface monitors the coil inputs, the RISC normally is set into POWER OFF state in order to minimize the system power consumption. The application can also power-down the active interface.

The preprocessor operates with the low power RC oscillator.

2.5.2.1 Manchester coding

The digitized input data of the preprocessor is Manchester coded and characterized by the time durations between the signals rising edges. Thus, all bit timings in the preprocessor section are timings measured between two consecutive rising edges of the decoded protocol.

The Manchester coded data have a bit length T of 128 µs (8 kbit/s), 256 µs (4 kbit/s) or 512 µs (2.1 kbit/s) and a pulse width of 50% of the overall bit length.

A zero of a Manchester coded bit at the input of the preprocessor is coded as a transition from high to low state, a one is coded as a transition from low to high state.

The Manchester coded bits and the related LF patterns are shown in Figure 24. During the high state of the coded bit the LF signal is on, during the low state the LF signal is off.

In case the device detects a violation of the Manchester coding (rising edge monitored only), the status flag BITFAIL is set, an interrupt is generated, the decoding process is stopped and the device waits for a new frame starting again with a code violation.

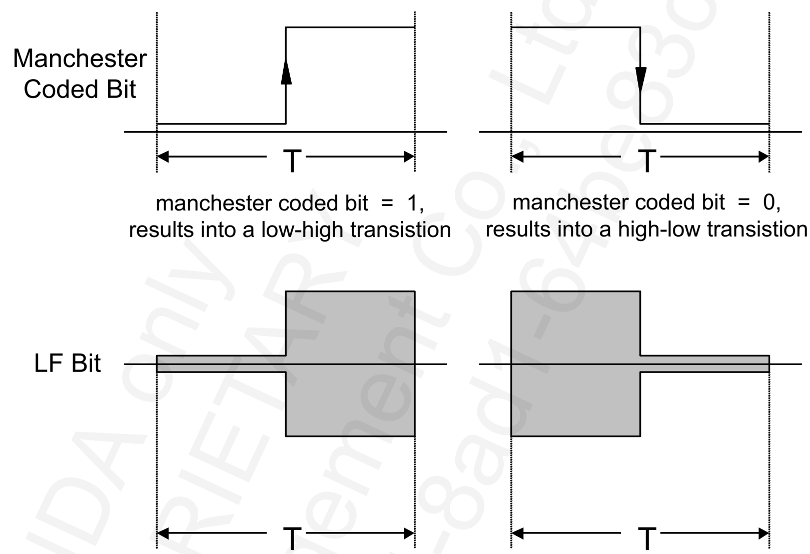


Fig 24. Manchester code

2.5.2.2 LF telegram

When enabled the LF interface autonomously monitors the coil inputs for a modulated LF carrier representing a distinct LF telegram to cause a device wake-up. The LF telegram organization is shown in Figure 25.

The LF telegram comprises:

- Preamble
- Code violation pattern (synchronization)
- Wake-up ID

Subsequently data might follow to be received and demodulated by the LF circuitry. All preprocessor bit timings are measured between two consecutive rising edges of the decoded protocol.

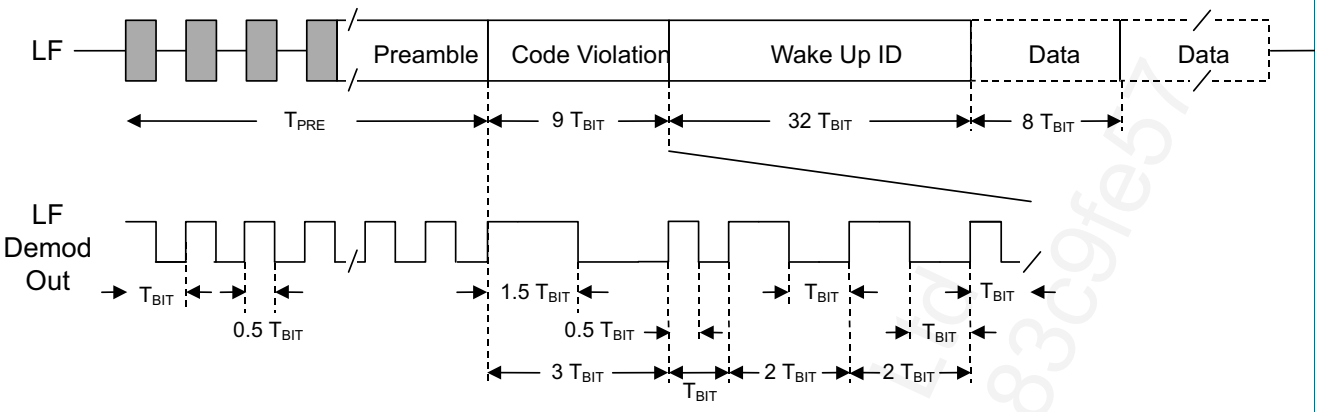


Fig 25. LF telegram

Preamble

The preamble is a sequence of Manchester coded “zeros” allowing the LF interface to settle its analog circuitry. The preamble shall feature a minimum length t_{PRE} depending on the baud rate as specified in Table 182 “Dynamic characteristics”.

Code violation pattern

During the wake-up sequence first a “code violation” (CV) pattern has to be detected, which is a pre-defined startup pattern transmitted at the beginning of the data telegram. The CV pattern features a fixed length of 8 bit times.

The code violation length is evaluated by a counter clocked from the low power RC oscillator (or from its divisions). The counter clock depends on the baud-rate.

A running code violation detection process is indicated by the MODE bits. If any deviation to the expected code violation is detected, the code violation detection unit is reset and starts again.

The synchronization pattern consists of the code violation pattern, followed by a Manchester coded zero bit.

Wake-up ID

After recognizing the synchronization pattern, the preprocessor decodes the Manchester coded data stream and searches for a user programmed wake-up code.

Each rising edge starts the decoding process and the position of the next rising edge is evaluated. If the position of one rising edge related to the previous one is out of the valid range, a code failure is detected and the decoding process is stopped. As only rising edges of the input signal are detected and processed, code failures caused by a wrong position of a falling edge will not be detected.

The preprocessor wakes up the RISC when at least one of the enabled user programmed wake-up patterns (by means of WUPSEL settings, Table 33) is detected. In case all wake-up patterns are disabled, the wake-up signal for the RISC is generated immediately after reception of the zero-bit following the code violation. A RISC wake-up brings the device into BATTERY state.

The preprocessor wake-up pattern detector features an optional tolerance of a single bit error during the wake-up pattern matching. This feature can be enabled by means of dedicated control bit, ERRTOLEN, in the PRECON6 register. When enabled, the fault tolerance mechanism will ignore the received erroneous bit in the wake-up pattern if it is associated with a Manchester-code timing violation detected within an expected bit time-frame. When the fault is detected and tolerated, the ERRTOL flag will be set in PRESTAT (Table 40) at the end of the wake-up pattern receiving. In this case, other status flags, e.g. WUPxM, will still indicate wake-up pattern match, followed by the WUP pattern match wake-up event. In case of double or multiple Manchester code violation, no WUP pattern match will occur.

Data reception

After RISC wake-up, the device will continue sampling the LF interface in order to detect and decode possible further data. This data is buffered in an 8 bit LF data register and available for the RISC for post-processing indicated by flag NEWBYTE set.

If subsequent data frames have been received without clearing NEWBYTE, the 8 bit register is overwritten at the end of each frame, while an interrupt is being generated and the flag NEWBYTE_OVF is set in PRESTAT (Table 40), at the same time. As a result, the application program has to read the 8 bit register and clear NEWBYTE prior to the end of the next frame. If the protocol is violated, e.g. due to mismatch of data frames, a BITFAIL is detected and the device sets the flag BITFAIL and generates an interrupt. Since there is no specific method to terminate a message the end of the message will typically be recognized by a NEWBYTE followed by a BITFAIL. In this case, the RISC may still read a valid data from PREDAT register when the NEWBYTE flag is set. Note that the PREDAT register shall be read before clearing the NEWBYTE flag. While the NEWBYTE flag can be reset by RISC and a successful wake-up pattern match, the NEWBYTE_OVF flag will also be reset by RISC and at next successful wake-up pattern match. To avoid the possibility of missing a NEWBYTE overflow, the simultaneous reset of the NEWBYTE_OVF flag when the RISC resets the NEWBYTE flag can be disabled by setting NEWBYTEOVFHOLD to 1.

For possible higher baud-rates and also to relax response time by the RISC, the LF data can be buffered optionally by means of the FIFO buffer. With the FIFO buffer enabled, the buffer time available following a pattern wake-up is up to (not longer than) the transmission time of 4 bytes of data, compared to 2 bytes of data without the FIFO enabled. The processor must read the first byte and clear the NEWBYTE flag before this period is finished to avoid a NEWBYTE_OVF.

When the FIFO buffer is enabled, e.g. when FIFOEN is set 1 in PRECON9, the preprocessor will receive the first byte, set the NEWBYTE flag and assert an interrupt as in case of single byte buffering. The RISC is expected to read the PREDAT register and to clear the NEWBYTE flag. When the RISC clears NEWBYTE, it may also check the NEXTFIFODATAOK flag (Table 40) indicating that a further byte is also present in the FIFO. If the NEWBYTE flag is not cleared by the RISC, the preprocessor will continue receiving up to 3 new bytes (24 payload data bits) before an interrupt is asserted and the NEWBYTE_OVF flag is set by the preprocessor, indicating the FIFO overflow. Note that in case the FIFO is enabled, the NEWBYTE_OVF flag is set and the related interrupt is fired, data in the FIFO buffer will be corrupted. Any reading of PREDAT before NEWBYTE or after NEWBYTE_OVF is set will return invalid data. For details refer to Ref. 1.

2.5.3 Polling of LF Active receiver

To minimize average power consumption in the system and to increase the external battery life time, the LF receiver in the key device can be powered-up and -down periodically. The LF transmitter in the car base-station is sending periodically repetitive wake-up messages. While powered-up, the LF receiver will monitor the LF pins for a repetitive wake-up message sent by the LF base-station. If a wake-up message is validated, the LF receiver will remain powered up for an extra T_{ON} period. T_{OFF} state will not be entered while the message is being received. In case no message is detected during the T_{ON} period, the LF receiver is powered-down and any wake-up message sent eventually by the base-station transmitter will be ignored until the next T_{ON} interval takes place.

In Figure 26 the basic principle of the polling mode based on configurable T_{ON} and T_{OFF} time is shown.

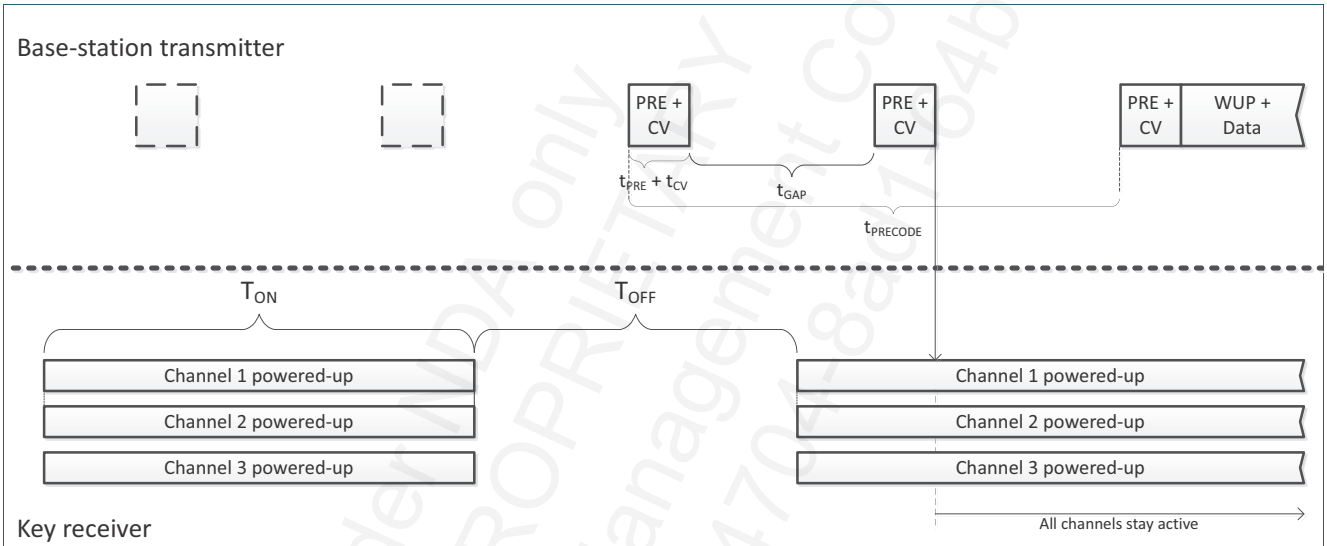


Fig 26. Polling principle

2.5.3.1 Polling protocol and receiver configuration

During PKE polling the base-station sends regularly spaced repetitions of preamble (PRE) and code violation (CV) patterns. After several repetitions a WUP-pattern is appended to the PRE+CV pattern. The TON time is chosen to guarantee detection of at least one of the PRE+CV patterns. Note that due to the accuracy of the low-power RC oscillator on the key side, a margin must be taken into account when choosing the TON and TOFF times.

The polling timing is affected by the combined preamble and code violation duration which is dependent on the baudrate and also on the Active receiver settling time for polling mode. The polling timing is also affected by the t_{GAP} time which is controlled by the car side base station depending on the desired activity level, e.g. 50% duty cycle. The value for $t_{PRECODE}$ from Figure 26 is controlled by the preceding factors and by the number of repetitions before a WUP pattern is found and is determined by the desired response time of the LFACTIVE protocol. Examples with possible protocol parameters are shown in Table 27.

Table 27. Protocol parameter examples

Base-station transmitter					Key receiver						
Baudrate [Kbaud]	$t_{PRE}+t_{CV}$ [µs]	t_{GAP} [ms]	Number PRE+CV	$t_{PRECODE}$ [ms]	t_{POLL_SETT} [µs]	t_{ON} [µs]	t_{OFF} [µs]	$f_{PrePro, typ}$ [KHz]	$T_{CLK,typ}$ [µs]	TON	TOFF
1.95	6656	20	3	53.3	2500	39393	39740	45	2844	0E	0D
3.91	4352	10	3	28.7	2500	23324	19667	90	1422	11	0D
3.91	4352	20	3	48.7	2500	34324	37667	90	1422	19	1A
3.91	4352	40	3	88.7	2500	56324	73667	90	1422	28	33
7.81	3200	20	3	46.4	2500	31790	36630	180	711	2D	33
1.95	6656	20	4	80.0	2500	39393	63731	45	2844	0E	16
3.91	4352	10	4	43.1	2500	23324	32548	90	1422	11	16
3.91	4352	20	4	73.1	2500	34324	59584	90	1422	19	29
3.91	4352	40	4	133.1	2500	56324	113584	90	1422	28	4F
7.81	3200	20	4	69.6	2500	31790	57510	180	711	2D	50
1.95	6656	20	5	106.6	2500	39393	87721	45	2844	0E	1E
3.91	4352	10	5	57.4	2500	23324	45500	90	1422	11	1F
3.91	4352	20	5	97.4	2500	34324	81500	90	1422	19	39
3.91	4352	40	5	177.4	2500	56324	153500	90	1422	28	6B
7.81	3200	20	5	92.8	2500	31790	78390	180	711	2D	6E

Considering target base-station transmitter parameters, the key receiver polling intervals, T_{ON} and T_{OFF} can be calculated as following.

T_{ON} can be chosen as higher or equal to:

- $T_{ON} = 1.1 * [\ 2 * (t_{PRE}+t_{CV}) + 1000 * t_{GAP} + t_{POLL\_SETT}\ ]$

while T_{OFF} time can be chosen as smaller or equal to:

- $T_{OFF}=0.9 * [\ (Number-2) * (t_{PRE} + t_{CV}) + (Number-1) * 1000 * t_{GAP} - t_{POLL\_SETT}\ ]$.

Remark: In the above expressions the factor 1.1 and 0.9 are introduced to allow for a 10% variation in the low power RC clock.

For a datarate of 3.91 Kbaud, a t_{GAP} of 10ms and 3 repetitions the T_{ON} and T_{OFF} is calculate as 23324µs and 19667µs. Adjusting TON and TOFF via registers PREPOLL0 and PREPOLL1 (Table 57 and Table 58) results finally into a power-up duty cycle of the receiver of 56.7% and a saving of 43.3%. The base-station duty cycle is given in this case with 45,5%. Higher savings in power consumption can be achieved with increasing t_{GAP} e.g. to 40 ms. The base-station transmission duty-cycle reduces to 14.7% and the resulting duty-cycle on the key-side to 44%.

2.5.3.2 Polling state machine

The preprocessor polling is enabled by ENPOLL (table 57). When polling is not enabled the polling state machine will be in INIT mode. When polling is active and no LF activity occurs then the polling state machine will go between the ACTIVE ON and ACTIVE OFF states with period determined by TON and TOFF times. When an LF active transmission is detected during the ACTIVE ON state then the ACTIVE ON state will be held until the end of the LF transmission and then the TON period will restart. The LF will be allowed to be active in INIT and ACTIVE ON states and will be forced to an inactive, low power state in the ACTIVE OFF state.

The polling state machine in the key receiver is shown in Figure 27.

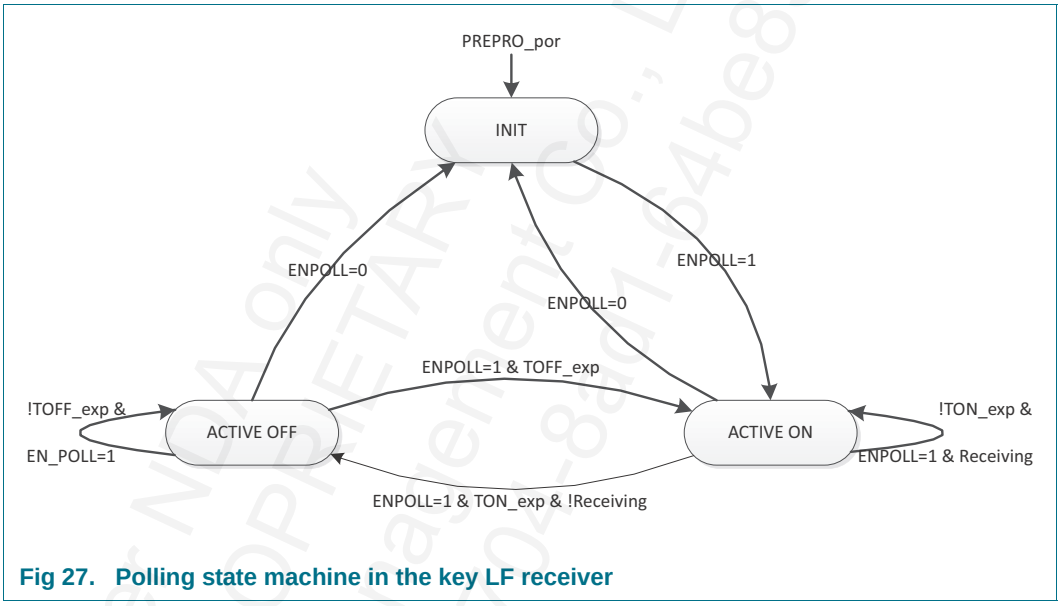


Fig 27. Polling state machine in the key LF receiver

2.5.4 Received signal strength indication (RSSI)

The received signal strength indication (RSSI) is intended as an analogue interface between the coil-input pins and the analog digital converter (ADC). The analog digital converter is described in Section 2.16 “Voltage, Temperature and RSSI Measurement”. The RSSI block in Figure 28 consists of:

- Q factor adjustment
- Attenuator
- Input multiplexer
- Programmable gain section
- Peak-detection stage

The Q-factor adjustment allows controlling the Q-factor of the resonant circuit. The attenuator is provided to limit the signal amplitude. The RSSI input signal can be chosen from all three coil-inputs via an input-multiplexer. The output signal of the multiplexer is fed to a configurable gain-chain. Due to the high dynamic range of the input signal (> 80 dB) several gain-settings can be adjusted. The appropriate gain-setting is identified with the help of a fast range overflow detector. The amplified signal is switched via a peak detection stage to the input of an ADC to provide the result of the RSSI measurement.

In order to save measurement time, the RSSI and ADC bandgap blocks can be powered on during normal communication sequences. In this case, the RSSI input-multiplexer has to be set to GND. Active communication sequences are not allowed during RSSI measurement.

The RSSI is accommodated in the VDDA supply domain. The application shall turn on the VDDA supply switch before the RSSI block can be used. The ADC bandgap block shall not be switched on in parallel to the RSSI block, instead first the RSSI block shall be switched on, then the ADC bandgap block can be switched on.

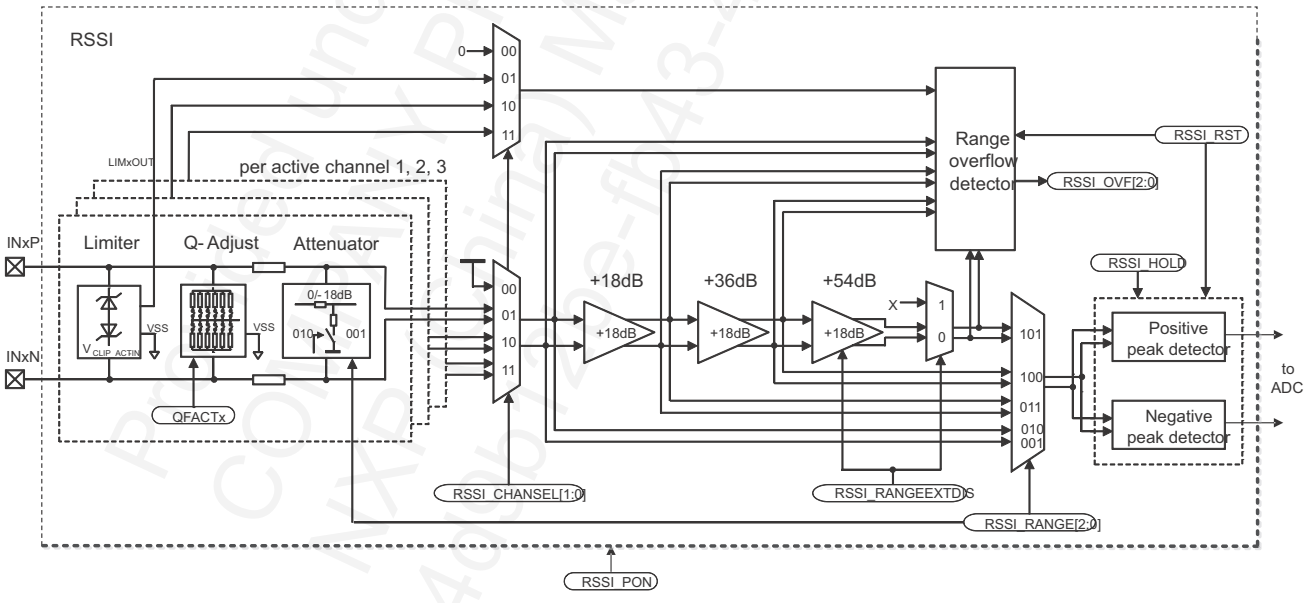


Fig 28. RSSI block diagram

2.5.4.1 Q factor adjustment

A Q-factor adjustment is provided to allow control of the Q-factor of the resonant circuit Figure 29. Therefore different coils can be used for each of the 3D LF channels. The Q factor adjustment on channel 1 shall be used in RSSI mode only. If used in standard reception mode the input pins will be loaded (if VBAT supply is present) and thus have influence on the immobilizer performance.

The Q-factor adjustment is implemented by loading the coil with different resistors, each enabled via a corresponding switch. Each resistor is divided into two equal parts that are connected to ground via switches. By this, the sinusoidal voltages at either end of the coil will be equal in amplitude (but opposite in phase) with respect to ground.

By providing six weighted resistors (R1Q to R6Q) in parallel, meaningful resistor values can be adjusted by switching on/off various combinations.

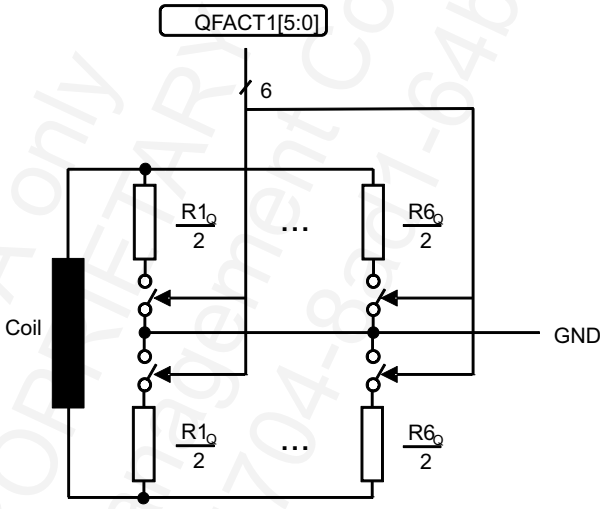


Fig 29. Q-factor adjustment

2.5.4.2 Input multiplexer

The input multiplexer selects the source for the RSSI measurement. All three channels can be selected. After selecting a channel, the active receivers of all channels have to be disabled (DISAGCCHx = 1) in order to disable the AGC.

It is also possible to choose GND as input for the RSSI measurement, which is needed for the recommended autozero-sequence.

The output signal of the multiplexer is fed to a configurable gain-chain.

2.5.4.3 Programmable gain section

Due to the wide dynamic range of the input signal, several gain settings and attenuations can be selected in order to ‘precondition’ the input signal into an appropriate voltage range for the ADC.

The corresponding gain setting is determined via a fast range overflow detector, which consists of several overflow stages.

2.5.4.4 Peak-detection stage

The previously determined gain setting can be selected by switching the corresponding output of the amplifier chain to the peak-detectors.

The peak-detector output voltage is stored and switched to the input stage of the ADC, which digital output code represents the analog input amplitude of the chosen channel (except the limiter signal is chosen, which ADC value is not relevant).

Dependent on the range setting and attenuation (RSSI_RANGE[2:0]), gain corrections have to be applied in order to calculate the applied input voltage. Raw-data have to be offset compensated first.

If very accurate measurement results (absolute value of measured input signal) are desired, it is recommended to perform the compensation/calibration with an additional look-up table or with stored calibration values.

2.5.4.5 RSSI measurement sequence

An RSSI measurement sequence consists in general of an offset measurement and afterwards of three consecutive single channel RSSI measurements. The offset measurement is needed to compensate non-idealities of the gain-chain and ADC. In order to get the final RSSI result, the offset has to be subtracted from the respective channel results. RSSI measurement software routines are provided as C library to be linked to the application program.

Condition for an RSSI measurement sequence is a constant carrier input signal on the selected input channel. Modulated input signals will lead to lower RSSI values caused by the averaging characteristic of the ADC. During the RSSI measurement it is necessary to deactivate the AGC of the LF active receivers (DISAGCCHx = 1), while the amplifiers in the respective channel can be kept on (PDAMPCHx = 0).

The RSSI measurement starts with powering on first the RSSI block and then the ADC bandgap block by setting RSSI_PON and then ADC_PON. After power-on, the application shall wait until the RSSI block, the ADC band-gap block and the related buffer block have settled ($t_{RSSI,PON}$ and $t_{BG,PON}$, respectively), before the first measurement can be started. It is recommended to power-on the RSSI block in the ‘autozero’ configuration (RSSI_CHANSEL[1:0] = 00). In this case, the first RSSI measurement (in general the offset measurement) can omit to wait the channel selection time $t_{CHANSEL}$.

In order to minimize the overall measurement time, it is recommended to select the next channel (RSSI_CHANSEL[1:0]) at the end of the respective single channel measurement as fast as possible. If the total measurement time of the RSSI measurement sequence is exceeding 2 ms, flag R2MSDET should be set regularly to reset the 2 ms detection.

Single channel RSSI measurement

A single channel RSSI measurement starts with setting the gain to 54 dB (RSSI_RANGE[2:0] = 101, RSSI_RANGEEXTDIS = 0) or 36 dB (RSSI_RANGE[2:0] = 100, RSSI_RANGEEXTDIS = 1) and with selecting the channel to be measured (RSSI_CHANSEL[1:0]). Together with the channel selection the peak-detectors have to be reset (RSSI_RST = 1). The reset-state has to be kept for the minimum channel selection time $t_{CHANSEL}$.

To avoid transitional effects, the peak detector must be kept in reset while changing range settings. The Range selection time $t_{RANGESEL}$ shall be counted after the instruction that sets new RSSI_RANGE settings. Similarly, after changing RSSI_RANGEEXTDIS it is recommended to wait at least twice the $t_{RANGESEL}$ time. After releasing reset (RSSI_RST=0), the application software must be waiting for new valid indicator output, t_{IND}, before proceeding with ADC conversion.

After releasing the peak-detector reset (RSSI_RST = 0) and waiting for the settling time t_{IND}, the range overflow bits (RSSI_OVF[2:0]) can be evaluated. The gain-chain has to be set accordingly (RSSI_RANGE[2:0], RSSI_RANGEEXTDIS). After the range change and after waiting the range selection time $t_{RANGESEL}$, again the peak-detector has to be reset (RSSI_RST = 1) and RSSI_HOLD has to be set to 0 for the minimum reset time t_{RESPR}. After releasing the reset again (RSSI_RST = 0) and after considering the peak-detector settling time $t_{PEAKDSET}$ the AD conversion can be started by setting ADCCON.CONVSTART. An interrupt (IF_ADC) is generated when the conversion is finished. The result (raw-data) of the measurement can be fetched from the ADC data registers.

Offset measurement of the RSSI-chain

The offset-measurement needs to be performed only once for all three channels, if the single channels are measured immediately afterwards one after the other.

For the offset measurement, the channel-selection multiplexer input has to select GND (RSSI_CHANSEL[1:0] = 00) and both the amplifier gain and the attenuator have to be set to 0 dB (RSSI_RANGE[2:0] = 010). The offset measurement is performed like a single channel RSSI measurement, except of the range overflow detection procedure, which is not required.

2.5.5 Interval Timer and Real-time Clock

The interval timer and the real time clock (RTC) use the same counter chain, but are able to activate two independent wake-up flags including the corresponding interrupts simultaneously. Due to the continuous operation with battery supply, both timers operate independently of the device supply state and can operate with the low power RC oscillator.

The interval timer can generate periodical events in order to wake-up the device from POWER OFF state. The wake-up times are selectable by IT_SEL. Dependent on the IT_MODE settings, the interval timer provides a 2.1 kHz clock at the LPDIVCLK output. DIGFILRST = 1, PRERST = 1: This setting can be used when a reset of the preprocessor is required or when only the interval timer shall be used without using the preprocessor.

The real time clock features a 16 bit register holding minutes, seconds and fractions of seconds with a resolution better than 100 ms. The provided information can be used to display the time or as time stamp for protocols. The application can extend the time with additional software counters stored in battery supplied registers. The wake-up times of the real-time clock can be set via RTC_SEL.

The status bits RTC_WUP, RTC_WUP_OVF and IT_WUP are located in register PRESTAT. The real time clock data is stored in the register RTCDAT.

2.5.6 Registers

When the device is in the field and the preprocessor is receiving data, it is recommended not to change the registers in order to prevent malfunction. If the application wants to change these bits, the control bits PRERST and DIGFILRST shall be set first. For turning off the active receiver and preprocessor the bit PDFLACT is provided. The registers are clocked with the low power RC oscillator and not buffered or synchronized to the CPU clock. While accessing the registers by the CPU it has to be ensured that the register content is stable, otherwise the data may be invalid.

2.5.6.1 Preprocessor data register PREDAT

The preprocessor data register provides access to a data byte received via the active interface, Table 28.

Table 28. Preprocessor data register PREDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	PREDATA[7:0]	R/W		Preprocessor data byte

2.5.6.2 Preprocessor real-time clock control register RTCCON

The interval timer and real-time clock control register RTCCON is shown in Table 29.

Table 29. Preprocessor control register RTCCON (reset value 80h)

Bit	Symbol	Access	Value	Description
7	ITRST	R/W		Interval timer reset
			0	No reset
			1	Reset and disable interval timer and real time clock
6 and 5	RTC_SEL[1:0]	R/W		Real time clock event period
			00	No wake-up
			01	1 sec
			10	1 min
			11	60 min
4 to 2	IT_SEL[2:0]	R/W		Interval timer event period
			000	No wake-up
			001	500 us
			010	100 ms
			011	500 ms
			100	1 sec
			101	2 sec
			110	1 min
			111	2 min

Table 29. Preprocessor control register RTCCON (reset value 80h)

Bit	Symbol	Access	Value	Description
1 and 0	IT_MODE[1:0]	R/W		Interval timer operation modes
			00	Interval timer and real time clock are stopped. FSEC, SEC and MIN registers can be written. Any write access to these registers re-initializes the interval timer, thus all bits are cleared. In case the LPRC oscillator clock is used, the lower nibble is loaded with the LPRC_CAL[3:0] bits. LPDIVCLK output (for details, see CLKCON3.TMUX0C) is stopped.
			01	Reserved for future use
			10	Interval timer is running and real time clock is stopped. FSEC, SEC and MIN registers can be written. If selected, the interval timer generates a periodical wake-up after 500 us [IT_SEL[2:0] = 001]. For all other settings of IT_SEL, no wake-up is generated. LPDIVCLK output provides 2.1 kHz clock.
			11	Interval timer and real time clock are running. If IT_SEL and RTC_SEL are zero, no interrupts are generated by the timers. LPDIVCLK output provides 2.1 kHz clock

ITRST, interval timer reset

Setting ITRST stops the counter chain for both the interval timer and the real time clock and clears FSEC, SEC, MIN, IT_WUP, RTC_WUP and RTC_WUP_OVF. ITRST is used if the interval timer and real time clock are not needed or if they shall be stopped and configured again.

ITRST can be set when the interval timer and real time clock are running. Setting ITRST permanently resets the interval timer and the values of MIN, SEC and FSEC can not be modified.

IT_SEL[2:0], interval timer wake-up period

If an application changes IT_SEL while the interval timer is running, the first wake-up for this new value may occur earlier than expected. If the application does not use the real time clock, it can avoid this by clearing the interval timer first (IT_MODE[1:0] = 00b – real time clock is cleared as well) and then changing IT_SEL.

IT_MODE[1:0], interval timer operation modes

The interval timer and the real time clock are controlled via IT_MODE[1:0]. It is recommended to check the bits after writing in order to consider a possible synchronization delay between the CPU and the interval timer clock sources.

Stopping the interval timer via IT_MODE[1:0] is recommended before IT_SEL, RTC_SEL and LPRC_CAL[3:0] are modified in order to generate even the first wake-up in the expected time.

2.5.6.3 Preprocessor control register PRECON2

The preprocessor control register PRECON2 is shown in Table 30.

Table 30. Preprocessor control register PRECON2 (reset value E0h)

Bit	Symbol	Access	Value	Description
7	DIGFILRST	R/W		Digital filter reset
			0	No reset
			1	Digital filter is reset and disabled
6	PRERST	R/W		Preprocessor reset
			0	No reset
			1	Preprocessor (except digital filter) is reset and disabled; status bits WUP1M, WUP2M, WUP3M, NEWBYTE and BITFAIL are cleared
5	PDLFACT	R/W		Power-down LF active receiver
			0	Disabled
			1	Enabled
4	RFU	R/W0		Reserved for future use
3 to 2	BDRATE[1:0]	R/W		Baud-rate
			00	Baud-rate 1.95 kbit/s Low power RC oscillator sampling clock 45 kHz
			01	Baud-rate 3.9 kbit/s Low power RC oscillator sampling clock 90 kHz
			10	Baud-rate 7.8 kbit/s Low power RC oscillator sampling clock 180 kHz
			11	Reserved for future use
1	RFU	R/W0		Reserved for future use
0	LPRC_EN	R/W		Low power RC oscillator enable
			0	Power-down mode, no clock provided
			1	Active mode

DIGFILRST, PRERST, digital filter reset and preprocessor reset

Dependent on the DIGFILRST and PRERST settings, the preprocessor can be used in different use cases.

DIGFILRST = 0, PRERST = 1: This setting can be used when a direct decoding of user defined protocols without using the hard-wired preprocessor is required. In this case the output of the digital filter can be directly connected to a capture port of timer 1. The software can use the timer values for decoding. Since the sampling clock depends on the baudrate and has influence on the filter structure, the correct baudrate shall be selected, even if the digital filter is used without the hard-wired preprocessor.

DIGFILRST = 1, PRERST = 1: This setting can be used when a reset of the preprocessor is required or when only the interval timer shall be used without using the preprocessor.

PDLFACT, power-down LF active receiver

The active receiver and the preprocessor are supplied by the regulated battery supply. Hence, they are supplied even when the RISC is not supplied. When the device is not used for a long time, the RISC has the possibility to power-down the LF active receiver (PDLFACT = 1).

Setting PDLFACT, the LF active circuit and the preprocessor are disabled in order to decrease the power consumption. Further, the settings of register PREPD and of the register bits DISCHxACT are ignored and all blocks controlled by these registers are set in power-down.

If bit PDLFACT is ‘1’, no keyless entry communication is possible and the battery supplied registers keep their contents. The only way to reset the power-down of the LF active receiver is to wake-up the RISC by any other wake-up event (e.g. a button press) and run a software routine that will set PDLFACT back to zero.

Setting PDLFACT does not turn off the low power RC oscillator, since these clocks might be used by other applications.

BDRATE[1:0], baud-rate

These bits determine the baud-rate for data reception. Changing these bits switches the internal sampling clock.

When selecting high baud-rates (e.g. 7.8 kbit/s,[BDRATE[1:0] = 10b) the boot time t_{BOOT_WUP} can be greater than the time to transmit the first data byte and data could be lost due to an overflow condition.

LPRC_EN, low power RC oscillator enable

This bit enables the low power RC oscillator. When the RC oscillator is not used, it should be set to power-down mode (LPRC_EN = 0) in order to reduce power consumption.

2.5.6.4 Preprocessor control registers PRECON3 to 5

The preprocessor control registers PRECON3, PRECON4 and PRECON5, which are related to channel 1, 2 and 3, respectively, are shown in Table 31

Table 31. Preprocessor control register PRECON3, 4 and 5 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	DISCHxACT	R/W		Disable active channel x
			0	Enable active channel
			1	Disable active channel
6	PDx_6DB	R/W		Legacy gain mode, when GAINCHx=11; otherwise, don’t care
			0	G01 mode (6dBm)
			1	G00 mode (0dBm)
5	QFACTx[5]	R/W		Q-factor adjustment of channel x receiver coil via resistor R6Qx
			0	Disable R6Qx
			1	Activate R6Qx
4	QFACTx[4]	R/W		Q-factor adjustment of channel x receiver coil via resistor R5Qx
			0	Disable R5Qx
			1	Activate R5Qx
3	QFACTx[3]	R/W		Q-factor adjustment of channel x receiver coil via resistor R4Qx
			0	Disable R4Qx
			1	Activate R4Qx
2	QFACTx[2]	R/W		Q-factor adjustment of channel x receiver coil via resistor R3Qx
			0	Disable R3Qx
			1	Activate R3Qx
1	QFACTx[1]	R/W		Q-factor adjustment of channel x receiver coil via resistor R2Qx
			0	Disable R2Qx
			1	Activate R2Qx
0	QFACTx[0]	R/W		Q-factor adjustment of channel x receiver coil via resistor R1Qx
			0	Disable R1Qx
			1	Activate R1Qx

DISCHxACT, disable AGC channel x:

Setting DISCHxACT to '1' disables the AGC operation and the AGC limiter for channel x. This setting is provided for RSSI measurement.

Setting DISCHxACT to ‘0’ enables the AGC operation and the AGC limiter for channel x. This setting is provided for LF active protocol reception. By clearing DISCHxACT, the attenuator clamp voltage of the corresponding channel (CHx) is decreased.

PDx_6DB, power-down additional 6dB gain of first stage in channel x

When the legacy gain control-mode is selected by GAINCHx=11, the PDx_6DB set 1 will select the 0dB gain of the first stage in channel x. This has the same effects as the GAINCHx=00, selecting the G00 mode. The opposite value, PDx_6DB=0, will select the 6dB gain, and will be equivalent to selecting G01 mode by GAINCHx=01. Note, the legacy gain-control mode supports two gain configurations only the 0dB and the 6dB.

QFACTx[5:0], Q-factor adjustment of receiver coil in channel x

With QFACTx[5:0] the Q-factor of the receiver coil in channel x is adjusted by loading the coil with different resistances. For this, six resistors are provided in parallel (R1Qx to R6Qx) which can be activated each on demand. This allows to use different coils for the respective 3D LF channel.

2.5.6.5 Preprocessor control register PRECON6

The preprocessor control register PRECON6 is shown in Table 32.

Table 32. Preprocessor control register PRECON6 (reset value 07h)

Bit	Symbol	Access	Value	Description
7	RFU	R/W0		Reserved for future use
6	ERRTOLEN	R/W		Error tolerance in WUP enable
			0	Error tolerance disabled
			1	Error tolerance enabled
5	CVTYPE	R/W		Code violation source pattern
			0	Calibrated 8T
			1	Reserved for future use
4	RFU	R/W0		Reserved for future use
3 to 0	LPRC_CAL[3:0]	R/W		Calibration of low power RC oscillator frequency
			1111	-8.8%
			1110	-7.7%
			1101	-6.6%
			1100	-5.5%
			1011	-4.4%
			1010	-3.3%
			1001	-2.2%
			1000	-1.1%
			0111	0.0%
			0110	+1.1%
			0101	+2.2%
			0100	+3.3%
			0011	+4.4%
			0010	+5.5%
			0001	+6.6%
			0000	+7.7%

ERRTOLEN, Enable error tolerance in WUP

When ERRTOLEN is set one, the single-bit error tolerance during wake-up pattern receive will be turned on. If this bit set to zero, no error tolerance will be enabled. Latter state is valid per default and is backwards compatible to the predecessors wake-up receive function.

CVTYPE, code violation source pattern

The CVTYPE bit is for future extensions and shall be set to 0. Zero indicates the calibrated 8T value used for internal manchester code timing limits.

LPRC_CAL[3:0], calibration of low power RC oscillator frequency

These bits are used to correct the inaccuracy of the low power RC oscillator (if selected) which influences the wake-up timing of the interval timer and of the real time clock.

2.5.6.6 Preprocessor control register PRECON7

The preprocessor control register PRECON7 is shown in Table 33.

Table 33. Preprocessor control register PRECON7 (reset value PRECON7 = xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7 to 5	WUPSEL[2:0]	R/W		Wake-up pattern selection
			000	All wake-up patterns have length zero
			001	WUP1 pattern is enabled
			010	WUP2 pattern is enabled
			011	WUP1 pattern is enabled WUP2 pattern is enabled
			100	WUP3 pattern is enabled
			101	WUP1 pattern is enabled WUP3 pattern is enabled
			110	WUP2 pattern is enabled WUP3 pattern is enabled
			111	WUP1 pattern is enabled WUP2 pattern is enabled WUP3 pattern is enabled
4 to 0	WUP1_LEN[4:0]	R/W		Length of first wake-up pattern

WUPSEL[2:0], wake-up pattern selection

WUPSEL defines the interrupt conditions for the patterns WUP1, WUP2 and WUP3.

In case all wake-up patterns have a length of zero, no wake-up matching process is done and after reception of zero bit (after code violation), WUP3M, WUP2M and WUP1M in the status register are set and an interrupt is generated.

In case the WUP1 pattern is enabled, the received wake-up pattern is compared with the content of the WUP1 register and when they match an interrupt is generated by setting the WUP1M bit. The length of WUP1 pattern is equal to WUP1_LEN + 1.

In case the WUP2 pattern is enabled, the received wake-up pattern is compared with the content of the WUP2 register and when they match an interrupt is generated by setting the WUP2M bit. The length of WUP2 pattern is equal to WUP2_LEN + 1.

In case the WUP3 pattern is enabled, the received wake-up pattern is compared with the content of the WUP3 register and when they match an interrupt is generated by setting the WUP3M bit. The length of WUP3 pattern is equal to WUP3_LEN + 1.

If more than one bit of WUPSEL is set, several wake-up pattern are enabled in parallel. The first pattern that matches generates a corresponding wake-up interrupt.

WUP1_LEN[4:0], length of first wake-up pattern

WUP1_LEN determines the length of the first wake-up pattern, whereby the pattern length is WUP1_LEN + 1. Hence, while the wake-up length register has a range from 0 to31, the pattern length becomes 1 to 32.

2.5.6.7 Preprocessor control register PRECON8

The preprocessor control register PRECON8 is shown in Table 34.

Table 34. Preprocessor control register PRECON8 (reset value 0x0xxxxxb)

Bit	Symbol	Access	Value	Description
7	NEWBYTEOVFHOLD	R/W		Prevent clear of NEWBYTE_OVF flag
			0	NEWBYTE_OVF flag will be cleared when the NEWBYTE flag is cleared
			1	NEWBYTE_OVF flag clear is prevented when the NEWBYTE flag is cleared
6	RFU	R/W0		Reserved for future use
5	PDIREFSTUP	R/W		Power down of the IREF startup circuit
			0	IREF startup circuit enabled (default value)
			1	IREF startup circuit disabled
4 to 0	WUP2_LEN[4:0]	R/W		Length of second wake-up pattern

NEWBYTEOVFHOLD, Prevent clear of NEWBYTE_OVF flag

In the rare circumstance that a new byte overflow occurs in the period between reading the overflow bits and clearing the NEWBYTE/NEWBYTE_OVF the NEWBYTE_OVF flag will typically be lost but data may be corrupted by the overflow. In order to preserve the NEWBYTE_OVF flag the NEWBYTEOVFHOLD bit should be set.

PDIREFSTUP, Power down control of the IREF startup circuit

To support proper timing of the LF active receive channels at startup, the software has to ensure that the IREF startup circuit is enabled, by means of PDIREFSTUP set to 0 during startup. Once when the LF Active circuit has been powered up after 50µs, to save current consumption during receiving, the IREF startup circuit can be disabled by software, by means of PDIREFSTUP set to 1.

WUP2_LEN[4:0], length of second wake-up pattern

WUP2_LEN determines the length of the second wake-up pattern, whereby the pattern length is WUP2_LEN + 1. Hence, while the wake-up length register has a range from 0 to 31, the pattern length becomes 1 to 32.

2.5.6.8 Preprocessor control register PRECON9

The preprocessor control register PRECON9 is shown in Table 35.

Table 35. Preprocessor control register PRECON9 (reset value x000_xxxxb)

Bit	Symbol	Access	Value	Description
7	RFU	R/W0		Reserved for future use
6 to 5	DIGFILMODE[1:0]	R/W		Digital filter mode
			00	Standard filter setting
			01	Reserved for future use
			10	Reserved for future use
			11	Reserved for future use
4	FIFOEN	R/W		FIFO buffer enable
			0	FIFO buffer disabled
			1	FIFO buffer enabled
3 to 0	WUP3_LEN[3:0]	R/W		Length of third wake-up pattern

DIGFILMODE[1:0], digital filter mode

These two bits shall be set to 00.

FIFOEN, Receiver FIFO buffer enable

When this bit is set one, the three-byte FIFO buffer is enabled to store the received data after the wake-up pattern. When equal zero, as per default, the FIFO buffer is disabled and the data buffer length is 1 byte as in predecessor devices.

WUP3_Len[3:0], length of third wake-up pattern

WUP3_LEN determines the length of the third wake-up pattern, whereby the pattern length is WUP3_LEN + 1. Hence, while the wake-up length register has a range from 0 to 15, the pattern length becomes 1 to 16.

2.5.6.9 Preprocessor control register PRECON10

The preprocessor control register PRECON10 is provided to limit the system Q factor of the LF active interface and to adapt the AGC bandwidth to the used baudrate. (Table 36).

Table 36. Preprocessor control register PRECON10 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 5	QLIM[2:0]	R/W		Q-factor limiter
			000	Off
			001	Reserved for future use
			010	Reserved for future use
			011	Reserved for future use
			100	Reserved for future use
			101	Activate R1QLIM
			110	Activate R2QLIM
			111	Activate R3QLIM
4 to 3	RFU	R/W0		Reserved for future use
2	AGCLOWBWEN	R/W		AGC low bandwidth enable
			0	Adapt AGC to high baudrate
			1	Adapt AGC to low baudrate
1 to 0	RFU	R/W0		Reserved for future use

QLIM[2:0], Q-factor limiter

QLIM[2:0] is provided to limit the Q-factor by adjusting the input resistance of the LF active channels.

When selecting a value RxQLIM, the Q-factor limiter becomes active for each active channel and applies a differential input resistance in parallel to the external resonant circuit. For small input voltages (in the range of Vsens), the selected value RxQLIM is directly applied. For higher input voltages, additionally a current limiter becomes active, thus increasing the differential input resistance.

During RSSI measurements, it is recommended to switch off the Q-factor limiter.

AGCLOWBWEN, AGC low bandwidth enable

Setting AGCLOWBWEN is provided to adapt the AGC bandwidth to the baudrate. This bit shall be set for a baudrate of 2.1 kBit/s (BDRATE[1:0] = 00) and shall be reset for other baudrates.

2.5.6.10 Preprocessor control register PRECON11

The preprocessor control register PRECON11 is shown in Table 37. Related to predecessor devices, PRECON11 is added to allow for the additional 12dB gain stage selection and to enable backwards-compatible gain settings control by the user software.

Table 37. Preprocessor control register PRECON11 (reset value FCh)

Bit	Symbol	Access	Value	Description
7 and 6	GAINCH3[1:0]	R/W		Channel 3 gain selection
			00	G00 mode, 0dB gain selected
			01	G01 mode, 6dB gain selected
			10	G10 mode, 12 dB gain selected
			11	Legacy gain-control mode
5 and 4	GAINCH2[1:0]	R/W		Channel 2 gain selection
			00	G00 mode, 0dB gain selected
			01	G01 mode, 6dB gain selected
			10	G10 mode, 12 dB gain selected
			11	Legacy gain-control mode
3 and 2	GAINCH1[1:0]	R/W		Channel 1 gain selection
			00	G00 mode, 0dB gain selected
			01	G01 mode, 6dB gain selected
			10	G10 mode, 12 dB gain selected
			11	Legacy gain-control mode
1	RFU	R/W0		Reserved for future use
0	RINMODE	R/W		Automated disable of the LF Active circuit in IMMO mode
			0	LF Active connected to INxP/INxN pins in IMMO mode
			1	LF Active automatically disconnected in IMMO mode

GAINCHx selection bits

GAINCHx selects one of the three provided gain configurations in the LF Gain block: the 0dB, the 6dB or the 12dB configuration, or so called G00, G01 and G10 gains, respectively.

With the default configuration GAINCHx=11, the PDx_6DB gain settings in PRECON3, PRECON4, and PRECON5 will have to be used to select between two legacy gains: 0dB and 6 dB. In this gain-control mode, maximal gain of 12dB cannot be selected.

RINMODE, LF Active loading LF pins control bits

The device is equipped with an optional feature of automated LF Active circuit disconnection during IMMO mode. By means of RINMODE, it is defined whether this feature is enabled or not. When the bit is set to 1, the LF Active circuit attenuator will be disconnected from the LF pins actively, which allows for more efficient LF-field energy consumption throughout the minimized leakage current flowing into the LF Active circuit when LF passive circuit is to be supplied.

2.5.6.11 Preprocessor control register PRECON12

The preprocessor control register PRECON12 is shown in Table 38.

Table 38. Preprocessor control register PRECON12 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 0	RFU	R/W0		Reserved for future use

2.5.6.12 Preprocessor status register PRESTAT

The preprocessor status register contains status information of the preprocessor block in order to detect e.g. matching wake-up patterns. After a battery insertion and when the CPU resets the preprocessor (by setting PRERST and ITRST) the status bits are cleared.

The preprocessor status register provides byte and word access.

Table 39. Word and byte access to the status register PRESTAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRESTAT	PRESTATH	PRESTATL

The specific status bits are cleared by writing a ‘1’, while writing a ‘0’ leaves the corresponding bit unchanged. For example, writing data = 01h, bit 0 of the status register is cleared.

Table 40. Preprocessor status register PRESTAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 14	MODE[1:0]	R		Preprocessor state
			00	No active communication
			01	Code violation running
			10	WUP matching
			11	Data reception
13	RTC_WUP_OVF	R		Real time clock wake-up overflow flag
			0	No real time clock wake-up detected while RTC_WUP was set
			1	Real time clock wake-up detected while RTC_WUP was set
12	NEXTFIFODATOK	R		Next byte OK in FIFO operation
			0	No new byte following current NEWBYTE
			1	New byte available following current NEWBYTE
11	NEWBYTE_OVF	R		New byte overflow
			0	No new byte received while NEWBYTE was set
			1	New byte received while preprocessor data buffer is full
10	WUP3MH	R		Wake-up pattern 3 matching history flag
			0	Wake-up pattern did not match reference pattern 3 before
			1	Wake-up pattern did match reference pattern 3 before
9	WUP2MH	R		Wake-up pattern 2 matching history flag
			0	Wake-up pattern did not match reference pattern 2 before
			1	Wake-up pattern did match reference pattern 2 before

Table 40. Preprocessor status register PRESTAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
8	WUP1MH	R		Wake-up pattern 1 matching history flag
			0	Wake-up pattern did not match reference pattern 1 before
			1	Wake-up pattern did match reference pattern 1 before
7	ERRTOL	R		Single bit error in the last wake-up pattern
			0	No error appeared
			1	Error appeared and tolerated
6	IT_WUP	R/W1->0		Interval timer wake-up
			0	No wake-up event
			1	Wake-up event
5	RTC_WUP	R/W1->0		Real time clock wake-up
			0	No wake-up event
			1	Wake-up event
4	BITFAIL	R/W1->0		Bit failure
			0	No Manchester timing violation during data reception
			1	Manchester timing violation during data reception
3	NEWBYTE	R/W1->0		New data byte received
			0	No new data byte received
			1	New data byte received
2	WUP3M	R/W1->0		Wake-up pattern 3 matching flag
			0	Wake-up pattern does not match reference pattern 3
			1	Wake-up pattern matches reference pattern 3
1	WUP2M	R/W1->0		Wake-up pattern 2 matching flag
			0	Wake-up pattern does not match reference pattern 1 before
			1	Wake-up pattern matches reference pattern 2
0	WUP1M	R/W1->0		Wake-up pattern 1 matching flag
			0	Wake-up pattern does not match reference pattern 1 before
			1	Wake-up pattern matches reference pattern 1

Remark: Register bits RTC_WUP_OVF, IT_WUP and RTC_WUP are sources for the CPU interrupt controller interval timer and real time clock interrupt, flag IF_IT. Register bits NEWBYTE_OVF, WUPxMH, BITFAIL, NEWBYTE, WUPxM are sources for the CPU interrupt controller LF active preprocessor interrupt, flag IF_PP. Only register bits RTC_WUP_OVF, WUPxMH, IT_WUP, RTC_WUP and WUPxM are wake-up sources for the power management block.

RTC_WUP_OVF, real time clock wake-up overflow flag

The real time clock wake-up overflow flag is cleared automatically when bit RTC_WUP is cleared. Separate clearing of RTC_WUP_OVF is not supported. Entering POWER OFF state is only possible when this bit is cleared.

NEXTFIFODATOK, the next data in FIFO valid flag

When the FIFOEN is set 1, the NEXTFIFODATOK will indicate whether further data is available in the FIFO following the current byte. NEXTFIFODATOK must be read before NEWBYTE is cleared. When NEXTFIFODATOK is set to 1, further data can be read from the FIFO. When NEXTFIFODATOK is set to 0, data in the FIFO is not valid.

NEWBYTE_OVF, new byte overflow flag

The new byte overflow flag is set whenever a new byte is received and the NEWBYTE flag was set already. NEWBYTE_OVF is cleared automatically when bit NEWBYTE is cleared. Separate clearing of NEWBYTE_OVF is not supported. However clear of NEWBYTE_OVF will be prevented when NEWBYTEOVFHOLD is set.

WUPxM, WUPxMH, wake-up pattern x matching (history) flag

The wake-up pattern matching flags WUPxM represent the status of the last detected wake-up pattern. The corresponding history flags WUPxMH accumulate the status of all detected wake-up patterns, which were not yet processed. Two different conditions cause an update of the wake-up and wake-up history flags.

The first condition is that a new wake-up pattern match is detected. In this case, the corresponding wake-up flag WUPxM is set and all other wake-up matching flags are cleared. If more than one wake-up pattern matches at the same time all corresponding wake-up matching flags WUPxM are set. At the same time a pending ‘1’ in a wake-up flag WUPxM is transferred into the corresponding wake-up history flag WUPxMH. A pending ‘0’ in a wake-up flag does not influence the state of the history flag, i.e. once a history flag is set it keeps its state.

The second condition that causes an update of the flags is that a positive edge of the RISC controller power-on reset is detected. In this case, all wake-up pattern flags WUPxM are cleared and the wake-up pattern history flags are updated as described for the first condition.The second case is intended for applications which cannot be interrupted by a pattern matching event. If these applications finish with a reset of the RISC controller, the device boots again. The application can then decide whether to process or discard any old wake-up matching events.

The wake-up pattern matching flags and their corresponding history flags can be cleared manually by writing a ‘1’ to the respective wake-up matching flag WUPxM. Separate clearing of the wake-up flag and the corresponding wake-up history flag is not supported.

If any of the flags WUPxM or WUPxMH is ‘1’, an interrupt and a wake-up request for the power management is generated. Entering POWER OFF state is only possible when these bits are cleared.

When the wake-up length is zero a wake-up match occurs at the end of the code violation frame.

ERRTOL, Tolerated wake-up pattern error flag

When set 1, the ERRTOL bit flags a single-bit error that has been identified while receiving wake-up pattern. This bit is maintained if the ERRTOLEN is set 1. In this case, when Manchester code violation is detected on a single bit, the ERRTOL flag will be set by hardware at the end of the wake-up pattern. This bit is cleared by the application or after the PRERST set 1, or by new code-violations received.

IT_WUP, interval timer wake-up

An interrupt request is generated when a periodical wake-up occurs. The period of the wake-up signal is defined by IT_SEL[2:0]. Once this bit is set, it remains '1' until it is cleared by the application. Entering POWER OFF state is only possible when this bit is cleared.

RTC_WUP, real time clock wake-up

An interrupt request is generated when there is a wake-up caused by the real time clock. The period of the wake-up is selected by RTC_SEL[1:0]. Once this bit is set, it remains '1' until it is cleared by the application. Entering POWER OFF state is only possible when this bit is cleared.

BITFAIL, bit failure

This bit is set in case of a Manchester timing violation during data reception. A Manchester timing violation during wake-up reception does not set this bit. A bit-failure resets the Manchester decoder and a new protocol has to be started with a code violation. BITFAIL will be reset with a detected new code violation.

NEWBYTE, new data byte received

This bit is set and an interrupt request is generated when a new data byte is received. Once this bit is set, it remains '1' until it is cleared by the application. Moreover, this bit is cleared automatically by any subsequent wake-up match.

2.5.6.13 Preprocessor power-down register PREPD

The preprocessor power-down register is shown in Table 41.

Table 41. Preprocessor power-down register PREPD (reset value 00h)

Bit	Symbol	Access	Value	Description
7	AGCSENSRST	R/W		AGC sensitivity reset
			0	Disabled
			1	Enabled
6 to 0	RFU	R/W0		Reserved for future use, these bits shall be set to 000_0000b by the application code

AGCSENSRST, AGC sensitivity reset

Setting AGCSENSRST for a time $t_{AGC\_SENSRST}$ resets the sensitivity of the AGC internal node. This can be necessary during or after active communication in order to set the active reception unit into the default state with highest sensitivity. This is recommended for applications where a LF signal with high field strength is followed by a signal with low field strength.

2.5.6.14 Preprocessor T value register PRET

This register contains minimum and maximum values for T detection during code violation and has to be set by the application. This register allows word and byte access.

Table 42. Word and byte access to preprocessor T value register PRET

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRET	PRETMAX	PRETMIN

Table 43. Preprocessor T value register PRET (reset value xxh)

Bit	Symbol	Access	Value	Description
15 to 8	PRETMAX[7:0]	R/W		Tmax value used for code violation detection
7 to 0	PRETMIN[7:0]	R/W	1	Tmin value used for code violation detection

Default values of PRET are given in Table 44.

Table 44. Default values for PRET

Clock	Baudrate	PRET
Low power RC oscillator	2, 4 or 8 kbit/s	1D10h

2.5.6.15 Preprocessor 3T value register PRE3T

This register contains minimum and maximum values for 3T detection during code violation and has to be set by the application. This register allows word and byte access.

Table 45. Word and byte access to preprocessor 3T value register PRE3T

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRE3T	PRE3TMAX	PRE3TMIN

Table 46. Preprocessor 3T value register PRE3T (reset value xxh)

Bit	Symbol	Access	Value	Description
15 to 8	PRE3TMAX[7:0]	R/W		3Tmax value used for code violation detection
7 to 0	PRE3TMIN[7:0]	R/W		3Tmin value used for code violation detection

Default values of PRE3T are given in Table 47.

Table 47. Default values for PRE3T

Clock	Baudrate	PRE3T
Low power RC oscillator	2, 4 or 8 kbit/s	6038h

2.5.6.16 Preprocessor wake-up pattern register WUPxWy

The first and second reference wake-up patterns are stored in the registers WUP1 and WUP2, respectively. These registers allow word and byte access.

Table 48. Word and byte access to reference wake-up pattern register WUPxWy

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
WUPxW1	WUPxB3	WUPxB2
WUPxW0	WUPxB1	WUPxB0

In order to compute whether a received wake-up pattern matches one of the first two reference wake-up patterns, the first received wake-up ID bit is compared with WUPxW1[31], the second received bit with WUPxW1[30] and so on. If the wake-up pattern is shorter than 32 bits, the unused bits are not evaluated during the matching process.

Table 49. Preprocessor reference wake-up pattern register WUPxW0/1 (reset value xxxx xxxxh)

Bit	Symbol	Access	Value	Description
31 to 16	WUPxW1[31:16]	R/W		Reference wake-up pattern 1 or 2, upper bytes
15 to 0	WUPxW0[15:0]	R/W		Reference wake-up pattern 1 or 2, lower bytes

2.5.6.17 Preprocessor wake-up pattern register WUP3W0

The third wake-up pattern is stored in the register WUP3W0, which allows word and byte access.

Table 50. Word and byte access to reference wake-up pattern register WUP3

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
WUP3W0	WUP3B1	WUP3B0

In order to compute whether a received wake-up pattern matches the third reference wake-up pattern, the first received wake-up ID bit is compared with WUP3[15], the second received bit with WUP3[14] and so on. If the wake-up pattern is shorter than 16 bits, the unused bits are not evaluated during the matching process.

Table 51. Preprocessor reference wake-up pattern register WUP3W0 (reset value xxxxh)

Bit	Symbol	Access	Value	Description
15 to 0	WUP3W0[15:0]	R/W		Reference wake-up pattern 3

2.5.6.18 RSSI control register RSSICON

The RSSI block is controlled via the RSSI control register. The control settings are stored in the VDD domain.

Table 52. RSSI control register RSSICON (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 12	RFU	R/W0		Reserved for future use
11 to 9	RSSI_RANGE[2:0]	R/W		RSSI range selection
			000	Limiter
			001	Range -18 dB
			010	Range 0 dB
			011	Range +18 dB
			100	Range +36 dB
			101	Range 54 dB (only if RSSI_RANGEEXTDIS = 0)
			110	Reserved for future use
			111	Reserved for future use
8	RSSI_RANGEEXTDIS	R/W		RSSI range extension disable (high sensitivity)
			0	RSSI range extension on
			1	RSSI range extension off
7	RSSI_PON	R/W		RSSI power on
			0	RSSI block turned off
			1	RSSI block turned on
6 and 5	RSSI_CHANSEL[1:0]	R/W		RSSI channel selection for input multiplexer
			00	GND (intended for zero calibration and RSSI deactivated state)
			01	LF active channel 1
			10	LF active channel 2
			11	LF active channel 3
4	RSSI_HOLD	R/W		RSSI peak detector output hold
			0	Track input
			1	Store output voltage
3 to 1	RSSI_OVF[2:0]	R		RSSI range overflow
			000	Range -18 dB overflow
			001	Range 0 dB overflow
			010	Range 18 dB overflow
			011	Range 36 dB overflow
			100	Range 54 dB overflow (for RSSI_RANGEEXTDIS = 0) No overflow (for RSSI_RANGEEXTDIS = 1)
			101	No overflow
			110 - 111	Reserved for future use
0	RSSI_RST	R/W		RSSI reset
			0	No effect
			1	Reset analog peak detectors and indication signal information

RSSI_RANGE[2:0], RSSI range selection

It is recommended to set RSSI_RST when changing RSSI_RANGE[2:0] in order to prevent switching transients at the output of the peak-detector.

RSSI_RANGEEXTDIS, RSSI range extension disable

RSSI_RANGEEXTDIS disables the extended range. Enabling the extended range provides high sensitivity, while the increased current has to be considered. The RSSI measurement and RSSI range selection shall be executed with the same RSSI_RANGEEXTDIS setting.

A separate calibration for RSSI_RANGEEXTDIS = 0 or 1 is necessary. After switching RSSI_RANGEEXTDIS twice the settling time $t_{RANGESEL}$ has to be considered.

RSSI_CHANSEL[1:0], RSSI channel selection

If RSSI is turned off (RSSI_PON = 0), no channel is selected.

RSSI_HOLD, RSSI peak detector output hold

Setting RSSI_HOLD to 0, the RSSI output is tracking the input signal. In case RSSI_HOLD is set to 1, the output voltage of the peak-detectors is stored in capacitors and thus independent of the actual input signal.

RSSI_OVF[2:0], RSSI range overflow

A RSSI range overflow is encoded in the RSSI_OVF[2:0] register. The bits represent overflows in the respective RSSI measurement ranges. A value of ‘000’ indicates an input signal that is higher than the dynamic range of the RSSI amplifier-chain.

RSSI_RST, RSSI reset

Setting RSSI_RST, the analog peak detectors and range overflow signals are reset and the overflow signal information is updated. In order to prevent that former input signals will influence the RSSI measurement, RSSI_HOLD has to be 0 (discharge storing capacitors) before RSSI_RST is set.

2.5.6.19 LF channel-shorting control register LFSHCON

The LF pins feature active switches for attenuating the LF signals on the unused RSSI channels. Hence, while RSSI measurement is taking place on one LF channel, the other two can be attenuated by means of SHCHx bits in register (Table 53).

Table 53. LF channel-shorting control register LFSHCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 4	RFU	R/W0		Reserved for future use
3	SHCH3	R/W		Channel 3 short-switch control
			0	No attenuation, switch open
			1	Channel 3 input attenuated, switch closed
2	SHCH2	R/W		Channel 2 short-switch control
			0	No attenuation, switch open
			1	Channel 2 input attenuated, switch closed
1	SHCH1	R/W		Channel 1 short-switch control
			0	No attenuation, switch open
			1	Channel 1 input attenuated, switch closed
0	STDIS	R/W		Safety timer disable
			0	Safety timer enabled
			1	Safety timer disabled

SHCHx, Channel x short-switch control

The LF signal attenuation on given channel (INxP/N pair) pins, can be applied when the internal active switch is closed by means of SHCHx control bit set 1. No attenuation is applied when SHCHx control bit set 0. If the short switch control is enabled then the RSSI R_{short} resistance between INxN and INxP applies at the selected channel.

The SHCHx bits are automatically cleared and cannot be set to 1 when the device is supplied from the LF field, i.e. when device is in the LF FIELD state (PMODE = 0). The SHCHx bits are also cleared automatically on transition to the POWER OFF state.

STDIS, Safety timer disable control

To ensure the shorting switches are released after RSSI measurements are finished, a safety mechanism is included by means of a fixed interval timer. The safety timer uses the same clock as the watchdog timer and has a time-out interval of ~ 2.4 ms. The safety timer is active whenever any of the SHCHx bits is set to 1 and the STDIS bit set to 0, hence in default configuration. The time-out period will be restarted whenever is written with any of the SHCHx bits set to 1, unless STDIS is set to 1. The SHCHx bits are automatically cleared. whenever the safety time-out limit is reached. The safety timer stops automatically in debug mode.

When STDIS is set 1, no safety timer will be triggered nor running regardless on SHCHx settings. In this case, user software has to assure the channel switches are driven open after the RSSI measurement.

2.5.6.20 Real time clock data register RTCDAT

The RTCDAT register allows word and byte access of the real time clock data (Table 54).

Table 54. Word and byte access to the real time clock data register RTCDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
RTCDAT	RTCDATH	RTCDATL

Content of the real time clock data register is shown in Table 55. The contents of MIN, SEC and FSEC can be read or updated via write access. During write access, dependent on IT_MODE, the remaining bits of the RTCDAT register may change also.

Table 55. Real time clock data register RTCDAT (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 10	MIN[5:0]	R/W		Minutes
9 to 4	SEC[5:0]	R/W		Seconds
3 to 0	FSEC[3:0]	R/W	1	Fractions of second

MIN, minutes

MIN holds the number of passed minutes and increments every minute. After reaching the upper limit value of 59d, MIN is cleared with the next increment signal. In case an invalid value (> 59d) is written to MIN, this value will be kept until the next increment signal sets MIN to 0 again.

SEC, seconds

SEC holds the number of passed seconds and increments every second. After reaching the upper limit value of 59d, SEC is cleared with the next increment signal. In case an invalid value (> 59d) is written to SEC, this value will be kept until the next increment signal sets SEC to 0 again.

FSEC, fractions of seconds

FSEC holds a value representing the number of passed fractions of seconds. Any write access clears these bits.

Using the LPRC clock, FSEC is incremented every 100 ms and FSEC is re-initialized every 500 ms to FSEC[3:0] = {!FSEC[3], 0, 0, 0}, resulting in the sequence shown in Table 56. The values FSEC[2:0] = 101, 110, 111 do not occur.

Table 56. FSEC values using the LPRC clock

Time [ms]	FSEC decimal value	FSEC[3:0] binary value
0	0	0000
+ 100	1	0001
+ 100	2	0010
+ 100	3	0011
+ 100	4	0100
+ 100	8	1000
+ 100	9	1001
+ 100	10	1010

Table 56. FSEC values using the LPRC clock

Time [ms]	FSEC decimal value	FSEC[3:0] binary value
+ 100	11	1011
+ 100	12	1100
+ 100	0	0000

2.5.6.21 Polling control register PREPOLL0

The preprocessor polling register PREPOLL0 is shown in Table 57.

Table 57. Preprocessor control register PREPOLL0 (reset value 0011_1111b)

Bit	Symbol	Access	Value	Description
7	ENPOLL	R/W		Polling enable control
			0	Polling disabled
			1	Polling enabled
6	RFU	R/W0		Reserved for future use
5 to 0	TON[5:0]	R/W		Length of the TON interval, expressed as number of pre-divided TPREPRO,typ periods

ENPOLL, Enable polling

When, in the INIT state, ENPOLL is set 1 by user application, the ACTIVE ON state is entered and the polling cycle starts with counting the TON interval. When in any of states ENPOLL is set 0 by the user application, the INIT state will be entered and further polling intervals counting will be inhibited before application sets it again.

TON[5:0], Polling TON settings

The TON[5:0] represents the number of pre-divided low-power RC oscillator clock periods depending on the target baud-rate as follows:

- When target baud-rate is 2kbaud, TON[5:0]=(180*TON[us])/(512*1000).
- When target baud-rate is 4kbaud, TON[5:0]=(180*TON[us])/(256*1000).
- When target baud-rate is 8kbaud, TON[5:0]=(180*TON[us])/(128*1000).

2.5.6.22 Polling control register PREPOLL1

The preprocessor polling register PREPOLL0 is shown in Table 58.

Table 58. Preprocessor control register PREPOLL1 (reset value 0000_0111b)

Bit	Symbol	Access	Value	Description
7 to 0	TOFF[7:0]	R/W		Length of the TOFF interval, expressed as number of pre-divided TPREPRO,typ periods

TOFF[7:0], Polling TOFF settings

The TOFF[5:0] represents the number of pre-divided low-power RC oscillator clock periods depending on the target baud-rate as follows:

- When target baud-rate is 2kbaud, TOFF[7:0]=(180*TOFF[us])/(512*1000).
- When target baud-rate is 4kbaud, TOFF[7:0]=(180*TOFF[us])/(256*1000).
- When target baud-rate is 8kbaud, TOFF[7:0]=(180*TOFF[us])/(128*1000).

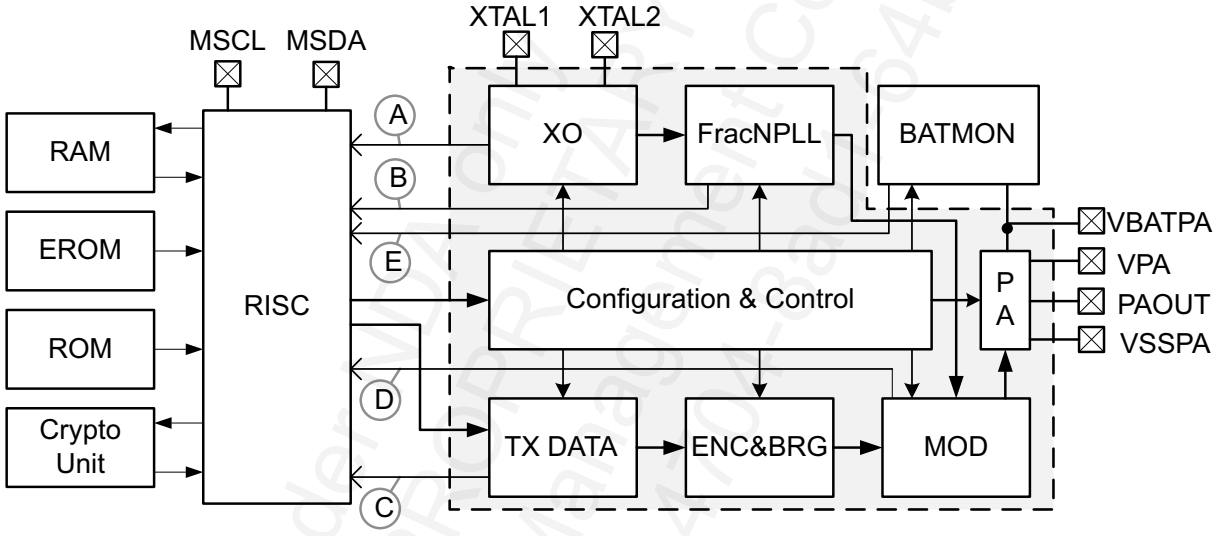
2.6 UHF transmitter

The NCF29A1 / NCF29A2 features a sophisticated on-chip ASK/FSK UHF transmitter designed for use in the ISM frequency ranges from 310 MHz to 447 MHz. The frequency bands
above 600 MHz can be supported on request. The transmitter incorporates a crystal oscillator, a fully integrated Phased-Locked-Loop frequency synthesizer and a power amplifier to drive an external antenna.

The transmitter comprises two mutually-exclusive modulators for Frequency Shift Keying (FSK) and for Amplitude Shift Keying (ASK). The ASK modulator can also perform On-Off Keying (OOK).

2.6.1 Block diagram

The functional blocks of the transmitter are shown in Figure 30, inside the dashed-line.



Transmitter interrupts: (A) XO Ready; (B) PLL Locked; (C) TX Buffer Empty; (D) Transmission Finished; (E) Battery Brownout

Fig 30. Transmitter block diagram

The transmitter includes baseband and RF signal processing. The baseband signal path includes the data buffer TX DATA, data encoder and baud rate generator, ENC & BRG. The RF-signal path consists of the frequency reference and frequency synthesizer blocks: the crystal oscillator XO and the Fractional-N Phase-Locked Loop - FracNPLL. The modulator block MOD provides a method to generate amplitude shift keying (ASK) waveforms with simple linear interpolation of amplitude levels. Similar linear interpolation of frequency deviation is supported for frequency shift keying waveforms (FSK). Simultaneous ASK and FSK modulation is not supported. Finally, the modulated RF signal gets amplified by the power amplifier PA.

The transmitter is typically operated by user software from EROM. The RAM may hold data for the transmission data buffer TX DATA.

2.6.2 Functional Description

The transmitter can be operated in BATTERY state only. The transmitter configuration is programmed via the Special Function Registers (SFR) in the digital core powered by the VDD domain. If a power on reset is asserted based on the VDD level threshold the configuration will be lost. The transmitter configuration may be changed in both, BATTERY and LF FIELD power states.

During UHF transmission it is recommended to select the crystal oscillator as clock source for the CPU and the micro controller peripherals, like generic timer modules.

2.6.2.1 Setting-up Transmission

In Figure 30 the *Configuration & Control* block represents the SFR registers containing the transmitter configuration. The user software needs to program the dedicated SFR locations to configure the target frequency, the modulation type and the modulation parameters before the UHF blocks are enabled for operation. Also the output power settings need to be configured before enabling the power amplifier. Finally, the data encoding mode and the data baud rate is set-up before initiating data transmission.

2.6.2.2 Transmission Control Sequence

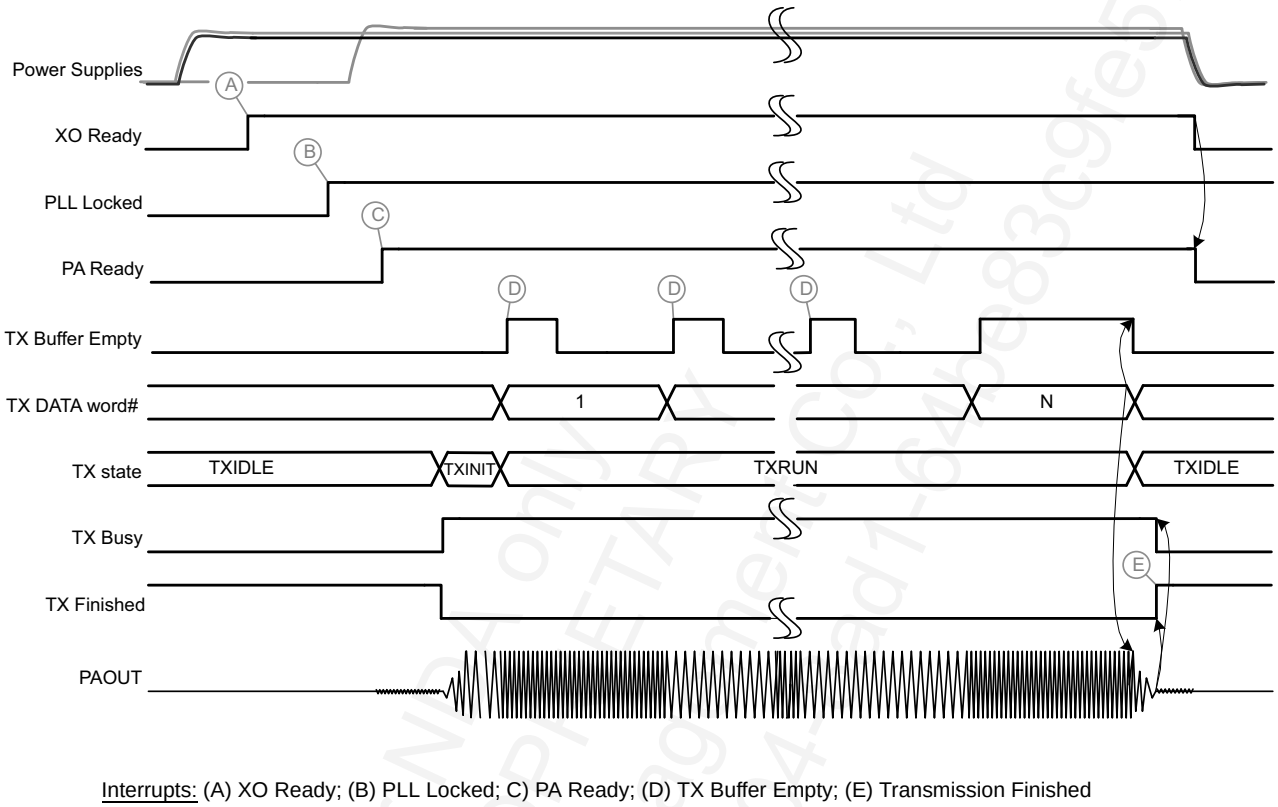
To optimize the RISC software execution time, various control sequences are possible. Every sequence of the user software has to obey the following minimal constraints:

1. Power supply High Performance Regulators from Figure 6, Low Drop-Out voltage regulators (LDOs), have to be enabled and supply voltage properly settled before any of the frequency generating blocks, XO or FracNPLL, can be operated. Detailed timing involved by enabling LDOs is described in Section 2.6.4.
2. The crystal oscillator circuit has to be settled and XO_READY flagged by the hardware before the FracNPLL is enabled. Detailed control sequence to setup XO is described in Section 2.6.5.3.
3. The target RF carrier signal frequency has to be configured before the FracNPLL is enabled. Detailed control sequence to setup the FracNPLL is described in Section 2.6.5.2.
4. The power ramping settings have to be configured before PA is enabled. Detailed control sequence including PA enable is covered in Section 2.6.4
5. Output power, modulation type, modulation parameters, encoder mode and data baud rate have to be configured before transmission is initiated.
   Detailed encoder- and baud rate configuration sequence is described in Section 2.6.6. Modulation setup can be found in Section 2.6.7. Control sequence driving modulation and data transmission is covered in Section 2.6.8.

Figure 31. shows a typical sequence to configure and control the RF-transmission.

Transmitter interrupts can be configured to release the RISC from unnecessary waiting or flag-polling states. If the TX buffer gets empty during transmission, this is indicated to the user software beside a flag (TXBE) also by an interrupt (TXBE). In response new data can be written into TX DATA or transmission is suspended. The application is able to determine end-of-transmission either by configure the number of data bits to be sent or by marking the last data word to be sent. Additionally, transmission can be stopped by software via the TXSTOP bit at the end of the current transmit bit interval. Transmission can be aborted immediately by setting the TXRESET bit. Both

methods can be used to react on a battery brownout depending on the severity. If a brownout threshold below 2.1 V is detected TXSTOP might be set whereas a threshold below 1.8 V should abort the transmission with TXRESET.



Interrupts: (A) XO Ready; (B) PLL Locked; C) PA Ready; (D) TX Buffer Empty; (E) Transmission Finished

Fig 31. Typical timing diagram of setup and operation

2.6.3 Clock and Reset Control

The crystal oscillator clock can be used also without the transmitter, e.g. for absolute time measurements or as ADC clock source. Setting the XODIV2CLKDIS bit in the CLKRSTCON register stops the clock and asserts the reset for the transmitter's clock domain UHFTXCLK. This reduces power consumption because the XODIV2 clock is interrupted to several digital transmitter blocks which are hold in their reset state. The XO divider for the CPU and other peripherals will continue to run regardless of XODIV2CLKDIS.

2.6.3.1 TX Clock and Reset Control Register, CLKRSTCON

The transmitter clock and reset is controlled by the CLKRSTCON register:

Table 59. UHF Tx Clock and Reset Control Register, CLKRSTCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 1	RFU	R/W0	-	Reserved for future use
0	XODIV2CLKDIS	R/W		UHFTX digital XODIV2 clock disable
			0	UHFTX digital XODIV2CLK is automatically enabled if XO is ready
			1	UHFTX digital XODIV2CLK is disabled

XODIV2CLKDIS shall only be configured while the PLL and PA are disabled. XODIV2CLKDIS must be cleared before enabling the PLL.

2.6.4 Transmitter Power On/Off and Output Power Control

The user application software must control the power-up and power-down for the RF blocks XO, PLL and PA. Each block is supplied with a dedicated LDO that must be sequentially enabled or disabled. This means the XO must be enabled before the PLL block, where the PLL must be enabled before the PA block (see also Figure 31). To avoid inrush current effects it is recommended to enable each LDO in three consecutive write access operations where the LDO settling time $t_{TX,LDO}$ has to be considered. Figure 32. describes the necessary software flow to control the different RF blocks of the transmitter from power on to data transmission and back to power down.

Enabling the PA before a valid RF signal is available (before PLL is locked) may lead to RF transmission out of band and may cause excessive current consumption. Furthermore, enabling the PA before stable carrier frequency may lead to a transmissions on wrong frequency channels.

The PA is enabled by PAEN set in the TXPCON register (see Table 60). After the settling time t_{PA_set} the PA_READY flag is set and transmission can be started by writing to the TXDATA register. The time t_{PA_set} comprises the programmable PA setup time t_{PA_STUP} defined by PA_CLK_OFF_TIME[1:0] and a state-machine latency and synchronization time of maximum 5.2 µs.

If configured, the RF output signal amplitude will ramp-up linearly towards the power level defined by the PA_POWER and the RF signal amplitude level settings (see Table 61), initiated by the first TXDAT write access. The amplitude ramping settings are determined by the amplitude setting, AMH and AML and the data rate.

Similarly if configured, the ramp-down of the output signal amplitude will be conducted by hardware after the last bit is sent. Ramp down will take place also after transmission is stopped or interrupted, i.e. TXSTOP or TXRESET bit is set by the user software. The output signal amplitude ramps down linearly towards the minimum ramping power settings (as described in Table 61). Reaching the minimum signal amplitude level defined by the ramping counter triggers the transmission finished interrupt signal (TXFIN) signal. In response to this interrupt, user software may disable the PA. In addition, user software may power down the FracNPLL circuit and the PLL regulators VDDPLL and VDDHS if no further transmission will be conducted. For power saving reasons and if the crystal oscillator is not required the XO circuit and its VDDXO regulator can be disabled.

In case of a power-on reset the PA will power down abruptly causing immediate loss of the RF signal.

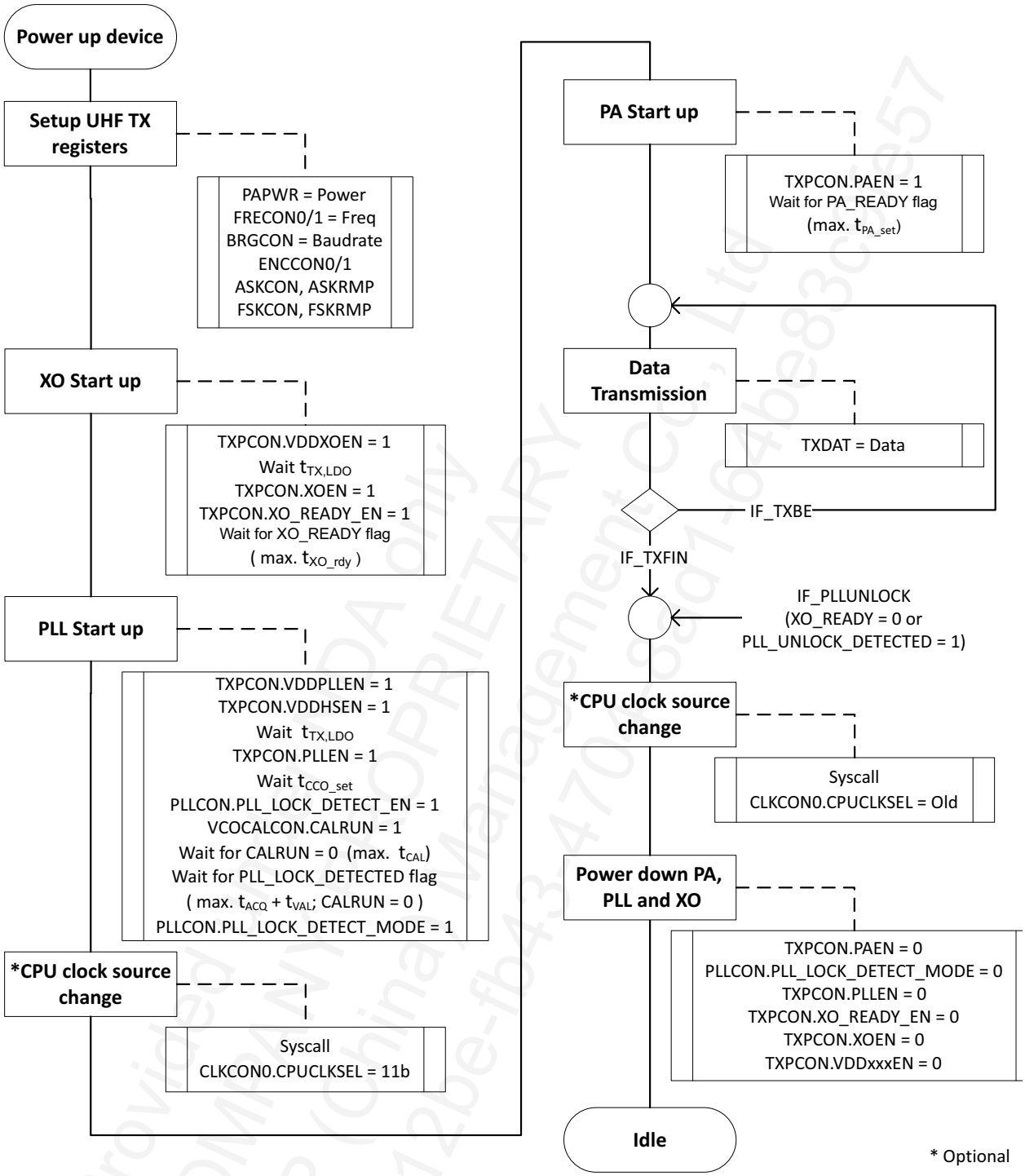


Fig 32. Transmitter Power On/Off and Output Power Control Program flow chart

2.6.4.1 Output Power Calculation

To prevent RF splatter effects at the beginning and at the end of transmission, the transmitter features a step-driven ramping of the output signal power by means of linear voltage amplitude stepping. When enabled, power ramping takes place at the beginning and at the end of data transmission, regardless of the modulation type chosen and according to the settings described in Table 73. In addition if ASK modulation is selected, the linear signal shaping is configured by the same amplitude ramping settings to minimize inter-modulation noise. Maximal ramping level of the signal amplitude is defined by the value of the AMH parameter in the ASKCON register (see Section 2.6.7.5).

If the frequency band, the operating temperature, and the battery voltage supply of the PA are within the specified limits, the following empirical equation is representing the expected output signal power P_{OUT}, related to the RF power settings and the ramping power level. Note that the equation provided in Equation 1 is only valid for a 10 dBm matching circuit. Refer to Ref. 1 for calculating signal power for different matching circuits.

$$P_{OUT}[dBm] = 10 + (-0{,}25) \cdot (\mathrm{PA\_POWER\_MAX} - \mathrm{PA\_POWER}) + 20 \cdot \log\left(\frac{rampinglevel}{31}\right) \quad (1)$$

Equation 1 is valid at 2.1 V < V_{BAT} < 3.6 V, T_{amb} = 25 °C, a frequency channel between 310 and 447MHz, a 10 dBm matching circuit and the maximum amplitude ramping level (AMH = 31 and AML = 0). The multiplying coefficient 0.25 represents the specified power step ($P_{o\ TX\ Step}$). Finally, the *ramping level* is the amplitude level defined by the amplitude-ramping signal shaping and is limited by the AMH and AML settings at the end of each ramping phase.

$$rampinglevel = |AMH - AML|$$

It is strongly recommended not to change the PA_POWER settings during transmission of the data telegram. Output power settings, amplitude ramping settings and signal amplitude settings (ramping limits) may be programmed before PA is enabled, and at latest before transmission is initiated.

2.6.4.2 Maximum Current Calculation

To prevent excessive current drawn from the VPA regulator at shorted antenna pins, in case of a de-tuned antenna or if wrong RF matching components are populated, the device features a programmable PA current limiter. Use of the current limiter is optional. When used, the limited current I_{VPA_lim} must not be set to a value which exceeds the maximum allowed peak current specified by the used battery. I_{VPA_lim} has to be set to a value that allows to reach the targeted output RF power level.

The current limiter can be enabled by setting the system bit PA_ILIM_EN in the PALIMIT register (see Table 62). I_{VPA_lim} can be programmed via PA_IMAX (5 bit) in a wide range with constant steps. The current limiter is enabled per default and the limiting current setting is PA_IMAX = 10. It has to be configured and enabled before starting the transmission. Typically, PA_IMAX values 5 and above allow reaching the nominal output power of Pout = 10dBm.

The status flag PA_ILIM is indicating if the antenna current I_{VPA} exceeds the programmed current limit I_{VPA_lim}. If configured, also an interrupt will be triggered. Continuing with transmission while I_{VPA} is limited will lead to RF-signal clipping effects, spurious signal power increases and accelerates battery discharge.

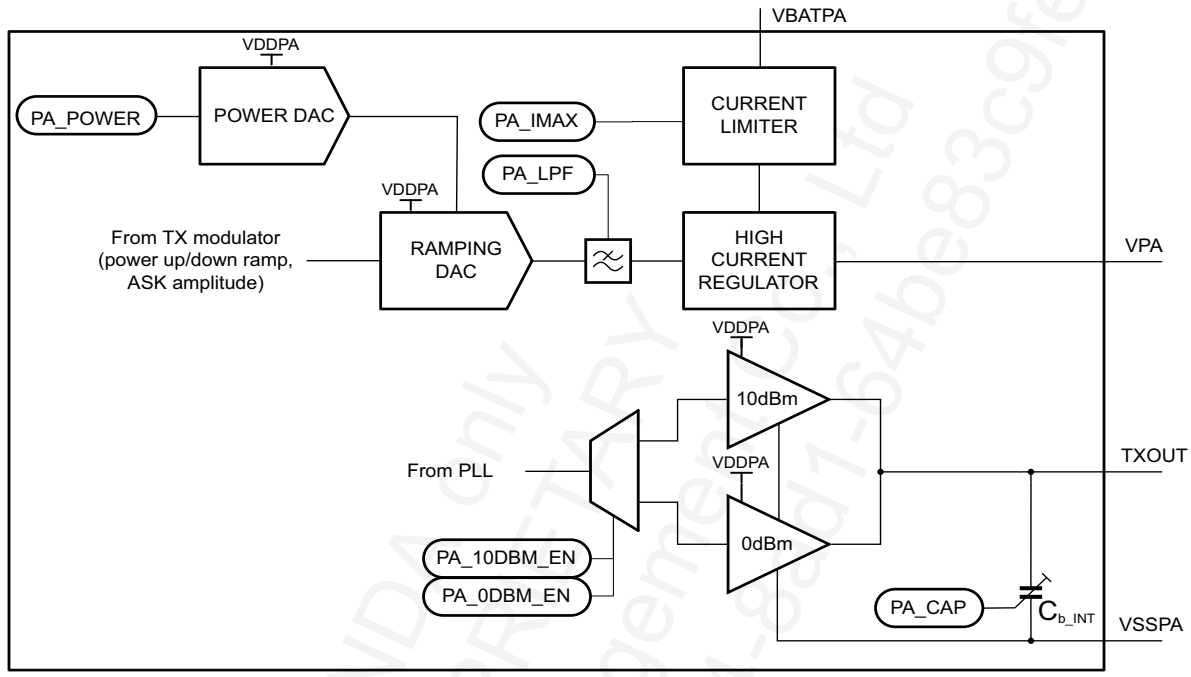


Fig 33. PA block diagram

Note that the current through the pin VBATPA can be calculated as:

$$I_{VBATPA} = I_{VPA} + I_{VDDPA}$$

I_{VDDPA} represents both the PA standby current and the PA driver current.
The PA driver current depends on the RF frequency and selected PA power mode (10dBm_PA or 0dBm_PA).

2.6.4.3 Power ON/OFF Register, TXPCON

The transmitter can be powered-on and powered-off by means of the TXPCON register:

Table 60. Power control settings in TXPCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7	XO_READY_EN	R/W		XO clock ready detector enable bit:
			0	Crystal oscillator clock validation disabled
			1	Crystal oscillator clock validation enabled
6	XO_READY	R		Crystal oscillator status bit:
			0	XO not enabled, or setting up – not ready
			1	XO ready, clock frequency and duty cycle within spec
5	PAEN	R/W		Enable bit for power amplifier operation:
			0	PA disabled
			1	PA enabled
4	PLLEN	R/W		Enable bit for FracNPLL operation:
			0	PLL disabled
			1	PLL enabled
3	XOEN	R/W		Enable bit for crystal oscillator (XTAL) operation:
			0	XO disabled
			1	XO enabled
2	VDDHSEN	R/W		PLL regulator for the high-speed digital part enable:
			0	HS regulator disabled
			1	HS regulator enabled
1	VDDPLLEN	R/W		PLL regulator for the analogue part enable:
			0	0 = PLL regulator disabled
			1	1 = PLL regulator enabled
0	VDDXOEN	R/W		XO regulator enable:
			0	XO regulator disabled
			1	XO regulator enabled

2.6.4.4 Output Power Setting Register, PAPWR

The actual output signal power depends on the application settings in the PAPWR register. The PA_POWER parameter defines maximal output power under typical use-case conditions, as shown in Table 61.

Table 61. Output power settings in PAPWR (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	R/W		Reserved for future use
6 to 0	PA_POWER[6:0]	R/W		Maximal output power settings by application:
			0	POUT =< -14 dBm
			1... PA_POWER_MAX	For output power calculation, refer to Section 2.6.4.1

Note: PA_POWER values must not be set to higher values than PA_POWER_MAX to avoid damage of the IC.

2.6.4.5 Current Limiter Control Register, PALIMIT

Current limiter can be configured by means of PALIMIT register:

Table 62. Current limiter settings register, PALIMIT (reset value 4Ah)

Bit	Symbol	Access	Value	Description
7	PA_ILIM	R[1]		Current limiter status flag
			0	Current limitation not activated, PA operating in the expected matching conditions
			1	Current limitation activated, PA operating in non-optimal matching conditions
6	PA_ILIM_EN	R/W		Current limiter enable control
			0	Current limiter disabled
			1	Current limiter enable
5	RFU	R[1]		Reserved for future use
4 to 0	PA_IMAX[4:0]	R/W		Maximal PA current settings
			0	Reserved for future use
			1 - 31	I_{VPA_lim} = (PA_IMAX -1) * I_{Limit_Step} + I_{Limit_Offset}

[1] Write operation to this bit has no effect

2.6.4.6 PA Setup and Output Mode Register, PACON

Two amplifier output stages for 10 dBm high POUT and 0 dBm for low POUT are provided and can be enabled by the SFR bits PA_10dBM_EN or PA_0DBM_EN. Only one of the control bits must be set. Enabling or disabling both output stages at once will have the same effects: no RF signal PAOUT.

To minimize the spurious signals coupled out through the VPA supply, a low-pass filter can be applied to the amplitude-modulated baseband signal which serves as VPA reference. The PA_LPF settings can be used to select the cut-off frequency of the filter for various output power matching. Recommended value for POUT = 10 dBm is PA_LPF = 01b.

When the power amplifier is enabled with CWC or a modulated RF signal, a time-out interval t_{PA_STUP} - PA setup time is required to avoid one-time transient glitches caused by the internal circuit settling. The PA setup time delay is defined by the PA_CLK_OFF_TIME bits. It is recommended to use the default value of PA_CLK_OFF_TIME = 10b.

Table 63. PA control register, PACON (reset value 29h)

Bit	Symbol	Access	Value	Description
7	PA_READY	R		PA settled and ready
			0	PA not enabled or not settled
			1	PA ready
6	PA_0DBM_EN	R/W		Output power PA enable, 0dBm stage
			0	RF-signal path disabled
			1	RF-signal path enabled

Table 63. PA control register, PACON (reset value 29h)

Bit	Symbol	Access	Value	Description
5 and 4	PA_CLK_OFF_TIME[1:0]	R/W		PA_CLK_OFF_TIME (PA power-up sequencer PA on / RF off time)
			00	t_{PA_STUP} =30 µs
			01	t_{PA_STUP} =50 µs
			10	t_{PA_STUP} =75 µs (default)
			11	t_{PA_STUP} = <1µs (sequencer disabled)
3	PA_10DBM_EN	R/W		Output power PA enable, 10dBm stage
			0	RF-signal path disabled
			1	RF-signal path enabled
2	RFU	R0/W0		Reserved for future use
1 and 0	PA_LPF[1:0]	R/W		PA power ramping DAC output, low-pass filter setting
			00	Reserved for future use
			01	200 kHz (default)
			10	1.2 MHz; recommended setting to be used when POUT matched to 10dBm
			11	700 kHz

2.6.4.7 Output Trimming Register, PATRIM

For the Class E power amplifier matching a configurable shunt capacitance must be applied to the PAOUT output. The device offers two internal capacitor values supporting the impedance matching. The internal switchable capacitor (C_{b_INT}) can be selected via the PA_CAP bit and should be configured dependent on the RF frequency. For frequencies below 500 MHz PA_CAP should be set and for higher frequencies reset.

Table 64. PA trimming register, PATRIM (reset value 2Ch)

Bit	Symbol	Access	Value	Description
7	RFU	R/W[1]		Reserved for future use
6	PA_CAP	R/W		Selection of PA capacitive bank; internal switchable capacitor (C_{b_INT})
			0	400 fF
			1	700 fF
5 to 0	RDT	R/W		Reserved for device test, these bits shall not be changed by the application code as this may influence the transmitter performance.

[1] Write operation to this bit has no effect

2.6.5 Frequency Control

The target frequency settings (RF channel frequency) must be set by the application software before the FracNPLL is enabled for operation. Following sections describe the FracNPLL configuration sequence as XO set-up, VCO calibration and PLL set-up.

2.6.5.1 Target Carrier Frequency Calculation

The carrier frequency is synthesized based on the crystal oscillator frequency and the FracNPLL control word represented by the integer- and the fractional divider parameters FCINT and FCFRAC. The divider parameters are scaled such that the target carrier frequency achieved is meeting the requested channel frequency accuracy and the specified phase-noise level. The carrier frequency f_{TX} is calculated as:

$$f_{TX} = \frac{1}{1 + \text{FIXDIV\_DIV2\_EN}} \cdot \left(FCINT + \frac{FCFRAC}{2^{19}} \right) \cdot f_{XO} \quad (2)$$

where f_{XO} is the crystal frequency, FCINT is the divider's integer part in the range from 21 to 35, and FCFRAC is the dividers fractional part in the range from 0 to 524287. FCINT and FCFRAC are the parameters from the F and FREQCON1 registers shown in Table 65 and Table 66. FIXDIV_DIV2_EN is set to 1 for low ISM bands (f_{TX} < 600 MHz) and set to 0 for high ISM bands.

Applying the inverse function for the desired carrier frequency f_{TX}, the FCINT and FCFRAC parameters can be determined as described in Equation 3 and Equation 4. To avoid wide band spurs, it is recommended to set the fractional PLL multiplication factor to an odd number by setting the lowest bit FCFRAC[0] always to 1.

$$FCINT = \left\lfloor (1 + \text{FIXDIV\_DIV2\_EN}) \cdot \frac{f_{TX}}{f_{XO}} \right\rfloor \quad (3)$$

$$FCFRAC = min\left((2^{19} - 1), \left\lfloor 0.5 + 2^{19} \cdot \left((1 + \text{FIXDIV\_DIV2\_EN}) \cdot \frac{f_{TX}}{f_{XO}} - FCINT \right) \right\rfloor \right) \quad (4)$$

2.6.5.2 Target Frequency Settings Registers, FREQCON0 and FREQCON1

To avoid unwanted PLL Unlocked interrupt flagging the target frequency has to be programmed before FracNPLL is enabled. It is strongly recommended not to change the target frequency settings during transmission of a data telegram.

Table 65. Frequency configuration settings in FREQCON0 (reset value 0f00h)

Bit	Symbol	Access	Value	Description
15 to 7	FCFRAC[8:0]	R/W		Frequency control fractional part low-high bits
6 to 1	RFU	R0/W0	-	Reserved for future use

Table 65. Frequency configuration settings in FREQCON0 (reset value 0f00h)

Bit	Symbol	Access	Value	Description
0	FCDISFRAC	R/W		Frequency control disable fractional
			0	Fractional part enabled
			1	Fractional part disabled, test mode only

Table 66. Target frequency settings in FREQCON1 (reset value 7dcch)

Bit	Symbol	Access	Value	Description
15 to 10	FCINT[5:0]	R/W		Integer part frequency control word
9 and 8	FCFRAC[18:17]	R/W		Frequency control fractional part high-high bits
7 to 0	FCFRAC[16:9]	R/W		Frequency control fractional part high-low bits

The above specified default settings result in a notional carrier (channel) frequency of f_{TX} = 434.000008 MHz, for f_{XO} = 27.6 MHz.

Setting FCDISFRAC = 1 enforces an integer-divided PLL operation that yields into lower current consumption of the PLL on the cost of lower carrier frequency accuracy and higher phase noise figures. In this configuration neither channel accuracy nor phase noise figures can be guaranteed to be within the specification limits. This mode should be used only for test purpose.

2.6.5.3 Crystal Oscillator Set-up

As first step the XO supply regulator (VDDXO) must be enabled. Once the settling time $t_{TX,LDO}$ is passed it can be continued to enable the XO and the XO Ready validation circuit. Latter will indicate with the XO Ready signal (step (A) Figure 31) when the oscillator has reached a valid frequency and duty cycle to start the PLL. The XO Ready will occur within the specified t_{XO_rdy} time, counted from the XO EN and XO READY EN set to 1. It is required to maintain the XO Ready validation circuit enabled (XO_READY_EN = 1) while UHF operation is ongoing. The UHFTXCLK clock is available only after XO_READY has changed to 1.

2.6.5.4 Phase Locked Loop Set-up and VCO Calibration

In response to the XO Ready interrupt, the user software can enable the FracNPLL and initiate VCO calibration. The FracNPLL is based on a current controlled ring-oscillator circuit (CCO). With the PLLEN bit set, the CCO settles after t_{CCO_set}. In this state the VCO calibration can be conducted depending on the target frequency set and previous transmission configurations. PLL lock detection has to be disabled while VCO calibration is running.

VCO calibration is intended to assure the CCO is biased such to retain the PLL in the regulating frequency range where PLL lock can be achieved and maintained during transmission. VCO calibration needs to be run during the PLL start-up sequence each time after a device is woken up from POWER OFF device power state. A new VCO calibration is recommended also when the target frequency (the transmission RF channel) is changed by more than 2 MHz between two transmission data frames. During VCO calibration user software must ensure that the PA is inactive by setting the power ramping value to zero or disable the PA to avoid out-of-band transmissions.

A calibration is triggered by setting CALRUN to 1 with both CALRESET and CAL_IDAC_FILT_EN set to 0. The automatic VCO calibration suspends the normal PLL operation and tunes the PLL oscillator biasing to achieve the programmed target frequency. If the target frequency is within the specified tolerance limits the VCO calibration finishes by resuming normal PLL operation and the CALRUN flag is reset to indicate the calibration status finished. If CALRUN = 0 is detected, the user software can enable the lock detector circuit for a valid PLL locked (PLLLOCK) interrupt generation (step (B) Figure 31).

To speed up the PLL start-up procedure, VCO calibration can be omitted and a known calibration value can be used. In case of repetitive transmissions and continuously powered on transmitter circuit or in case of a near-by transmission channel to be programmed, the user software can store the last obtained calibration value and set it back into the VCOCALCON register before initiating the next transmission.

For correct skipping the VCO calibration, the user software has to access VCOCALCON twice:
1) To enable the weighted current source IDAC biasing the CCO, the calibration value CAL_IDAC_CTRL has to be written with internal filter circuit and automatic calibration disabled (CAL_IDAC_FILT_EN = 0; CALRUN = 0).
2) The same calibration value CAL_IDAC_CTRL needs to be written again with internal filter circuit enabled (CAL_IDAC_FILT_EN = 1) and automatic calibration disabled (CALRUN = 0).

Between the two steps of controlling the current-DAC (IDAC), and enabling its output filter the t_{IDAC_set} needs to be considered. After the IDAC is settled, the IDAC output filter shall be enabled. It takes t_{FILT_set} before the PLL lock can be expected. Note that this time sequence is automated when VCO calibration is used.

2.6.5.5 VCO Calibration Control Register, VCOCALCON

VCO Calibration is controlled by the VCOCALCON register:

Table 67. VCO calibration control in VCOCALCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 3	CAL_IDAC_CTRL[4:0]	R/W		CCO offset current trimming:
			0	lowest trim / lowest frequency sub band
			31	highest trim / highest frequency sub band
2	CAL_IDAC_FILT_EN	R/W		Noise filter control in the calibration circuit, automatically cleared when TXPCON.PLLEN is set to 0
			0	filter disabled
			1	filter enabled
1	CALRESET	R0/W		VCO calibration engine reset control:
			0	no effects (also, the value returned at reading)
			1	A running calibration is aborted.
0	CALRUN	R/W		VCO calibration engine run control/status:
			0	status calibration idle/finished
			1	trigger calibration/status calibration running

2.6.5.6 PLL Lock and Unlock Control

With completed VCO calibration the user software can configure and enable the PLL Lock detecting circuit. Lock-detection should be activated to avoid false PLL unlock interrupts and to optimize the current consumption. The transmitter features lock and unlock detection mode (PLL_LOCK_DETECT_MODE). Two PLL Lock detection types can be selected covering different frequency accuracy (PLL_LOCK_DETECT_BLOCK). Once coarse or fine detector is selected, lock detection is enabled by the PLL_LOCK_DETECT_EN bit set.

The PLL_LOCK_DETECTED flag can be expected after t_{ACQ} plus t_{VAL} and can be captured also by interrupt (PLLLOCK). The user software should react by swapping to unlock detection mode while keeping the coarse or fine detector type with a single write access to the PLLCON register. This supports also a safe automated PA shut down in case of PLL Unlock.

If PLL Unlock is detected and the related interrupt PLLUNLOCK is generated, the lock/unlock detectors themselves will not be powered-down automatically nor the detector mode configuration bit will be set back to lock detection. Therefore a complete power-down sequence of the transmitter has to be executed. The user software has to disable the lock/unlock detection first, followed by the PLL and the XO function including VDDXO.

2.6.5.7 FracNPLL Control Register, PLLCON

The PLL control settings are described in Table 68.

Table 68. PLL control in PLLCON (reset value 11h)

Bit	Symbol	Access	Value	Description
7	PLL_LOCK_DETECTED	R		PLL lock detector status
			0	No lock – PLL unlocked, or circuit disabled
			1	PLL Locked
6	PLL_UNLOCK_DETECTED	R		PLL lock detector status
			0	No unlock - PLL locked, or the circuit disabled
			1	PLL lock lost
5 and 4	PLL_LOCK_DETECT_TIME[1:0]	R/W		Validation time tVAL or frequency offset selection:
			00	16 µs – in case of phase-lock detector 175 µs – in case of frequency offset detector, with 100 kHz as target offset (@ fVCO = 970MHz)
			01	32 µs - in case of phase-lock detector 108 µs - in case of frequency offset detector, with 162 kHz as target offset (@ fVCO = 970MHz)
			10	48 µs - in case of phase-lock detector 88 µs - in case of frequency offset detector, with 200 kHz as target offset (@ fVCO = 970MHz)
			11	64 µs - in case of phase-lock detector 63 µs - in case of frequency offset detector, with 275 kHz as target offset (@ fVCO = 970MHz)

Table 68. PLL control in PLLCON (reset value 11h)

Bit	Symbol	Access	Value	Description
3	PLL_LOCK_DETECT_BLOCK	R/W		Selects coarse or fine detector:
			0	Lock mode: Phase lock detector - coarse Unlock mode: PLL tuning voltage out of range based detector - coarse
			1	Frequency offset based detector - fine
2	PLL_LOCK_DETECT_MODE	R/W		Selects lock or unlock mode:
			0	Lock detection mode
			1	Unlock detection mode
1	PLL_LOCK_DETECT_EN	R/W		Enables the selected PLL lock/unlock detector automatically cleared when TXPCON.PLLEN is set to 0
			0	Lock/unlock disabled
			1	Lock/unlock enabled
0	FIXDIV_DIV2_EN	R/W		VCO clock indication for PA[1]
			0	divided by 1 clock to PA – for the bands 868 MHz and 915 MHz[2]
			1	divided by 2 clock to PA – for the bands between 310 MHz and 447 MHz

[1] For low-band locked devices, the effective value of FIXDIV_DIV2_EN is 1 regardless of the value in the PLLCON register.

[2] The frequency bands 868 MHz and 915 MHz can be supported on request.

2.6.6 Encoding Control

The transmitter can be configured for a deterministic transmission with configurable data length, ranging from 1 to 16 bits. It is also possible to transmit the data repetitively a multiple number of times or continuously. The initial transmitter configuration (see Figure 31) needs to define also the encoding mode before transmission.

A deterministic transmission can be configured with a predefined number of TXDAT bits to be sent (BTCNT) and optionally repeated (RPTFE, RPTCNT). In addition the encoding mode NRZ or Manchester (DATENC) and the desired bit order MSB-first or LSB-first (DATLSBF) can be selected. The transmission baud rate must be configured according Section 2.6.6.3.

If Manchester encoding is selected, a data bit value '0' is encoded as a pair of half-bits '01', and the value '1' is encoded as '10'. With NRZ encoding, the encoder output value is identical to the data bit value. Setting DATINV = 1 inverts the encoder output.

The TX input signal can be selected via DATSRC between direct TXDAT data buffer output or the data buffer output XORed with a pseudo-random binary sequence (TXPRBSPOLY). For test purposes also two additional data sources from device pin P14 and related encoder modes are provided. See Section 2.6.7 “Modulation Control”, for details of application of encoder levels to PA output.

The DATLAST indicator has to be set for the last data word written into the TXDAT register. DATLAST and RPTCNT/BITCNT respectively indicate the hardware state machine when to stop requesting and stop sending data. Transmission can be stopped

part way through a requested data sequence by using the TXSTOP or TXRESET control bits. If TXSTOP is set the transmission stops after the current bit has been sent. Setting TXRESET stops the transmission immediately. In both cases, power ramping will behave according to the programmed settings covered in Table 73.

2.6.6.1 Encoder Configuration Registers, ENCCON0 and ENCCON1

Data transmission has to be configured in the ENCCON0 and ENCCON1 registers before transmission is started. The configuration from ENCCON0, ENCCON1, ASKCON.ASK bit (Table 72) and TXSPC (Table 77) take effect at next time TXDAT is written.

Table 69. Encoder control in ENCCON0 (reset value 0000h)

Bit	Symbol	Access	Value	Description
15	DATLAST	R/W		Last data word indicator:
			0	More words to come
			1	Last data word written. Suppresses the assertion of the TXBE interrupt, TXBE status bit and TXBU status bit.
14 to 12	DATENC[2:0]	R/W		Encoder mode selection:
			000	NRZ encoding with *bit rate* = f_{BRG}.
			001	Manchester encoding with bit rate = f_{BRG} / 2.
			010	NRZ encoding with *bit rate* = 2× f_{BRG}
			011	Manchester encoding with *bit rate* = f_{BRG}.
			100	Test only: RAW mode - data is synchronized with UHFTXCLK; data source determines the baud rate
			101 - 111	reserved
11	DATINV	R/W		Data inversion control:
			0	No inversion
			1	Data inverted
10	DATLSBF	R/W		Data bit-order for sending:
			0	MSB first; transmission started/updated when TXDAT[15:8] is written.
			1	LSB first; transmission started/updated when TXDAT[7:0] is written.
9 and 8	DATSRC[1:0]	R/W		Data source selection:
			00	TX data buffer, i.e. shift register output
			01	Test mode only: TXDAT pin, P14, input synchronized to UHFTXCLK
			10	TX data buffer XORed with pseudo-random binary sequence (PRBS).
			11	Test mode only: TXDATA pin, P14 [1], input synchronized to UHFTXCLK and XORed with the PRBS output
7	TXBU	R&C		Transmission buffer underflow flag: bit is cleared when read.
			0	Not initialized transmission, or, transmission ongoing and no buffer underflow
			1	TXDAT data buffer underflow: TXDAT was not written on time and the transmission will be stopped.
6	TXBE	R		Transmission buffer empty flag:
			0	Not initialized transmission, or, transmission ongoing and buffer not empty
			1	Transmission ongoing and TXDAT data buffer empty

Table 69. Encoder control in ENCCON0 (reset value 0000h)

Bit	Symbol	Access	Value	Description
5	TXBUSY	R		Transmission busy flag:
			0	Idle transmission - not initialized, or finished
			1	Transmission ongoing
4	TXPRBSINIT	R/W		Pseudo Random Binary Sequence initiation:
			0	no effects
			1	Reinitializes the PRBS the next time TXDAT is written; Can be used to reinitialize the PRBS after a transmission space for example.
3 and 2	TXPRBSPOLY [1:0]	R/W		Polynomials selection for the pseudo random bit sequence, according to ITU / CCITT ITU-T recommendations [2]:
			00	511 bit pseudo-random test sequence; non-inverted signal.
			01	2047 bit pseudo-random test sequence; non-inverted signal.
			10	1 048 575 bit pseudo-random test sequences; non-inverted signal.
			11	8 388 607 bit pseudo-random test sequences; inverted signal.
1	TXRESET	R0/W		Request to immediately stop transmission:
			0	0 = No effects, also, value at read
			1	Causes immediate state change to TXIDLE; The output begins ramping down following the ramping settings; PA is not disabled.
0	TXSTOP	R0/W		Transmission stop by the end of current bit:
			0	0 = No effects, also, value at read
			1	Causes state change to TXIDLE after current bit is sent. The output begins ramping down according the ramping settings; PA is not disabled.

[1] For the pin configuration, see Section 2.14.2.6

[2] ITU / CCITT ITU-T Recommendation O.150, and ITU-T Recommendation O.153

Table 70. Encoder control in ENCCON1 (reset value 0000h)

Bit	Symbol	Access	Value	Description
15	RPTFE	R/W		Repeat forever enable:
			0	No effect
			1	Transmit data - repeat forever; Continues until TXSTOP request or TXRESET request or TXDAT update
14 to 8	RPTCNT[6:0]	R/W		TX data repeat count; Content is ignored when DATENC mode “RAW” is selected:
			0	No repetition; data is sent one time.
			1-127	Repetition requested; data is sent RPTCNT + 1 times.
7 to 4	RFU	R[1]		Reserved for future use
3 to 0	BITCNT[3:0]	R/W		Bit count, number of bits to send in each iteration.
			0	16 bits data word to be transmitted
			1-15	the number of bits to be transmitted from the TXDAT register

[1] Write operation to this bit has no effect

2.6.6.2 Signal Baud Rate Calculation

The baud rate is generated based on the crystal oscillator clock frequency:

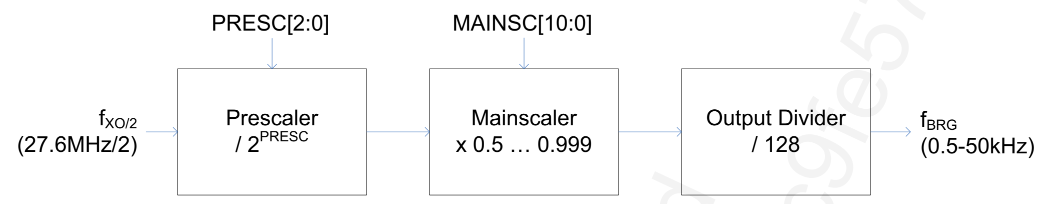


Fig 34. Baud rate generator

The chip-rate can be either equal or twice the baud rate as defined by the DATENC setting (NRZ or Manchester; Table 69). The coefficient representing the ratio between the baud rate and chip rate is designated as ENC FACT. The value is assigned as ENC FACT = 2 for DATENC = 2 or 3, and ENC FACT = 1 for all other modes.

$$baud\ rate = f_{BRG} = \frac{f_{REF}}{2^{PRESC}} \cdot \frac{2^{11} + MAINSC}{2^{12}} \cdot \frac{1}{128} \quad (5)$$

$$chip\ rate = f_{CHIP} = ENC\ FACT \cdot f_{BRG} \quad (6)$$

$$bit\ rate_{NRZ} = f_{CHIP};\ bit\ rate_{MAN} = f_{CHIP}/2 \quad (7)$$

$f_{REF} = f_{XO} / 2$ corresponds to 27.6 MHz / 2 = 13.8 MHz, the PRESC is an exponent in the range from 0 to 7, and 2^{11} + MAINSC is the mantissa in the range 2048 through 4095. PRESC and MAINSC are the parameters set in the BRGCON register in Table 71.

Applying the inverse function for the desired baud rate,
PRESC and MAINSC parameters can be determined as:

$$PRESC = \left\lfloor \mathbf{log}_2\left(\frac{107786.1786}{max(421.15, min(baud\ rate, 107786.17))}\right) \right\rfloor \quad (8)$$

$$MAINSC = max\left(0, min\left(2047, \left\lfloor \frac{baud\ rate}{26.3214} \cdot 2^{PRESC} - 2047.5 \right\rfloor\right)\right) \quad (9)$$

2.6.6.3 Baud Rate Register, BRGCON

Baud rate settings can be configured by the parameters in the BRGCON register:

Table 71. Baud rate settings in BRGCON (reset value 317fh)

Bit	Symbol	Access	Value	Description
15 and 14	RFU	R[1]		Reserved for future use
13 to 11	PRESC [2:0]	R/W		Baud rate generator prescaler
10 to 0	MAINSC [10:0]	R/W		Baud rate generator main scaler

[1] Write operation to this bit has no effect

The default / reset settings result in a notional baud rate of f_{BRG} = 1 kHz.

2.6.7 Modulation Control

Modulation has to be configured before transmission is initiated. It is recommended to conduct configuration before the PA is activated (see Figure 31) to avoid noticeable effects on the device transmitter pins. The user software can chose between ASK and FSK modulation type (ASKCON.ASK bit) and can select the amplitude level of the modulated signal (AMH) in a single write access to the ASKCON register (see Section 2.6.7.5). The transmitter selects *Deep* ASK modulation when the RF_MUTE_EN bit is set to further extend the dynamic range of ASK beyond the amplitude ramping settings.

Modulation is initiated by a write to the TXDAT register. Shaping of ASK and FSK modulation is done by a linear ramping amplitude or frequency with a programmable step period to achieve the desired slew rate. Selection of parameters to achieve the desired slew-rate is described in Section 2.6.7.2.

In parallel to the internal data transfer from TXDAT into the TX buffer, the selected signal shaping gets initiated with the new modulation settings. Each chip-interval later, the selected counter gets synchronized to the baud-rate clock and is counting back or maintaining the value, based on the baseband signal from the encoder. The counters run on UHFTXCLK for ASK and on the divided CCO frequency close to f_{XO} for FSK when the PLL is locked.

In case of ASK, the RF-signal amplitude is ramped between two levels defined by AMH and AML. In case of FSK the signal frequency ramps between $f_{TX} \pm f_{DEV}$. A binary '0' from the encoder translates to the ASK amplitude AMH level and a '1' to the AML level. For FSK a binary '0' is represented by the positive frequency deviation. Modulation is ongoing for the time data bits are being sent from the TX buffer. If no new data is written into TXDAT and the last bit from the TX buffer is sent, the modulation stops. Modulation can be interrupted using the encoder control bits TXSTOP or TXRESET (see Table 69).

If the modulation configuration is changed while transmission is running the new settings will apply to the first bit sent from the new written TXDAT word. However, to support the synchronization procedure between the transmitter and the receiver consistently, it is recommended to maintain the modulation settings during transmission of the whole data telegram. Signal amplitude or frequency deviation, configured before the PA was enabled, should preferably stay unchanged along the telegram transmission.

When required by protocol, a modulation type and/or encoding mode change has to be programmed between two transmit data words. To achieve that, it will be necessary to program the frame length and swap modulation or encoder type before new data is written into TXDAT. The new configuration settings will be applied when the written TXDAT data word bits are sent.

2.6.7.1 Continuous Wave Carrier (CWC)

With amplitude ramping configured (ARMPMANT > 0) and enabled PA the minimal-power CWC RF-signal will drive the antenna circuit. It is defined by the minimal amplitude ramping counter value that is overruling the power and amplitude configuration settings.

A CWC transmission can be established with fully configurable power settings by setting NRZ-encoder mode (DATENC), ASK modulation (ASK), continuous transmission (RPTFE) set, TXDAT selected as data source (DATSRC), and the amplitude settings as desired (AMH > 0). CWC transmission is initiated by writing 0000h into TXDAT.

2.6.7.2 Signal Shaping

The transmitter features soft-ASK and soft-FSK modulation selected by the ASK bit and the ASKRMP and FSKRMP register settings.

Soft-ASK employs linear amplitude ramping between two amplitude settings AML and AMH assigned to the binary modulating data values. The difference between the two signal amplitudes represents the ASK modulation index (ASK modulation depth). The ramping time between the amplitude values is defined by ARMPEXP and ARMPMANT in the AKSRMP register (see Table 73).

Soft-FSK is based on linear frequency ramping between two equidistant signal frequency values around the RF carrier. The positive and negative offset from the carrier frequency representing the binary modulation is defined as frequency deviation f_{DEV}. The soft-FSK ramping time should be configured for lowest spectral noise in the received baseband.

For both soft modulation types the ratio between the ramping time of the linearly shaped signal T_{RAMP} and the transmitted symbol time T_{CHIP} is defined as signal slope:

$$Slope = \frac{T_{RAMP}}{T_{CHIP}} \tag{10}$$

Figure 35 shows the timing parameters defining the *Slope*.

The slope can be varied between 0 and 100%. Hard modulation equates to *Slope* = 0% where amplitude or the frequency ramping configuration has to be set to 0. A triangular convolution appears when *Slope* is set to 100%. Spectral purity of modulation base band signal rises with linear curve slope value. In order to avoid sensitivity reduction at the receiver, the linear curve slope should not be higher than a sinusoidal slope at zero-crossing point, equal to *Slope* = $2/\pi$ = 63.7%.

For the optimal slope, an optimal signal ramping time expressed in number of reference clock periods can be programmed. Section 2.6.7.3 and Section 2.6.7.4 provide expressions to determine the optimal ramping settings for a given baud rate and programmed modulation parameters (amplitude levels or frequency deviation).

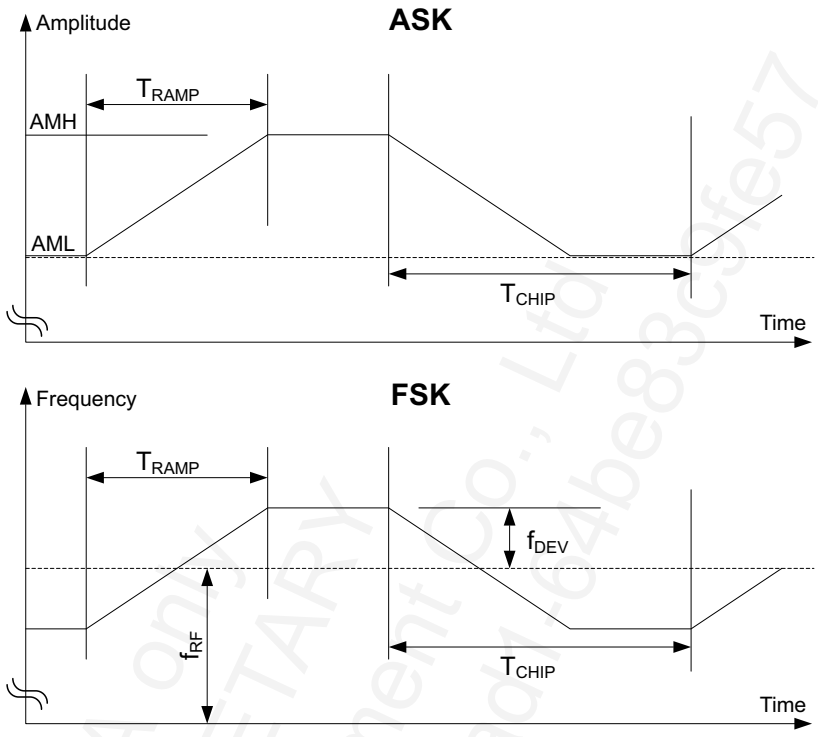


Fig 35. Timing parameters for RF-transmission slope

2.6.7.3 Soft-ASK

The choice between the hard modulation ASK and linearly shaped soft-ASK can be made via the ASKRMP register. The two parameters *ARMPMANT* and *ARMPEXP* define the number of f_{REF} clock cycles to ramp the ASK amplitude during one amplitude step.

$$N_{STEP} = ARMPMANT \cdot 2^{ARMPEXP} \tag{11}$$

In case of normal modulation the number of amplitude steps is equal to:

$$N = |AMH - AML| - 1 \tag{12}$$

With deep modulation when RF_MUTE_EN is set and AML is cleared (AML = 0) the number of amplitude steps is equal to:

$$N = AMH \tag{13}$$

The total ramp time for the Soft-ASK can be obtained from Equation 11 and Equation 12. and gives for normal modulation:

$$T_{RAMP} = N \cdot N_{STEP} \cdot T_{REF} = \frac{|AMH - AML| - 1}{f_{ref}} \cdot ARMPMANT \cdot 2^{ARMPEXP} \quad (14)$$

In case of deep modulation when the total ramp time is given with:

$$T_{RAMP} = N \cdot N_{STEP} \cdot T_{REF} = \frac{AMH}{f_{ref}} \cdot ARMPMANT \cdot 2^{ARMPEXP} \quad (15)$$

T_{REF} represents the period of the reference clock signal $f_{REF} = f_{XO/2}$.

The definition for the *ENC FACT* factor applies to Soft-ASK as well as to Soft-FSK (see Section 2.6.6.2). This results with a optimal slope with $T_{BRG} = 1 / baud\ rate$ into:

$$Slope = ENC\ FACT \cdot \frac{T_{RAMP}}{T_{BRC}} = \frac{2}{\pi} \quad (16)$$

The optimal signal slope is depending on the encoding type, the signal ramping time, and the baud rate. From Equation 14 and Equation 5, Equation 6, and Equation 7, the amplitude ramping parameters *ARMPEXP* and *ARMPMANT* for an optimal slope can be shown as function of baud rate and amplitude level. For normal modulation Equation 17 applies:

$$ARMPMANT \cdot 2^{ARMPEXP} = \frac{1}{|AMH - AML| - 1} \cdot \frac{2}{\pi} \cdot \frac{128 \cdot 2^{12} \cdot 2^{PRESC}}{(2^{11} + MAINSC)} \cdot \frac{1}{ENC\ FACT} \quad (17)$$

In case of deep modulation Equation 18 is valid:

$$ARMPMANT \cdot 2^{ARMPEXP} = \frac{1}{AMH} \cdot \frac{2}{\pi} \cdot \frac{128 \cdot 2^{12} \cdot 2^{PRESC}}{(2^{11} + MAINSC)} \cdot \frac{1}{ENC\ FACT} \quad (18)$$

Several combinations of mantissa and exponent are possible to achieve the same ramp. Choosing a smaller value of *ARMPEXP* can increase the accuracy of the slope rate. Note that it is not possible to select ramp settings that results to a 63.7% slope at baud rates less than 600 Hz. For such baud rate values the application may chose smaller modulation depth to meet the optimal slope value.

2.6.7.4 Soft-FSK

The difference between minimal and maximal modulation frequency is equal to twice the frequency deviation f_{DEV}. Frequency deviation is derived from the FDEVMANT and FDEVEXP settings:

$$f_{DEV} = \frac{FDEVMANT \cdot 2^{FDEVEXP}}{2^{16}} \cdot \frac{f_{REF}}{(1 + \mathrm{FIXDIV\_DIV2\_EN})} \quad (19)$$

f_{REF} can be assumed to be equal to the crystal oscillator frequency when PLL lock is valid, $f_{REF} = f_{XO}$ = 27.6 MHz. With FIXDIV_DIV2_EN defining the CCO frequency setting (Table 68) and applying the inverse function, following equations can be derived:

$$FDEVEXP = min\left(7, max\left(0, \left\lfloor \log_2 \frac{f_{DEV} \cdot (1 + \text{FIXDIV\_DIV2\_EN}) \cdot 2^{16}}{f_{REF} \cdot 15{,}75} \right\rfloor\right)\right) \quad (20)$$

$$FDEVMANT = min\left(31, \left\lfloor \frac{f_{DEV} \cdot (1 + \text{FIXDIV\_DIV2\_EN}) \cdot 2^{16}}{f_{REF} \cdot 2^{FDEVEXP}} \right\rfloor\right) \quad (21)$$

Note that the values should be rounded down to the nearest integer.
For soft-FSK the ramp frequency step is derived from the reference clock:

$$f_{STEP} = \frac{1}{2^{16}} \cdot \frac{f_{REF}}{(1 + \text{FIXDIV\_DIV2\_EN})} \quad (22)$$

Out of Equation 19 and Equation 22, the number of frequency steps over the whole ramp frequency range can be calculated as:

$$N = 2 \cdot \frac{f_{DEV}}{f_{STEP}} = 2 \cdot FDEVMANT \cdot 2^{FDEVEXP} \quad (23)$$

The programmed frequency ramp settings, FRMPMANT and FRMPEXP define together with the reference frequency the frequency step duration:

$$T_{STEP} = \frac{FRMPMANT \cdot 2^{FRMPEXP - 4}}{f_{REF}} \quad (24)$$

From the number of frequency steps N in Equation 23 and the single frequency step duration in Equation 24, the overall time for the frequency ramp is given as:

$$T_{RAMP} = N \cdot T_{STEP} = 2 \cdot \frac{FRMPMANT \cdot 2^{FRMPEXP - 4}}{f_{REF}} \cdot FDEVMANT \cdot 2^{FDEVEXP} \quad (25)$$

This equation applied to the optimal slope according Equation 16 and with the T_{BRG} taken from Equation 5, Equation 6, and Equation 7 yields to the frequency ramping settings:

$$FRMPMANT \cdot 2^{FRMPEXP - 4} = \frac{1}{FDEVMANT \cdot 2^{FDEVEXP}} \cdot \frac{2}{\pi} \cdot \frac{128 \cdot 2^{12} \cdot 2^{PRESC}}{(2^{11} + MAINSC)} \cdot \frac{1}{ENC\ FACT} \quad (26)$$

where the *ENC FACT* is defined in Section 2.6.6.2.
Several combinations of mantissa and exponent are possible to achieve the same ramp.

2.6.7.5 Modulation Amplitude Register, ASKCON

Signal amplitude as signal-high and signal-low level need to be defined by AMH and AML settings in the ASKCON register:

Table 72. ASK Modulation Magnitude in ASKCON (reset value 009Fh)

Bit	Symbol	Access	Value	Description
15 to 13	RFU	R[1]		Reserved for future use
12 to 8	AML[4:0]	R/W		Low amplitude level in case of ASK
			0-31	
7	ASK	R/W		Modulation mode selection:
			0	FSK Modulator
			1	ASK Modulator
6	RF_MUTE_EN	R/W		Switch on/off RF-carrier signal during Off-data-keying
			0	Low level PA output will remain at AML. (Shallow low)
			1	PA output will be turned hard off when outputting low. (Deep low)
5	RFU	R[1]		Reserved for future use
4 to 0	AMH[4:0]	R/W		High amplitude level in case of ASK (ASK = 1) Signal amplitude in case of FSK (ASK=0)
			0-31	

[1] Write operation to this bit has no effect

It is strongly recommended to maintain the AMH and AML settings unchanged during transmission of a data telegram. In case a different modulation scheme is required for a telegram, it is allowed to change configuration before new data is written into TXDAT.

RF_MUTE_EN, switch on/off RF-carrier signal during Off-data-keying

When RF_MUTE_EN is set the RF-carrier signal will be switched off during off-data-keying. If ASK signal shaping is configured, the RF carrier will be muted at the lowest ramping step when AML is cleared (AML = 0).

2.6.7.6 Modulation Ramp Register, ASKRMP

The amplitude ramping can be configured by the parameters provided in Table 73. These settings have to be configured before PA is enabled.

Table 73. ASK amplitude ramping settings in ASKRMP (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	ARMPEXP[1:0]	R/W		Amplitude ramping, exponent parameter
5 to 0	ARMPMANT [5:0]	R/W		Amplitude ramping, mantissa parameter
			0	No amplitude ramping – Hard-ASK
			1-63	Linear amplitude ramp

The default value after reset selects Hard ASK - no linear ramping.
The amplitude ramping parameters can be calculated by applying Equation 17.

2.6.7.7 Frequency Deviation Register, FSKCON

Frequency deviation parameters calculated from Equation 22 have to be programmed to the FSKCON register. The settings have to be configured before transmission is initiated.

Table 74. FSK frequency deviation in FSKCON (reset value 0ah)

Bit	Symbol	Access	Value	Description
7 to 5	FDEVEXP[2:0]	R/W		Frequency deviation, exponent parameter
4 to 0	FDEVMANT [4:0]	R/W		Frequency deviation, mantissa parameter

The default value after reset sets f_{DEV} = 2073 Hz. This is the closest setting to 2 kHz for FCDISFRAC = 0 and FIXDIV_DIV2_EN = 1. Typically a receiver must stay tuned to a certain sensitivity level obtained during transmission of the synchronization frame. Therefore, it is strongly recommended to maintain the *FDEVMANT* and *FDEVEXP* settings unchanged during transmission of the whole data telegram.

2.6.7.8 Frequency Ramping Register, FSKRMP

The timing of each frequency step duration is defined by the frequency ramping settings FRMPMANT and FRMPEXP. This settings have to be configured before transmission is initiated. Frequency ramping can be configured by the settings provided in Equation 26.

Table 75. FSK frequency ramping settings in FSKRMP (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 5	FRMPEXP[2:0]	R/W		Frequency ramping, the exponent part
4 to 0	FRMPMANT [4:0]	R/W		Frequency ramping, the mantissa part
			0	No frequency ramping – Hard-FSK
			1-31	Linear frequency ramp

The default value after reset released selects Hard-FSK modulation - no linear frequency ramping. It is recommended to maintain the FRMPMANT and FRMPEXP settings unchanged during transmission of the whole data telegram.

2.6.8 Data Transfer Control

Transmission is initiated when the user software places transmit-data into the transmission buffer via TXDAT. A transmission should not be attempted before the PLL has been locked and PA has been enabled. Following the TXDAT write the transmitter hardware automatically loads the new TXDAT value into an internal shift-register. Consequently, the encoded data will be passed serially to the modulation block with the configured baud rate. The modulator transfers the encoded serial data into an RF-signal and passes it to the PA.

At each succeeding TXDAT write access the entire data transmission configuration (ENCCON0, ENCCON1, TXSPC and ASKCON.ASK registers) will be reloaded. New configurations will take effect with the first bit sent from the newly written TXDAT word.

2.6.8.1 Transmission State Diagram

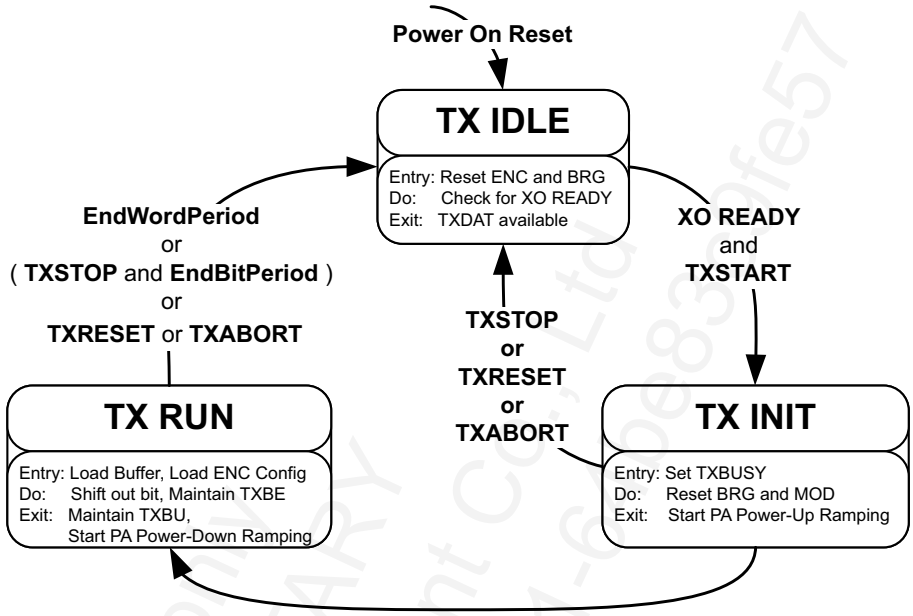


Fig 36. Transmission State Diagram

The transmission state machine starts in TXIDLE. This state is entered after switching-on the RF-transmitter before any data is written into the TXDAT register. In TXIDLE the RF-output signal is defined by the minimal ramping level and the PA_POWER settings.

The state machine transits into the TXINIT state when data is written to TXDAT (TXSTART request in Figure 36.). With this step the status bit TXBUSY is set. In TXINIT the baud rate generator is reset to ensure the correct timing with the first data bit. The linear shaping filters and the related ramping counter generators will be also reset to ensure the expected slope and bit-period alignment.

The TXINIT state changes to TXRUN with the next reference clock pulse. The transmission of the first data bit starts with the RF-output power ramping.

In TXRUN state first the encoder configuration is loaded and the transmission can be continued by successive writing to TXDAT in response to the TX buffer empty interrupt. Before writing new data to TXDAT it must be verified that the buffer is empty (TXBE) otherwise old data in TXDAT will be overwritten and discarded from transmission. If no new data is written before the last bit of the buffered TXDAT is sent the transmission will end. TXIDLE is entered without underflow indication (TXBU) if the last TXDAT content is set as last data by the DATLAST bit. Transmission stops after the last bit period and after an optional RF-signal ramp down.

If TXSTOP is requested in the TXRUN state, RF ramp down will start at the end of the current bit transmission as the state machine transitions to the TXIDLE state. Any data not sent in the TX buffer will be discarded.

If TXRESET is requested in the TXRUN state, RF ramp down will start immediately and the state machine will transition to the TXIDLE state. Any data not sent will be discarded.

The TXABORT event is an exception caused by a PLL lock loss or XO_READY loss. It causes the state machine to enter immediately the TXIDLE state and forces the PA output signal abruptly to the minimum ramping power level. Any TX data not sent will be discarded and the PAEN bit will be cleared. Transmission interruption due to PLL lock loss (PLL_UNLOCK_DETECTED) can be caused by starting VCO calibration, a crystal oscillator failure or significant supply depletion.

Transmission will also stop immediately if the device state changes to POWER OFF.

Note that a VBAT supply brownout indication will not prevent a transmission start. Also an ongoing transmission remains active regardless of the battery brownout status. A battery supply brownout event needs to be handled via a dedicated user software interrupt routine.

2.6.8.2 Transmission Data Register, TXDAT

Transmission is initiated when the first bit to be transmitted is written to the TXDAT register. If TXDAT is written using byte access, the DATLSBF register bit setting (see Table 69) determines whether writing the high byte or low byte starts the transmission .

Table 76. Transmission data in TXDAT (rest value 0000h)

Bit	Symbol	Access	Value	Description
15 to 8	TXDAT[15:8]	R/W		Data to be transmitted, high byte
7 to 0	TXDAT[7:0]	R/W		Data to be transmitted, low byte

2.6.8.3 Advanced Protocol Support Register, TXSPC

An application RF protocol can make use of spaced telegram segments in which part of the TXDAT data is masked by the content of TXSPC, e.g. a receiver expects to identify some parts of the telegram as idle transmission that can be provided without changing power or other transmission settings. Also a hand-over between preamble and payload-data can be supported by transmitting at the minimal RF power level for the required period. These low-power bit intervals can be masked in a TXDAT data frame by marking corresponding bits in the TXSPC register, as shown in Table 77.

Table 77. Transmission space masking in TXSPC (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 8	SPC[15:8]	R/W		Space masking, high byte:
			0	(at an arbitrary position from 8 to 15) - No masking of that TXDAT bit
			1	(at an arbitrary position from 8 to 15) - the output signal power will be decayed according to ASKRMP settings, to the min. amplitude- and output power level
7 to 0	SPC[7:0]	R/W		Space masking, low byte:
			0	(at an arbitrary position from 0 to 7) - No masking of that TXDAT bit
			1	(at an arbitrary position from 0 to 7) - the output signal power will be decayed according to ASKRMP settings, to the min. amplitude- and output power level

The TXSPC settings shall be written before TXDAT register.
Masking will take effects when the new data written into TXDAT is transmitted.

2.7 Tuning capacitors for LF

The LF tuning function provides a facility for adjusting the input capacitance seen at the LF input pins, INxP and INxN. This allows fine tuning of the resonant frequency of the external antenna circuit to optimize reception of an incoming LF signal.

The tuning capacitance is implemented as a selectable array of unit capacitors connected between the input pin and ground.

Each channel pair, IN1P/N, IN2P/N and IN3P/N can be independently controlled by writing the contents of the special function registers, LFTUNEVBAT and LFTUNEVDD. Control bits within these registers comprise a disable bit and a 4-bit selection code, one for each channel. Capacitor selection can be controlled from either the VBAT domain registers or the VDD domain registers depending on the supply state and whether the LF front-end is in passive immobilizer mode or not. Further details are described in Section 2.7.2. The register LFTUNEVBAT and LFTUNEVDD are described in Table 78.

For weakly-coupled input signals, the LF front-end rectifier has no effect and the voltages on INxP and INxN are differential with a common-mode voltage around ground. In this case, the LF tuning capacitors on INxP and INxN are in series resulting in an effective tuning value of half the single-ended value.

For strongly-coupled signals, the LF front-end rectifier creates half-wave rectified voltage signals on INxP and INxN. In this case the capacitance to ground on each pin is in circuit for each half-wave. The effective tuning capacitance is the single-ended value.

Table 78. Tuning configuration registers LFTUNEVBAT and LFTUNEVDD (reset value 0000h)

Bit	Symbol	Access	Value	Description
15	RFU	R/W0		Reserved for future use
14	LF_CAP_CH3_DIS	R/W		IN3P/N tuning capacitance disable
			0	Tuning capacitance enabled
			1	Tuning capacitance disabled
13	LF_CAP_CH2_DIS	R/W		IN2P/N tuning capacitance disable
			0	Tuning capacitance enabled
			1	Tuning capacitance disabled
12	LF_CAP_CH1_DIS	R/W		IN1P/N tuning capacitance disable
			0	Tuning capacitance enabled
			1	Tuning capacitance disabled
11 to 8	LF_CAP_CH3[3:0]	R/W	0h to Fh	Applied IN3P/N tuning capacitance, see Table 79
7 to 4	LF_CAP_CH2[3:0]	R/W	0h to Fh	Applied IN2P/N tuning capacitance, see Table 79
3 to 0	LF_CAP_CH1[3:0]	R/W	0h to Fh	Applied IN1P/N tuning capacitance, see Table 79

Strongly-coupled and weakly-coupled signal are influencing the equivalent resonance capacitance as it can be seen in Figure 37, with the help of the LF-front-end rectifier AC-model (A). The LF front-end rectifier for strongly-coupled signals is AC-grounding the INxN side through-out the VSS-clamp diode D3 in (B), while for the weakly-coupled signals, the complete model of the rectifier can be replaced by “opens” (C).

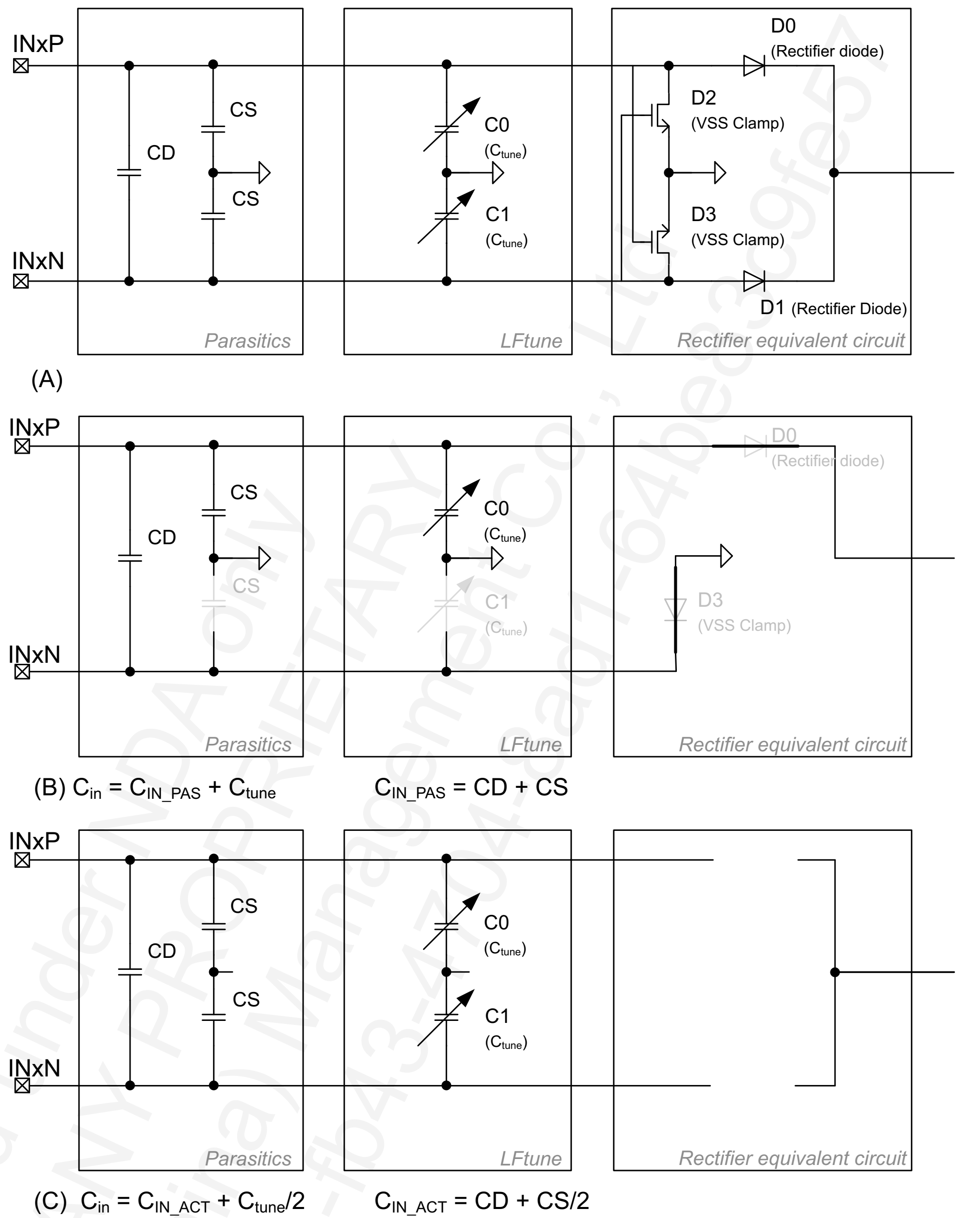


Fig 37. LF input capacitance, (A) AC-model, (B) Strongly-coupled signals, and (C) Weakly-coupled signals

Remark: Figure 37 shows a simplified model of the rectifier, wherein the limiter, the active demodulator and the passive (de)modulator are omitted.

2.7.1 Tuning Capacitance

Table 79 details LF tune decoding and shows how much capacitance is added to each pin (single-ended) for each code depending on which supply domain the selection is active. C_{STEP} represents the unit capacitor in the LF tuning array.

If the LF tuning function is disabled, there is no added capacitance. The input capacitance at each pin is as specified by parameters C_{IN_PAS} (large signal) and C_{IN_ACT} (small signal) in the Static Characteristics section.

Table 79. Tuning capacitance selection in LF_CAP_CHx[3:0]

SFR content LF_CAP_CHx[3:0]	VBAT Domain Capacitance	VDD Domain Capacitance
0000 (reset value)	9 x C_{STEP}	3 x C_{STEP}
0001	10 x C_{STEP}	4 x C_{STEP}
0010	11 x C_{STEP}	7 x C_{STEP}
0011	12 x C_{STEP}	8 x C_{STEP}
0100	13 x C_{STEP}	1 x C_{STEP}
0101	14 x C_{STEP}	2 x C_{STEP}
0110	15 x C_{STEP}	5 x C_{STEP}
0111	16 x C_{STEP}	6 x C_{STEP}
1000	1 x C_{STEP}	11 x C_{STEP}
1001	2 x C_{STEP}	12 x C_{STEP}
1010	3 x C_{STEP}	15 x C_{STEP}
1011	4 x C_{STEP}	16 x C_{STEP}
1100	5 x C_{STEP}	9 x C_{STEP}
1101	6 x C_{STEP}	10 x C_{STEP}
1110	7 x C_{STEP}	13 x C_{STEP}
1111	8 x C_{STEP}	14 x C_{STEP}

2.7.2 Use Cases

Each use case begins with the device in the POWER OFF state. In this state VDD is below the POR threshold. Each use case assumes that an LF signal is received on one or more of the INxP/N input channels.

2.7.2.1 LF Active with Battery Supplied

The battery supply voltage exceeds the internal BATPOR threshold. The LF tuning capacitance is enabled with the selection code loaded from LFTUNEVBAT special function registers. By default, the code value is 0000b. This value can be modified at any time after battery insertion. The modified value will be maintained indefinitely provided the battery remains above the BATPOR threshold.

When the LF signal is received, the state of the LF tuning capacitance will remain unchanged as long as entry into passive immobilizer mode is avoided.

As stated in before, for very small signals, the effective LF tuning capacitance is half that for larger (rectified) signals. The code stored in LFTUNEVBAT should be chosen to optimize small-signal operation with the knowledge that for stronger signals, tuning is not optimal. However, at such signal levels, LF Active reception should not be compromised by a small reduction in LF amplitude caused by sub-optimal tuning.

2.7.2.2 Passive Immobilizer with No Battery

The battery supply voltage is absent or below the internal BATPOR threshold. The device has no power supply.

In this case, with no battery, the LF Active receiver is not functional. Only LF Passive (immobilizer) communication is possible.

When an LF signal is first received, LF tune selection defaults to a state equivalent to the reset state of LFTUNEVDD. This state is internally defined, independent of the contents of LFTUNEVDD and cannot be altered.

If the LF input signal is strong enough to exceed the field-flag threshold, V_{THR,FD_ATIC_VIN}, and is unmodulated for more than 2ms, the device enters passive immobilizer mode and the internal VDD supply is powered from the LF signal. When VDD exceeds the internal POR threshold, LF tune selection switches to the contents of LFTUNEVDD, which at this point is the reset state 0000b. The LF tuning capacitance is unchanged.

After this time, the device boot routine executes, during which, LFTUNEVDD is loaded with values stored in the configuration EEPROM. This value is user-definable and may be different from the default (reset) value. A system call can be used by the application software to overwrite the value for LFTUNEVDD in the configuration EEPROM.

2.7.2.3 Passive Immobilizer with Battery Supplied

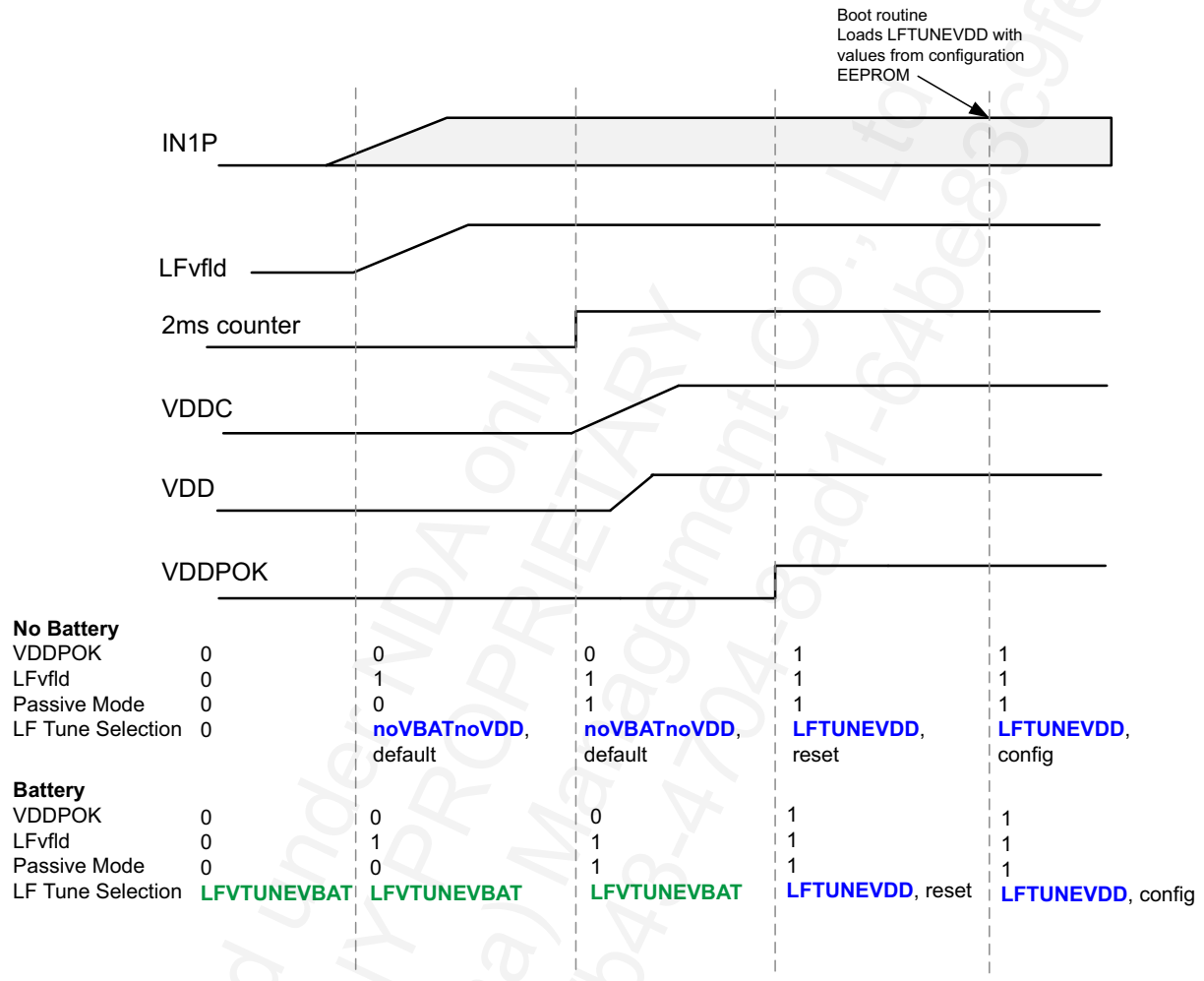
The battery supply voltage exceeds the internal BATPOR threshold.

Prior to reception of the LF signal, LF tune selection is taken from LFTUNEVBAT special function registers. When an LF signal is received, the LF tune state is maintained until passive immobilizer mode is started and VDD exceeds the internal POR threshold. At this point, LF tune selection switches to the contents of LFTUNEVDD, which at this point is the reset state 0000b.

After this time, the device boot routine executes, during which, LFTUNEVDD is loaded with values stored in the configuration EEPROM. This value is user-definable and may be different from the default (reset) value.

2.7.2.4 LF Tune for Passive Immobilizer - Timing Diagram

The diagram below shows the sequence of events for use cases described in Section 2.7.2.2 and Section 2.7.2.3 and how LF tune selection changes when the LF input is applied.



No Battery					
VDDPOK	0	0	0	1	1
LFvfld	0	1	1	1	1
Passive Mode	0	0	1	1	1
LF Tune Selection	0	**noVBATnoVDD**, default	**noVBATnoVDD**, default	**LFTUNEVDD**, reset	**LFTUNEVDD**, config
Battery					
VDDPOK	0	0	0	1	1
LFvfld	0	1	1	1	1
Passive Mode	0	0	1	1	1
LF Tune Selection	**LFVTUNEVBAT**	**LFVTUNEVBAT**	**LFVTUNEVBAT**	**LFTUNEVDD**, reset	**LFTUNEVDD**, config

Fig 38. LF Tune for Passive Immobilizer - Timing Diagram

2.7.2.5 LF Tune for LF-Active - Timing Diagram

The diagram below shows the sequence of events for the use case described in Section 2.7.2.1 and how LF tune selection changes when the LF input is applied.

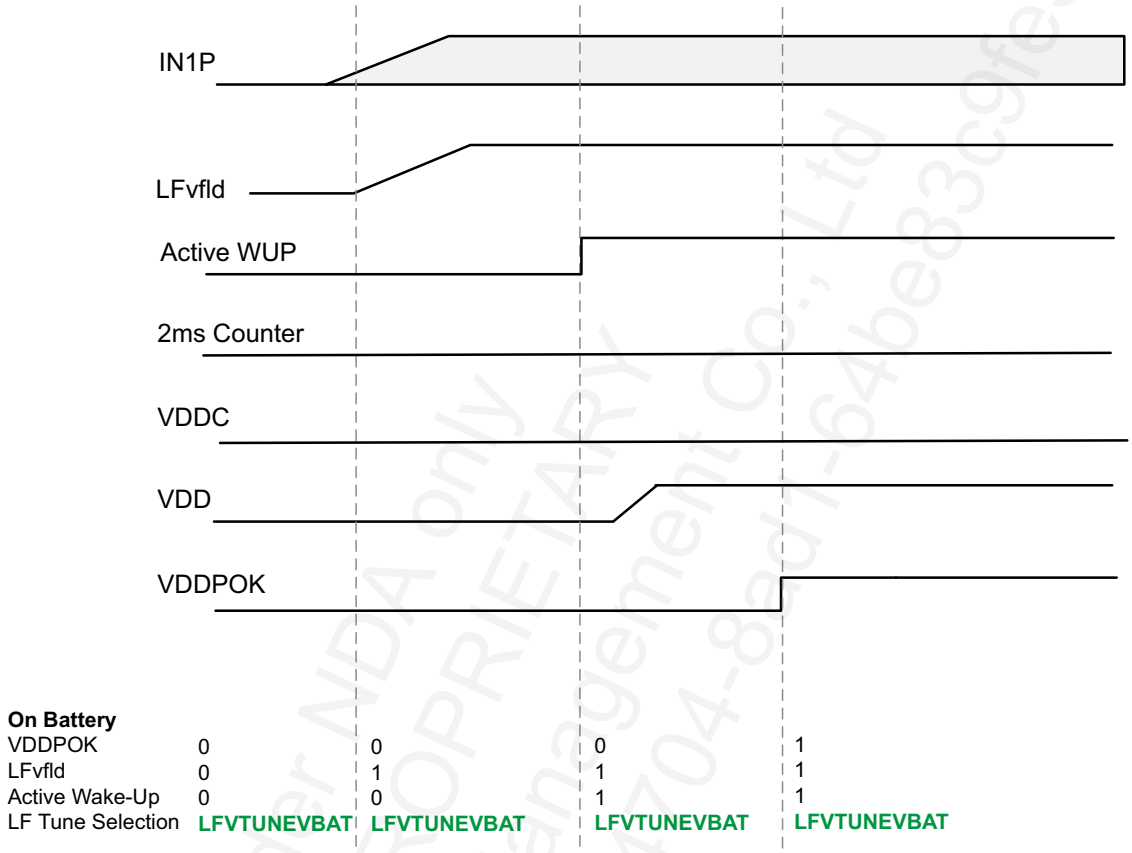


Fig 39. LF Tune for LF-Active - Timing Diagram

2.7.3 Suggested Settings

When designing the external antenna circuit, the capacitor chosen should take account of the device input capacitance and the state of LF tune. Any stray capacitance from the PCB should also be considered. This would require that the off-chip tuning capacitor is reduced compared to the value calculated for optimal tuning.

As discussed in Section 2.7.2.2, values stored in LFTUNEVDD are updated during the boot routine when LF passive mode has been detected by loading values from the Device Configuration Page DCFG D located in EEPROM. In the first instance it is suggested that these values are the same as the LFTUNEVDD reset state (0000b) to avoid a change in the LF tune capacitance during boot. If it is necessary to optimize tuning to account for external component spreads, then the values stored in the configuration EEPROM can be modified with the knowledge that prior to loading these values, the antenna circuit will not be optimally tuned.

If the off-chip tuning capacitor is designed to give optimal tuning for passive immobilizer operation, the values stored in LFTUNEVBAT can be adjusted after battery insertion to optimize tuning for small-signal LF Active operation.

This approach would lead to optimized tuning for use cases described in Section 2.7.2.2 and Section 2.7.2.3.

The use case in Section 2.7.2.3 is pertinent for applications in which LF Active is not used. In such circumstances it would be advisable to load LFTUNEVBAT with values that result in the same LF tune capacitance as those stored in LFTUNEVDD. This would avoid any discontinuity when switching from VBAT domain selection to VDD domain selection.

2.8 RISC controller

The NCF29A1 / NCF29A2 is powered by NXP's 3rd generation low power 16 bit extended Micro RISC Kernel (MRK III) with enhanced instruction set (MRK III-e), which controls device operation in LF FIELD and BATTERY state.

The MRK III utilizes a Harvard architecture featuring a 16 bit ALU and supports hardware extended MUL and DIV operations. The instruction set supports 8 bit and 16 bit operations and is optimized for C programming. Due to the efficient 2-stage pipeline (fetch/execute), most instructions execute in a single machine cycle (two clock cycles), resulting in ultra-low power consumption.

The MRK III provides 64 kByte of linear data address range and 128 kByte linear code address range, powerful addressing modes and high code density. Besides, the MRK III supports a power saving mode and code/data protection mechanisms (privilege modes).

2.8.1 Power saving modes

2.8.1.1 RUN mode

In RUN mode the MRK III is regularly clocked and processes the program instructions.

2.8.1.2 IDLE mode

The IDLE mode is a power saving mode and invoked via the command IDLE. In IDLE mode the MRK III CPU is halted by gating the internal clock signal for the MRK III CPU.

IDLE mode can only be entered, if the level sensitive wake-up signal of the MRK III controller is not active. As soon as the wake-up signal becomes active, the MRK III resumes operation and switches to RUN mode.

2.8.2 Privilege modes

2.8.2.1 SYSTEM mode

In SYSTEM mode, the NXP implemented firmware (system code, e.g. transponder emulation) is processed. SYSTEM mode is entered by a software interrupt via the SYS command or by serving a system interrupt request. SYSTEM mode is also used while executing the BOOT routine and during MDI operation.

After completing the system routines, the MRK III switches back to USER mode and control is given back to the application program.

2.8.2.2 USER mode

The application program is executed in USER mode. In USER mode, all MRK III instructions can be processed. If the MRK III is in SYSTEM mode, USER mode is entered via the USR command or by serving a user interrupt request.

2.8.3 Memory organization

Dedicated RISC controller part, Memory Management Unit - MMU, is responsible for decoding and addressing memory space in SYSTEM and USER mode.

Depending on device configuration DCFG A in the ULP module 15, i.e. CXDIS[3:0] in Table 86, MMU will be detecting three possible exceptions and treat them either as device reset or NMI, depending on CXNMIEN bit in the INTEN0 register (see Table 102).

When application tries to access undefined program memory range, or when undefined instruction is detected by the instruction decoder, the RISC will execute a NOP instruction if CXDIS is previously set to 9h. By design, stack operation are always word-aligned. However, if stack pointer is set with an odd value, (ie MOV R7, #(2*x+1)), the operation will continue if CXDIS is previously set to 9h. If the CXDIS value is 9h, any of the above exceptions will cause device reset or an NMI - depending on CXNMIEN value.

2.8.3.1 System code memory

The NXP implemented system ROM functions contain (see Section 2.24)

- Boot routine
- Transponder emulation functions
- In-circuit Monitor and Download Interface

The system code memory is not visible for the application.

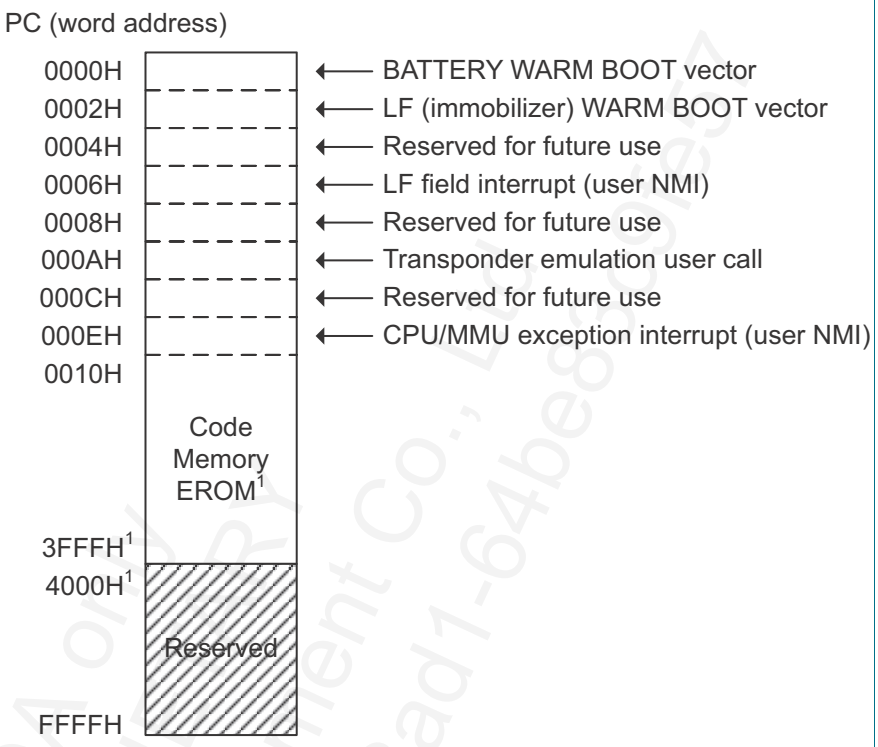
2.8.3.2 System data memory

The NCF29A1 / NCF29A2 has a dedicated data memory area including system RAM for device execution in SYSTEM mode. The system data memory area is not visible for the application. All system calls, the built-in transponder emulations and the in-circuit debugging functions use the system RAM.

2.8.3.3 Application code memory

The memory for application code is in EROM. Each instruction consists of 16/32 bit and thus occupies two/four bytes (see Figure 40).

After a device reset or a wake-up from power-down mode, program execution starts with the BOOT routine and subsequently continues with the application code that starts at the corresponding WARM BOOT vector. Execution starts from different locations, depending on the state (BATTERY or LF FIELD).



(1) The NCF29A1 / NCF29A2 can support up to 32.1 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative.

Fig 40. Application code memory

2.8.3.4 Application data memory

The NCF29A1 / NCF29A2 provides ultra-low power (ULP) serial EEPROM for persistent application data storage. The ULP EEPROM is intended for the immobilizer and remote keyless entry applications.

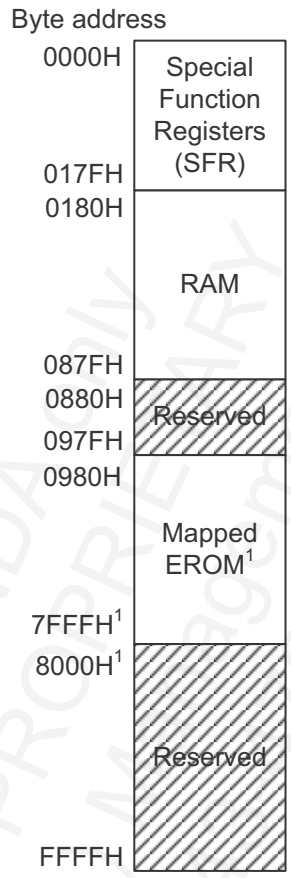
The access to the ULP EEPROM is handled via the ULP EEPROM interface.

The data memory address space is split to cover also the Special Function Registers (SFR) and User RAM (Figure 41). The SFR enable full read/write access to the peripherals. The User RAM provides memory for volatile application data and stack storage and is available for the application program without any limitations, because device execution in SYSTEM mode uses system RAM only. The stack starts at the end of the User RAM and increases with decreasing addresses.

In order to give access to constant data stored in the EROM (like look-up tables, constants, etc.) the unoccupied data address range is mapped to the code memory with the same logical address. Since the lower addresses of the application data memory are already used by the SFR and RAM, the EROM mapping starts at addresses after the RAM section. Thus, the EROM code memory content at addresses corresponding to the SFR

and RAM sections in the data memory cannot be accessed via data mapping. Although the instructions in the code memory have word granularity, read-only data can also be accessed with byte granularity.

The memory mapping scheme supports the standard ANSI-C memory model and avoids performance losses caused by generic pointer types, which are able to address different memory types dynamically.



(1) The NCF29A1 / NCF29A2 can support up to 32.1 kByte of application code memory. The actual amount of available application code memory and the end address of the code memory space may vary depending on an orderable type number. For details contact your local NXP sales representative.

Fig 41. Application data memory

2.8.4 Registers

The MMU exceptions can be monitored by two SFRs powered in the VDD domain as described in the following section.

2.8.4.1 Register, CXSW

This register reports MMU exception status.

Table 80. MMU exception status word register, CXSW (reset value 00h)

Bit	Symbol	Access	Value	Description
7	SYSMODE	R		System mode flag when the exception occurred
			0	USER mode when the exception occurred
			1	SYSTEM mode when the exception occurred
6 to 3	I[3:0]	R		Interrupt request level when the exception occurred during interrupt routine
			0000 - 1111	For details, see interrupt request level assignment in Table 99
2	XPMEM	R		MMU program memory exception flag
			0	No exception in accessing program memory
			1	Addressed program memory out of range
1	XSTACK	R		Misaligned CPU stack flag
			0	No exception in CPU stack, even value in the CPU stack
			1	CPU stack misaligned, odd value in CPU stack
0	XINSTR	R		Unknown instruction exception flag
			0	No exception in detecting instructions
			1	Unknown instruction detected

2.8.4.2 Register, CXPC

This register contains the registered program counter value when the exception occurred.

The register is read-only and provides byte and word access.

Table 81. Word and byte access to the status register CXPC

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
CXPC	CXPCH	CXPCL

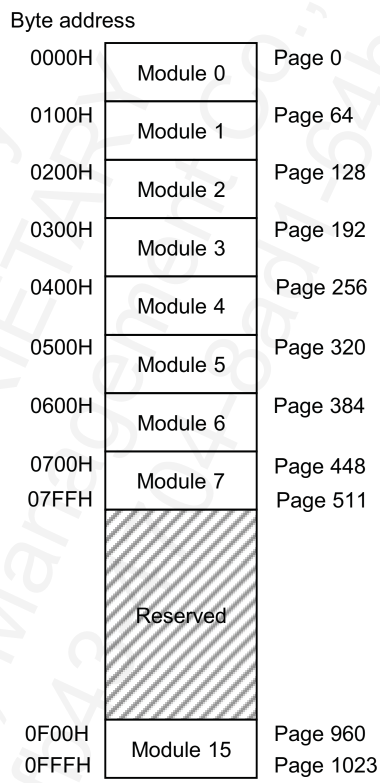
Table 82. Register, CXPC (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 0	PC[15:0]	R		Program counter value when MMU exception occurred

2.9 ULP EEPROM

The ultra-low power (ULP) serial EEPROM is intended for persistent data storage for the immobilizer, boot routine and system functions in ROM and the application software. The ULP EEPROM consists of up to 9 modules (module 0 to 7 and module 15). In Figure 42 the ULP EEPROM data memory map is given in case 2048 Byte EEPROM (Module 0..7) plus 256 Bytes for Module 15 is actually available. In this case the application has full read/write/program access to modules 0 to 7. Module 15 holds trim and configuration data and can only be read but not written or programmed by the application. Each module consists of 64 pages containing 4 byte (32 bit) each.

The ULP modules are optimized in terms of power consumption for read access and programming by having a separate power-on bit for each module.



(1) The NCF29A1 / NCF29A2 can support up to 2048 Byte of ULP EEPROM (excluding module 15). The actual amount of available ULP EEPROM and the available modules may vary depending on the type number. Here the ULP EEPROM data memory map is given in case the actual available EEPROM is 2048 Bytes. For details contact your local NXP sales representative.

Fig 42. ULP EEPROM data memory map (2048 Byte EEPROM configuration)

2.9.1 Available ULP EEPROM modules

The NCF29A1 / NCF29A2 supports up to 2048 Byte ULP Serial EEPROM (excluding module 15). The actual amount of available ULP Serial EEPROM and thus the number of available EEPROM pages may vary depending on the type number. For details contact your local NXP sales representative. The actual ULP EEPROM data memory map is dependent on the actual amount of available ULP Serial EEPROM and the supported transponder type.

2.9.1.1 ULP EEPROM data memory map (512 Bytes available ULP EEPROM)

On NCF29A1 / NCF29A2 product types supporting only 512 Bytes ULP EEPROM only ULP module 0, module 1 and module 15 are available. The ULP modules 0 and 1 contain the memory pages 0 to 127 which are available for user data storage. These pages can be accessed (read/write/program) by the application.

Dependent on the provided transponder emulation, some parts of module 0 and 1 are used for transponder specific data. For HT-Pro2 transponder types the EEPROM pages 488 to 511 in Module 7 are available and used as distance memory and configuration memory by the transponder emulation. For details refer to transponder data sheet.

During transponder emulation, page 1023 (ULP module 15) containing the device identifier (IDE) is mapped to page 0 (ULP module 0), thus the physical content of page 0 is not accessible by the application in this case.

2.9.1.2 ULP EEPROM data memory map (1024 Bytes available ULP EEPROM)

On NCF29A1 / NCF29A2 product types supporting only 1024 Bytes ULP EEPROM only ULP module 0 to module 7 and module 15 are available. The ULP modules 0 to 3 contain the memory pages 0 to 255 which are available for user data storage. These pages can be accessed (read/write/program) by the application.

Dependent on the provided transponder emulation, some parts of module 0 and 1 are used for transponder specific data. For HT-Pro2 transponder types the EEPROM pages 488 to 511 in Module 7 are available and used as distance memory and configuration memory by the transponder emulation. For details refer to transponder data sheet.

During transponder emulation, page 1023 (ULP module 15) containing the device identifier (IDE) is mapped to page 0 (ULP module 0), thus the physical content of page 0 is not accessible by the application in this case.

2.9.1.3 ULP EEPROM data memory map (2048 Bytes available ULP EEPROM)

On NCF29A1 / NCF29A2 product types supporting 2048 Bytes ULP EEPROM module 0 to module 7 and module 15 are available. The ULP modules 0 to 7 contain the memory pages 0 to 511 which are available for user data storage. These pages can be accessed (read/write/program) by the application.

Dependent on the provided transponder emulation, some parts of module 0 and 1 are used for transponder specific data. For HT-Pro2 transponder types the EEPROM pages 488 to 511 in Module 7 are available and used as distance memory and configuration memory by the transponder emulation. For details refer to transponder data sheet.

During transponder emulation, page 1023 (ULP module 15) containing the device identifier (IDE) is mapped to page 0 (ULP module 0), thus the physical content of page 0 is not accessible by the application in this case.

2.9.2 ULP module 15

Independent from the actual amount of available ULP Serial EEPROM supported, ULP module 15 is always available and contains the 64 bit device identifier (IDE64) consisting of the 32 bit device identifier (IDE) and the 32 bit enhanced device identifier (EIDE). Further, ULP module 15 locates the device configuration pages (see Figure 43). Module 15 contains trim and configuration data in the reserved areas.

All pages are readable by the MRK III CPU core. The pages 960 to 975 and 992 to 1023 contain factory programmed data which can be read, but not altered. The pages 976 to 991 locate the device configuration data which can only be modified in INIT mode (see Section 2.26) via the Monitor and Download Interface (MDI).

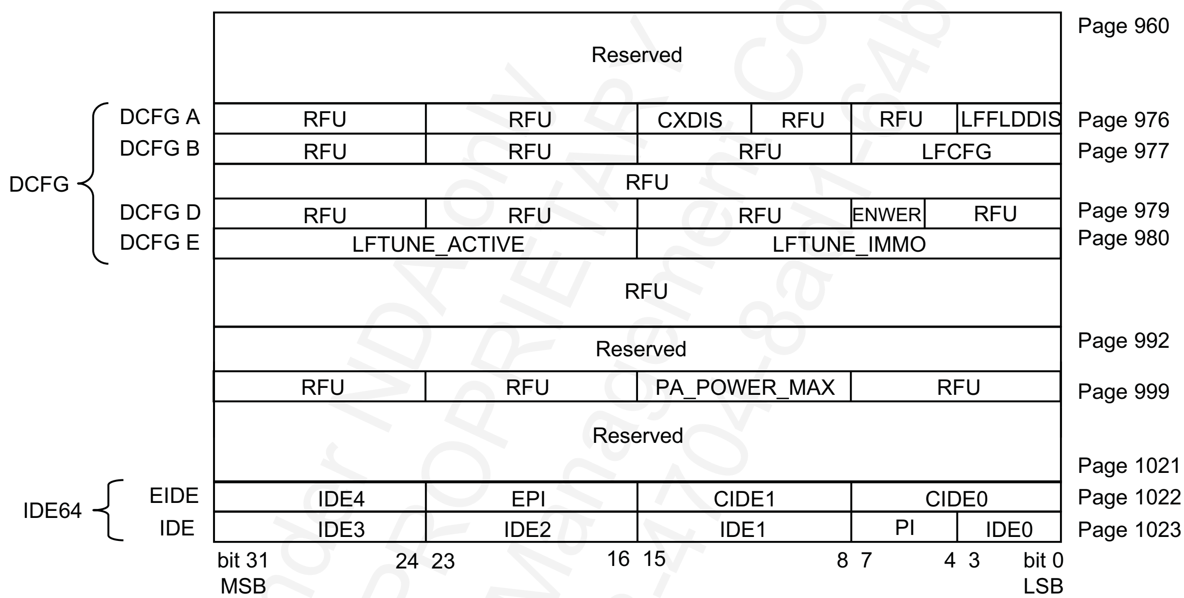


Fig 43. ULP EEPROM memory module 15

2.9.2.1 Identifier (IDE)

The device identifier (IDE) is a 32 bit pattern representing the lower 32 bits of the unique device serial number (SN).

The IDE is located in ULP memory page 1023. IDE bits 4 to 7 represent the product type identifier (PI). IDE bit 7 contains the value 1 for all MRKIII devices. The IDE is typically employed in the process of device authentication in transponder mode as well as during rolling code or challenge response generation for keyless entry applications.

Table 83. Device identifier IDE (content upon delivery Section 2.26)

Bit	Symbol	Access	Value	Description
31 to 24	IDE3[7:0]	R		Device serial number bit 24 to 31
23 to 16	IDE2[7:0]	R		Device serial number bit 16 to 23
15 to 8	IDE1[7:0]	R		Device serial number bit 8 to 15
7 to 4	PI[3:0]	R	1110b	Device product identifier
3 to 0	IDE0[3:0]	R		Device serial number bit 0 to 3

2.9.2.2 Enhanced identifier (EIDE)

The enhanced identifier, EIDE, is located in ULP memory page 1022 and serves to enlarge the unique device serial number (SN) by 8 bits (IDE4). Further, the EIDE contains the enhanced product identifier (EPI) and the customer identifier (CIDE).

Table 84. Device enhanced identifier EIDE (content upon delivery see Section 2.26)

Bit	Symbol	Access	Value	Description
31 to 24	IDE4[7:0]	R		Device serial number bit 32 to 39
23 to 16	EPI[7:0]	R		Device enhanced product identifier
15 to 8	CIDE1[7:0]	R		Customer identifier bit 8 to 15
7 to 0	CIDE0[7:0]	R		Customer identifier bit 0 to 7

2.9.2.3 PA_POWER_MAX

PA_POWER_MAX is a trimmed value for the UHF transmitter VPA voltage regulator optimized for the 10dBm mode. PA_POWER_MAX is located in ULP memory page 999.

Table 85. PA_POWER_MAX trimming value (content upon delivery see Section 2.26)

Bit	Symbol	Access	Value	Description
31 to 16	RFU[15:0]	R		Reserved for future use
15 to 8	PA_POWER_MAX[7:0]	R		PA_POWER_MAX trimming value optimized for the 10dBm mode
7 to 0	RFU[7:0]	R		Reserved for future use

2.9.2.4 Device configuration (DCFG)

The device configuration DCFG pages contain device configuration information, which is locked against overwriting. The DCFG bits can be initialized via the Monitor and Download Interface (MDI) only and are evaluated after each device reset within the boot routine.

Table 86. Device configuration page DCFG A (content upon delivery see Section 2.26)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 16	RFU[15:0]	R/W0	R		Reserved for future use
15 to 12	CXDIS[3:0]	R/W	R		CPU/MMU exceptions
				1001	Disabled
				others	Enabled

Table 86. Device configuration page DCFG A (content upon delivery see Section 2.26)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
11 to 4	RFU[3:0]	R/W0	R		Reserved for future use
3 to 0	LFFLDDIS[3:0]	R/W	R		LF field reset and non-maskable interrupt
				1001	Disabled
				others	Enabled

Table 87. Device configuration page DCFG B (content upon delivery see Section 2.26)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 5	RFU	R/W0	R		Reserved for future use
4	STRONGMOD	R/W	R		Strong LF modulator in transponder emulation
				0	Enable standard LF modulator
				1	Enable strong LF modulator
3 to 1	RFU	R/W0	R		Reserved for future use
0	LFTEN	R/W	R		LF transponder emulation enable
				0	Use LF warm boot vector
				1	Enable emulation in system ROM

LFTEN, LF transponder emulation enable

If set, after each device reset the monolithic transponder emulation is enabled. If cleared, the boot sequence does not invoke the transponder emulation. Instead control is passed to the application program, starting at the LF (immobilizer) WARM BOOT vector.

2.9.2.5 LF tuning capacitors

Internal tuning capacitors configuration including capacitor selection value as well as the three tuning disabling control bits is stored into the page 3D4h. Bit 0 to 15 contain the Immobilizer mode configuration and will be loaded into the LFTUNEVDD SFR by the boot-routine when LF passive mode has been detected.

Table 88. Device configuration page DCFG E (content upon delivery see Section 2.26)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 16	LFTUNE_ACTIVE[15:0]	R/W	R		Reserved for tuning capacitors configuration for LF active mode
15 to 0	LFTUNE_IMMO[15:0]	R/W	R		Tuning capacitors configuration for Immobilizer mode

2.9.2.6 ENWER (ENable Write EROM)

Bits 7..6 of this byte (byte address 3916 dec.) must be 10 (bin) to enable system call phcaiKEyLLGenFunc_CS_EROM_write.

Table 89. Device configuration page DCFG D (content upon delivery see Section 2.26)

Bit	Symbol	Access via MDI in INIT mode	Access by User Software	Value	Description
31 to 8	RFU	R/W0	R		Reserved for future use
7 to 6	ENWER	R/W	R	00	disable system call phcaiKEyLLGenFunc_CS_EROM_write
				01	disable system call phcaiKEyLLGenFunc_CS_EROM_write
				10	enable system call phcaiKEyLLGenFunc_CS_EROM_write
				11	disable system call phcaiKEyLLGenFunc_CS_EROM_write
5 to 0	RFU	R/W0	R		Reserved for future use

2.9.3 ULP EEPROM interface

The memory modules consist of 256 bytes each and are bit oriented, thus allowing random read access to every bit (Figure 44). In case byte access is required, the ULP EEPROM interface provides byte oriented read access via an 8 bit data register to minimize the CPU load. Programming of the ULP serial EEPROM is supported on 32 bit pages only. An internal state machine handles the low level access to the module. The interface performs the read/write and programming operations autonomously and indicates the status via busy flag and optional wake-up from idle mode.

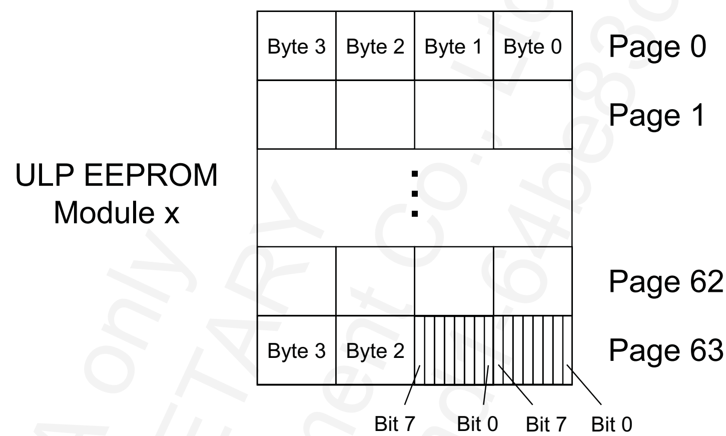


Fig 44. ULP EEPROM module

The ULP EEPROM interface contains an address register with bit addressing capabilities and auto-increment feature (modulo 32 bit for write access). The auto increment function allows reading of consecutive bytes/bits without additional access to the address register.

2.9.3.1 Read access

For read access to the ULP EEPROM, the module, the page, the byte and the bit address have to be specified. Starting at this bit position, the specified number of bits (maximum 8) is transferred into the 8 bit data register ULPDAT(Figure 45).

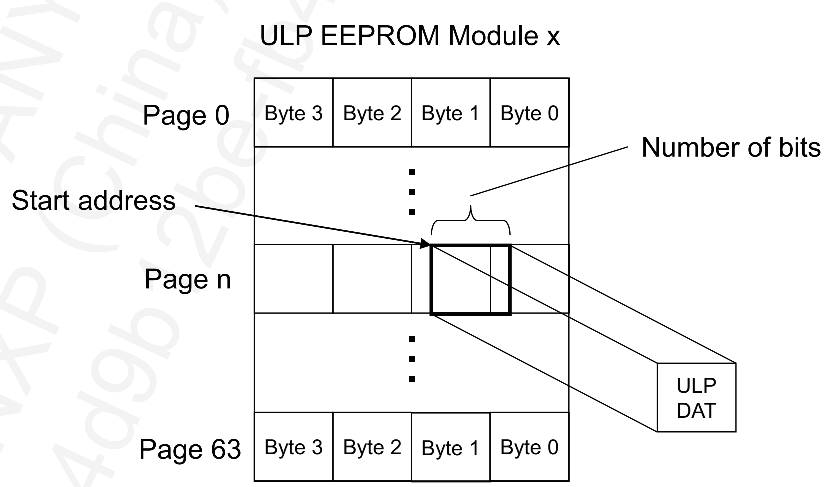


Fig 45. ULP EEPROM read access

Afterwards, the auto increment function increments the start address by the number of bits read. Hence, in case the start address is not changed by command, the next read operation starts with the bit adjacent to the last bit read. The auto increment function increments without being influenced by page or module boundaries (Figure 46), thus in case all ULP EEPROM modules have been powered, the whole addressable memory range can be read without additional manual address change.

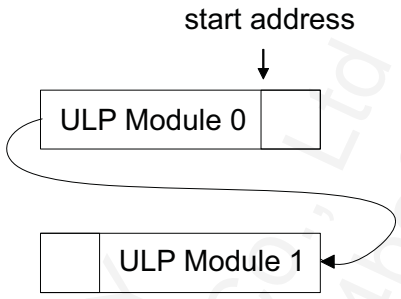


Fig 46. Auto increment during read operation

2.9.3.2 Write access and programming

Write access to the ULP EEPROM is performed with the help of a page register having a length of 32 bit. During programming, always the content of the complete page register is written to the addressed ULP EEPROM page (see Figure 47).

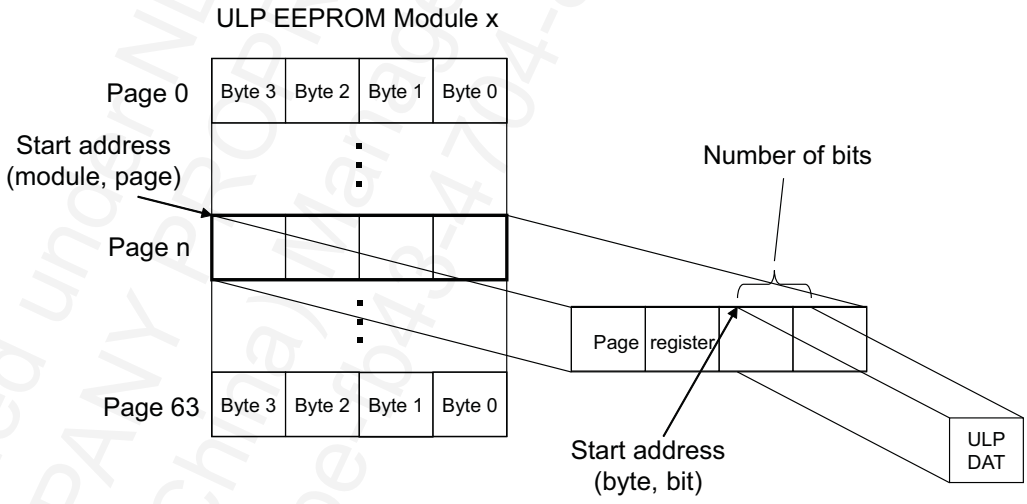


Fig 47. ULP EEPROM write access

The page register has to be written successively via the 8 bit data register ULPDAT. The start address for writing within the page register is specified by the corresponding byte and bit number. Starting at the dedicated position, the specified number of bits (maximum 8) is transferred from the data register to the page register.

Afterwards, the auto increment function increments the start address in the page register by the number of bits written. In difference to read access, the start address for writing will be chosen inside the page register only, thus reaching the register end, the start address will begin at the first bit position in the page register again (see Figure 48).

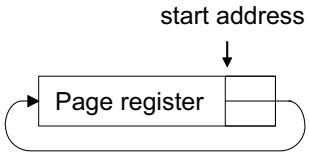


Fig 48. Auto increment during write operation

After writing data to the page register, the ULP EEPROM page selected via the module and page number can be programmed by a dedicated system call. During the programming operation the content of the page register is transferred into the EEPROM cell matrix. Each bit of the page register shall be written once via ULPDAT only, otherwise the bit content is undefined. Hence, in case the page register is written without programming the ULP EEPROM afterwards, it has to be reset manually before the next write access is performed. In case some bits of the page register have not been written prior to the programming operation, their content is '1', which is the reset state of the page register. The page register is reset after device reset, ULP EEPROM reset and after each programming operation has finished. In case the application wants to program several pages it has to set the address manually to the next desired page after every programming operation.

2.9.3.3 ULP access sequence

Figure 49 shows an example of an ULP access sequence. Both ULPPON and ULPSELx have to be set (order of setting not relevant) before the module gets powered. The module is accessible after $t_{ULP,PON}$. In the example, first a write and program sequence is executed, followed by a read access.

The module powers down immediately after clearing either ULPPON or ULPSELx

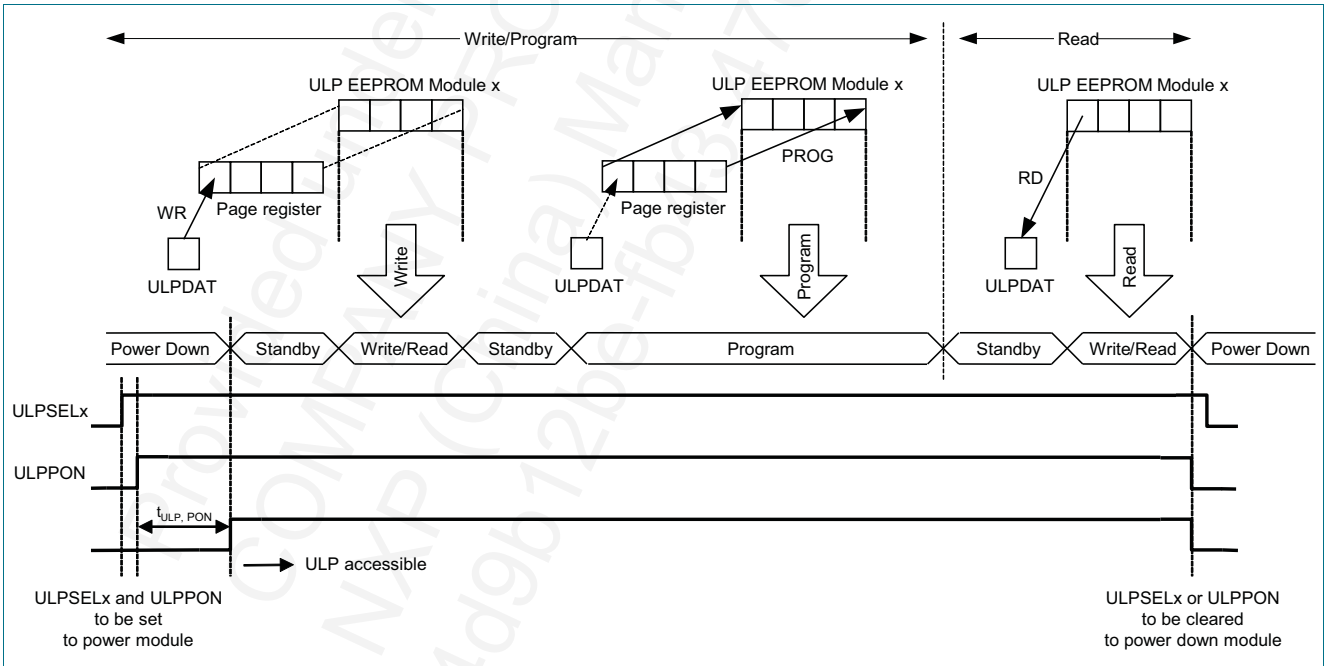


Fig 49. ULP access sequence

2.9.4 Registers

2.9.4.1 ULP EEPROM data register ULPDAT

The ULP data register ULPDAT buffers one data byte for data exchange with the ULP EEPROM. During read operation, the data byte is read directly from the ULP EEPROM, while during write operation the buffered data byte is transferred into the page register first, before this is written to the ULP EEPROM.

The data can be read via ULPDAT if ULPRUN is cleared. ULPDATA[0] holds always the LSB of the read/write data, even if less than 8 bits are read/written.

Table 90. ULP EEPROM data register ULPDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	ULPDATA[7:0]	R/W		ULP EEPROM data

2.9.4.2 ULP EEPROM control register ULPCON0

The register ULPCON0 is used to control the read and write access of the ULP EEPROM interface.

Table 91. ULP EEPROM control register ULPCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	ULPRUN	R/W		Start read/write access from/to ULP EEPROM; programming indicator
			0	Read: Access finished Write: No effect
			1	Read: Read/write access or programming in operation Write: Start access
6	ULPPROGERR	R/-		ULP EEPROM programming error
			0	No error detected
			1	Error detected
5	ULPRST	R0/W		Global ULP EEPROM and interface reset
			0	No reset
			1	Reset
4	ULPPON	R/W		Power on selected ULP EEPROM modules
			0	Disable
			1	Enable
3	ULPWR_RD	R/W		Write or read access
			0	Read access
			1	Write access

Table 91. ULP EEPROM control register ULPCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
2 to 0	ULPBITAMOUNT[2:0]	R/W		Amount of bit to read/write
			000	1 bit
			001	2 bit
			010	3 bit
			011	4 bit
			100	5 bit
			101	6 bit
			110	7 bit
			111	8 bit

ULPRUN, Start read/write access from/to ULP EEPROM

Setting ULPRUN starts the read/write access from/to the addressed ULP EEPROM location. Dependent on the settings of WRULPWR_RD data is read from the ULP EEPROM via ULPDAT or data is written to the page register via ULPDAT. By reading ULPRUN the current status of the read/write/program sequence can be detected. After the respective sequence is finished, ULPRUN is reset automatically. While the sequence is running, all registers provided to configure an ULP EEPROM access (ULPDAT, ULPCON0 except bit ULPRST, ULPCON1, ULPSEL and ULPADDR) are locked for writing by the CPU and the content of ULPDAT and ULPADDR is gated to zero. The bits RUN and ULPRST shall not be set to '1' simultaneously. Otherwise the behavior of the ULP interface is not predictable. This means that also read-modify-write operations on bit ULPRST shall be avoided when ULPRUN is '1'.

ULPPROGERR, ULP EEPROM programming error

ULPPROGERR signals an ULP EEPROM programming error and can be checked after programming. If the bit is set the programming needs to be performed again. This bit shall be cleared manually via ULPRST before new data can be written to the ULP EEPROM.

ULPRST, Global ULP EEPROM and interface reset

ULPRST performs a global reset of the ULP EEPROM interface. If ULPRST is set, any running read/write sequence is interrupted and the write/read sequencer, the register ULPDAT, the page registers of all ULP EEPROM modules and bit ULPPROGERR are reset. Further, an ongoing programming operation is interrupted immediately. Please note that this can lead to corrupted data in the affected page of the selected ULP EEPROM module. The bits ULPRST and ULPRUN shall not be set to '1' simultaneously. Otherwise the behavior of the ULP interface is not predictable. This means that also read-modify-write operations on bit ULPRST shall be avoided when ULPRUN is '1'.

ULPPON, Power on selected ULP EEPROM modules

ULPPON is the global power on switch for the ULP EEPROM modules. After powering, a dedicated start-up time $t_{ULP,PON}$ has to be considered before a read/write access to the modules can be performed. The same start-up time shall be considered, if ULPPON is set and a bit within ULPSEL is changed from '0' to '1'.

ULPWR_RD, Write or read access

WRULPWR_RD is used to distinguish between read and write access to the ULP EEPROM. Write access is granted if WRULPWR_RD is set, while read access is granted for WRULPWR_RD = '0'.

ULPBITAMOUNT[2:0], Amount of bits to read/write

ULPBITAMOUNT[2:0] defines the number of bits either to read via ULPDAT from the ULP EEPROM or to write via ULPDAT to the page register. It is possible to define 1 to 8 bit. ULPBITAMOUNT remains unchanged during a read/write access and needs thus not to be set again if the same amount of bit should be accessed in a next sequence.

2.9.4.3 ULP EEPROM control register ULPCON1

The register ULPCON1 is used to program the content of the page register after successful writing in the ULP EEPROM. The smallest possible unit to be stored is 32 bits.

ULPCON1 is fully accessible in SYSTEM mode only. An application executed in USER mode shall use a system call to change the register.

Table 92. ULP EEPROM control register ULPCON1 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	BUSYPROG	R/W	R		Programming
				0	Read: Programming not active Write: No effect
				1	Read: Programming active Write: Start programming
6 to 0	RDT	R/W	R		Reserved for device test

BUSYPROG, Programming

In order to start programming the BUSYPROG bit has to be set. BUSYPROG stays set as long as the programming is active. The bit can be polled during programming or can be used as interrupt source.

After programming the page register is cleared automatically.

2.9.4.4 ULP EEPROM selection register ULPSEL

The ULP EEPROM modules have to be activated via ULPSEL first, before a read or write access can be performed. After changing a bit within ULPSEL from '0' to '1', a dedicated start-up time $t_{ULP,PON}$ has to be considered for powering the module(s). In order to reduce power consumption, only accessed modules should be enabled.

The ULP selection register ULPSEL provides byte and word access.

Table 93. Word and byte access to the ULPEEPROM selection register ULPSEL

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ULPSEL	ULPSELH	ULPSELL

Table 94. ULP EEPROM selection register ULPSEL (reset value 0000h)

Bit	Symbol	Access	Value	Description
15	ULP_SEL[15]	R/W		ULP EEPROM module 15 selection
			0	Power down module
			1	Activate module
14 to 8	RFU	R/W0		Reserved for future use
7	ULPSEL[7]	R/W		ULP EEPROM module 7 selection
			0	Power down module
			1	Activate module
6	ULPSEL[6]	R/W		ULP EEPROM module 6 selection
			0	Power down module
			1	Activate module
5	ULPSEL[5]	R/W		ULP EEPROM module 5 selection
			0	Power down module
			1	Activate module
4	ULPSEL[4]	R/W		ULP EEPROM module 4 selection
			0	Power down module
			1	Activate module
3	ULPSEL[3]	R/W		ULP EEPROM module 3 selection
			0	Power down module
			1	Activate module
2	ULPSEL[2]	R/W		ULP EEPROM module 2 selection
			0	Power down module
			1	Activate module
1	ULPSEL[1]	R/W		ULP EEPROM module 1 selection
			0	Power down module
			1	Activate module
0	ULPSEL[0]	R/W		ULP EEPROM module 0 selection
			0	Power down module
			1	Activate module

ULPSEL, ULP EEPROM module selection

The ULP memory modules 0 to 7 and 15 are powered by setting ULPSEL[0] to ULPSEL[7] and ULPSEL[15], respectively. It has to be considered that additionally the global power on switch ULPPON has to be set in order to provide power to the modules.

2.9.4.5 ULP EEPROM address register ULPADDR

The start address for an ULP EEPROM read or write access is defined via ULPADDR, which provides byte and word access.

Table 95. ULP EEPROM address register ULPADDR (reset value xxxxh)

Bit	Symbol	Access	Value	Description
15	RDT	R0/W0		Reserved for device test
14 to 0	ULP_ADDR[14:0]	R/W		ULP EEPROM start address

ULPADDR[14:0], ULP EEPROM start address

ULPADDR is used to select the ULP EEPROM start address for reading and writing data. The bits of ULPADDR are related to the module, page, byte and bit address of the ULP EEPROM section to be accessed (Table 96).

Table 96. ULP EEPROM address register bit assignment

Symbol	Addressed section
ULPADDR[14:11]	Module
ULPADDR[10:5]	Page
ULPADDR[4:3]	Byte
ULPADDR[2:0]	Bit

During read operation, the address given in ULPADDR selects directly the ULP EEPROM address (module, page, byte and bit) where reading starts.

During write operation, the address specified via ULPADDR[4:0] (byte and bit) is related to the page register, while the address given in ULPADDR[14:5] (module and page) is related to the ULP EEPROM.

2.10 Interrupt system

The NCF29A1 / NCF29A2 contains an interrupt controller featuring 15 hardware interrupt priority levels. If more than one hardware interrupt request is pending at the same time the source with the highest request level is selected, independent of the RISC controller privilege mode (SYSTEM or USER mode).

The priority levels for LF field detection, CPU/MMU exception and user hardware interrupts are fixed. All user hardware interrupts use one common interrupt vector, which address is defined by the application via a dedicated SFR. This allows flexible software controlled handling of interrupt priorities, dynamic assignment of different interrupt service routines and the definition of distinct interrupt service routines for different applications.

The application can switch dynamically between single or nested interrupt execution and whether a selected event causes an interrupt or a wake-up event. If an interrupt is enabled, it causes the RISC controller to perform a CALL operation to the configured location, where execution of the Interrupt Service Routine (ISR) starts.

User interrupts (maskable and non-maskable) are usually disabled during the execution of system code (SYS instructions). In this case any interrupt request is latched and execution is delayed until control is returned to the application code. Please note that the system is basically able to allow user interrupts also during execution of system code. Any system call using this feature will describe this behavior explicitly.

2.10.1 Interrupt sources

The interrupt sources are summarized in Table 97. Every interrupt source has a dedicated interrupt request flag. Maskable interrupts have additionally an interrupt enable bit. If an interrupt source is used as user and system interrupt two different interrupt enable bits are provided to allow separate control in every mode.

The supported interrupt types are maskable system interrupts (System), maskable user interrupts (User) and non-maskable user interrupts (User NMI).

Table 97. Interrupt sources

Interrupt Description	Interrupt type	Sensitivity
LF field interrupt	User NMI, system	Edge
CPU/MMU exception interrupt	User NMI, system	Edge
Port interrupt	User	Edge
Timer 0 interrupt	User, system	Edge
Timer 1 compare interrupt	User, system	Edge
Timer 1 capture interrupt	User, system	Edge
Alternative port interrupt	User	Edge
System timer 0 interrupt	System	Level
Immobilizer interface unit interrupt	User, system	Level
ULP EEPROM interrupt	User, system	Edge
ADC interrupt	User, system	Edge
AES calculation unit interrupt	User, system	Edge
Random number generator interrupt	User, system	Edge
Interval timer and real time clock interrupt	User	Level
LF active preprocessor interrupt	User	Level

Table 97. Interrupt sources

Interrupt Description	Interrupt type	Sensitivity
SPI 0 interrupt	User	Level
SPI 1 interrupt	User	Level
Timer 2 interrupt	User	Edge
Motion sensor interface interrupt	User	Level
VBAT brownout monitor interrupt	User	Level[1]
UHF crystal oscillator ready interrupt	User	Edge
UHF PLL VCO calibration finished interrupt	User	Edge
UHF PLL locked interrupt	User	Edge
UHF PLL unlocked interrupt	User	Edge
UHF PA ready interrupt	User	Edge
UHF PA current limiter interrupt	User	Edge
UHF transmit buffer empty interrupt	User	Level
UHF transmission finished interrupt	User	Edge

[1] The source of this interrupt is the registered VBAT brownout monitor flag, bit VBATBRNREG in PCON2, which implies a special treatment for reading or clearing the interrupt flag

Interrupt sources can be level sensitive or edge sensitive.

A level sensitive interrupt has a transparent interrupt request flag, which is set as long as the request remains active (Figure 50). A level sensitive interrupt cannot be cleared directly since the interrupt request flag is transparent. Thus, a level sensitive interrupt request has to be cleared by acknowledging the event in the corresponding peripheral.

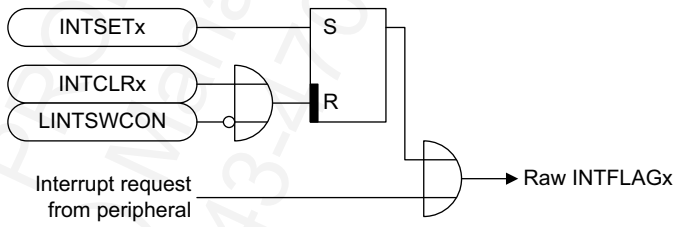


Fig 50. Interrupt request flag for level sensitive interrupts

An edge sensitive interrupt uses an edge detector as interrupt request flag (Figure 51). Edge sensitive interrupts shall be acknowledged by clearing the interrupt request flag via the application program. This is necessary, as several interrupts use a common interrupt vector and the system cannot determine which one is served by the application, if several interrupts occur simultaneously.

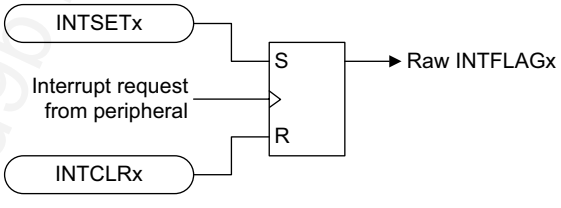


Fig 51. Interrupt request flag for edge sensitive interrupts

Non-maskable user interrupts are a specific form of edge sensitive interrupt sources.

Non-maskable interrupts have dedicated interrupt vectors. The interrupt request flag is cleared automatically when the interrupt is vectored (Figure 52).

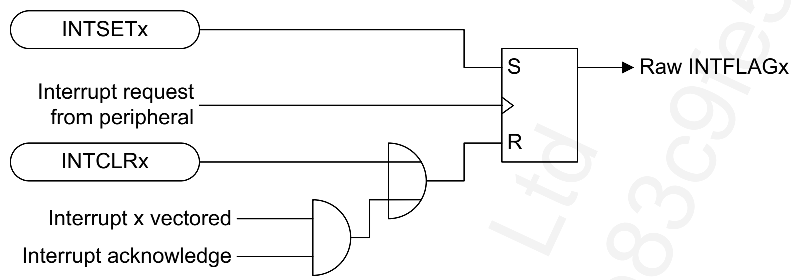


Fig 52. Interrupt request flag for non-maskable user interrupts

2.10.1.1 Interrupt vector addresses

The interrupt vector addresses depend on the interrupt type (Table 98).

Table 98. Interrupt vector addresses

Interrupt source	Address range	Address (word address)
Break interrupt	SYSTEM	0002h
Maskable system interrupt	SYSTEM	0040h
CPU/MMU exception interrupt (user NMI)	SYSTEM	0016h
	USER	000Eh
LF field interrupt (user NMI)	SYSTEM	000Ch
	USER	0006h
Maskable user interrupt	USER	Selectable (INTVEC)

All interrupt sources except the maskable user interrupt are called in SYSTEM mode and have fixed interrupt addresses.

Directly after vectoring a non-maskable user interrupt in SYSTEM mode, a USER call (call back) is generated to return to USER mode and to proceed the program execution at the corresponding interrupt vector address in the USER address range (0006h or 000Eh for the LF or CPU/MMU exception interrupt, respectively).

The maskable user interrupt features a configurable interrupt vector address by use of the special function register INTVEC. This gives the following possibilities:

- Define different interrupt service routines for different applications
- Define different interrupt service routines with different priority schemes (even in one application)
- Allow dynamic switching of interrupt service routines in an application (e.g. to provide different priority schemes)

2.10.2 Interrupt priorities

2.10.2.1 Interrupt request levels

The interrupt controller processes the events from the peripherals and generates an interrupt request with the interrupt request level for every source. All interrupt sources are synchronized to the CPU clock before they generate an interrupt request (Figure 53).

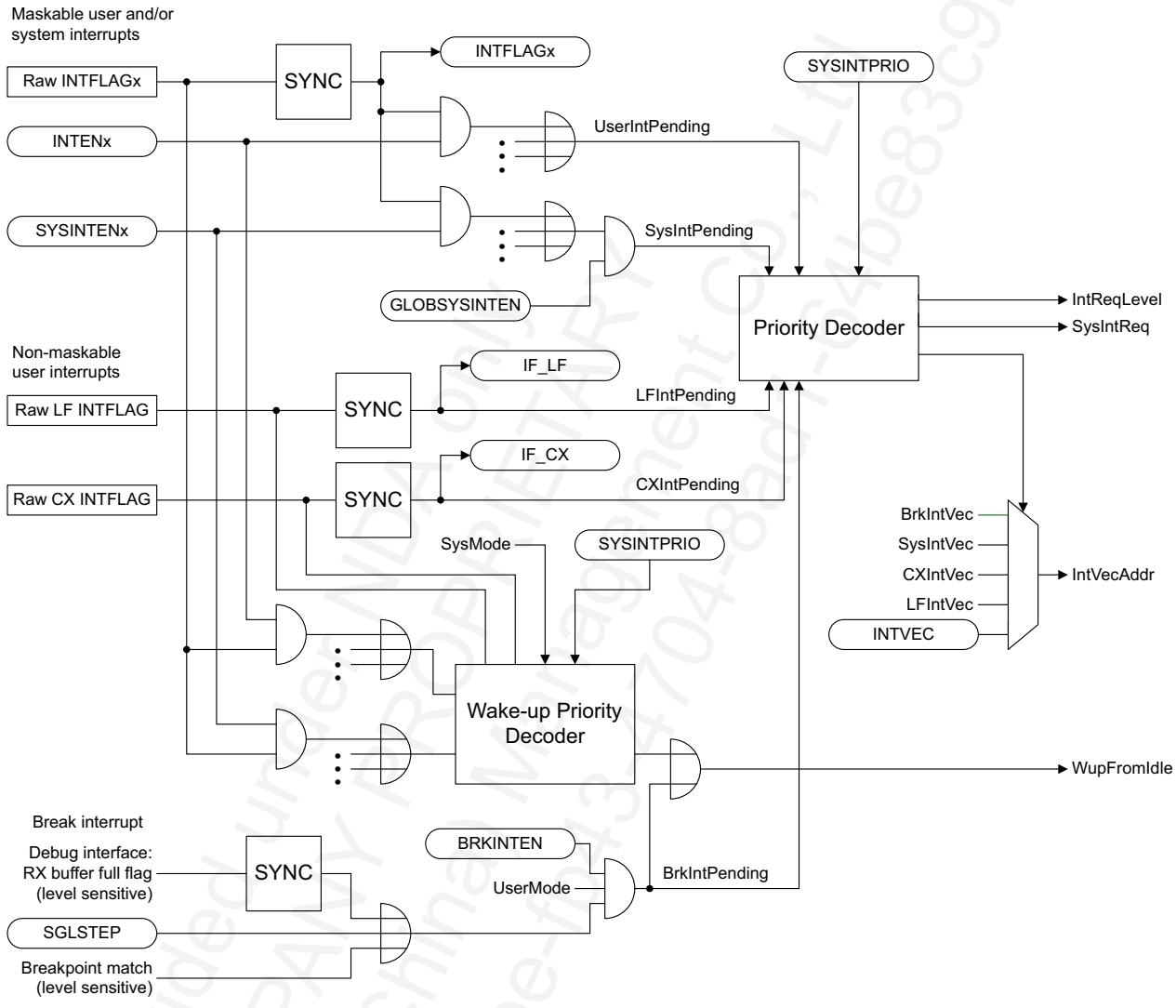


Fig 53. Priority decoding with interrupt controller

Table 99 summarizes the interrupt request levels and their assignment to interrupt events. If more than one interrupt request is pending at the same time the source with the highest request level is selected, independent of the privilege mode (SYSTEM or USER mode).

Table 99. Interrupt request level assignment to interrupt events

Interrupt request level	Source
15	Break interrupt
	Maskable system interrupt (SYSINTPRIO= 11b, GLOBSYSINTEN = 1)
14	CPU/MMU exception interrupt (user NMI)
13	LF field interrupt (user NMI)
12	Reserved for future use
11	Maskable system interrupt (SYSINTPRIO= 10b, GLOBSYSINTEN = 1)
10	Maskable system interrupt (SYSINTPRIO= 01b, GLOBSYSINTEN = 1)
9 to 3	Reserved for future use
2	Maskable user interrupt
1	Maskable system interrupt (SYSINTPRIO= 00b, GLOBSYSINTEN = 1)

System interrupts (except the LF field and CPU/MMU exception interrupts) are usually disabled (i.e. GLOBSYSINTEN = 0). It will be stated explicitly, if any system function makes use of system interrupts.

2.10.2.2 Interrupt priority levels

The responsiveness to hardware interrupt requests is controlled by the interrupt priority level. After device reset the CPU starts with interrupt priority level 15 in SYSTEM mode.

The CPU always operates in a certain interrupt priority level ranging from 0 to 15. An interrupt request is granted, if the hardware interrupt request level is greater than the current interrupt priority level of the CPU (exception: break interrupt, see below).

The following actions are executed when an interrupt is served:

- The current interrupt priority level, the privilege mode (SYSTEM or USER mode), the program counter and the flags are pushed on the stack
- The priority level is set to the new interrupt request level (i.e. it is increased)
- If necessary the privilege mode is changed
- The program counter is set to the provided interrupt vector address

The interrupt priority level increases with every acknowledged interrupt, hence all interrupts with the same or lower priority are inhibited. Consequently, once the interrupt priority level reaches the value 15 all further interrupt requests are ignored.

At the end of an interrupt service routine the command RETI triggers the following operations:

- The content stored at the beginning of the interrupt service routine is popped from the stack (including the stored interrupt priority level and privilege mode)
- The interrupt priority level is set to the stored value
- If necessary the privilege mode is changed
- The program counter is set to the stored value where the program was interrupted.

A RETI command decreases the interrupt priority level unless nested interrupts were used (see Section 2.10.2.3).

The interrupt request level 0 means that no hardware interrupt is pending. Level 0 cannot be used as request level as such an interrupt would never be served.

2.10.2.3 Interrupt priority level adjustment

The interrupt priority level can be changed in the allowed range by the application program with the dedicated command SIL, considering following restrictions dependent on the privilege mode:

- In USER mode the interrupt priority levels can be set to values from 0 to 10. Any attempt to set it to a higher value will yield value 10 instead.
- In SYSTEM mode, all values from 0 to 15 can be selected.

If the interrupt priority level is set to 10, all maskable user interrupts are disabled.

The modification of the interrupt priority level can be used to allow and inhibit interrupts (interrupt nesting).

2.10.2.4 Break interrupt

The break interrupt is active only in USER mode and causes the device to switch to SYSTEM mode immediately. The break interrupt has the highest interrupt request level and is executed independently of the current interrupt priority level (i.e. it is executed even though the interrupt priority level is at its maximum value 15).

The following sources can generate a break interrupt:

- A hardware breakpoint is reached
- The single step bit SINGLESTEP is set
- The monitor and download interface received a command that causes an interruption of the application program in USER mode

Acknowledgement of the break interrupt sets the interrupt priority level to 15.

2.10.2.5 LF field and CPU/MMU exception interrupts

The LF field and CPU/MMU exception non-maskable user interrupts have an interrupt request level (13 and 14 respectively) which are higher than the maximum possible interrupt execution level in USER mode (10). These two interrupt sources are not gated with GLOBSYSINTEN, thus the LF field and CPU/MMU exception interrupts are always vectored when the device is in USER mode.

The LF field and CPU/MMU exception interrupts are vectored in SYSTEM mode. Directly afterwards a USER call (call back) is generated to return the execution to the user program. Although the interrupt request level of the LF field and CPU/MMU exception NMIs are higher than 10 the execution of the USER call is executed with interrupt execution level 10.

Consequently, if the user call was caused by an LF field interrupt it is granted that an emerging CPU/MMU exception interrupt is properly recognized later on (and vice versa).

If the device runs in SYSTEM mode the LF field and CPU/MMU exception interrupts are treated as any other interrupt source and they are only vectored, if the interrupt request level exceeds the current interrupt execution level. An application in SYSTEM mode can therefore select whether an LF field or CPU/MMU interrupt shall be vectored or not.

2.10.3 Interrupt request by software

It is possible to trigger an interrupt request for every interrupt source by software. This could be helpful e.g. during software development in order to support convenient and efficient testing of the interrupt service routines. Every interrupt request flag has two assigned control bits to set (INTSETx) and to clear (INTCLRx) the corresponding interrupt request flag.

For edge sensitive interrupt sources there is no difference whether the interrupt was triggered by the peripheral or by the software. In both cases the application program has to acknowledge the interrupt via bit INTCLRx (unless it was a non-maskable user interrupt).

The software trigger for level sensitive interrupt sources is only supported, if this feature is released by setting the global control bit LINTSWCON. As a level sensitive interrupt does not have a storage element in the interrupt controller a parallel flip-flop is necessary to generate an interrupt request by software. The output of this flip-flop is logically ORed to the genuine level sensitive interrupt source. In contrast to the normal behavior of a level sensitive interrupt the software triggered interrupt request shall be acknowledged via the corresponding bit INTCLRx. Please note that bit INTCLRx does not have any influence on the genuinely generated interrupt request from the peripheral.

2.10.4 Software interrupts

Software interrupts are initiated via a system call (SYS command) or user call (USR command) and are not affected by the current interrupt priority level, thus they are always executed. Software interrupts allow switching the privilege mode (SYSTEM or USER mode).

Software interrupts influence the interrupt priority level dependent on the privilege mode.

2.10.4.1 USER mode, execution of a system call (SYS)

- The privilege mode changes to SYSTEM mode
- The interrupt priority level is set to 15

2.10.4.2 USER mode, execution of a user call (USR)

- The privilege mode and the priority level do not change

2.10.4.3 SYSTEM mode, execution of a system call (SYS)

- The privilege mode and the priority level do not change.

2.10.4.4 SYSTEM mode, execution of a user call (USR)

- The privilege mode changes to USER mode
- The interrupt priority level is set to 10

User calls in USER mode and system calls in SYSTEM mode are handled like normal call routines with the difference that these routines shall finish with a RETI instead of a normal RET command.

2.10.5 Wake-up from IDLE mode

The wake-up from IDLE mode is controlled by the interrupt controller. Even if the interrupts are globally disabled, it is possible to select the wake-up from IDLE mode function. Once the CPU is in IDLE mode it resumes operation as soon as the wake-up signal becomes active.

The wake-up from IDLE mode is controlled with the interrupt enable and system interrupt enable bits. A wake-up from IDLE mode is generated under the following circumstances:

- The device is in USER mode and a source is pending, which is enabled by its (user) interrupt enable bit
- The device is in USER mode and a non-maskable user interrupt is pending
- The device is in USER mode and a break interrupt is pending
- The device is in SYSTEM mode and a source is pending, which is enabled by its system interrupt enable bit
- A source is pending which generates an interrupt (mode independent, but dependent on the current interrupt priority level and interrupt request level)

The bit GLOBSYSINTEN has no influence on the wake-up from IDLE mode when the device operates in SYSTEM mode. However, it disables all system interrupts also in USER mode, thus in USER mode a pending system interrupt source will not cause a wake-up from IDLE mode.

If more than one wake-up source is selected or either system interrupts in USER mode or user interrupts in SYSTEM mode can occur, it is recommended to use a safe routine for the invocation of the IDLE mode where the interesting interrupt flag is checked additionally.

Example: The routine uses the IDLE mode in USER mode safely although a system interrupt is enabled. Even if this routine is interrupted, it will work as intended and will not finish the routine prematurely.

1. `INTCLR0.val = 0x08;`
2. `while ((INTFLAG0.val & 0x08) == 0 ) go_idle();`

2.10.6 System and user stack

The NCF29A1 / NCF29A2 has a system and a user stack. If the device executes in SYSTEM mode all data is pushed on and popped from the system stack. The same applies for the user stack if the device is in USER mode.

Every interrupt invocation stores 2 words on the stack, the return address and the flags (including the system mode flag and the interrupt priority level).

If an interrupt request causes a change of the privilege mode, the return address is pushed on the current stack and the flags are pushed on the target stack (e.g. if a USR call is executed in SYSTEM mode, the return address is pushed on the system stack and the flags are pushed on the user stack).

If a return from interrupt is executed, the flags are popped from the current stack. Dependent on the popped system mode flag the controller might perform a privilege mode switch and then pops the return address from the target stack (e.g. if the USR call finishes with a RETI and the device branches back to SYSTEM mode, the return address is retrieved from the system stack again).

2.10.7 Registers

The register groups 0 to 2 of the interrupt controller allow either byte or word access (Table 100). For register group 3, only byte access is meaningful.

Table 100. Word and byte access to interrupt controller registers

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
INTENW0	INTEN1	INTEN0
INTENW1	INTEN2	INTEN1
SYSINTENW0	SYSINTEN1	SYSINTEN0
INTFLAGW0	INTFLAG1	INTFLAG0
INTFLAGW1	INTFLAG2	INTFLAG1
INTSETW0	INTSET1	INTSET0
INTSETW1	INTSET2	INTSET1
INTCLRW0	INTCLR1	INTCLR0
INTCLRW1	INTCLR2	INTCLR1
INTVEC	INTVECH	INTVECL

2.10.7.1 Interrupt control register INTCON

The INTCON register defines the behavior of the system interrupts and is write accessible in SYSTEM mode only.

Table 101. Interrupt control register INTCON (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	LINTSWCON	R/W	R		Software control of level sensitive interrupts
				0	Software control of level sensitive interrupts disabled
				1	interrupt flags controlled by application
6	GLOBSYSINTEN	R/W	R		Global system interrupt enable
				0	System interrupts are disabled
				1	System interrupts are enabled
5 and 4	SYSINTPRIO[1:0]	R/W	R		System Interrupt Priority
				00	System interrupts have lowest priority. System interrupts can be disabled in USER mode.
				01	System interrupts have higher priority than maskable user interrupts but lower priority than the non-maskable user interrupt. System interrupts can be disabled in USER mode.
				10	System interrupts have higher priority than maskable user interrupts but lower priority than the non-maskable user interrupt. System interrupts cannot be disabled in USER mode.
				11	System interrupts have highest priority. System interrupts cannot be disabled in USER mode.
3 to 0	RFU	R0/W0	R		Reserved for future use

LINTSWCON, Software control of level sensitive interrupts

If this bit is set to '1', the interrupt flags of level sensitive interrupt sources can be controlled by the application via the corresponding interrupt set and interrupt clear bit.

SYSINTPRIO[1:0], System interrupt priority

If an interrupt source has the user interrupt enable flag and the system interrupt enable flag set to '1' simultaneously, it depends on the settings of GLOBSYSINTEN and SYSINTPRIO whether this interrupt is served as a user or system interrupt.

2.10.7.2 Interrupt enable registers INTENx

The INTENx registers control the selection of user interrupts and sources for wake-up from IDLE mode. These registers are also used to accomplish interrupt masking.

Table 102. User interrupt enable register INTEN0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	R0/W0		Reserved for future use
6	IE_ALTPORT	R/W		Alternative port interrupt
			0	Interrupt disabled
			1	Interrupt enabled
5	IE_T1CAP	R/W		Timer 1 capture interrupt
			0	Interrupt disabled
			1	Interrupt enabled
4	IE_T1CMP	R/W		Timer 1 compare interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_T0	R/W		Timer 0 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	IE_PORT	R/W		Port interrupt
			0	Interrupt disabled
			1	Interrupt enabled
1	IE_CXNMI	R/W		CPU/MMU exception non-maskable interrupt
			0	Generate device reset
			1	Generate non-maskable user interrupt
0	IE_LFNMI	R/W		LF non-maskable interrupt
			0	Generate device reset
			1	Generate non-maskable user interrupt

IE_CXNMI, CPU/MMU exception non-maskable interrupt enable

The bit IE_CXNMI is intended to select whether a CPU/MMU exception generates a device reset or a non-maskable user interrupt request.

IE_LFNMI, LF non-maskable interrupt enable

The bit IE_LFNMI is intended to select whether an emerging LF field generates a device reset or a non-maskable user interrupt request.

Table 103. User interrupt enable register INTEN1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5	IE_RNG	R/W		Random number generator interrupt
			0	Interrupt disabled
			1	Interrupt enabled

Table 103. User interrupt enable register INTEN1 (reset value 00h)

Bit	Symbol	Access	Value	Description
4	IE_AES	R/W		AES calculation unit interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_ADC	R/W		ADC interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	RFU	R/W0		Reserved for future use
1	IE_ULP	R/W		ULP EEPROM interrupt
			0	Interrupt disabled
			1	Interrupt enabled
0	IE_IIU	R/W		Immobilizer interface unit interrupt
			0	Interrupt disabled
			1	Interrupt enabled

Table 104. User interrupt enable register INTEN2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IE_VBATBRN	R/W		VBAT brownout monitor interrupt
			0	Interrupt disabled
			1	Interrupt enabled
6	IE_MSI	R/W		Motion sensor interface interrupt
			0	Interrupt disabled
			1	Interrupt enabled
5	RFU	R0/W0		Reserved for future use
4	IE_T2	R/W		Timer 2 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_SP1	R/W		SPI 1 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	IE_SP0	R/W		SPI 0 interrupt
			0	Interrupt disabled
			1	Interrupt enabled
1	IE_PP	R/W		LF active preprocessor interrupt
			0	Interrupt disabled
			1	Interrupt enabled
0	IE_IT	R/W		Interval timer and real time clock interrupt
			0	Interrupt disabled
			1	Interrupt enabled

Table 105. User interrupt enable register INTEN3 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IE_TXFIN	R/W		UHF transmission finished interrupt
			0	Interrupt disabled
			1	Interrupt enabled
6	IE_TXBE	R/W		UHF transmit buffer empty interrupt
			0	Interrupt disabled
			1	Interrupt enabled
5	IE_PAILIM	R/W		UHF PA current limiter interrupt
			0	Interrupt disabled
			1	Interrupt enabled
4	IE_PARDY	R/W		UHF PA ready interrupt
			0	Interrupt disabled
			1	Interrupt enabled
3	IE_PLLUNLOCK	R/W		UHF PLL unlocked interrupt
			0	Interrupt disabled
			1	Interrupt enabled
2	IE_PLLLOCK	R/W		UHF PLL locked interrupt
			0	Interrupt disabled
			1	Interrupt enabled
1	IE_VCOCAL	R/W		UHF PLL VCO calibration finished interrupt
			0	Interrupt disabled
			1	Interrupt enabled
0	IE_XORDY	R/W		UHF crystal oscillator ready interrupt
			0	Interrupt disabled
			1	Interrupt enabled

2.10.7.3 System interrupt enable register SYSINTENx

These registers control the selection of system interrupts and sources for wake-up from IDLE mode. Write access is granted only in SYSTEM mode.

Table 106. System interrupt enable register SYSINTEN0 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7	SIE_ST0	R/W	R		System Timer 0 interrupt
				0	Interrupt disabled
				1	Interrupt enabled
6	RFU	R0/W0	R		Reserved for future use
5	SIE_T1CAP	R/W	R		Timer 1 capture system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
4	SIE_T1CMP	R/W	R		Timer 1 compare system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
3	SIE_T0	R/W	R		Timer 0 system interrupt
				0	Interrupt disabled
				1	Interrupt enabled
2 to 0	RFU	R0/W0	R		Reserved for future use

Table 107. System interrupt enable register SYSINTEN1 (reset value 00h)

Bit	Symbol	Access SYSTEM mode	Access USER mode	Value	Description
7 and 6	RFU	R0/W0	R		Reserved for future use
5	SIE_RNG	R/W	R		Random number generator interrupt
				0	Interrupt disabled
				1	Interrupt enabled
4	SIE_AES	R/W	R		AES calculation unit interrupt
				0	Interrupt disabled
				1	Interrupt enabled
3	SIE_ADC	R/W	R		ADC interrupt
				0	Interrupt disabled
				1	Interrupt enabled
2	RFU	R/W0	R		Reserved for future use
1	SIE_ULP	R/W	R		ULP EEPROM interrupt
				0	Interrupt disabled
				1	Interrupt enabled
0	SIE_IIU	R/W	R		Immobilizer interface unit interrupt
				0	Interrupt disabled
				1	Interrupt enabled

2.10.7.4 Interrupt request flag registers INTFLAGx

The registers INTFLAGx signal interrupt requests pending that were generated by the corresponding peripheral. These registers give read access to the synchronized interrupt request flags. Any write access is ignored.

Table 108. Interrupt request flag register INTFLAG0 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_ST0	R		System timer 0 interrupt
			0	No interrupt request
			1	Interrupt request
6	IF_ALTPORT	R		Alternative port interrupt
			0	No interrupt request
			1	Interrupt request
5	IF_T1CAP	R		Timer 1 capture interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_T1CMP	R		Timer 1 compare interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_T0	R		Timer 0 interrupt
			0	No interrupt request
			1	Interrupt request
2	IF_PORT	R		Port interrupt
			0	No interrupt request
			1	Interrupt request
1	IF_CX	R		CPU/MMU exception non-maskable interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_LF	R		LF field non-maskable interrupt
			0	No interrupt request
			1	Interrupt request

Table 109. Interrupt request flag register INTFLAG1 (reset value XXh)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0		Reserved for future use
5	IF_RNG	R		Random number generator interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_AES	R		AES calculation unit interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_ADC	R		ADC interrupt
			0	No interrupt request
			1	Interrupt request

Table 109. Interrupt request flag register INTFLAG1 (reset value XXh)

Bit	Symbol	Access	Value	Description
2	RFU	R		Reserved for future use
1	IF_ULP	R		ULP EEPROM interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_IIU	R		Immobilizer interface unit interrupt
			0	No interrupt request
			1	Interrupt request

Table 110. Interrupt request flag register INTFLAG2 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_VBATBRN	R		VBAT brownout monitor interrupt
			0	No interrupt request
			1	Interrupt request
6	IF_MSI	R		Motion sensor interface interrupt
			0	No interrupt request
			1	Interrupt request
5	RFU	R0		Reserved for future use
4	IF_T2	R		Timer 2 interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_SP1	R		SPI 1 interrupt
			0	No interrupt request
			1	Interrupt request
2	IF_SP0	R		SPI 0 interrupt
			0	No interrupt request
			1	Interrupt request
1	IF_PP	R		LF active preprocessor interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_IT	R		Interval timer and real time clock interrupt
			0	No interrupt request
			1	Interrupt request

Table 111. Interrupt request flag register INTFLAG3 (reset value XXh)

Bit	Symbol	Access	Value	Description
7	IF_TXFIN	R		UHF transmission finished interrupt
			0	No interrupt request
			1	Interrupt request
6	IF_TXBE	R		UHF transmit buffer empty interrupt
			0	No interrupt request
			1	Interrupt request
5	IF_PAILIM	R		UHF PA current limiter interrupt
			0	No interrupt request
			1	Interrupt request
4	IF_PARDY	R		UHF PA ready interrupt
			0	No interrupt request
			1	Interrupt request
3	IF_PLLUNLOCK	R		UHF PLL unlocked interrupt
			0	No interrupt request
			1	Interrupt request
2	IF_PLLLOCK	R		UHF PLL locked interrupt
			0	No interrupt request
			1	Interrupt request
1	IF_VCOCAL	R		UHF VCO calibration finished interrupt
			0	No interrupt request
			1	Interrupt request
0	IF_XORDY	R		UHF crystal oscillator ready interrupt
			0	No interrupt request
			1	Interrupt request

2.10.7.5 Interrupt set registers INTSETx

The INTSETx registers can be used to trigger a corresponding interrupt request by software. Reading of these registers is not supported and will yield '0'.

Table 112. Interrupt set register INTSET0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_ST0	R0/W		System Timer 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	IS_ALTPORT	R0/W		Alternative port interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
5	IS_T1CAP	R0/W		Timer 1 capture interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_T1CMP	R0/W		Timer 1 compare interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_T0	R0/W		Timer 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	IS_PORT	R0/W		Port interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
1	IS_CX	R0/W		CPU/MMU non-maskable interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_LF	R0/W		LF non-maskable interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

Table 113. Interrupt set register INTSET1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5	IS_RNG	R0/W		Random number generator interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_AES	R0/W		AES calculation unit interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_ADC	R0/W		ADC interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	RFU	R0/W0		Reserved for future use

Table 113. Interrupt set register INTSET1 (reset value 00h)

Bit	Symbol	Access	Value	Description
1	IS_ULP	R0/W		ULP EEPROM interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_IIU	R0/W		Immobilizer interface unit interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

Table 114. Interrupt set register INTSET2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_VBATBRN	R0/W		VBAT brownout monitor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	IS_MSI	R0/W		Motion sensor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
5	RFU	R0/W0		Reserved for future use
4	IS_T2	R0/W		Timer 2 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_SP1	R0/W		SPI 1 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	IS_SP0	R0/W		SPI 0 interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
1	IS_PP	R0/W		LF active preprocessor interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_IT	R0/W		Interval timer and real time clock interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

Table 115. Interrupt set register INTSET3 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IS_TXFIN	R0/W		UHF transmission finished interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
6	IS_TXBE	R0/W		UHF transmit buffer empty interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
5	IS_PAILIM	R0/W		UHF PA current limiter interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
4	IS_PARDY	R0/W		UHF PA ready interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
3	IS_PLLUNLOCK	R0/W		UHF PLL unlocked interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
2	IS_PLLLOCK	R0/W		UHF PLL locked interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
1	IS_VCOCAL	R0/W		UHF PLL VCO calibration finished interrupt
			0	Interrupt request unchanged
			1	Set interrupt request
0	IS_XORDY	R0/W		UHF crystal oscillator ready interrupt
			0	Interrupt request unchanged
			1	Set interrupt request

2.10.7.6 Interrupt clear registers INTCLRx

The INTCLRx registers can clear a corresponding interrupt request by software. Reading of these registers is not supported and will yield '0'.

Table 116. Interrupt clear register INTCLR0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_ST0	R0/W		System timer 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	IC_ALTPORT	R0/W		Alternative port interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
5	IC_T1CAP	R0/W		Timer 1 capture interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_T1CMP	R0/W		Timer 1 compare interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_T0	R0/W		Timer 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	IC_PORT	R0/W		Port interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
1	IC_CX	R0/W		CPU/MMU exception non-maskable interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_LF	R0/W		LF non-maskable interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

Table 117. Interrupt clear register INTCLR1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5	IC_RNG	R0/W		Random number generator interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_AES	R0/W		AES calculation unit interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_ADC	R0/W		ADC interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	RFU	R0/W0		Reserved for future use

Table 117. Interrupt clear register INTCLR1 (reset value 00h)

Bit	Symbol	Access	Value	Description
1	IC_ULP	R0/W		ULP EEPROM interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_IIU	R0/W		Immobilizer interface unit interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

Table 118. Interrupt clear register INTCLR2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_VBATBRN	R0/W		VBAT brownout monitor interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	IC_MSI	R0/W		Motion sensor interface interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
5	RFU	R0/W0		Reserved for future use
4	IC_T2	R0/W		Timer 2 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_SP1	R0/W		SPI 1 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	IC_SP0	R0/W		SPI 0 interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
1	IC_PP	R0/W		LF active preprocessor interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_IT	R0/W		Interval timer and real time clock interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

Table 119. Interrupt clear register INTCLR3 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	IC_TXFIN	R0/W		UHF transmission finished interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
6	IC_TXBE	R0/W		UHF transmit buffer empty interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
5	IC_PAILIM	R0/W		UHF PA current limiter interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
4	IC_PARDY	R0/W		UHF PA ready interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
3	IC_PLLUNLOCK	R0/W		UHF PLL unlocked interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
2	IC_PLLLOCK	R0/W		UHF PLL locked interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
1	IC_VCOCAL	R0/W		UHF PLL VCO calibration finished interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request
0	IC_XORDY	R0/W		UHF crystal oscillator ready interrupt
			0	Interrupt request unchanged
			1	Clear interrupt request

2.10.7.7 User interrupt vector address INTVEC

The INTVEC register features a configurable interrupt vector address for the maskable user interrupt.

Table 120. User interrupt vector address INTVEC (reset value 0040h)

Bit	Symbol	Access	Value	Description
15 to 8	INTVECH [7:0]	R/W		User interrupt vector address High Byte (MSByte)
7 to 0	INTVECL [7:0]	R/W		User interrupt vector address Low Byte (LSByte)

2.11 Timer/Counter 0, 2

Timer/Counter 0 and Timer/Counter 2 are identical. The following description takes Timer/Counter 0 as reference. All descriptions are also valid for Timer/Counter 2 if T0 is replaced by T2 in names and figures.

Timer/Counter 0/2 is a 16 bit timer/counter with 12 bit pre-scaler and can operate as interval and event counter, as digital modulator or as clock divider. Timer 0/2 is also suitable as alternative clock source for the immobilizer interface unit and digital modulator.

Timer 0/2 has two operating modes, auto-reload mode and single shot mode, which are selected by bit T0SGL. For auto-reload mode, a 16 bit reload register is provided (see Figure 54).

Different clock sources can be applied (RCCLK/2 , XCLK, TMUX0CLK, TMUX1CLK). The timer can run with undivided clock to achieve best possible resolution even with slow clock sources.

If Timer 0/2 reaches the zero value, an interrupt is generated and a control line or I/O pin can be set, cleared or toggled. The output of Timer 0/2 can be used to provide the divided clock output at an I/O port, as capture input for Timer 1 or as clock source for a digital modulator (realized in software).

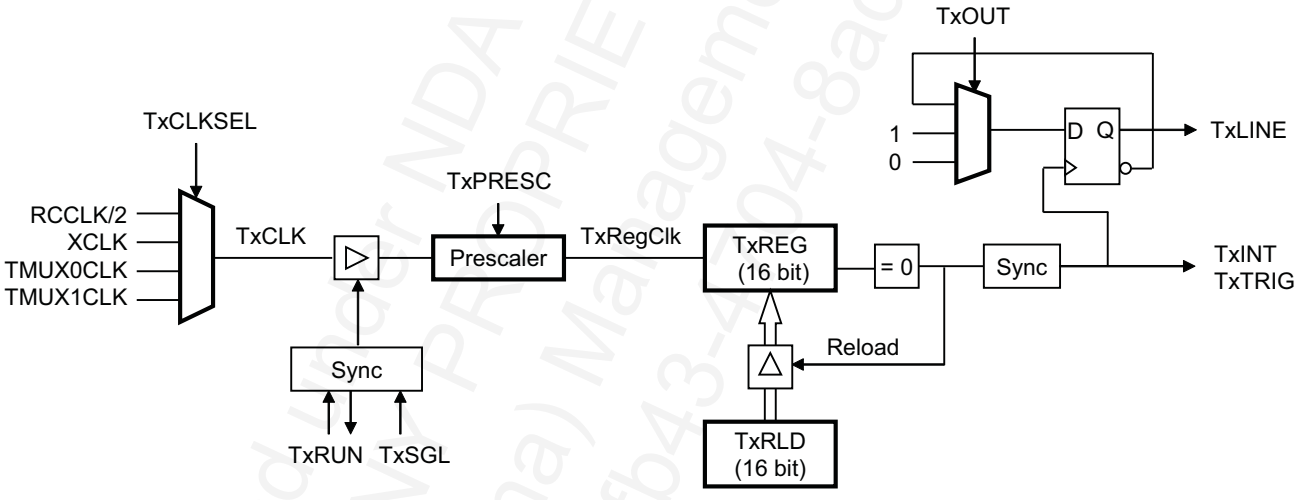


Fig 54. Block diagram of Timer 0/2

The timer starts by loading the reload value from register TxRLD into register TxREG. Afterwards, it counts down automatically. Reaching the zero value, timer register TxREG is reloaded with the value from reload register TxRLD, an interrupt request is generated and other peripheral functions are triggered.

The timer is clocked with the output of the pre-scaler. The clock for the timer register is:

$$\mathrm{TxRegClk} = 2^{TxPRESC} \cdot TxCLK, \quad for \quad TxPRESC < 13 \tag{27}$$

The timer interval becomes:

$$TxINTERVAL = 2 \cdot TxCLK, \ for\ TxPRESC = 0\ and\ TxRDL = 0 \tag{28}$$

$$TxINTERVAL = (TxRDL + 1) \cdot TxRegClk, \quad for\ all\ other\ settings \tag{29}$$

2.11.1 Registers

2.11.1.1 Timer 0/2 register TxREG

Timer 0/2 supports read access to the timer register. The content of the timer register is not buffered or synchronized. Therefore, reading of TxREG is only recommended when the timer is stopped (TxRUN = 0). When the timer is running reading of TxREG can generate unstable and wrong values as the timer value is not necessarily settled when reading takes place.

Write access to timer register TxREG is not supported.

Table 121. Timer 0/2 Register TxREG (reset value xx_xxh)

Bit	Symbol	Access	Value	Description
15 to 8	TxREGH [7:0]	R		Timer 0/2 Register High Byte (MSByte)
7 to 0	TxREGL [7:0]	R		Timer 0/2 Register Low Byte (LSByte)

2.11.1.2 Timer 0/2 control register TxCON0

Timer 0/2 is operated and controlled by Timer 0/2 Control Registers 0 and 1.

Table 122. Timer 0/2 Control Register TxCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	TxOUT [1:0]	R/W		Timer 0/2 output line configuration
			00	Value unchanged, output line flip-flop after timer reset 0
			01	Value is set to ‘0’, output line flip-flop after timer reset 0
			10	Value toggles, output line flip-flop after timer reset 0
			11	Value is set to ‘1’, output line flip-flop after timer reset 1
5 to 3	RFU	R0/W0		Reserved for future use
2	TxSGL	R/W		Timer 0/2 single shot
			0	Timer 0/2 is configured in auto reload mode
			1	Timer 0/2 is configured in single shot mode
1	TxRST	R0/W		Timer 0/2 reset
			0	No effect
			1	Timer reset
0	TxRUN	R/W		Timer 0/2 run
			0	Timer 0/2 is stopped
			1	Timer 0/2 is running. While reading, a 1 can also indicate the synchronization phase for start or stop

TxOUT[1:0], Timer 0/2 output line configuration

Timer 0/2 has an output line flip-flop driving the signal TxLINE. The behavior of this signal can be configured with the output line configuration bits TxOUT. The content of the output flip-flop is updated every time the timer register reaches zero. The initial value of the output line flip-flop after a reset of Timer 0/2 can also be controlled with TxOUT.

If bit TxOUT[0] is set, it is possible to generate a synchronized bit data stream by writing the desired data to bit TxOUT[1]. The output line is then updated with the new data bit when the timer register reaches the value zero for the next time.

The selection of TxOUT = 10 allows the generation of a divided clock output with 50 % duty cycle.

TxSGL, Timer 0/2 single shot

Timer 0/2 has two different operating modes: an auto-reload mode and a single shot mode. If bit T0SGL is set, Timer 0/2 operates in single shot mode. If the timer is started by setting the bit T0RUN to '1' the counter starts decrementing until the timer register reaches zero. Simultaneously an interrupt is generated and the timer stops automatically. This clears bit TxRUN and reloads the timer register TxREG. The bit TxSGL itself is not influenced and stays '1'.

TxRST, Timer 0/2 reset

The reset bit TxRST can be used to generate an asynchronous reset of Timer 0/2 comprising the prescaler, the synchronization logic and the output line flip-flop. Moreover the current content of the reload register TxRLD is loaded into timer register TxREG. A '1' shall be written to TxRST to execute the reset. Writing a '0' has no effect and reading of TxRST always yields '0'.

Launching a reset when the timer is running causes the timer to stop immediately and TxRUN is cleared. If TxRST and TxRUN are set simultaneously the reset bit has priority and the timer does not start.

TxRUN, Timer 0/2 run

Timer 0/2 can be started and stopped with the control bit TxRUN. Reading TxRUN gives the current status of Timer 0/2. If a '1' is written to TxRUN the timer is enabled and it starts counting with the rising edge of TxCLK. Writing a '0' to TxRUN forces the timer to stop operation. Every change of signal TxRUN is synchronized to TxCLK before it becomes effective. Reading of TxRUN yields '1' if the timer is running and during the synchronization phase to start and stop the timer.

2.11.1.3 Timer 0/2 control register TxCON1

Timer 0/2 control register 1 stores the selection of the prescaler value TxPRESC[3:0] and the used clock source TxCLKSEL[1:0].

The control bits in register TxCON1 are not buffered nor synchronized to the timer clock TxCLK. The content of register TxCON1 shall only be modified, if the timer is stopped (TxRUN = 0). Any alteration of TxCON1 when the timer is running can cause unpredictable behavior.

Table 123. Timer 0/2 Control Register TxCON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU[1:0]	R0/W0		Reserved for future use
5 and 4	TxCLKSEL[1:0]	R/W		Timer 0/2 clock source selection
			00	RCCLK/2 (8 MHz nominal)
			01	External clock, XCLK
			10	Output of timer source multiplexer 0, TMUX0CLK
			11	Output of timer source multiplexer 1, TMUX1CLK
3 to 0	TxPRESC[3:0]	R/W		Timer 0/2 prescaler selection
			0000	TxREGClk = 1 * TxCLK
			0001	TxREGClk = 2 * TxCLK
			0010	TxREGClk = 4 * TxCLK
			0011	TxREGClk = 8 * TxCLK
			0100	TxREGClk = 16 * TxCLK
			0101	TxREGClk = 32 * TxCLK
			0110	TxREGClk = 64 * TxCLK
			0111	TxREGClk = 128 * TxCLK
			1000	TxREGClk = 256 * TxCLK
			1001	TxREGClk = 512 * TxCLK
			1010	TxREGClk = 1024 * TxCLK
			1011	TxREGClk = 2048 * TxCLK
			1100	TxREGClk = 4096 * TxCLK
			1101 - 1111	RFU

TxCLKSEL[1:0], Timer 0/2 clock source selection

The Timer 0/2 clock source selection selects the clock source.

TxPRESC[3:0], Timer 0/2 prescaler selection

The Timer 0/2 prescaler selection selects the clock speed for the timer register according to Equation 27.

2.11.1.4 Timer 0/2 reload register TxRLD

The reload register TxRLD is used to set the time-out interval of Timer 0/2. The behavior of any write access to register TxRLD depends on the current state of Timer 0/2.

If the timer is stopped (TxRUN = 0) any write access to TxRLD updates also the timer register with the new value and clears the prescaler. When the timer is started, the first interval corresponds to the newly selected time-out.

If the timer is running (TxRUN = 1), the reload register itself is not buffered and its value is taken to reload the timer register. Writing to register TxRLD at the same moment when the timer register is reloaded can cause unpredictable behavior. Therefore, when the timer is running the application shall only write the reload register if it is ensured that the write access is finished prior to the next timer underflow.

The reload register shall not be written in the time window from the request to stop the timer (setting TxRUN from '1' to '0') until the timer has stopped. If the timer is stopped by setting the reset bit TxRST, there is no limitation.

Table 124. Timer 0/2 Reload Register TxRLD (reset value xx_xxh)

Bit	Symbol	Access	Value	Description
15 to 8	TxRLDH [7:0]	R/W		Timer 0/2 Compare Register High Byte (MSByte)
7 to 0	TxRLDL [7:0]	R/W		Timer 0/2 Compare Register Low Byte (LSByte)

It is possible to use Timer 0/2 as 8 bit instead of a 16 bit counter in order to optimize the code density of the software. For this, register TxRLDH has to be set to zero once and the time-out interval is determined by setting TxRLDL.

2.12 Timer/Counter 1

Timer 1 is an 8/16 bit timer with 12 bit prescaler and is intended as interval and event counter for general purpose applications, as demodulator or signal generator and modulator. Together with Timer 0 it can be used as versatile clock measurement and/or trimming unit. Timer 1 features four operating modes (see Table 125).

Table 125. Operating Modes

Symbol	Addressed section
0	16 bit timer register with 16 bit compare and 16 bit capture register
1	Mode 0 in single shot operation
2	8 bit timer register with two 8 bit compare and two 8 bit capture registers
3	8 bit timer register with one 8 bit compare register, two 8 bit capture registers and one 8 bit guard time register for capture event processing

The input signal which is used as capture source is sampled with the gated timer clock T1CLK. Two samples are necessary to decide whether the input has a rising or falling edge. Thus, the low and the high pulse of this signal shall be longer than 1/T1CLK in order to be properly processed.

When selected, the capture mechanism is only active, if the timer is running. The first sample after start is discarded and the capture logic is initialized instead, i.e. no capture event will be generated, even if the first sample after start is different to the last sample of the previous run.

In all modes, an interrupt is generated if a compare event or a capture event is generated. Further, a reset upon capture and/or compare event is selectable. A capture event can be triggered on the signals rising edge, falling edge or on both signal edges, dependent on the configuration.

2.12.1 Modes

2.12.1.1 Mode 0

In Mode 0 Timer 1 is a synchronous 16 bit timer / counter with 12 bit prescaler, providing a 16 bit compare and a 16 bit capture register. The timer is operating continuously in auto reload mode, thus allowing generating a divided clock output at an I/O port. On a timer event, a control line or an I/O pin can be set, cleared or toggled (see Figure 55).

The timer register T1REG is implemented as incrementing counter and its content is continuously compared to the buffered compare value T1CMPSync. If both registers match an interrupt request is generated and the peripheral functions are triggered.

T1REG is cleared automatically, if selected. The compare register T1CMP has an internal synchronization stage, ensuring safe operation even if the value of T1CMP is changed when the timer is running.

The timer register is clocked with the output of the prescaler. The clock for the timer register is:

$$T1RegClk = 2^{T1PRESC} \cdot T1CLK, \ for \ T1PRESC < 13 \quad (30)$$

The timer interval depends on the settings of T1RSTCAP and T1RSTCMP. For interval generation the setting T1RSTCAP = 0 and T1RSTCMP = 1 is recommended. In this case the interval yields:

$$T1INTERVAL = (T1CMP + 1) \cdot T1RegClk, \text{ for } T1PRESC \neq 0 \quad (31)$$

$$T1INTERVAL = 2 \cdot T1CLK, \text{ for } T1PRESC = 0 \text{ and } T1CMP = 0 \quad (32)$$

A capture interrupt is triggered, if T1CAP is loaded due to an external event.

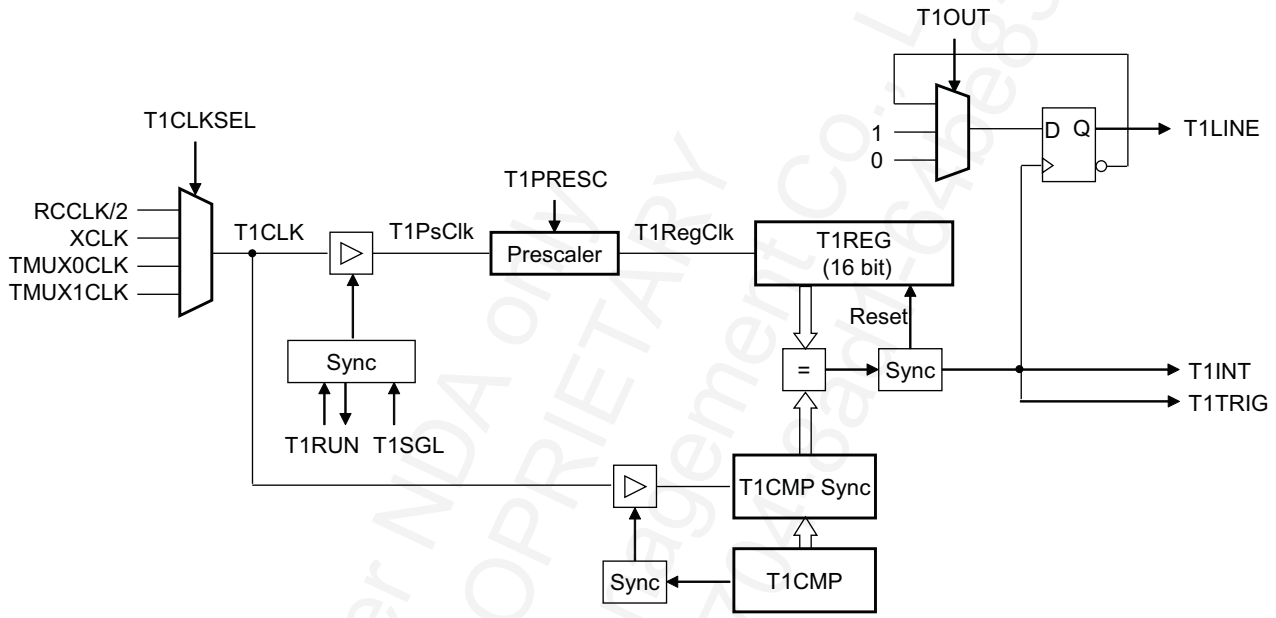


Fig 55. Block diagram of Timer 1 configured in Mode 0 and 1

2.12.1.2 Mode 1

Mode 1 has the same properties as Mode 0 with the exception that the timer automatically stops when the first compare match occurs. If bit T1RSTCMP is set, the timer register is cleared when the timer stops.

2.12.1.3 Mode 2

In Mode 2, Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

Mode 2 is intended to generate flexible bit sequences and PWM signals. Both 8 bit timer registers T1REGL and T1REGH run in parallel. It is recommended to clear the timer register prior to start to ensure that both timer registers contain the same value (see Figure 56).

With the two compare registers T1CMPL and T1CMPH it is possible to select two different values. When register T1REGH matches T1CMPH the output line T1LINE is set, whereas it is cleared upon a match between T1REGL and T1CMPL. If bit T1RSTCMP is set, it is possible to generate a PWM signal with variable pulse length and duty cycle.

A match between T1REGL and T1CMPL generates a compare interrupt request.

If both registers T1CMPL and T1CMPH match at the same time T1CMPL has priority. The reset signal upon compare is derived from T1REGL for both timer registers.

The capture interrupt is generated, if T1CAPL is loaded.

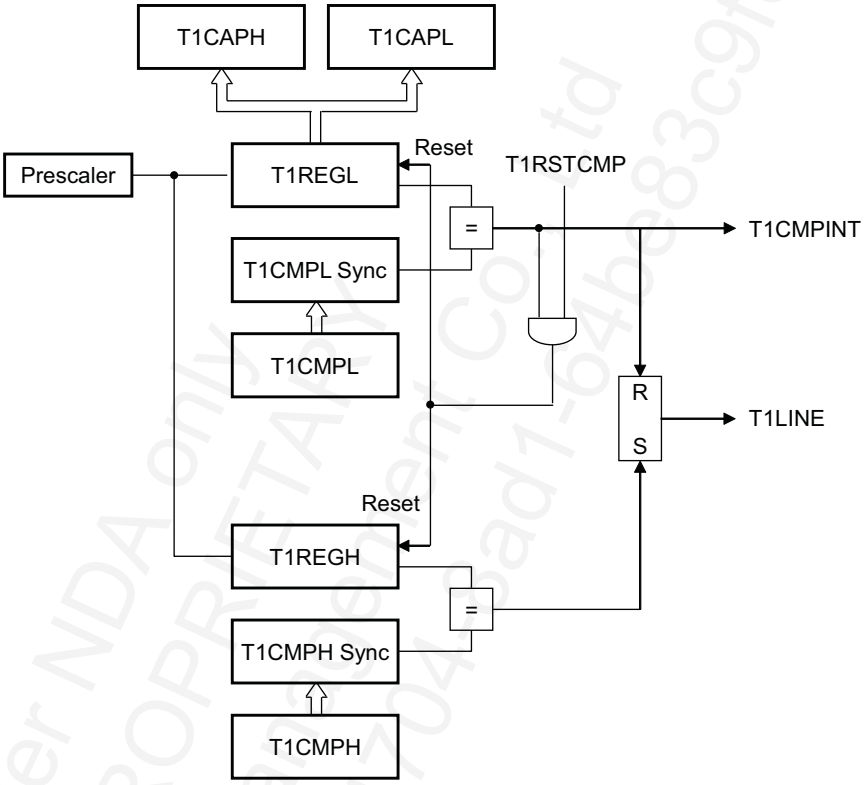


Fig 56. Block diagram of Timer 1 configured in Mode 2

It is possible to generate a pulse position like bit sequence by use of the output signal of an additional timer as capture source. If the reset upon capture feature is used this defines the period. With T1CMPL and T1CMPH it is possible to place a single pulse within this interval.

2.12.1.4 Mode 3

As in Mode 2, in Mode 3 Timer 1 is operating as 8 bit timer / counter with 12 bit prescaler, providing two 8 bit compare and two 8 bit capture registers.

The capture event processing with programmable guard time is useful for signal de-spiking and debouncing as well as for convenient signal demodulation.

The timer is running in 8 bit mode with T1REGL as main timer register. Both capture registers T1CAPL and T1CAPH are connected to T1REGL. A match between T1REGL and T1CMPL generates a compare interrupt request. A capture interrupt is generated, if T1CAPL is loaded. With the help of the two capture registers continuous pulse interval, pulse width and duty cycle measurements can be realized, allowing the implementation of an efficient pulse width demodulator with time-out notification (see Figure 57).

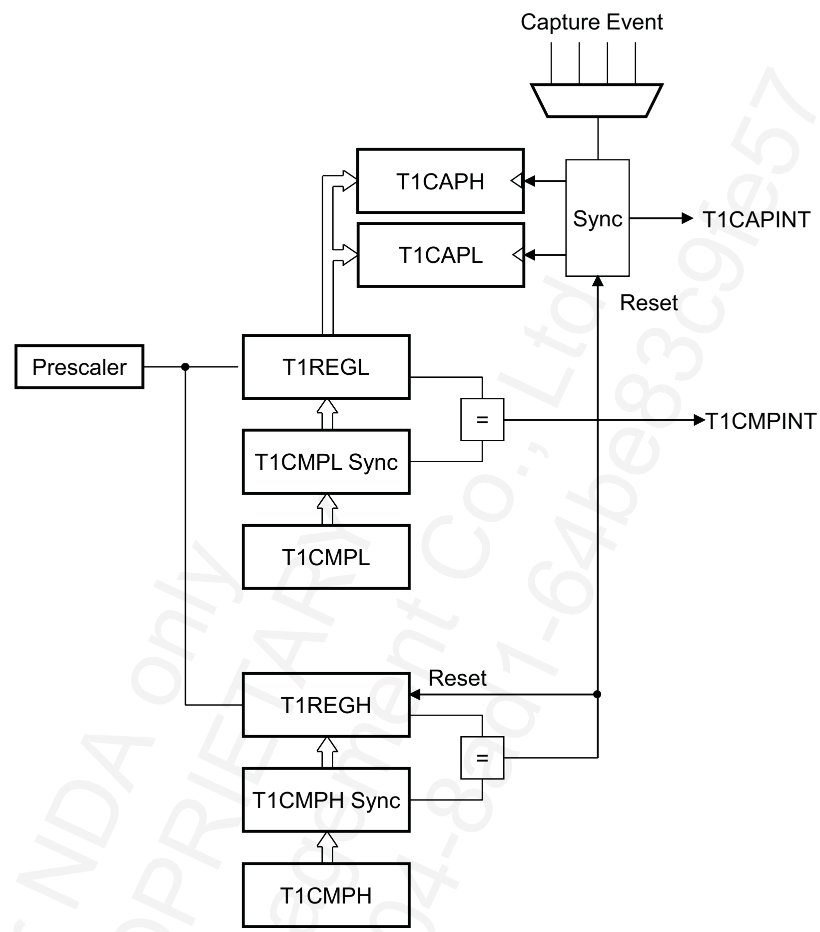


Fig 57. Block diagram of Timer 1 configured in Mode 3

It is possible to specify a guard time after every capture event or signal transition. This is useful if the timer is used to demodulate noisy signals. Only the first transition triggers the capture logic. Any other signal transition is ignored until the guard time elapses.

Register T1REGH is used together with T1CMPH to set the guard time. The timer register shall be cleared manually before start of the timer. If the timer is started and a capture event is detected, T1REGH starts counting. It is stopped and cleared if a match between T1REGH and T1CMPH occurs. The capture logic is blocked as long as T1REGH is running. The guard time is triggered on every selected signal transition no matter whether this generates an interrupt/capture event or not.

The signal level of the selected capture event is evaluated directly after release of the capture logic. If both the rising and the falling edge are selected as capture events it can happen that a new capture event is generated immediately. This would for example be the case if a rising edge was detected first and then the signal becomes statically low again when the guard time has not yet elapsed. In this case a falling edge is detected directly after release of the capture logic.

2.12.2 Registers

2.12.2.1 Timer 1 register T1REG

Timer 1 supports read access to the timer register. The content of the timer register is not buffered or synchronized. Therefore, reading of T1REG is only recommended when the timer is stopped (T1RUN = 0). When the timer is running reading of T1REG can generate unstable and wrong values as the timer value is not necessarily settled when reading takes place. It is recommended to use the manual capture function when the timer is running.

Write access to timer register T1REG is not supported.

Table 126. Timer 1 register T1REG (reset value 00 00h)

Bit	Symbol	Access	Value	Description
15 to 8	T1REGH [7:0]	R		Timer 1 Register High Byte (MSByte)
7 to 0	T1REGL [7:0]	R		Timer 1 Register Low Byte (LSByte)

2.12.2.2 Timer 1 control register T1CON0

Timer 1 control register 0 holds the control bits to adjust the timer mode and output line. Further, bits to configure the reset and run conditions are provided.

Table 127. Timer 1 control register 0 T1CON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	T1OUT [1:0]	R/W		Timer 1 output line configuration (T1LINE)
			00	No change T1LINE after Timer 1 reset: 0
			01	Mode 0,1,3:Set to ‘0’ Mode 2:Set to ‘1’, if T1REGH = T1CMPH Set to ‘0’, if T1REGL = T1CMPL T1LINE after Timer 1 reset: 0
			10	Mode 0,1,3:Toggles Mode 2: Toggles, if T1REGH = T1CMPH or T1REGL = T1CMPL T1LINE after Timer 1 reset: 0
			11	Mode 0,1,3:Set to ‘1’ Mode 2:Set to ‘0’, if T1REGH = T1CMPH Set to ‘1’, if T1REGL = T1CMPL T1LINE after Timer 1 reset: 1
5	T1RSTCAP	R/W		Timer 1 reset at capture event
			0	No reset
			1	Reset T1REGL, T1REGH and prescaler
4	T1RSTCMP	R/W		Timer 1 reset after compare match
			0	No reset
			1	Mode 0,1: Reset T1REG after T1REG = T1CMP Mode 2,3: Reset T1REGL and T1REGH after T1REGL = T1CMPL

Table 127. Timer 1 control register 0 T1CON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
3 and 2	T1MODE[1:0]	R/W		Timer 1 mode selection
			00	Mode 0
			01	Mode 1
			10	Mode 2
			11	Mode 3
1	T1RST[1]	R0/W		Timer 1 reset
			0	No reset
			1	Timer 1 reset
0	T1RUN[1]	R/W		Timer 1 run bit
			0	Timer 1 is stopped
			1	Timer 1 is started/running. While reading, a 1 can also indicate the synchronization phase for start or stop

[1] If T1RST and T1RUN are set simultaneously, T1RST has priority and the timer does not start.

T1OUT[1:0], Timer 1 output line configuration

Timer 1 has an output line flip-flop driving the signal T1LINE. The behavior of this signal depends on the selected timer operating mode and can be configured with the output line configuration bits T1OUT.

The content of the output flip-flop is updated with every compare match. In Mode 0 and 1, T1LINE is updated, if T1REG = T1CMP. In Mode 3, T1LINE is updated, if T1REGL = T1CMPL.

The initial value of the output line flip-flop after a Timer 1 reset is also controlled via T1OUT.

T1RSTCAP, Timer 1 reset upon capture bit

It is possible to reset the timer register in parallel to a capture event. The timer register is reset to zero at the same time when the content is transferred into the capture register. The prescaler is reset to its start value simultaneously. All these events are accomplished with the prescaler clock T1PsClk instead of the timer register clock T1RegClk. Due to the additional reset of the prescaler it is ensured that the result of consecutive interval measurements always yield values independent of the previous interval.

T1RSTCMP, Timer 1 reset after compare match bit

It is possible to reset the timer register after a compare match with the next rising edge of the timer register clock T1RegClk. The prescaler is not influenced.

Example: T1CMP = 4, T1RSTCMP = 1, the timer counts 0, 1, 2, 3, 4, 0, 1, 2, 3, 4, 0, 1, …

T1MODE[1:0], Timer 1 mode selection

Whenever the timer mode is changed the application shall perform a reset of Timer 1 via bit T1RST. It is allowed to set T1RST with the same command that modifies T1MODE.

T1RST, Timer 1 reset bit

The reset bit T1RST can be used to generate an asynchronous reset of Timer 1 comprising the prescaler, the timer register, the synchronization logic, the capture logic and the output line flip-flop. The current content of register T1CMP is loaded into the synchronization register T1CMPSync. A '1' shall be written to T1RST to execute the reset. Writing a '0' has no effect and reading of bit T1RST always yields '0'.

Launching a reset when the timer is running causes the timer to stop immediately and the bit T1RUN is cleared. If T1RST and T1RUN are set simultaneously the reset bit has priority and the timer does not start.

T1RUN, Timer 1 run bit

Timer 1 can be started and stopped with the control bit T1RUN. Reading of T1RUN gives the current status of Timer 1. If a '1' is written to T1RUN the timer is enabled and it starts counting with the rising edge of T1CLK. Writing a '0' to T1RUN forces the timer to stop operation. Every change of signal T1RUN is synchronized to T1CLK before it becomes effective. Reading of T1RUN yields '1' if the timer is running and during the synchronization phase to start and stop the timer.

2.12.2.3 Timer 1 control register T1CON1

The Timer 1 control register 1 stores the selection of the prescaler value T1PRESC[3:0] and the used clock source T1CLKSEL[1:0].

The control bits in register T1CON1 are not buffered nor synchronized to the timer clock T1CLK. The content of register T1CON shall only be modified, if the timer is stopped (T1RUN = 0). Any alteration of T1CON1 when the timer is running can cause unpredictable behavior.

Table 128. Timer 1 control register 1 T1CON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5 and 4	T1CLKSEL[1:0]	R/W		Timer 1 clock source selection
			00	RCCLK/2 (8 MHz nominal)
			01	External clock, XCLK
			10	Output of timer source multiplexer 0, TMUX0CLK
			11	Output of timer source multiplexer 1, TMUX1CLK
3 to 0	T1PRESC[3:0]	R/W		Timer 1 prescaler selection
			0000	T1RegClk = 1 * T1CLK
			0001	T1RegClk = 2 * T1CLK
			0010	T1RegClk = 4 * T1CLK
			0011	T1RegClk = 8 * T1CLK
			0100	T1RegClk = 16 * T1CLK
			0101	T1RegClk = 32 * T1CLK
			0110	T1RegClk = 64 * T1CLK
			0111	T1RegClk = 128 * T1CLK
			1000	T1RegClk = 256 * T1CLK
			1001	T1RegClk = 512 * T1CLK
			1010	T1RegClk = 1024 * T1CLK
			1011	T1RegClk = 2048 * T1CLK
			1100	T1RegClk = 4096 * T1CLK
			1101 - 1111	RFU

T1CLKSEL[1:0], Timer 1 clock source selection

The Timer 1 clock source selection selects the clock source.

T1PRESC[3:0], Timer 1 prescaler selection

The Timer 1 prescaler selection selects the clock speed for the timer register according to Equation 30.

2.12.2.4 Timer 1 control register T1CON2

Timer 1 control register 2 holds the control bits to adjust the capture functionality.

Table 129. Timer 1 control register 2 T1CON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	T1MANCAP	R/W		Timer 1 manual capture bit
			0	No manual capture event
			1	Mode 0,1: Content of T1REG is transferred into T1CAP (16 bit) Mode 2,3: Content of T1REGL is transferred into T1CAPL (8 bit)
6 to 4	T1CAPMODE[2:0]	R/W		Timer 1 capture mode selection
			000	No event
			001	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Rising edge
			010	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Falling edge
			011	Mode 0,1 (event for T1CAP): Both edges Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Both edges Mode 3 (event to trigger guard time): Both edges
			100	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): Rising edge Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Both edges
			101	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Both edges
			110	Mode 0,1 (event for T1CAP): Falling edge Mode 2,3 (event for T1CAPH): None Mode 2,3 (event for T1CAPL): Falling edge Mode 3 (event to trigger guard time): Both edges
			111	Mode 0,1 (event for T1CAP): Rising edge Mode 2,3 (event for T1CAPH): Falling edge Mode 2,3 (event for T1CAPL): Rising edge Mode 3 (event to trigger guard time): Both edges

Table 129. Timer 1 control register 2 T1CON2 (reset value 00h)

Bit	Symbol	Access	Value	Description
3 to 0	T1CAPSRC[3:0]	R/W		Timer 1 capture signal source selection
			0000	Input of port P17
			0001	Input of port P21
			0010	Output signal line of Timer 0
			0011	Output signal line of Timer 2
			0100	Output signal of LF IMMO demodulator
			0101	Output signal of LF active demodulator (filtered)
			0110	Output signal of LF active demodulator (direct, unfiltered)
			0111	Input of port P13
			1000	Output signal of timer source multiplexer 0 (TMUX0CLK)
			1001 - 1101	Reserved for future use
			1110	Constant ‘0’
			1111	Constant ‘1’

T1MANCAP, Timer 1 manual capture bit

A capture operation can be requested manually when the timer is running. Thereby it is possible to read a consistent counter value even if the timer is running.

Once the bit T1MANCAP is set by the application, it will stay '1' until the capture request has been executed, causing the control bit to be cleared. Thus, T1MANCAP can be polled by the application to verify, if the capture request has been carried out.

A manual capture event never generates an interrupt request or triggers a reset upon capture or starts the guard time. The manual capture works independently of the selected setting of the capture mode T1CAPMODE. It even works, if T1CAPMODE = 000.

The manual capture event is accomplished with the prescaler clock T1PsClk to minimize the latency.

The manual capture functionality is not supported, if the timer is stopped. If T1MANCAP is set when the timer is stopped, the manual capture event will be accomplished as soon as the timer is started again. If the timer is stopped, the application can instead read the timer register directly.

The bit T1MANCAP cannot be cleared by the application except by executing a timer reset with bit T1RST.

Dependent on the selected timer operating mode the manual capture function transfers different portions of data into different registers.

T1CAPMODE[2:0], Timer 1 capture mode selection

With the timer 1 capture mode selection it is possible to select which event of the capture source signal is used to generate a capture event and to load the respective capture register. In timer operating mode 2 and 3 it is possible to select different actions for the two capture registers T1CAPH and T1CAPL. In timer mode 3 it is also possible to select the behavior of the guard time logic.

If all three bits of T1CAPMODE are zero, the capture function is disabled completely in all timer operating modes.

In timer mode 3 the difference between setting 001 and 101 (and 010 and 110) is the behavior of the guard time. If the settings 101 or 110 are selected, the guard time is activated even if an inactive edge is detected. This avoids false triggers in case there are multiple signal transitions in the vicinity of the unselected event. The settings 001 and 010 are intended for signals with very different behavior of the rising and falling edges. For these signals it can be more appropriate to define a longer guard time after the significant edge that covers also the unselected edge. Thereby it is possible to generate a shorter guard time after the unselected edge if the pulse width is known.

In timer mode 2 and 3 the selection of either value 100 or 111 for T1CAPMODE can be used to distinguish the event that causes the generation of the capture interrupt (only a capture event of T1CAPL generates an interrupt).

T1CAPSRC[3:0], Timer 1 capture signal source selection

With this setting it is possible to select the source signal for the capture event.

The settings 1110b and 1111b are intended for debugging and test purposes. Therewith it is possible to trigger a capture event on either edge by software.

2.12.2.5 Timer 1 compare register T1CMP

The compare register T1CMP is used to set the time-out interval of Timer 1. The compare register has an internal synchronization stage (T1CMPSync) to allow safe operation even when the timer is running. The behavior of any write access to register T1CMP depends on the current state of the timer. If the timer is stopped (T1RUN = 0) any write access to T1CMP updates also the synchronization stage T1CMPSync. The prescaler and the timer register T1REG are not influenced. If the timer is running (T1RUN = 1), a write access to T1CMP triggers the synchronization logic first. The new value of T1CMP is transferred with one of the next rising edges of T1CLK into the synchronization register T1CMPSync. The value of T1CMP shall stay constant for this time period to allow a correct data transfer. Any write access to either T1CMPL or T1CMPH causes a resynchronization of the complete register T1CMP. Therefore, if both values T1CMPL and T1CMPH are intended to be changed a word access to register T1CMP shall be used rather than two consecutive byte accesses to T1CMPL and T1CMPH. Any read access to T1CMP yields the content of the register itself and not the content of the synchronization register T1CMPSync.

Table 130. Timer 1 compare register T1CMP (reset value T1CMP = xxxx_xxxx_xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
15 to 8	T1CMPH [7:0]	R/W		Timer 1 Compare Register High Byte (MSByte)
7 to 0	T1CMPL [7:0]	R/W		Timer 1 Compare Register Low Byte (LSByte)

2.12.2.6 Timer 1 capture register T1CAP

The Timer 1 Capture Register is loaded automatically with the content of the timer register. Reading shall only be performed if the content is stable. Write access to T1CAP is not supported.

Table 131. Timer 1 capture register T1CAP (reset value XX XXh)

Bit	Symbol	Access	Value	Description
15 to 8	T1CAPH [7:0]	R		Timer 1 Capture Register High Byte (MSByte)
7 to 0	T1CAPL [7:0]	R		Timer 1 Capture Register Low Byte (LSByte)

2.12.3 Interaction with I/O port interface

If an I/O pin is selected as capture input the application shall assure that the corresponding I/O pin is configured as input.

2.13 Watchdog timer

The device incorporates a watchdog timer to recover the system from application program deadlocks. This avoids that the connected battery is unnecessarily discharged. The watchdog timer consists of a 16 bit incrementing main timer with 11 bit prescaler. Each tap of the main timer can be selected to generate the watchdog time-out.

The watchdog timer is active when the device is supplied from the battery (PMODE = 1, BATTERY state), while it is disabled when the device is supplied from the LF field (PMODE = 0). The watchdog timer stops automatically in debug mode.

If the watchdog timer is active and not periodically restarted, it forces the Supply Switch logic to set the Supply Switch to Field supply (PMODE = 0) and generates a device reset. Consequently, the device supply is no longer derived from the battery and the further system behavior depends on the field supply condition and the voltage at pin VDDC. The device may continue program execution, starting with the boot routine, as long as the field supply is sufficient. A battery buffered flag indicates a previous watchdog time-out and can be evaluated after processing of the boot routine.

The clock for the watchdog timer is derived from the auxiliary RC oscillator and has a nominal frequency of 125 kHz ($T_{REF,LF}$ = 8 μs). The timeout is selectable in 16 steps from approximately 16 ms to 537 s. The selected time-out value can be locked.

In single shot mode, the clearing of the watchdog is prevented, thus the application shall finish prior to the selected fixed watchdog time-out. This mode is intended for applications which do not handle the watchdog at all.

2.13.1 Registers

2.13.1.1 Watchdog timer control register WDCON

The watchdog timer is controlled via the watchdog timer control register WDCON.

Table 132. Watchdog timer control register WDCON (reset value 50h)

Bit	Symbol	Access	Value	Description
7 to 4	WDTIM[3:0]	R/W		Watchdog time-out selection
			0000	2^{11} $T_{REF,LF}$ ~ 16 ms
			0001	2^{12} $T_{REF,LF}$ ~ 33 ms
			0010	2^{13} $T_{REF,LF}$ ~ 66 ms
			0011	2^{14} $T_{REF,LF}$ ~ 131 ms
			0100	2^{15} $T_{REF,LF}$ ~ 262 ms
			0101	2^{16} $T_{REF,LF}$ ~ 524 ms
			0110	2^{17} $T_{REF,LF}$ ~ 1.05 s
			0111	2^{18} $T_{REF,LF}$ ~ 2.10 s
			1000	2^{19} $T_{REF,LF}$ ~ 4.19 s
			1001	2^{20} $T_{REF,LF}$ ~ 8.39 s
			1010	2^{21} $T_{REF,LF}$ ~ 16.8 s
			1011	2^{22} $T_{REF,LF}$ ~ 33.6 s
			1100	2^{23} $T_{REF,LF}$ ~ 67.1 s
			1101	2^{24} $T_{REF,LF}$ ~ 134 s
			1110	2^{25} $T_{REF,LF}$ ~ 268 s
			1111	2^{26} $T_{REF,LF}$ ~ 537 s
3 and 2	WDMODE[1:0]	R/W[1]		Watchdog mode selection
			00	Standard operation, all control bits in register WDCON can be written. Use this mode if the application requires changing the watchdog time-out value.
			01	Fixed time-out selection: The bits WDTIM and WDMODE0 cannot be changed. Use this mode to select a fixed time-out.
			10 or 11	Single shot mode: The bits WDTIM, WDMODE and WDCLR cannot be changed. Use this mode to select a fixed time-out for an application, which does not handle the watchdog at all. The application shall finish prior to the selected watchdog time-out. It is not possible to clear the watchdog.
1	WDTRIG	R0/W		Trigger watchdog time-out
			0	No effect
			1	Trigger watchdog time-out
0	WDCLR	R0/W		Watchdog clear
			0	No effect
			1	Clears watchdog prescaler and main timer

[1] Note: Write access to all control bits except bit 1 depends on the setting of WDMODE

WDTIM[3:0], watchdog time-out selection

The register bits WDTIM select a tap from the watchdog main timer. If the selected tap holds a '1', a watchdog time-out is generated. All other bits of the main timer as well as the prescaler are not considered. After the watchdog has been cleared, the watchdog time-out can be calculated to be:

$$WDTIMEOUT = 2^{(11 + WDTIM)} \cdot T_{REF, LF} \quad (33)$$

If WDMODE = 00b, WDTIM can be changed at any time without influencing the current state of the watchdog timer. When changing the time-out value, it is recommended to clear the watchdog counter simultaneously.

If WDTIM is changed to a lower value and the watchdog is not cleared simultaneously it depends on the state of the selected tap of the main timer whether a time-out is generated immediately or not. It can happen that no time-out is generated even though the current value of the main timer is greater than WDTIMEOUT.

After a device reset WDTIM is set to 0101b, hence, the watchdog time-out value is set to 2^{16} $T_{REF,LF}$ (approximately 524 ms).

WDMODE[1:0], watchdog mode selection

The watchdog timer supports three different application modes.

Please note that the bits WDMODE have the character of one time programmable bits. It is not possible to clear one of the WDMODE bits by the application program once they are set. It is possible to set WDMODE from 01b to 11b in order to enter the single shot mode once a fixed time-out has already been selected. Changing WDMODE = 10 to WDMODE=11 does not change anything as both settings are equivalent.

If the bits WDMODE1 and WDCLR are set simultaneously the request to clear the watchdog is already ignored and no reset is accomplished.

WDTRIG, trigger watchdog time-out

If a '1' is written to this bit it can be used to trigger a watchdog time-out intentionally. The effect is the same as if a real watchdog time-out has occurred. This functionality can be used to check the behavior of the application program after a watchdog time-out. Writing a '0' to WDTRIG has no effect. Reading of WDTRIG always yields '0'.

WDCLR, watchdog clear

To prevent the watchdog timer from generating a time-out, a '1' has to be written periodically to the control bit WDCLR by the application program. This clears the watchdog prescaler and main timer. Writing a '0' to WDCLR has no effect. Reading of WDCLR always yields '0'.

WDTOF, watchdog time-out flag

A watchdog time-out event sets the watchdog time-out flag WDTOF in special function register PRESWUP0 This flag is located in the battery supplied domain and keeps its state even in POWER-DOWN mode. Bit WDTOF can only be cleared by the user by writing a '1', writing a '0' has no effect. This bit is for notification purpose only and has no other effects.

2.14 I-O ports

The device incorporates one I/O port, P1, with 8 independently configurable bi-directional port lines, P10 to P16 and P17_LED. The P17_LED is multiplexed with an LED driver function. The device incorporates a second I/O port, P2, with two I/Os: P21_MD and P20. The P21_MD pin is multiplexed with a motion-sensor interface function. Some I/O pins provide alternative port functions. All I/O ports can be controlled individually.

Eight of the ten I/O pins can provide wake up function on high to low and low to high transition. These I/O pins have a battery buffered configurable wake up edge selection (falling/rising) and wake up disabling function. All ten pins feature configurable pull-up strength as weak or strong pull-up. Additionally P21_MD features a very-weak pull-up configuration. The wake up edge and pull-up strength configuration settings are preserved in POWER OFF state, hence any activated pull-up/pull-down resistor is operable also in this state. The two fail-safe wake up pins P10 and P11 are featuring a permanent pull-up resistor that is only active when configured for input mode. Eight pins can be configured to generate port interrupt requests on rising and falling edges of the pin. Configuration and access of the I/O Port is provided by means of a Direction, Output and Input Sense registers.

The I/O pins are configured as Input in POWER OFF state and during device Reset, whereas the port direction and output flip-flops are cleared. Ports in output mode are configured in "push-pull" fashion except P10 and P11 where a pull-up is only active when they're in input mode. In Input configuration an internal pull-up resistor is always connected (see Figure 58) to the pin in digital mode. The pull-up resistors are automatically disabled in output or an alternative-function mode.

2.14.1 Port wake up

The port wake up logic can wake up the device from POWER-OFF mode or to trigger a corresponding interrupt request during program execution. The wake up feature is supported by all I/O pins. A port wake up from POWER OFF state transits the device to the BATTERY state. If the device is field-supplied (LF FIELD state), the port wake up information is stored and can be used for branch decision in the boot routine. For all wake-up ports, the wake-up mono-flop is triggered for the specified time t_{PSMF} in input mode and disabled if the port operates in output mode. Due to spurious events, the port wake-up mono-flop can be triggered if the direction of a port pin changes.

Example: A device is operating in BATTERY state. A wake-up port is used as output and set to high level. The port is configured to use the internal pull-down and to wake-up on a falling edge. Setting the device to POWER OFF state, the port is set to input and due to the configured internal pull-down set to low level. Consequently, a falling edge is detected which could result in a wake-up event. To avoid this behavior the power-off routine should first clear the port direction and then wait for t_{PSMF} (plus the time the external circuitry needs to establish static conditions at the port lines) to ignore this possible wake-up event.

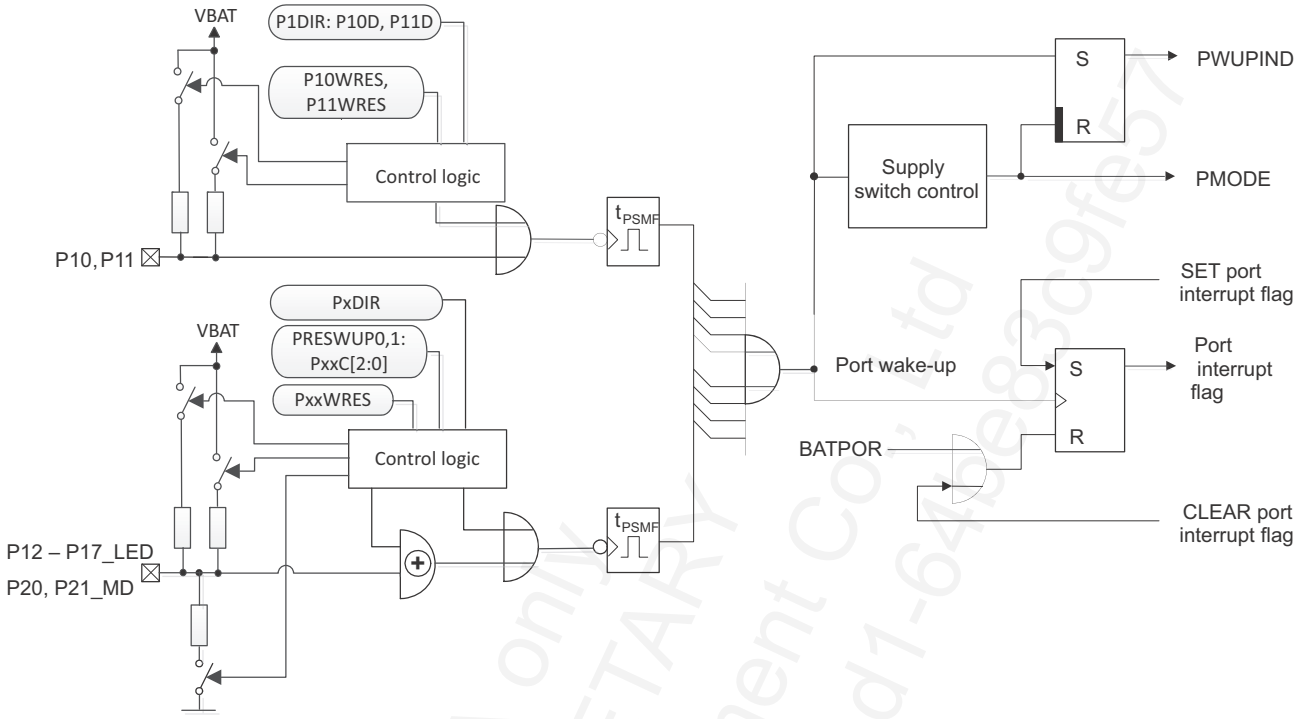


Fig 58. Port wake up logic

For P10 and P11, the port wake-up is sensitive at high to low transitions of the port pin. These ports feature fixed pull-up resistors which are only active when they're in input mode. The wake-up mono-flop is enabled if the port pin is in input mode. Due to this, P10 and P11 support a fail-safe wake-up from POWER OFF state regardless of the setting of any battery supplied control register. It is strongly recommended that every application uses at least one of these two ports for wake-up generation in order to avoid deadlock situations if the battery supplied registers are not correctly configured. The weak or strong pull-up for P10 and P11 permanently connected in POWER OFF state, will be defined according to the PxWRES settings in Table 141 and Table 142.

The port pins P12 to P17_LED, P21_MD and P20 feature a selectable pull-up or pull-down resistor and a user selectable wake-up either on high to low or low to high transition of the port. The wake-up on low to high transition of the port can be used by the application to detect the release of a button. Either the internal pull-up resistor or an external pull-up device shall be used for correct operation. If a port pin is needed as general purpose pin and not as button input it is possible to disable the wake-up function.

2.14.2 Registers

The port wake-up indicator flag PWUPIND (from Figure 58) is hosted in the power control register PCON1.

2.14.2.1 Port direction control registers, PxDIR

The I/O port lines can be configured as input or output as defined in the P1DIR register. If the corresponding direction bit is set the port line is configured for output and the corresponding port I/O driver forces the port line high or low, depending on the state of the

corresponding data output source selected. If the corresponding direction bit is cleared, the I/O port driver is configured for input and the corresponding push-pull stage is forced into tri-state.

It is important to notice that the port direction control bit can be overruled the alternative port functions (see also Section 2.14.2.7).

Table 133. Port 1 direction control register P1DIR (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17D	R/W		Port 1.7 direction
			0	Input
			1	Output
6	P16D	R/W		Port 1.6 direction
			0	Input
			1	Output
5	P15D	R/W		Port 1.5 direction
			0	Input
			1	Output
4	P14D	R/W		Port 1.4 direction
			0	Input
			1	Output
3	P13D	R/W		Port 1.3 direction
			0	Input
			1	Output
2	P12D	R/W		Port 1.2 direction
			0	Input
			1	Output
1	P11D	R/W		Port 1.1 direction
			0	Input
			1	Output
0	P10D	R/W		Port 1.0 direction
			0	Input
			1	Output

Table 134. Port 2 direction control register P2DIR (reset value xxxxxx00b)

Bit	Symbol	Access	Value	Description
7 to 2	RFU	R/W0		Reserved for future use
1	P21D	R/W		Port 2.1 direction
			0	Input
			1	Output
0	P20D	R/W		Port 2.0 direction
			0	Input
			1	Output

2.14.2.2 Port xInterrupt Disable register PxINTDIS

PxINTDIS disables the corresponding Portx interrupt if the corresponding bit is set. Compared to PRESWUPx the PxINTDIS register allows deactivating also interrupts on the fail safe wake-up ports P10 and P11 and it allows disabling port interrupts when running from field supply.

Table 135. Port 1 Interrupt Disable register P1INTDIS (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17INTDIS	R/W		Port 1.7 interrupt disable
			0	enabled
			1	disabled
6	P16INTDIS	R/W		Port 1.6 interrupt disable
			0	enabled
			1	disabled
5	P15INTDIS	R/W		Port 1.5 interrupt disable
			0	enabled
			1	disabled
4	P14INTDIS	R/W		Port 1.4 interrupt disable
			0	enabled
			1	disabled
3	P13INTDIS	R/W		Port 1.3 interrupt disable
			0	enabled
			1	disabled
2	P12INTDIS	R/W		Port 1.2 interrupt disable
			0	enabled
			1	disabled
1	P11INTDIS	R/W		Port 1.2 interrupt disable
			0	enabled
			1	disabled
0	P10INTDIS	R/W		Port 1.0 interrupt disable
			0	enabled
			1	disabled

Table 136. Port 2 Interrupt Disable register P2INTDIS (reset value xxx0_0000b)

Bit	Symbol	Access	Value	Description
7 to 2	RFU	R/W0		Reserved for future use
1	P21INTDIS	R/W		Port 2.1 interrupt disable
			0	enabled
			1	disabled
0	P20INTDIS	R/W		Port 2.0 interrupt disable
			0	enabled
			1	disabled

2.14.2.3 Port output control registers PxOUT

The port output register controls the respective port output flip-flop in case the port line is used in output mode. Any read operation from the port output control register will return the state of the flip-flop rather than the state of the port line.

Table 137. Port 1 output control register P1OUT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	P17O	R/W		Port 1.7 output
			0	Low (‘0’)
			1	High (‘1’)
6	P16O	R/W		Port 1.6 output
			0	Low (‘0’)
			1	High (‘1’)
5	P15O	R/W		Port 1.5 output
			0	Low (‘0’)
			1	High (‘1’)
4	P14O	R/W		Port 1.4 output
			0	Low (‘0’)
			1	High (‘1’)
3	P13O	R/W		Port 1.3 output
			0	Low (‘0’)
			1	High (‘1’)
2	P12O	R/W		Port 1.2 output
			0	Low (‘0’)
			1	High (‘1’)
1	P11O	R/W		Port 1.0 output
			0	Low (‘0’)
			1	High (‘1’)
0	P10O	R/W		Port 1.0 output
			0	Low (‘0’)
			1	High (‘1’)

Table 138. Port 2 output control register P2OUT (reset value xxxxxx00b)

Bit	Symbol	Access	Value	Description
7 to 2	RFU	R/W0		Reserved for future use
1	P21O	R/W		Port 2.1 output
			0	Low (‘0’)
			1	High (‘1’)
0	P20O	R/W		Port 2.0 output
			0	Low (‘0’)
			1	High (‘1’)

2.14.2.4 Port input sense registers PxINS

Reading from the port lines is accomplished by means of the special function registers port input sense PxINS. Reading these registers directly sense the port pins and returns the corresponding states of the I/O lines. The port input sense logic is disabled for port pins if an analogue port function is active. The corresponding port input sense bits return a '0' in this case.

If no battery supply is available, all port input sense bits return a '1'.

Table 139. Port 1 input sense register P1INS (reset value xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7	P17S	R		Port 1.7 input
			0	Low (‘0’)
			1	High (‘1’)
6	P16S	R		Port 1.6 input
			0	Low (‘0’)
			1	High (‘1’)
6	P15S	R		Port 1.5 input
			0	Low (‘0’)
			1	High (‘1’)
4	P14S	R		Port 1.4 input
			0	Low (‘0’)
			1	High (‘1’)
3	P13S	R		Port 1.3 input
			0	Low (‘0’)
			1	High (‘1’)
2	P12S	R		Port 1.2 input
			0	Low (‘0’)
			1	High (‘1’)
1	P11S	R		Port 1.1 input
			0	Low (‘0’)
			1	High (‘1’)
0	P10S	R		Port 1.0 input
			0	Low (‘0’)
			1	High (‘1’)

Table 140. Port 2 input sense register P2INS (reset value xxxx_xxxxb)

Bit	Symbol	Access	Value	Description
7 to 2	RFU	R		Reserved for future use
1	P21S	R		Port 2.1 input
			0	Low (‘0’)
			1	High (‘1’)
0	P20S	R		Port 2.0 input
			0	Low (‘0’)
			1	High (‘1’)

2.14.2.5 Port pull up strength control register PxWRES

Port pins feature a pull-up strength control register, stored in VBAT domain. Configuration is kept even when VDD disappears and device is in POWER-OFF mode. All port pins can be configured to strong pull-ups (typ. 100uA when VBAT=3V) or weak pull-ups (typ. 10uA). Reading PxWRES returns the pull up strength (0 = weak, 1 = strong). The pull up strength information is stored in the VBAT domain. The pull-up strength is also latched in POWER OFF state but cannot be guaranteed (e.g. in case of battery bouncing or insertion) and should be refreshed from time to time per software. Strong pull-ups are used as default on battery power-on reset. This register is located in the constantly battery supplied domain and is not initialized with the battery power-on reset. It is not possible to disconnect the pull-up resistor. The pull-up resistor is temporarily disabled if the I/O pin is switched to output. Moreover, the resistors are temporarily disabled for all I/O if an alternative function of the corresponding port is active.

Table 141. Port pull up strength control register P1WRES (reset value FFh)

Bit	Symbol	Access	Value	Description
7	P17WRES	R/W		Port 1.7 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
6	P16WRES	R/W		Port 1.6 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
5	P15WRES	R/W		Port 1.5 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
4	P14WRES	R/W		Port 1.4 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
3	P13WRES	R/W		Port 1.3 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
2	P12WRES	R/W		Port 1.2 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
1	P11WRES	R/W		Port 1.1 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
0	P10WRES	R/W		Port 1.0 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})

Table 142. Port pull up strength control register P2WRES (reset value xx0x_xx11b)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5	P21MRES	R/W		Port 2.1 pull up strength, control bits has only an effect if P21WRES is cleared
			0	very weak (R_{PU_MD}) disabled
			1	very weak (R_{PU_MD}) enabled,
4 to 2	RFU	R/W1		Reserved for future use
1	P21WRES	R/W		Port 2.1 pull up strength, control bits only has an effect if P21WRES is cleared
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})
0	P20WRES	R/W		Port 2.0 pull up strength
			0	weak (R_{PU_WK})
			1	strong (R_{PU_STR})

2.14.2.6 Port resistor/wake up configuration, PRESWUPx

The port resistor and wake-up configuration registers are used to configure the pull-up or pull-down resistor of the respective I/O port and to configure the port pin wake-up function. For every I/O port featuring a selectable pull-up or pull-down resistor and wake-up function three control bits are available.

It is possible to select a pull-up resistor or a pull-down resistor or to deactivate both, but not to turn on the pull-up and the pull-down resistor simultaneously.

The port resistor and wake-up configuration registers allow either byte or word access (Table 143).

Table 143. Word and byte access to port resistor and wake-up configuration registers PRESWUPx

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
PRESWUP0	PRESWUP0H	PRESWUP0L
PRESWUP1	PRESWUP1H	PRESWUP1L
PRESWUP2	PRESWUP2H	PRESWUP2L

Table 144. Port resistor and wake-up configuration register PRESWUP0 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15 to 13	P15C[2:0]	R/W		Port 1.5 wake up configuration
			000	Resistors off; Wake-up on falling edge of P15
			001	Resistors off; Wake-up on rising edge of P15
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P15
			101	Pull-up resistor activated; Wake-up on rising edge of P15
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
12	RFU	R0/W0		Reserved for future use
11 to 9	P14C[2:0]	R/W		Port 1.4 wake up configuration
			000	Resistors off; Wake-up on falling edge of P14
			001	Resistors off; Wake-up on rising edge of P14
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P14
			101	Pull-up resistor activated; Wake-up on rising edge of P14
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
8	RFU	R0/W0		Reserved for future use

Table 144. Port resistor and wake-up configuration register PRESWUP0 (reset value 8888h)

Bit	Symbol	Access	Value	Description
7 to 5	P13C[2:0]	R/W		Port 1.3 wake up configuration
			000	Resistors off; Wake-up on falling edge of P13
			001	Resistors off; Wake-up on rising edge of P13
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P13
			101	Pull-up resistor activated; Wake-up on rising edge of P13
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
4	RFU	R0/W0		Reserved for future use
3 to 1	P12C[2:0]	R/W		Port 1.2 wake up configuration
			000	Resistors off; Wake-up on falling edge of P12
			001	Resistors off; Wake-up on rising edge of P12
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P12
			101	Pull-up resistor activated; Wake-up on rising edge of P12
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
0	WDTOF	R/W1->0		Watchdog time-out flag
			0	Write access: No effect Read access: No watchdog time-out event
			1	Write access: Clear flag Read access: Watchdog time-out event

Table 145. Port resistor and wake-up configuration register PRESWUP1 (reset value 8888h)

Bit	Symbol	Access	Value	Description
15 to 13	P21C[2:0]	R/W		Port 2.1 wake up configuration
			000	Resistors off; Wake-up on falling edge of P21
			001	Resistors off; Wake-up on rising edge of P21
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P21
			101	Pull-up resistor activated; Wake-up on rising edge of P21
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
12	RFU	R0/W0		Reserved for future use

Table 145. Port resistor and wake-up configuration register PRESWUP1 (reset value 8888h)

Bit	Symbol	Access	Value	Description
11 to 9	P20C[2:0]	R/W		Port 2.0 wake up configuration
			000	Resistors off; Wake-up on falling edge of P20
			001	Resistors off; Wake-up on rising edge of P20
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P20
			101	Pull-up resistor activated; Wake-up on rising edge of P20
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
8	RFU	R0/W0		Reserved for future use
7 to 5	P17C[2:0]	R/W		Port 1.7 wake up configuration
			000	Resistors off; Wake-up on falling edge of P17
			001	Resistors off; Wake-up on rising edge of P17
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P17
			101	Pull-up resistor activated; Wake-up on rising edge of P17
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
4	RFU	R0/W0		Reserved for future use
3 to 1	P16C[2:0]	R/W		Port 1.6 wake up configuration
			000	Resistors off; Wake-up on falling edge of P16
			001	Resistors off; Wake-up on rising edge of P16
			010	Pull-down resistor activated; Wake-up disabled
			011	Resistors off; Wake-up disabled
			100	Pull-up resistor activated; Wake-up on falling edge of P16
			101	Pull-up resistor activated; Wake-up on rising edge of P16
			110	Pull-up resistor activated; Wake-up disabled
			111	Reserved for future use
0	RFU	R0/W0		Reserved for future use

Table 146. Port resistor and wake-up configuration register PRESWUP2 (reserved for future use, reset value 0888h)

Bit	Symbol	Access	Value	Description
15 to 0	RFU	R/W		Reserved for future use, this register shall be set to 0888h by the application code

2.14.2.7 Port alternative functions register PxALTF

Alternative digital ports functions can be selected for every port pin separately via the port alternative function register PxALTF which allows either byte or word access (Table 148 and Table 149).

Table 147. Word and byte access to the status registers PxALTF

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
P1ALTF	P1ALTFH	P1ALTFL
P2ALTF	P2ALTFH	P2ALTFL

If an alternative port function is enabled, it overrules the direction bit (PxyD) and output register (PxyO) for this port.

Table 148. Port 1 alternative digital functions, P1ALTF (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 and 14	P17AF[1:0]	R/W		alternative function port pin P17
			00	no alternative function
			01	LED driver function is enabled driven from P17O
			10	LED driver function is enabled driven from Timer 1 output (T1LINE)
			11	LED driver function is enabled driven from Timer 2 output (T2LINE)
13 and 12	P16AF[1:0]	R/W		alternative function port pin P16
			00	no alternative function, normal operation
			01	Timer 0 output (T0LINE)
			10	RFU
			11	RFU
11 and 10	P15AF[1:0]	R/W		alternative function port pin P15
			00	no alternative function, normal operation
			01	RFU
			10	RFU
			11	RFU
9 and 8	P14AF[1:0]	R/W		alternative function port pin P14
			00	no alternative function, normal operation
			01	Clock multiplexer output TMUX1
			10	RFU
			11	SPI1 SDIO
7 and 6	P13AF[1:0]	R/W		alternative function port pin P13
			00	no alternative function
			01	Clock multiplexer output TMUX0
			10	IIU port modulator output
			11	SPI1 CK

Table 148. Port 1 alternative digital functions, P1ALTF (reset value 0000h)

Bit	Symbol	Access	Value	Description
5 and 4	P12AF[1:0]	R/W		alternative function port pin P12
			00	no alternative function
			01	Timer 2 output (T2LINE)
			10	RFU
			11	SPI1 SDI
3 and 2	P11AF[1:0]	R/W		alternative function port pin P11
			00	no alternative function
			01	Timer 1 output (T1LINE)
			10	RFU
			11	SPI0 SDIO
1 and 0	P10AF[1:0]	R/W		alternative function port pin P10
			00	no alternative function
			01	Timer 0 output (T0LINE)
			10	IIU port modulator output
			11	SPI0 CK

Table 149. Port 2 alternative digital functions, P2ALTF (reset value 0000h)

Bit	Symbol	Access	Value	Description
15 to 8	RFU	R/W0		Reserved for future use
7 to 4	RFU	R/W0		Reserved for future use
3 and 2	P21AF[1:0]	R/W		alternative function port pin P21
			00	no alternative function
			01	Timer 2 output (T2LINE)
			10	RFU
			11	SPI0 SDI
1 and 0	P20AF[1:0]	R/W		alternative function port pin P20
			00	no alternative function
			01	Timer 1 output (T1LINE)
			10	RFU
			11	RFU

2.15 LED driver

The NCF29A1 / NCF29A2 features an integrated LED driver to directly drive an external LED from VBAT. Port P17_LED can be configured as a current sink to drive an LED without the need for external current limiting or pull up resistors.

The LED driver is enabled by setting P17AF in Port 1 alternative digital functions register P1ALTFH (see Table 148). The P17_LED driver can also be controlled by the Timer 1 or 0. The LED current is switched with bit P17O in Port output control registers P1OUT (see Figure 59 and Table 150).

Table 150. P17O port output control bit in port output control registers P1OUT (LED driver is enabled)

Bit	Symbol	Access	Value	Description
7	P17O	R/W		P17 current sink to VSS enable
			0	P17 pull-up enabled to prevent P17 / LED cathode connection from floating P17 current sink to VSS disabled, LED is OFF.
			1	P17 pull-up disabled P17 current sink to VSS enabled, LED is ON.

In LED driver mode the GPI/O output function is deactivated and the port direction bit have no influence on the port behavior (see grey circuitry in Figure 59). The P17 input sense is disabled and the read value of P1INS.P17S is 0. The maximum driving capability is limited to prevent damage of a connected LED. In POWER_OFF mode P17_LED is configured as GPI/O input and the LED current driver is off. An internal pull-up is connected in parallel to the external diode to avoid any parasitic current when the driver is not enabled. P17WRES determines the internal pull-up resistor strength. The internal pull-up is deactivated as soon as the LED driver is activated in LED driver mode or when the port alternative function is configured.

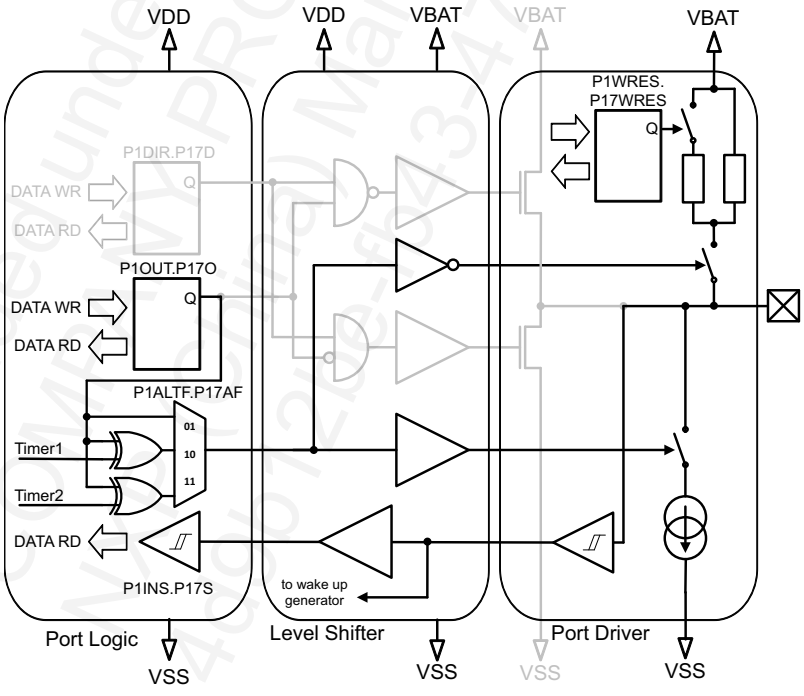


Fig 59. LED driver combined with the general purpose digital I/O port P1.7

2.16 Voltage, Temperature and RSSI Measurement

The NCF29A1 / NCF29A2 has a Successive Approximation Analog/Digital Converter (ADC) which can be used to measure voltage levels (battery voltage or external voltage levels), temperature and RSSI. The ADC is optimized regarding conversion time and overall power consumption. Note that the VBAT brown-out monitor (see VBATBRNREG bit in Section 2.2.4.5) shall be used to monitor the supply voltage level at VBAT to verify whether the supply voltage at VBAT was sufficient for the complete duration of the ADC conversion.

2.16.1 Battery Voltage Measurement

The NCF29A1 / NCF29A2 features battery voltage measurement to analyze and track the condition and life cycle status of the battery. The measurement setup with battery voltage scaling, supply and the voltage source are shown in Figure 60.

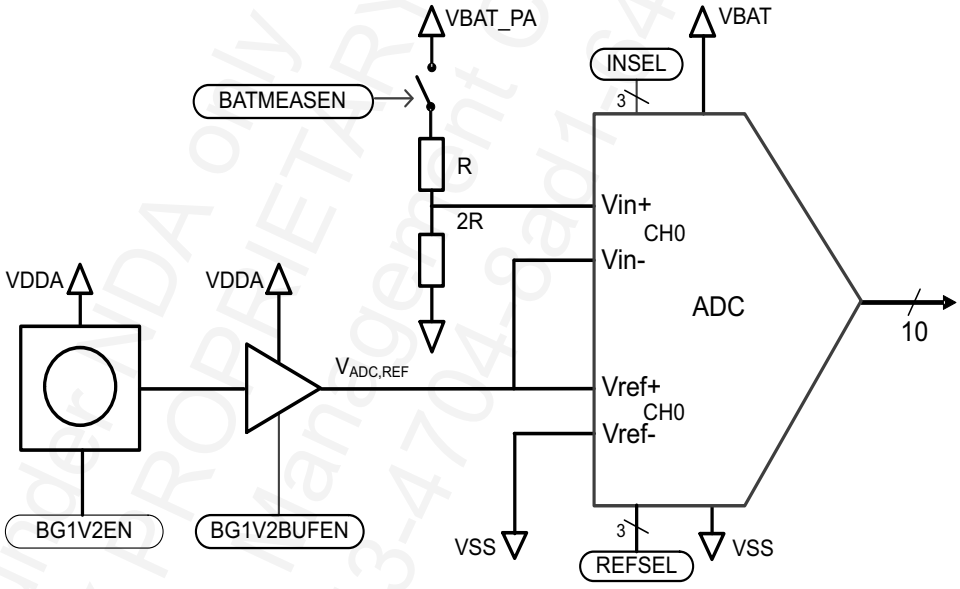


Fig 60. Battery supply voltage measurement

Similar to the default ADC input selection (INSEL = 000b), the default ADC reference selection (REFSEL = 000b) has to be used for battery voltage measurements.

The reference block is accommodated in the VDDA supply domain. The application software must turn on the VDDA supply (PCON0.VDDARGLEN = 1) before the supply voltage measurement unit can be used, considering the VDDA regulator start-up time $t_{VDDA,PON}$. A buffered band-gap provides the reference voltage for the ADC, $V_{ADC,REF}$. It must be switched on by setting BG1V2EN = 1 and BG1V2BUFEN = 1 in the register. The buffered reference voltage, $V_{ADC,REF}$ is assumed settled after $t_{BG,PON}$.

The battery voltage is scaled down via a switched resistive divider and is measured against the reference voltage for the best resolution. The measurement output is given by:

(34)

$$VBATmeas = ADCDATA \cdot \left(\frac{2 \cdot V_{ADC,REF}}{1024}\right) \cdot \frac{3}{2}$$

Excluding VDDA supply, band-gap and band-gap buffer power-up times, the time for a single conversion is:

(35)

$$t_{ADC,\,CONV} = t_{PON} + t_{SAMPLE} + t_{CONV} + t_{ADC,\,PDWN}$$

Before triggering A-D conversion for the battery voltage input, the battery voltage sensor (a voltage divider) has to be enabled by means of BATMEASEN bit set 1. When default sampling time used, SAMTIM=00b, and the Main RC oscillator selected as ADC clock source, CLKCON2.ADCCLKSEL=0, the ADC clock frequency will be $f_{ADC,CLK}$ = 4MHz. As typical battery measurement time is defined by 8 clock cycles for t_{PON} (2 µs), 4 cycles for t_{SAMPLE} (1 µs), 21 cycles for t_{CONV}, and one cycle for the power down, $t_{ADC,PDWN}$, of the ADC, the $t_{ADC,\,ONV}$ will be equal to 34 clock cycles duration, or 8.5 µs.

For achieving an optimal sampling rate, in software, it is recommended to poll the ADCCON.CONVSTART flag, or the ADC end-of-conversion interrupt flag IF_ADC. User interrupt from ADC testing the IF_ADC flag can also be used.

2.16.2 Temperature measurement

The NCF29A1 / NCF29A2 contains a build-in temperature measurement unit to get feedback of the environmental conditions of the key. The temperature sensor is powered on in case the temperature sensor is enabled by means of ADCCON.TSENSEN bit set 1.

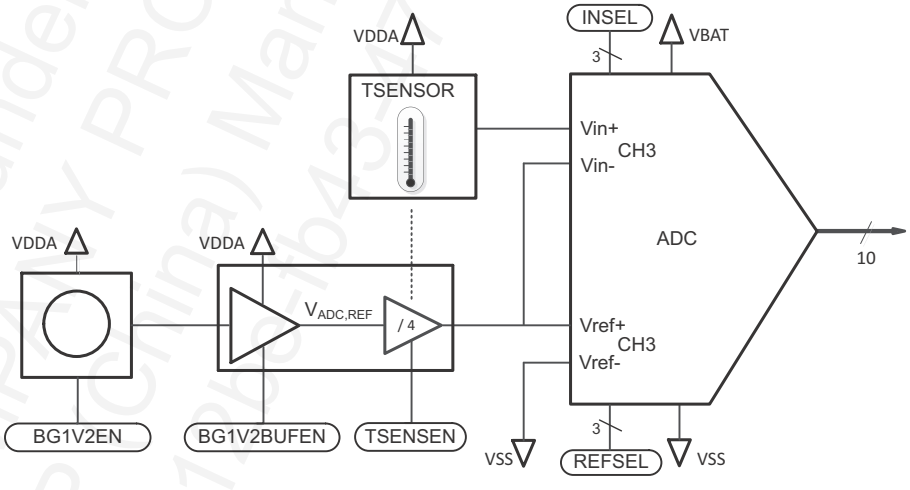


Fig 61. Temperature measurement

Before triggering AD-conversion, the ADC input (INSEL =011b) from temperature sensor has to be selected. Also, an optimized voltage reference must be chosen (REFSEL =011b) for measuring the temperature sensor differential output more accurately.

The measured differential voltage of the temperature sensor is in range between V_{TEMP_min} = -287mV and V_{TEMP_max} = +278mV, and for the obtained ADCDATA, it can be calculated as:

(36)

$$VTEMPmeas = (ADCDATA - 512) \cdot \left(\frac{2 \cdot V_{ADC,REF}}{4 \cdot 1024}\right)$$

The Temperature Sensor (TSENSOR) and reference block are accommodated in the VDDA supply domain. Hence, the application software must switch-on the VDDA supply (PCON0.VDDARGLEN = 1) before the temperature measurement unit and the ADC can be used, considering the VDDA regulator start-up time $t_{VDDA,PON}$. The buffered band-gap must be switched on via BG1V2EN = 1 and BG1V2BUFEN = 1 to provide the optimized voltage reference after $t_{BG,PON}$. Due to limited drive capability of the temperature sensor output, an increased ADC sampling time of at least 16 µs has to be chosen (SAMTIM[1:0] = 10b).

(37)

$$Temp[°C] = 25 + \frac{(ADCDATA - OFF_{TADC})}{G_{TADC}}$$

The output of the A-D converter, ADCDATA, is proportional to the temperature. The typical gain of the temperature sensor is G_{TADC}. Nominal temperature measurement offset at 25°C is specified as OFF_{TADC}. Best accuracy can be achieved by an application calibration measurement and compensation of a possible offset.

2.16.3 External Voltage measurement

The NCF29A1 / NCF29A2 features external voltage measurement for voltage levels applied between P13 and P14.

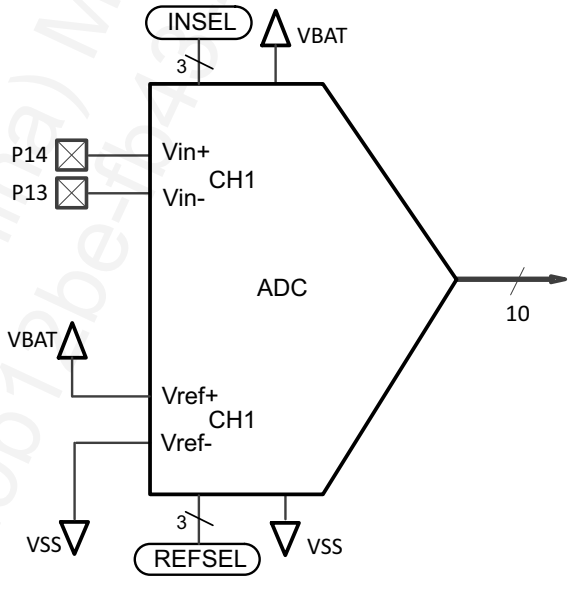


Fig 62. External voltage measurement - CH1

To enable the external input measurements, pins P14 and P13 have to be connected to the ADC as external voltage inputs. Application software is requested to use dedicated system-call to change the pin configuration. In the external voltage measurement, the buffered reference is used and the application is requested to do both, to enable the VDDA supply, the band-gap circuit with the output buffer, and to set the INSEL=001b and REFSEL (optionally, the SAMTIM) according to Table 152. After the measurement is done, the application software is requested to revert the P14 and P13 pin configuration by using dedicated system-call.

Three reference selections and thereby three dynamic ranges, are possible for the external voltage measaurements.The ADC reference settings REFSEL = 010b select two external pins P17_LED and P12 as Vref+ and Vref- levels. REFSEL = 001b offers dynamic range Vin_diff = ($-V_{BAT}$, $+V_{BAT}$) while selecting REFSEL=000b will enable for dynamic range Vin_diff = ($-V_{ADC,REF}$, $+V_{ADC,REF}$). Latter requires the reference block enabled as explained in Section 2.16.1 and Section 2.16.2.

The external voltage is directly measured against the selected reference voltage, Vref = Vref_ext, Vref = $V_{ADC,REF}$, or Vref = V_{BAT}, allowing for 10-bit resolution.

(38)

$$VEXTmeas = ADCDATA \cdot \left(\frac{2 \cdot V_{ref}}{1024}\right)$$

According to the limiting values, it is not allowed to apply negative voltages lower than -0.3V to any I/O pin, hence to P14, P13, P17_LED and P12.

For achieving an optimal sampling rate by software, it is recommended to use the ADC end-of-conversion interrupt flag, IF_ADC, and optionally, create and use dedicated interrupt routine.

2.16.4 RSSI measurement

The NCF29A1 / NCF29A2 features RSSI measurement of the LF Active received carrier for PKE distance approximation. The measurement setup with RSSI peak detectors voltage scaling, supply and the voltage sources are shown in Figure 63.

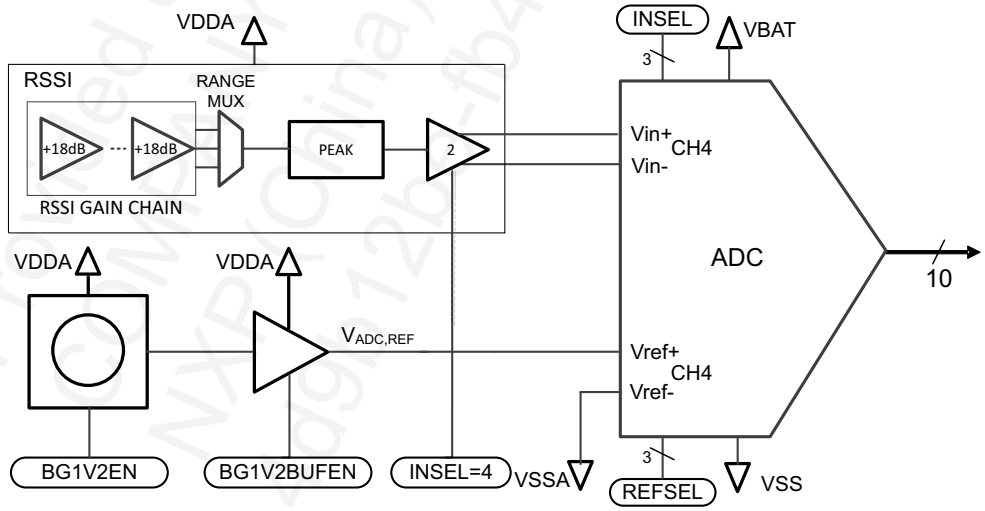


Fig 63. RSSI voltage management

Outputs from the RSSI peak detectors are amplified by roughly 2 (1.8/0.89).

Amplifying by 2 is enabling full-scale dynamic range and 10-bit conversion result, according to:

$$VRSSImeas = ADCDATA \cdot \frac{2 \cdot V_{ADC,REF}}{1024} \cdot \frac{1}{1,8} \quad (39)$$

To enable the RSSI measurements, application is requested to enable the VDDA regulator first, the RSSI signal chain, the Bandgap reference and the reference buffer. For the RSSI input, INSEL=100b and REFSEL=100b is dedicated.

For an accurate value of the $V_{RSSImeas}$, it is recommended to compensate each RSSI converted value for the RSSI channel offset. The RSSI channel offset shall be measured when no LF-signal input, rather DC-voltage input is applied to the RSSI chain. In this case, the equation above will include subtraction of the RSSI channel offset from ADCDATA.

2.16.5 ADC Registers

ADC access to configure the ADC and trigger measurements is done via ADCCON. The converted data is stored in ADCDAT. ADCCON and ADCDAT are described in Table 152 to Table 154.

The register ADCCON provides byte and word access.

Table 151. Word and byte access to the status register ADCCON

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ADCCON	ADCCONH	ADCCONL

Table 152. ADC control register ADCCON (reset value 00000000_0000xx00b)

Bit	Symbol	Access	Value	Description
15 to 13	INSEL[2:0]	R/W		ADC input selection
			000	Battery voltage measurement
			001	External input measurement, voltage applied on P14 and P13
			010	RFU
			011	Temperature sensor measurement
			100	RSSI measurement
			101 - 111	RFU
12 to 10	REFSEL[2 :0]	R/W		Reference selection
			000	Buffered bandgap reference voltage, $V_{ref} = V_{ADC,ref}$ (for battery voltage measurement)
			001	VBAT and VSS
			010	External reference, applied on P17_LED and P12
			011	Optimized reference selection for temperature measurement
			100	Buffered bandgap reference voltage, $V_{ref} = V_{ADC,ref}$ (for RSSI measurement)
			101 - 111	RFU

Table 152. ADC control register ADCCON (reset value 00000000_0000xx00b)

Bit	Symbol	Access	Value	Description
9 and 8	SAMTIM[1:0]	R/W		ADC sampling time selection[1]
			00	1 µs / 1.16 µs (Main RC / XO)[2] - 4 ADC clocks
			01	8 µs / 9.27 µs (Main RC / XO) - 32 ADC clocks
			10	16 µs / 18.55 µs (Main RC / XO) - 64 ADC clocks
			11	64 µs / 74.20 µs (Main RC / XO) - 256 ADC clocks
7	TSENSEN	R/W		Temperature sensor enable
			0	Temperature sensor disabled
			1	temperature sensor enabled
6	BATMEASEN	R/W		Battery voltage sensor enable
			0	Battery voltage sensor disabled
			1	Battery voltage sensor enabled
5	BG1V2BUFEN	R/W		Bandgap reference buffer enable
			0	Bandgap reference buffer off
			1	Bandgap reference buffer on (VDDA supply needed)
4	BG1V2EN	R/W		Bandgap reference enable
			0	Bandgap reference off
			1	Bandgap reference on (VDDA supply needed)
3 and 2	RFU	R0/W0		Reserved for future use
1	CONVRESET	R0/W		ADC Conversion Reset
			0	no effect
			1	Reset conversion; aborts a running conversion
0	CONVSTART	R/W		ADC Conversion Run/Start
			0	Write access: no effect Read access: no conversion running
			1	Write access: Start Conversion, triggers automatic power-on of ADC Read access: Conversion running

[1] For the conversion time, see t_{CONV}

[2] For the ADC clock source selection, see CLKCON2, ADCCLKSEL

The register ADCDAT provides byte and word access.

Table 153. Word and byte access to the status register ADCDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
ADCDAT	ADCDATH	ADCDATL

Table 154. ADC data register ADCDAT (reset value x0xxxx00_00000000b)

Bit	Symbol	Access	Value	Description
15	RFU	R		Reserved for future use
14	CONV_OV	R&C		Conversion overflow result (Read and Cleared)
			0	valid data
			1	previous data has not been read when new data is generated

Table 154. ADC data register ADCDAT (reset value x0xxxx00_00000000b)

Bit	Symbol	Access	Value	Description
13 to 10	RFU	R	-	Reserved for future use
9 and 8	ADCDATA[9:8]	R	00	Sign and MSB of the converted data
7 to 0	ADCDATA[7:0]	R	00	Lower (LSB) eight bits of data

2.17 HT calculation unit

If not used by the immobilizer, the HT calculation unit is controllable by the application for general purposes, e.g. in the context of keyless entry functions. The application program can operate the calculation unit in HT2 mode or in HT3 mode.

The calculation unit consists of a 64 bit shift register (HTSR) with linear feedback (LF) and nonlinear feedback (OWF, one way function) capabilities (see Figure 64).

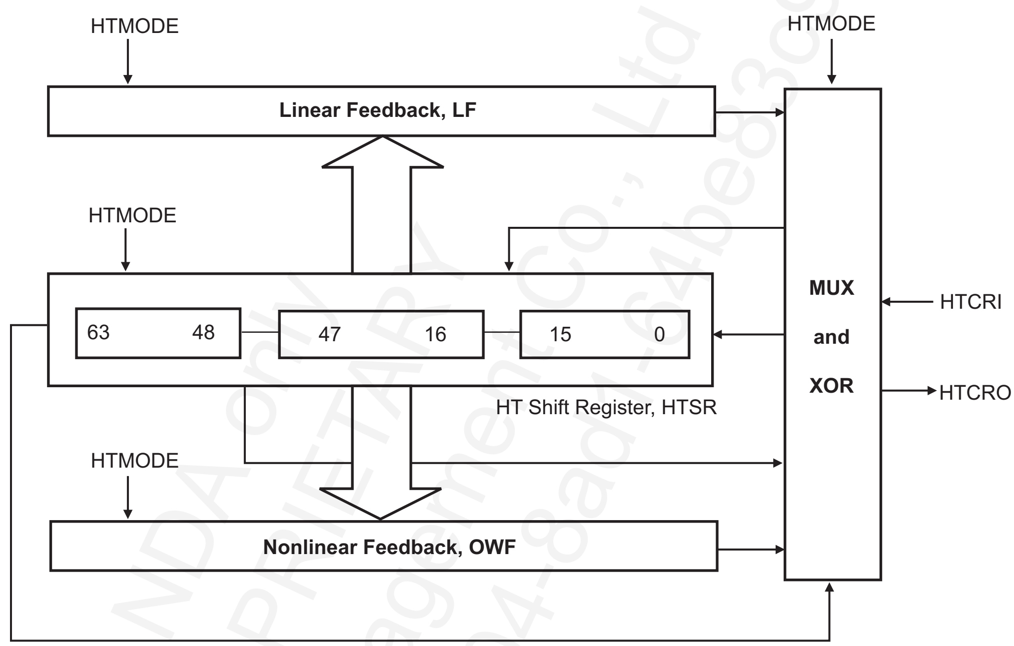


Fig 64. Block diagram of HT calculation unit

The identifier, random number, secret key and data processed shall be loaded into the calculation unit via the Immobilizer interface Unit (see Section 2.4.6).

2.17.1 HT2 mode

Operating the calculation unit in HT2 mode involves

- 48 bit secret key
- 32 bit identifier
- 32 bit random number

The algorithm operates on a 48 bit shift register. All values are fully determined by the application program.

The HT calculation unit initialization and operation in HT2 mode is provided by functions. Switching between the functions does not clock the calculation unit.

2.17.1.1 Load 16

This function is typically used to initialize the shift register bit by bit. The HT shift register (HTSR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their values are undefined (see Figure 65).

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 15 - 1

$(HTSR_{0}^{+}) \leftarrow (HTSR_{47})$

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 47 - 17

$(HTSR_{16}^{+}) \leftarrow (HTCRI)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG2}\ (HTSR^{+})$

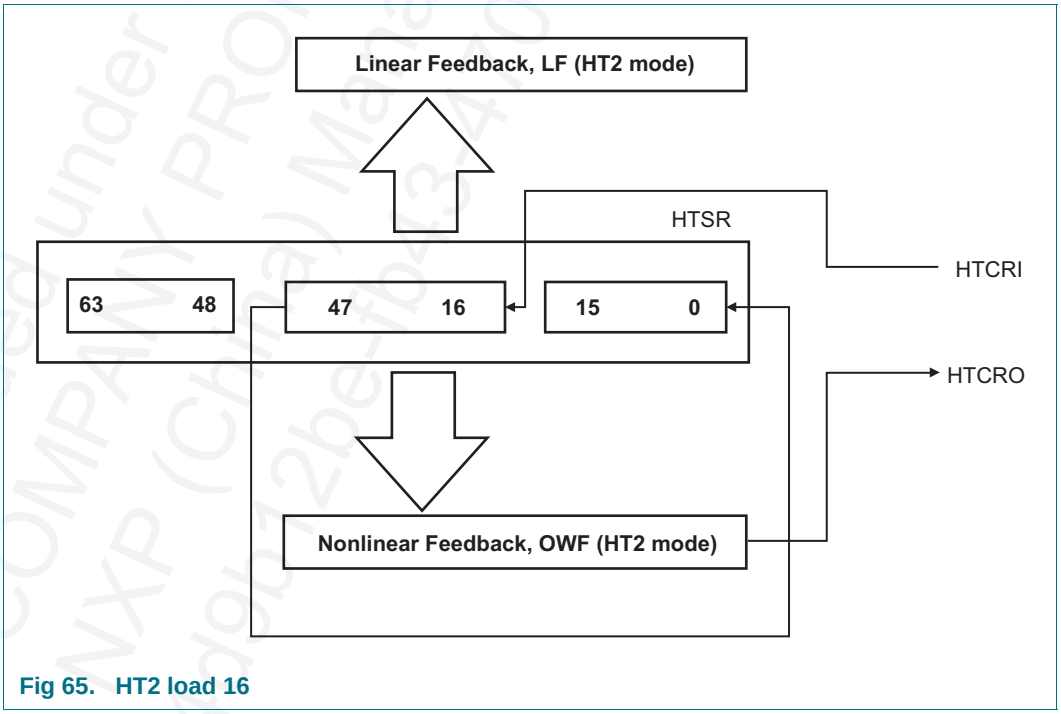


Fig 65. HT2 load 16

Load 0

This function is typically used to initialize the shift register bit by bit. The HT shift register (HTSR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined (see Figure 66). The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 47- 1

$(HTSR_{0}^{+}) \leftarrow (HTCRI)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG2}(HTSR^{+})$

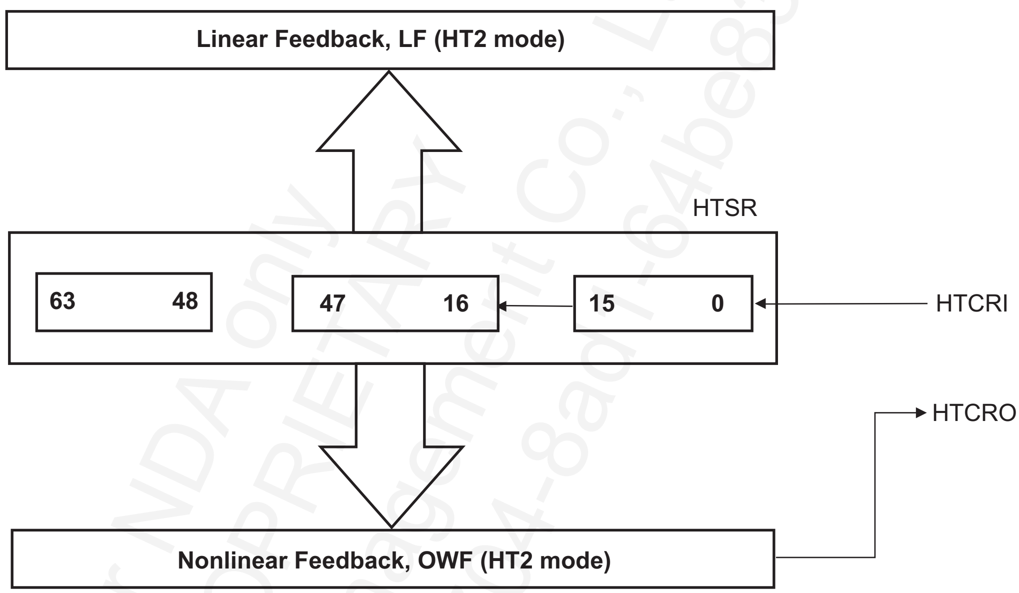


Fig 66. HT2 load 0

LF (linear feedback)

This function is typically used to convey the HT Shift Register (HTSR) bit by bit involving the linear feedback, which operates in HT2 mode. The Shift Register (SR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined (see Figure 67).

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 47- 1

$(HTSR_{0}^{+}) \leftarrow LF_{HITAG2}(HTSR)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG2}(HTSR^{+})$

Input data at HTCRI is ignored in this mode.

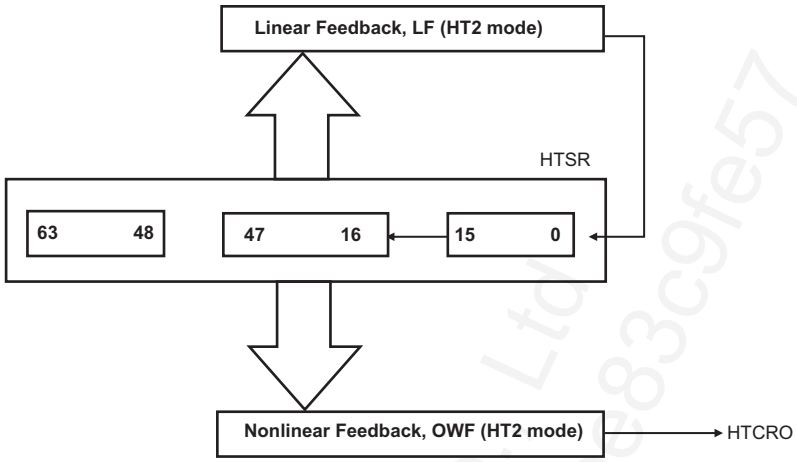


Fig 67. HT2 linear feedback

OWF (one way function, nonlinear feedback)

This function is typically used to convey the shift register bit by bit involving the nonlinear feedback, which operates in HT2 mode. The HT shift register (HTSR) is operated in 48 bit fashion, bit 48 to bit 63 are not applicable and their value is undefined (Figure 68).

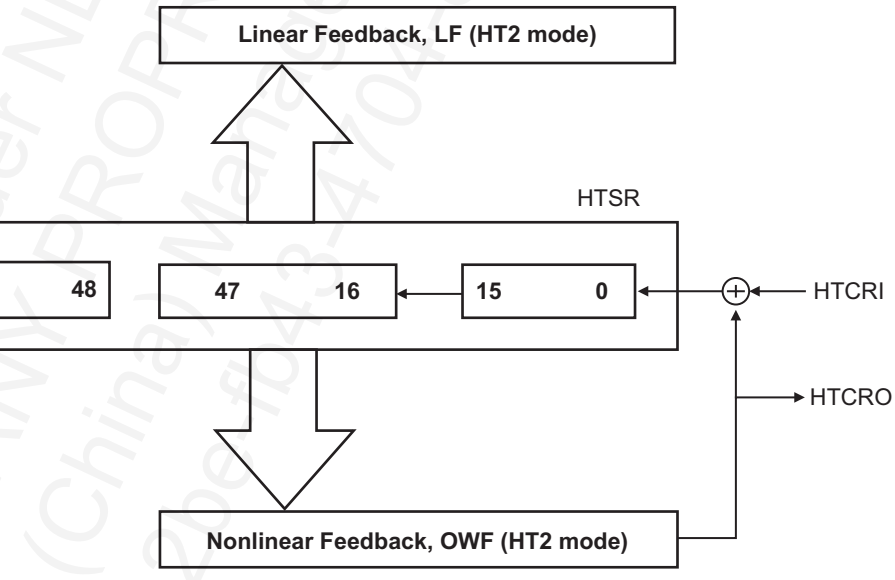


Fig 68. HT2 nonlinear feedback

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_N^+) \leftarrow (HTSR_{N-1})$; N = 47 - 1

$(HTSR_0^+) \leftarrow (HTCRI) \oplus OWF_{HITAG2}\ (HTSR)$

$(HTCRO^+) \leftarrow OWF_{HITAG2}\ (HTSR^+)$

2.17.2 HT3 mode

Operating the calculation unit in HT3 mode involves

- 96 bit secret key
- 32 bit identifier
- 64 bit random number

The algorithm operates on a 64 bit shift register. All values are fully determined by the application program.

The HT calculation unit initialization and operation in HT3 mode is provided by functions. Switching between the functions does not clock the calculation unit.

2.17.2.1 Load 16

This function is typically used to initialize the shift register bit by bit. The HT shift register (HTSR) is operated in 64 bit fashion (see Figure 69).

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 15 - 1

$(HTSR_{0}^{+}) \leftarrow (HTSR_{63})$

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 63 - 17

$(HTSR_{16}^{+}) \leftarrow (HTCRI)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG3}(HTSR^{+})$

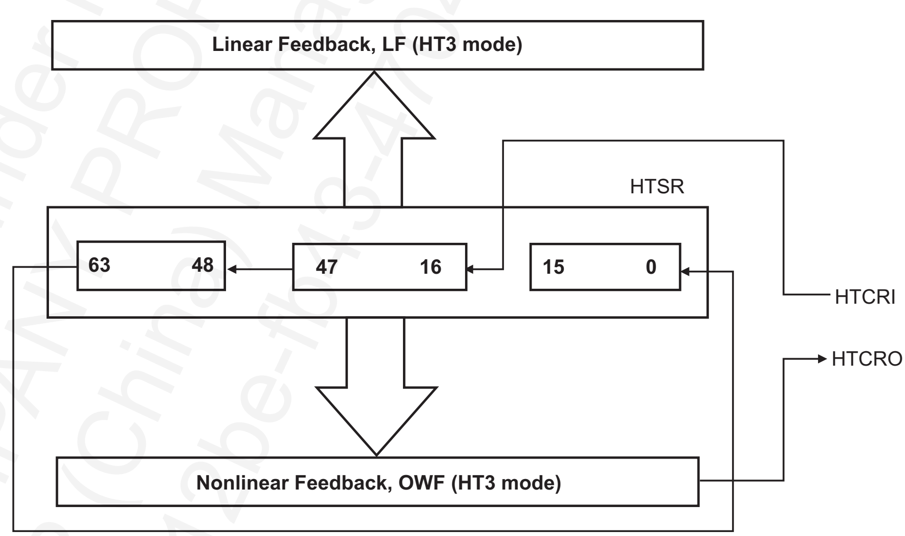


Fig 69. HT3 load 16

2.17.2.2 Load 0

This function is typically used to initialize the HT Shift Register (HTSR) bit by bit (see Figure 70).

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 63 - 1

$(HTSR_{0}^{+}) \leftarrow (HTCRI)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG3}(HTSR^{+})$

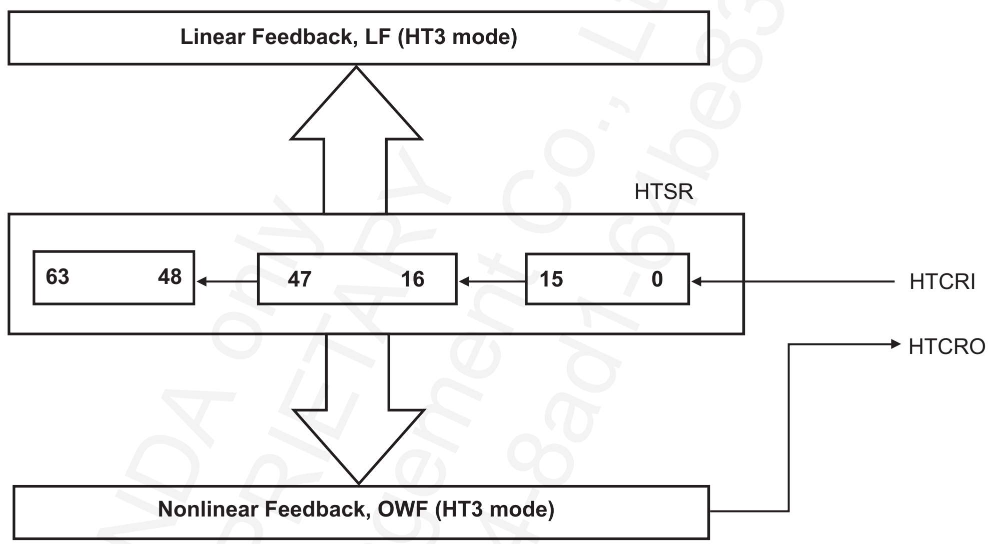


Fig 70. HT3 load 0

2.17.2.3 LF (linear feedback)

This function is typically used to convey the shift register bit by bit involving the linear feedback, which operates in Enhanced mode. The HT Shift Register (HTSR) is operated in 64 bit fashion (Figure 71).

The following course of events is triggered with each clock applied to the Calculation Unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 63 - 1

$(HTSR_{0}^{+}) \leftarrow LF_{HITAG3}(HTSR)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG3}(HTSR^{+})$

Input data at HTCRI is ignored in this mode.

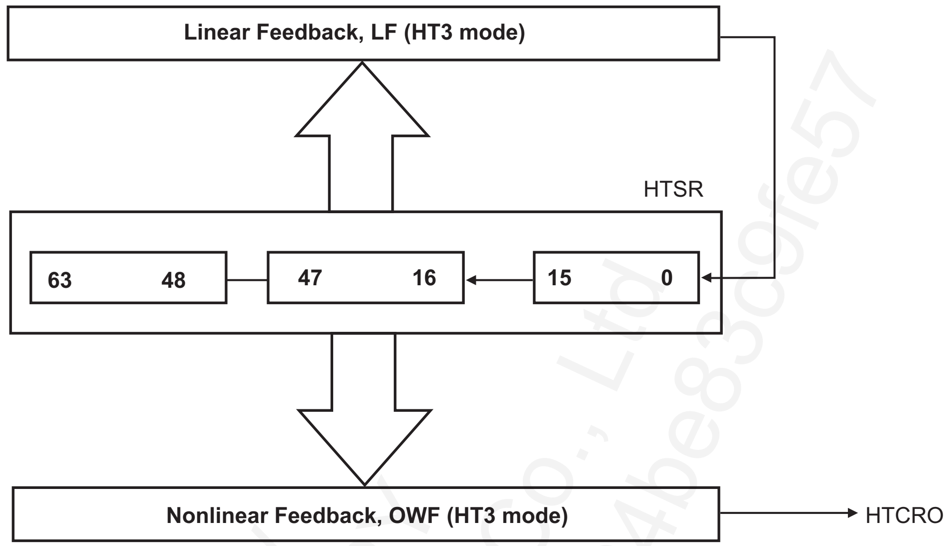


Fig 71. HT3 linear feedback

2.17.2.4 OWF (one way function, nonlinear feedback)

This function is typically used to convey the shift register bit by bit involving the nonlinear feedback, which operates in HT3 mode. The HT shift register (HTSR) is operated in 64 bit fashion (see Figure 72).

The following course of events is triggered with each clock applied to the calculation unit:

$(HTSR_{N}^{+}) \leftarrow (HTSR_{N-1})$; N = 63 - 1

$(HTSR_{0}^{+}) \leftarrow (HTCRI) \oplus (HTSR_{63}) \oplus OWF_{HITAG3}\ (HTSR)$

$(HTCRO^{+}) \leftarrow OWF_{HITAG3}\ (HTSR^{+})$

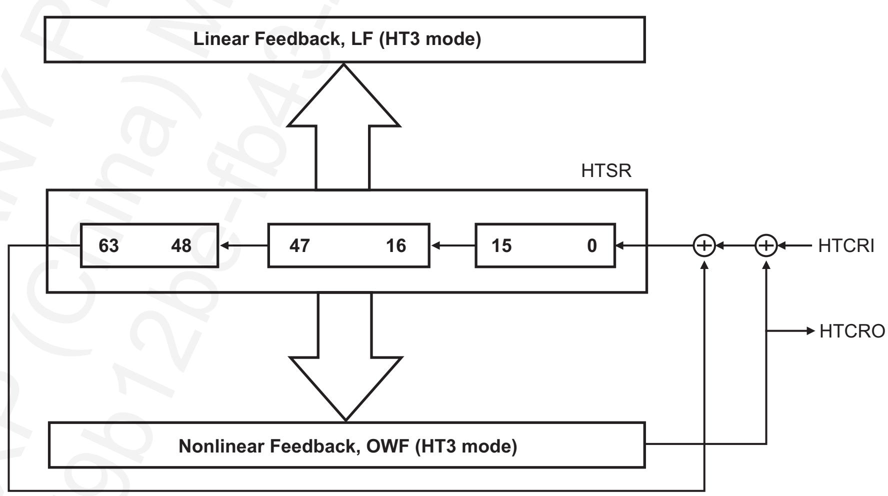


Fig 72. HT3 nonlinear feedback

2.17.3 Registers

The data exchange with the HT encryption unit (reading and writing) is performed via the register IIUDAT.

2.17.3.1 HT control register HTCON

The HT calculation unit is controlled via the HT control register HTCON.

Table 155. HT control register HTCON (reset value 08h)

Bit	Symbol	Access	Value	Description
7 and 6	RFU	R0/W0		Reserved for future use
5	HTEN	R/W		HT calculation unit enable
			0	Disable HT calculation unit
			1	Enable HT calculation unit
4 and 3	HTOSEL[1:0]	R/W		HT calculation unit output select
			00	Output: 0
			01	Output: HT calculation unit input (HTCRI, bypass mode)
			10	Output: HT calculation unit output (HTCRO)
			11	Output: HTCRI xor HTCRO
2 to 0	HTMODE[2:0]	R/W		HT calculation mode and function selection
			000	HT2: Load 16
			001	HT3: Load 16
			010	HT2: Load 0
			011	HT3: Load 0
			100	HT2: LF
			101	HT3: LF
			110	HT2: OWF
			111	HT3: OWF

HTEN, HT calculation unit enable

HTEN enables / disables the HT calculation unit. In case it is disabled, the unit is not clocked, however the registers in the calculation unit remain in their previous state.

HTOSEL[1:0], HT calculation unit output select

HTOSEL selects the output of the HT calculation unit which is the input for the IIU shift register and encoder. It provides means to enable / disable the output of the HT calculation unit, and also to bypass the encryption unit.

HTMODE[2:0], HT mode and function selection

HTMODE[0] selects the mode (HT2 or HT3), while via HTMODE[2:1] the respective function is chosen

- Initialization (load 0 and load 16)
- Linear feedback (LF)
- Nonlinear feedback (one way function, OWF)

The functions are available for HT2 and HT3.

2.18 AES calculation unit

The hardwired AES co-processor provides encryption with a fixed secret key length of 128 bits and forward encryption.

The co-processor operates with two internal 128 bit registers (AESKEYREG and AESDATAREG) for storage of the secret key and plain/enciphered data, respectively (Figure 73). Both registers have to be loaded prior to an AES calculation. Enciphered data supersedes initial plain data and can be retrieved from register AESDATAREG after the calculation. The content of AESKEYREG is not altered.

A reset function allows clearing of all registers and the internal state of the AES co-processor on request.

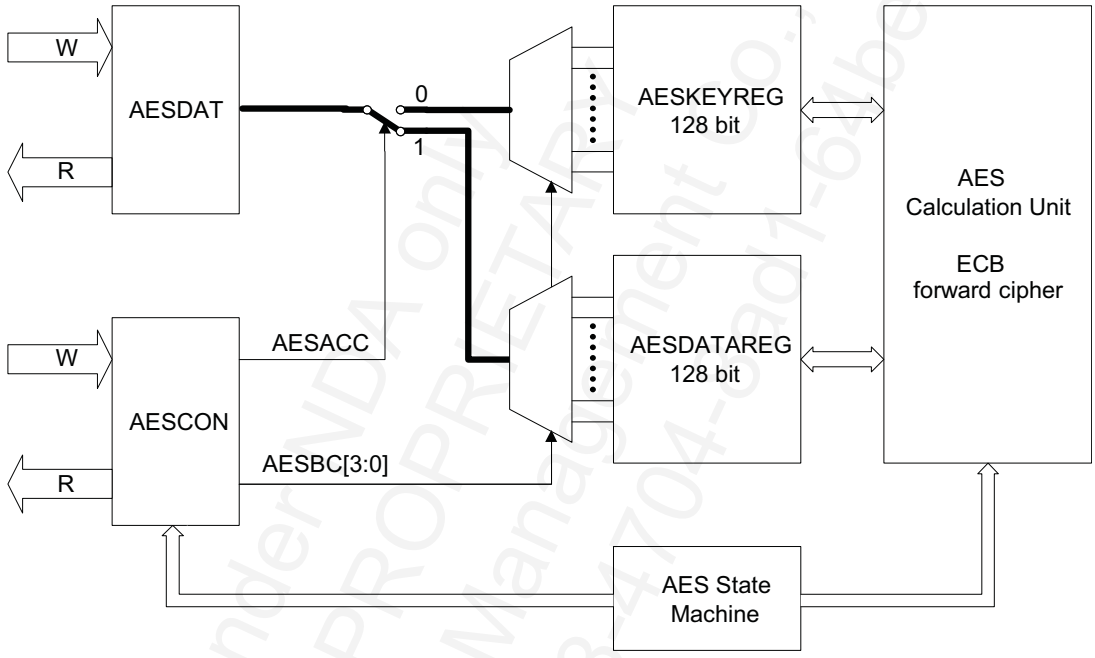


Fig 73. Block diagram of AES calculation unit

2.18.1 Modes

2.18.1.1 Electronic codebook mode (ECB)

The following steps have to be performed for a single AES calculation in Electronic Codebook Mode (ECB):

1. Load 16 bytes secret key into the internal AES register AESKEYREG
2. Load 16 bytes plain data into the internal AES register AESDATAREG
3. Start AES calculation
4. Retrieve enciphered data from AESDATAREG
5. If another calculation is desired with the same secret key, proceed with point 2

If consecutive calculations use the same secret key, it can be re-used without reloading.

2.18.1.2 Output feedback mode (OFB)

The following steps have to be performed for AES calculations in Output Feedback Mode (OFB):

1. ad 16 bytes secret key into the internal AES register AESKEYREG
2. Load 16 bytes initialization vector into the internal AES register AESDATAREG
3. Start AES calculation
4. Retrieve enciphered data from AESDATAREG and XOR it with plain text
5. Proceed with 3)

It is not necessary to reload AESDATAREG between several AES calculations as data stored in AESDATAREG at the end of one calculation is automatically used as input data for the next calculation.

2.18.2 Registers

2.18.2.1 AES data register AESDAT

This register provides the access to both the AESKEYREG and the AESDATAREG. It allows for reading these registers or for writing the registers with an initial value, dependent on the settings.

The AES data register provides byte and word access (Table 156). Any read access to AESDAT while an active AES calculation is ongoing yields an undefined result.

Table 156. Word and byte access to the AES data register AESDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
AESDAT	AESDATH	AESDATL

Table 157. AES data register AESDAT (reset value xxxxh)

Bit	Symbol	Access	Value	Description
15 to 0	AESDATA[15:0]	R/W		AES data

2.18.2.2 AES control register AESCON

The AES calculation unit is controlled via the AES Control Register AESCON.

Table 158. AES control register AESCON (reset value 00h)

Bit	Symbol	Access	Value	Description
7	AESRUN	R/W		AES run
			0	Read: AES calculation finished Write: No effect
			1	Read: AES calculation in operation Write: Start AES calculation
6	AESRST	R0/W		AES reset
			0	No effect
			1	Reset

Table 158. AES control register AESCON (reset value 00h)

Bit	Symbol	Access	Value	Description
5	RFU	R0/W0		Reserved for future use
4	AESACC	R/W		AES register access
			0	Select AESKEYREG, write only
			1	Select AESDATAREG, read and write
3 to 0	AESBC[3:0]	R/W		AES register byte counter
			0000	Addressed via AESDL: Byte 0 Addressed via AESD: Word 0
			0001	Addressed via AESDL: Byte 1 Addressed via AESD: Word 0
			0010	Addressed via AESDL: Byte 2 Addressed via AESD: Word 1
			0011	Addressed via AESDL: Byte 3 Addressed via AESD: Word 1
			0100	Addressed via AESDL: Byte 4 Addressed via AESD: Word 2
			0101	Addressed via AESDL: Byte 5 Addressed via AESD: Word 2
			0110	Addressed via AESDL: Byte 6 Addressed via AESD: Word 3
			0111	Addressed via AESDL: Byte 7 Addressed via AESD: Word 3
			1000	Addressed via AESDL: Byte 8 Addressed via AESD: Word 4
			1001	Addressed via AESDL: Byte 9 Addressed via AESD: Word 4
			1010	Addressed via AESDL: Byte 10 Addressed via AESD: Word 5
			1011	Addressed via AESDL: Byte 11 Addressed via AESD: Word 5
			1100	Addressed via AESDL: Byte 12 Addressed via AESD: Word 6
			1101	Addressed via AESDL: Byte 13 Addressed via AESD: Word 6
			1110	Addressed via AESDL: Byte 14 Addressed via AESD: Word 7
			1111	Addressed via AESDL: Byte 15 Addressed via AESD: Word 7

AESRUN, AES run

AESRUN is used to start the AES calculation and to monitor its execution status. The internal AES registers (AESKEYREG and AESDATAREG) shall be loaded prior to the start of calculation. The bit AESRUN stays 1 as long as the AES calculation continues. The bit is automatically cleared when the calculation is finished. Writing a zero to bit AESRUN does not have any effect.

Once AESRUN is set any write access to register AESDAT and AESCON is inhibited. The only exception is bit AESRST, which can be used to interrupt the current calculation. Any read access to AESDAT while an active AES calculation is ongoing yields an undefined result.

AESRST, AES reset

AESRST is intended to clear the internal AES registers AESKEYREG and AESDATAREG. This can be used to clear the content of the internal AES registers after a calculation in order to prevent that a program that is executed thereafter has any unintended access to secret information used before.

Setting bit AESRST while an AES calculation is ongoing causes an immediate interruption of the calculation. If bit AESRUN and AESRST are set at the same time, bit AESRST has priority and the AES calculation is not started.

AESACC, AES register access

AESACC selects which internal register is accessed through the special function register AESD and AESDL. Any read or write access to AESD operates directly on the internal AES registers.

The internal register AESKEYREG does not support read access, the secret key can only be written. AESDATAREG has full read and write access and supports read-modify-write operations.

Once the AES calculation has started any read access of bit AESACC yields '0'. After completion of the AES calculation AESACC is undefined.

AESBC[3:0], AES register byte counter

AESBC[3:0] controls which of the 16 bytes of the internal AES register is addressed by a read or write access through register AESDAT.

A byte access to AESDATL uses AESBC[3:0] to select a byte whereas a word access to AESDAT ignores bit AESBC[0] and uses AESBC[3:1] as a pointer to the respective word. Bit AESBC[0] is treated as zero in this case regardless of the current value. Hence, a word access at an odd byte address of the internal AES registers is not supported.

The AES register byte counter features an auto-increment after every read or write access to register AESDAT. A byte access causes an increment by 1 and a word access an increment by 2 (independent of AESBC is even or odd).

Once the AES calculation has started any read access of the bits AESACC and AESBC yields 0. After completion of the AES calculation these bits are undefined.

2.19 Random number generator

The device features a random number generator for seed generation of HT2-E, HT3 and/or AES calculations (see Figure 74). The random number generator can be used as not-deterministic (NRNG) as well as pseudo random number generator (PRNG). All generated random numbers have a size of 16 bits.

The NRNG is also suitable to generate a seed for the PRNG for fast generation of subsequent random numbers.

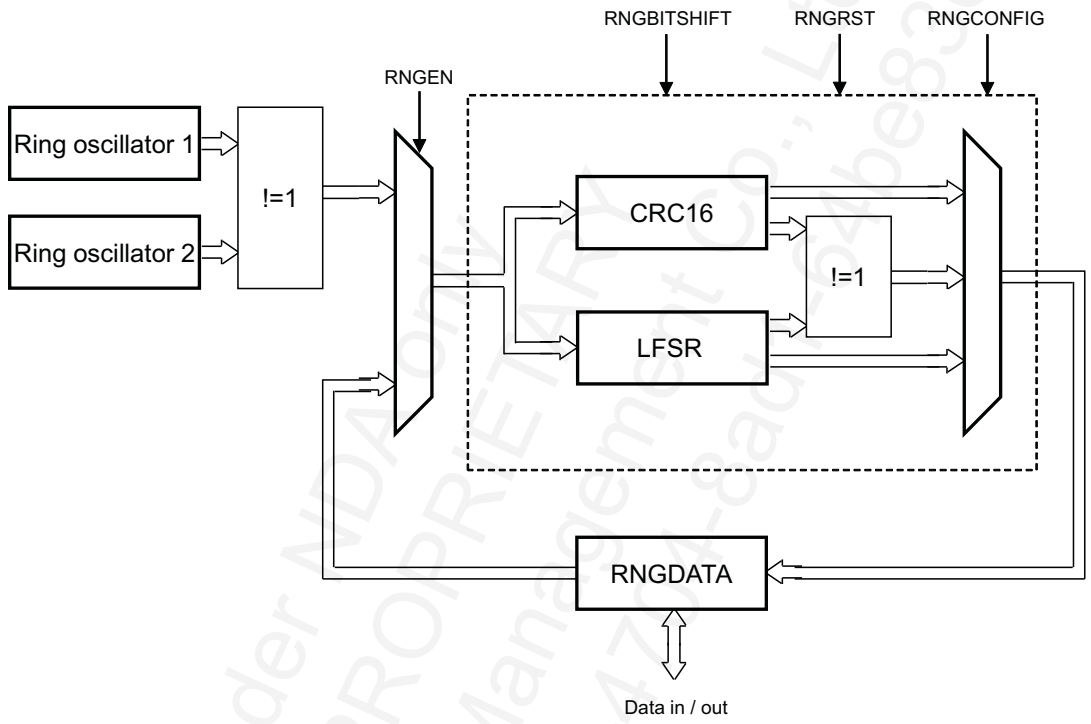


Fig 74. Random number generator block diagram

2.19.1 Ring oscillators

Two free running ring oscillators serve as entropy source. Performing an XOR operation on these two signals, a random bit stream is generated, from which a configured number of bits are sampled. These bits are shifted in a 16 bit cyclic redundancy check (CRC) register or in a 16 bit linear feedback shift register (LFSR), where they are post-processed. RNG1CLK and RNG2CLK shall not be used as timer clock source by the application.

2.19.2 Post-processing

The oscillating entropy signal coming from the ring oscillators is post-processed to increase the amount of random numbers that can be generated. Three post-processing approaches are available (selected via RNGCONFIG).

- 16 bit cyclic redundancy check register (CRC16)
- 16 bit linear feedback shift register (LFSR)

- both the CRC16 and the LFSR register (hybrid mode)

In the first two cases the 16 bit random number is read out directly from the registers, while in the last scenario the random number is generated by an XOR operation on the values of both registers.

2.19.2.1 Cyclic redundancy check register

The 16 bit cyclic redundancy check (CRC16) implements the polynomial

$x^{16} + x^{12} + x^{5} + 1$

The register can be supplied with random bits from the ring oscillators or can be used as linear feedback shift register with length 2^{15}-1 in PRNG mode. Since the polynomial is not irreducible the CRC used as LFSR has not a period of maximum length.

Before the PRNG can be used the CRC16 register shall hold an initial value. The initial values 0000h and F80Fh have to be avoided since they cause the CRC16 to stuck at the corresponding value. After power-on reset the CRC16 holds the value AAAAh.

When the CRC16 is used as NRNG all initial values are allowed.

When the CRC16 is used as PRNG two different sets of random numbers can be generated dependent on the initial value. Both sets have a period of 2^{15}-1 and the two sets do not have any random numbers in common. Example initial values for the first set are all powers of 2 (2^{1} … 2^{15}) and for the second set AAAAh.

2.19.2.2 Linear feedback shift register

The linear feedback shift register (LFSR) implements the polynomial

$x^{16} + x^{14} + x^{13} + x^{11} + 1$

The register can be supplied with random bits from the ring oscillators (RNGEN = '1') or can be used as linear feedback shift register with length 2^{16}-1 in PRNG mode (maximum length LFSR).

When used as PRNG the initial value 0000h has to be avoided since otherwise the LFSR cannot produce any other values. The application shall not use the setting RNGBITSHIFT = 01b (17 bit shift), otherwise the RNG cannot generate all 2^{16}-1 different random numbers.

When used for NRNG post-processing all initial values are allowed.

After power-on reset the LSFR holds the value AAAAh.

2.19.2.3 Hybrid mode

The hybrid mode performs an XOR operation on the outputs of the CRC16 and the LFSR and combines thus both methods described in the previous sections.

All restrictions mentioned for CRC16 and LSFR have to be considered also in hybrid mode.

When used as PRNG the period of the random numbers is $(2^{15}-1)*(2^{16}-1)$.

2.19.2.4 Random number generation

In order to generate a non-deterministic random number (NRNG), the following steps have to be executed:

1. Activate the ring oscillators (RNGEN = 1)
2. Wait $t_{RNG,Sett}$ until the ring oscillators have settled.
3. If desired write an initial value to the CRC16 and/or LSFR (optional step)
4. Start the RNG (RNGRUN = '1'). When the operation is finished a new 16 bit random number can be fetched from RNGDAT. The quality of the random number increases when starting the RNG several times. It is recommended to start the RNG nine times for generating a NRNG.
5. If no further random number is required, deactivate the ring oscillators (RNGEN = '0')

In order to generate a pseudo random number (PRNG), the following steps have to be executed:

1. Write a valid initial value to the CRC16 and/or LSFR. In case the initial value was generated with the NRNG the application has to check that the CRC16 or the LSFR does contain valid seed values. When the hybrid mode is selected this shall be checked for the CRC16 and LSFR separately.
2. Start the RNG (RNGRUN = '1'). When the operation is finished a new 16 bit random number can be fetched from RNGDAT.

The following operation modes are recommended:

- NRNG: Hybrid mode, 17 bit shifts
- PRNG: LSFR mode, 16 bit shifts, if little dependency between consecutive random numbers is required
- PRNG: LSFR mode, 1 bit shift, if dependency between consecutive numbers is of less importance (fastest operation mode)

2.19.3 Registers

2.19.3.1 RNG data register RNGDAT

This register provides access to both the CRC register and the LFSR register. It allows for reading 16 bit random numbers or for seeding the RNG with an initial value.

The random number generator data register RNGDAT provides byte and word access (Table 159).

Table 159. Word and byte access to the random number generator data register RNGDAT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
RNGDAT	RNGDATH	RNGDATL

Table 160. Random number generator data register RNGDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
15 to 0	RNGDATA[15:0]	R/W		Random number generator data

RNGDATA[15:0], Random number generator data

RNGDATA is read either from the CRC16 register or from the LFSR register, depending on the setting of RNGCONFIG. When writing seed data to RNGDATA, the value is assigned to either one or both the CRC16 register and the LFSR register, depending on the setting of RNGCONFIG. Reading and writing RNGDATA is only allowed when the random number generator is not running.

2.19.3.2 RNG control register RNGCON

The random number generator control register RNGCON is used to configure and operate the random number generator.

Table 161. Random number generator control register RNGCON (reset value 26h)

Bit	Symbol	Access	Value	Description
7	RNGRUN	R/W		Random number generator run
			0	Read: Random number generation finished Write: No effect
			1	Read: Random number generation in operation Write: Start random number generation
6 and 5	RNGBITSHIFT[1:0]	R/W		Number of bit shifts
			00	16
			01	17
			10	19
			11	1
4 and 3	RNGCONFIG[1:0]	R/W		Random number generator configuration
			00	Initialization mode
			01	Cyclic redundancy check (CRC16)
			10	Linear feedback shift register (LFSR)
			11	Hybrid (CRC16 xor LFSR)
2	RNGTRIMOSC	R/W		Oscillator trim setting
			0	Main setting
			1	Alternative setting
1	RNGEN	R/W		Random number generator enable
			0	PRNG mode Ring oscillators disabled RNG is running with PCLK
			1	NRNG mode Ring oscillators enabled RNG is running with REFCLK
0	RNGRST	R0/W		Random number generator reset
			0	No effect
			1	Reset

RNGRUN, Random number generator run

RNGRUN is used to start generating a new 16 bit random number. During calculations RNGRUN is set indicating that the RNG is busy. As long as RNGRUN is set, any write access to registers RNGDAT and RNGCON is inhibited. The only exception is bit RNG_RST, which can be used to stop a running operation.

RNGRUN is cleared automatically and the RNG interrupt flag IF_RNG is set when a new random number is available.

RNGCONFIG, Random nunber generator configuration

RNGCONFIG is used to select the type of RNG for generating random numbers. Additionally, RNGCONFIG is used to select the internal register(s) for read and write access via RNGDAT.

Setting the random number generator in initialization mode (RNGCONFIG = 00) and enabling the ring oscillators (RNGEN = 1) initializes the RNG automatically. During this initialization, the RNG starts nine times in hybrid mode for generating a non-deterministic random number (NRNG) with 17 bit shifts. The setting of RNGBITSHIFT[1:0] is ignored. The RNG oscillators keep activated (RNGEN = 1) after finishing the automatic initialization.

Each time the device wakes-up the BOOT routine starts the automatic initialization to generate a seed. The seed becomes valid after RNGRUN is set to 0. The random number generator can be reset after booting, thus refusing the seed calculation.

RNGBITSHIFT[1:0], Number of bit shifts

RNGBITSHIFT selects the number of bit shifts that are applied to generate a new 16 bit random number. The setting is used in both NRNG and PRNG mode.

RNGTRIMOSC, Oscillator trim settings

Two oscillator trim settings are provided, which give two different pairs of RNG oscillator frequencies.

RNGEN, Random number generator enable

RNGEN is used to enable the ring oscillators and to switch the RNG from PRNG to NRNG mode.

In case RNGEN is not set, the ring oscillators are turned off and the RNG is used as PRNG, generating new 16 bit random numbers by shifting the value of the registers according to the number of shifts configured in the control register.

RNGRST, random number generator reset

RNGRST resets the CRC16 register and the LFSR register, independent of the RNGCONFIG settings.

Setting bit RNGRST while the RNG operation is ongoing causes an immediate interruption. If bit RNGRUN and RNGRST are set at the same time, bit RNGRST has priority and the RNG is not started.

2.20 Registers for mathematical/logical operations

2.20.1 Bit swap register BITSWAP

The bit swap register BITSWAP is provided to change the bit order of a byte. A byte is written to register BITSWAP first. After writing, it is swapped. If it is read again from the same location, the bit order is reversed.

The application shall not use read-modify-write instructions with this register.

Table 162. Bit swap register BITSWAP (reset value xxh)

Bit	Access	Bit order write access	Bit order read access
7	R/W	BITSWP[7]	BITSWP[0]
6	R/W	BITSWP[6]	BITSWP[1]
5	R/W	BITSWP[5]	BITSWP[2]
4	R/W	BITSWP[4]	BITSWP[3]
3	R/W	BITSWP[3]	BITSWP[4]
2	R/W	BITSWP[2]	BITSWP[5]
1	R/W	BITSWP[1]	BITSWP[6]
0	R/W	BITSWP[0]	BITSWP[7]

2.20.2 Bit count register (parity generator) BITCNT

The bit count register BITCNT counts the number of bits being '1' in an input byte or input word.

The bit count register BITCNT provides byte and word access. In case of byte access, the unused input byte is set to 0. The application shall not use read-modify-write instructions with this register.

Table 163. Word and byte access to bit count register BITCNT

Word Register	Byte 1 (MSByte)	Byte 0 (LSByte)
BITCNT	BITCNTH	BITCNTL

If a byte/word is written to BITCNT it is evaluated immediately and the number of bits with content '1' can be read back from BITCNTL, independent of whether BITCNT, BITCNTH or BITCNTL was used as data input.

Table 164. Bit count register BITCNT (reset value 0000 0000 000X XXXXb)

Bit	Symbol	Access	Value	Description
15 to 5	BITCNT[15:5]	R0/W		Write: Input value, bits 15 to 5 Read: Always 0
4 to 0	BITCNT[4:0]	R/W		Write: Input value, bits 4 to 0 Read: Bit count value

The 11 most significant bits BITCNT[15:5] always read '0', while BITCNT[4] always reads '0' if a byte calculation was performed. Therefore, the application does not need to mask the read value before further processing.

Example: The following tasks can be accomplished with this register:

- Check a data byte/word versus a known byte or bit mask: XOR the data byte/word with the mask and write the result into register BITCNT. The result is the number of bits unequal to the expected value or bit mask.
- Determine the parity of a byte/word: If the bit BITCNT[0] reads a '1', the input byte/word has an odd number of '1's.
- Determine whether a byte is fully set: The bit BITCNT[3] is only '1', if the value of the provided input byte is FFh.
- Determine whether a word is fully set: The bit BITCNT[4] is only '1', if the value of the provided input byte is FFFFh.

2.20.3 CRC register

The NCF29A1 / NCF29A2 supports an 8 bit CRC polynomial for HT-Pro2 applications and user defined RKE frames. It is based on the polynomial:

$$x^8 + x^2 + x + 1 \tag{40}$$

The CRC value is stored in a CRC data register. The CRC data register can be initialized and read by directly accessing the data register CRCDAT.

An update of the CRC data register with new data according to the CRC polynomial takes place by writing to the data input register CRC8DIN. The CRC calculation is performed byte-wise bit parallel in way that is equivalent to the bit serial calculation using the CRC8DIN data in MSB to LSB bit order.

2.20.3.1 CRC data register CRCDAT

CRCDAT stores the CRC value and can be read or written for CRC initialization.

According to the HT-Pro2 protocol, CRCDAT shall be loaded with the initial value 00h before data is exchanged.

Table 165. CRC data register CRCDAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 0	CRCDATA[7:0]	R/W		CRC result register

2.20.3.2 CRC8 data input register CRC8DIN

CRC8DIN is provided to add data to the CRC calculation. Any write access to CRC8DIN updates CRCDAT with the newly calculated CRC value considering CRC8DIN according to the 8 bit CRC polynomial.

Table 166. CRC8 data input register CRC8DIN (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	CRC8DIN[7:0]	W		CRC 8 data input value

2.21 Motion sensor

The device provides the capability to operate with an external Motion Sensor component via the dedicated GPIO Pin P21_MD (rolling-ball movement sensor). The main anticipated use of this feature is to enable the LF Active frontend to be completely de-activated if the key has not been moved for a specific period of time. The primary benefits of this feature are:-

- Reduction in standby current when the key is known to be inactive, leading to increased battery life and/or smaller batteries.
- Increased resistance to relay station attack.

2.21.1 Motion Sensor Physical Interface

The basic concept of operation of the interface to the motion sensor itself is as follows:

- The external sensor behaves like a digital switch.
- The rest position of the switch may be either open or closed.
- The device provides an internal switchable pull up resistor and pull down resistor.
- The device may also operate with an external pull up resistor.

2.21.2 Motion Sensor Functional Summary

The device provides internal logic implemented in the pre-processor power domain to interface to the motion sensor device which has the following key features:-

- An edge detector capable of detecting rising or falling edges on the Motion Sensor input.
- A Low Power RC Oscillator (180 kHz) clocked counter to count the period of time elapsed since last motion was detected.
- A CPU controllable threshold for the counter, variable from 2 seconds to 126 seconds in 2 second steps, to determine the length of time which must elapse without motion for motion to be interpreted as having ceased.
- A state machine based control function to assert and clear wakeups and interrupts to the CPU and to control the power to the LF Active frontend.
- Programmable wakeups & interrupts for “motion” and “motion ceased” events.
- Programmable LF Active power-down and power-up enables.
- A CPU-controllable reset to the No-Motion Counter via the SFR interface.
- A frequency compensation capability to increase the absolute accuracy of timer measurements for variable Low Power RC Oscillator clock frequencies.

2.21.3 Detailed Functional Description

2.21.3.1 Top Level Enable

The entire module is enabled by the SFR bit MSI_EN. Unless activated by this bit the edge detect, timer and state machine functions are disabled. The SFR interface however remains activated.

2.21.3.2 Mode Of Operation

If the module is enabled it may be operated either as a motion sensor interface (primary function) or alternatively as an auxiliary timer. This is controlled by SFR bit MSI_MODE.

2.21.3.3 Motion Sensor Mode

The MSI contains an internal “Idle” Timer having the following properties:

- The “Idle” Timer is always reset to zero by any motion (as long as MSI_MODE is enabled).
- As long as no motion is observed, the “Idle” Timer counts up in 2 second increments, the time since last motion was observed.
- The “Idle” Timer continues counting to a SFR programmable threshold.
- On reaching the threshold the “Idle” Timer stops which indicates that the tag has been motionless for the programmed time.

The MSI contains a State Machine which

- Inhibits the entire Motion Sensor Mode of operation if not enabled by SFR Bit MSI_MODE=0
- If enabled, remains in a state where it cannot control LF Active Power Down until SFR Bit MSI_LFA_PD_EN is asserted. In this state the idle timer is inhibited
- Enables the Idle Timer and waits for the timer to reach its programmed threshold.

2.21.3.4 Motion Sensor Input Edge Detection

This block generates a single positive going Low Power RC Oscillator Clock pulse whenever a positive or negative going edge is detected on the motion sensor input.The output from this block is ORed with the timer clear signal from the SFR interface and used as a clear for the motion timeout counter.

2.21.3.5 Divider

The divider block is clocked by the LPRCOsc Clock with nominal 180 kHz frequency and its purpose is to generate a 1Hz clock pulse for the Idle Timer. It has the following stages:-

- An initial variable divider (from 82 to 97 – nominal 90) to 500us nominal period followed by a divide by 2 to a nominal 1ms period.
- A further divide by 50 to a nominal 50ms period followed by
- A further divide by 20 to a nominal 1s period.

2.21.3.6 Low Power RC Oscillator Frequency Calibration

Depending on the measured or calibrated value determined for the actual value of the clock frequency of the LPRC oscillator alternative values of PRECON6 LPRC_CAL[3:0] may be used to compensate for the actual LPRC frequency as defined in the following table.

Table 167. Pre-divider LPRC Oscillator Frequency Calibration

LPRC_CAL[3:0]	Pre-Divider Value	Total Divide Value	Actual LPRC Osc Freq
0x0	97	388000	194kHz
0x1	96	384000	192kHz
0x2	95	380000	190kHz
0x3	94	376000	188kHz
0x4	93	372000	186kHz
0x5	92	368000	184kHz
0x6	91	364000	182kHz
0x7	90	360000	180kHz
0x8	89	356000	178kHz
0x9	88	352000	176kHz
0xA	87	348000	174kHz
0xB	86	344000	172kHz
0xC	85	340000	170kHz
0xD	84	336000	168kHz
0xE	83	332000	166kHz
0xF	82	328000	164kHz

Through the use of the LPRC_CAL[3:0] input - actual values of LPRC Oscillator frequency from 164kHz to 194kHz may be compensated to achieve an internal Idle Timer clock of 0.5Hz

2.21.3.7 State Machine

The following diagram illustrates the State Transitions implemented by the Motion Sensor interface State Machine.

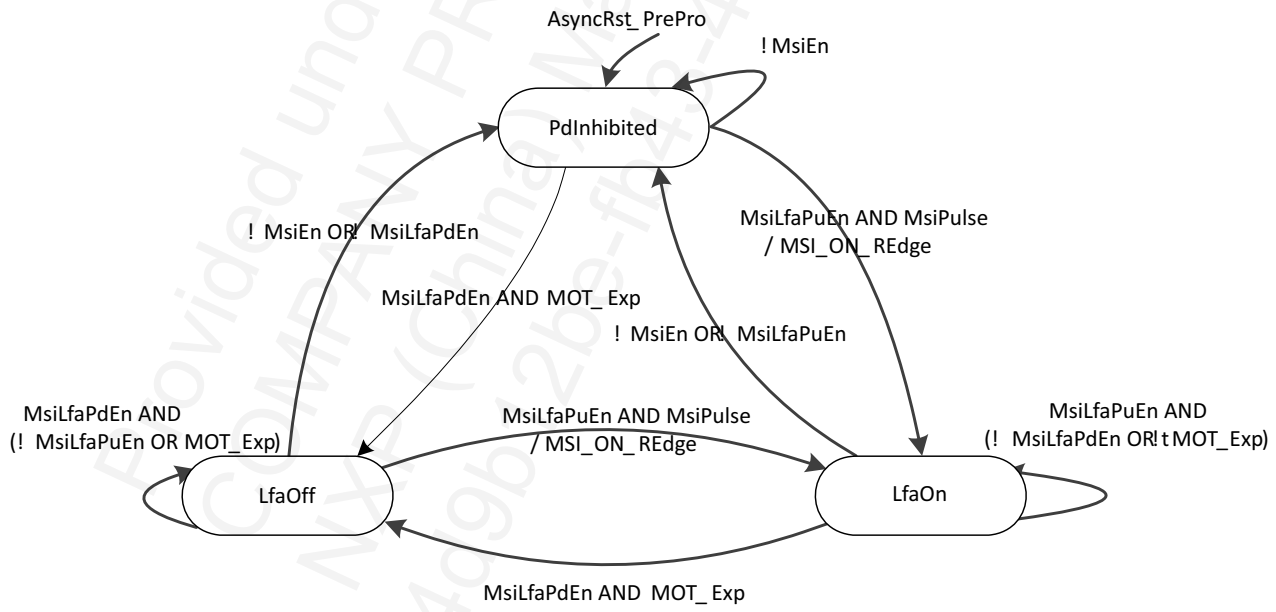


Fig 75. State Machine Transition Diagram

2.21.3.8 Interrupts and Wakeups

The Motion Sensor Interface can generate a single wakeup and a single interrupt for either motion events or no-motion events. Wakeups and interrupts for motion and no-motion can be separately enabled via SFR bit-fields and are logically ORed together to create a module wakeup output and a module interrupt output. This is illustrated in the following figure.

The module wakeup output is combined with the wakeup of the Pre-processor module before being directed to the Power Management block. The module interrupt output is connected directly to a dedicated interrupt port on the MRK3 interrupt controller.

Note that for both the Motion and No-Motion events the interrupt and wakeup signals share the same source but that the Interrupt enable for the event has a higher priority than the wakeup enable. ie whenever a wakeup is enabled for a particular event the associated interrupt must also be enabled.

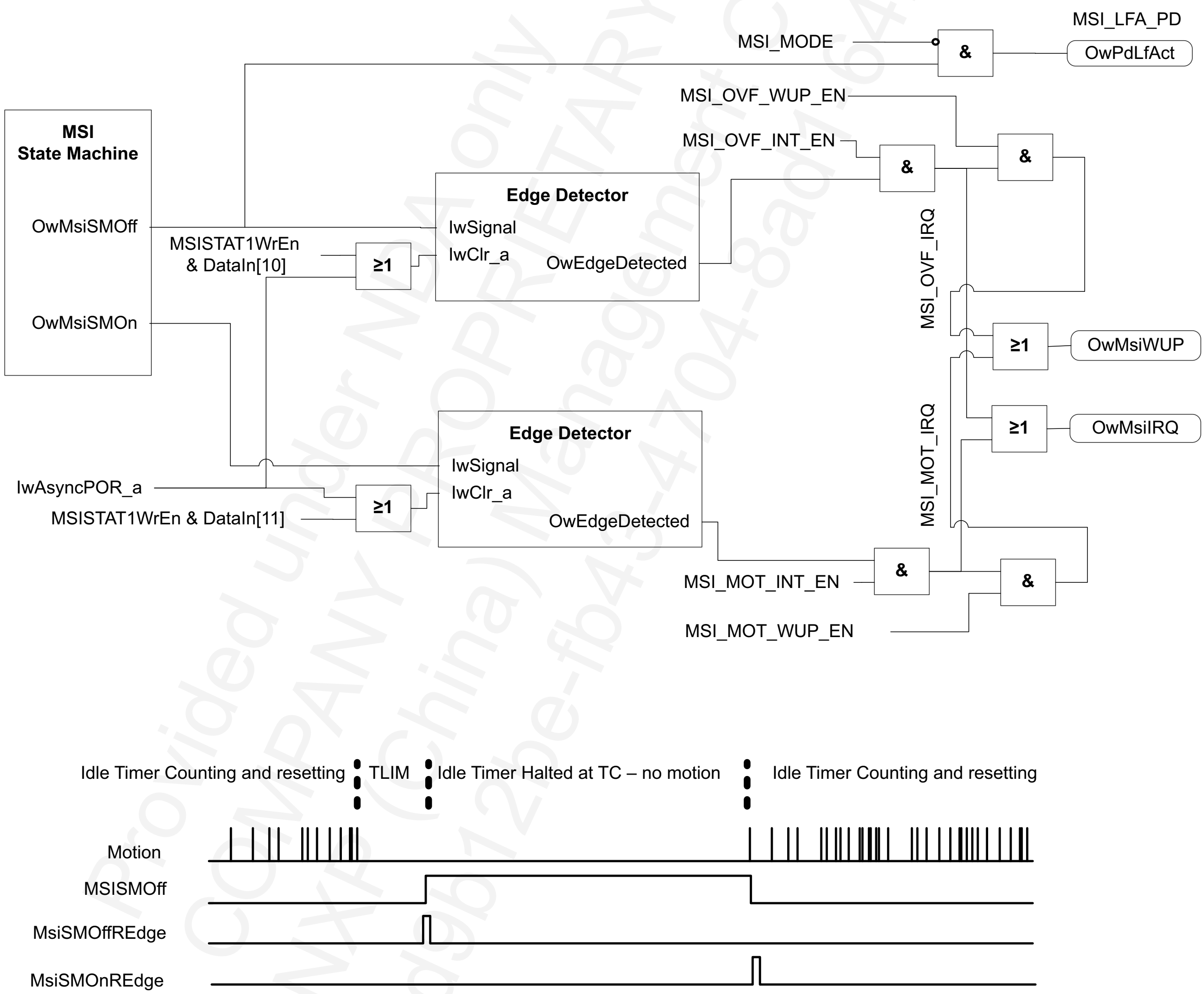


Fig 76. Interrupts and Wakeups

2.21.3.9 Pre-Processor Polling Combined Operation

Power-down of the LF Active front-end may be controlled by a polling algorithm within the Pre-Processor as well as Motion Sensor Interface. The polling algorithm within the Pre-Processor is also designed to reduce energy consumption. Both the MSI LFActive Power-down and the Pre-processor polling LFActive Power-down mechanisms can be independently enabled so all four conditions of mechanism to enable the LFActive Power-down are possible. The design is such that the two mechanisms work independently and the Active HIGH LFActive powerdown controls of both modules are logically ORed. Design features are in place to ensure that if, for example in the case where both power-down mechanisms are enabled, the MSI LFActive Powerdown interrupts the Pre-Processor while receiving a telegram, the Pre-processor will resume operation in its listening state.

2.21.4 Registers

The Motion Sensor Interface is controlled and monitored by 4 SFRs powered in the VBATREG domain as described in the following section.

2.21.4.1 MSI Timer Control Register, MSICON0

This register controls the Idle Timer Counter limit value and the clearing of this counter.

Table 168. MSI Timer Control Register, MSICON0 (reset value 1Eh)

Bit	Symbol	Access	Value	Description
7	RFU	R0/W0		Reserved for future use
6	MSI_TCLR	R0/W		Idle timer restart request one-shot. Writing a 1 resets the idle timer. Always read as 0
			0	No Action
			1	Reset the Idle Timer
5 to 0	MSI_TLIM[5:0]	R/W		Idle Timer Overflow Limit - The un-interrupted length of time (in units of 2 seconds) for which there must be no motion detected by the sensor for the counter to flag that motion has ceased. Reset Value is 1Eh = 1 minute. A value of 00h is not permitted.
			00_0001	2 seconds No Motion Timeout
			00_0010	4 seconds No Motion Timeout
			00_0011	6 seconds No Motion Timeout
			00_0100	8 seconds No Motion Timeout
			....	....
			11_1111	126 seconds No Motion Timeout

2.21.4.2 MSI Enable Control Register, MSICON1

This register controls the enable for the Motion Sensor Interface module, mode of operation (Motion Sensor or Auxiliary Timer), LFActive power UP and Down Enable and Wakeup and Interrupt enables for the “Motion Detected” and “Motion Ceased” events.

Table 169. MSI Enable Control Register, MSICON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	MSI_EN	R/W		Motion sensor interface / auxiliary interval timer enable.
			0	Module Disabled
			1	Module Enabled
6	MSI_MODE	R/W		Motion sensor interface / auxiliary interval timer mode selection
			0	Motion sensor interface mode - monitor P21_MD.
			1	Auxiliary interval timer mode - ignore P21_MD.
5	MSI_LFA_PD_EN	R/W		LF Active power down enable
			0	The motion sensor interface is not able to switch off power to LF Active Front End
			1	The motion sensor interface is able to switch off power to LF Active Front End
4	MSI_LFA_PU_EN	R/W		LF Active power up enable
			0	The motion sensor interface is not able to switch on power to LF Active Front End
			1	The motion sensor interface is able to switch on power to LF Active Front End
3	MSI_MOT_WUP_EN	R/W		"Motion detected" wake-up enable. - overridden by higher priority associated interrupt enable (MSI_MOT_INT_EN)
			0	Wakeup disabled for “Motion Detected” event
			1	Wakeup enabled for “Motion Detected” event
2	MSI_OVF_WUP_EN	R/W		"Motion ceased" wake-up enable.
			0	Wakeup disabled for “Motion Ceased” event
			1	Wakeup enabled for “Motion Ceased” event
1	MSI_MOT_INT_EN	R/W		Motion detected interrupt enable.[1]
			0	Interrupt disabled for “Motion Detected” event
			1	Interrupt enabled for “Motion Detected” event
0	MSI_OVF_INT_EN	R/W		Motion ceased interrupt enable.[1]
			0	Interrupt disabled for “Motion Ceased” event
			1	Interrupt enabled for “Motion Ceased” event

[1] Interrupts are only generated in case of MSI_LFA_PD_EN = 1 or MSI_LFA_PU_EN = 1.

This register enables the CPU to read the status of the LFA Power Down, Motion Interrupt, Overflow Interrupt and Counter Overflow flags

2.21.4.3 MSI Idle Timer Count Register, MSISTAT0

Table 170. MSI Idle Timer Count Register, MSISTAT0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	R0/W0		Reserved for future use
5 to 0	MSI_TREG[5:0]	R		Idle timer value; time since timer (re)start or last motion event in multiples of 2s. - Binary Value

2.21.4.4 MSI Flag and Interrupt Register, MSISTAT1

Table 171. MSI Flag and Interrupt Register, MSISTAT1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7 to 6	RFU	R0/W0		Reserved for future use
5	MSI_LFA_PD	R		LF active power-down request status flag.
			0	The Motion Sensor Interface is requesting LF active powered-up.
			1	Motion Sensor Interface is requesting LF active powered-down. MSI_LFA_PD is required in addition to MSI_OVF to tell the CPU that the motion sensor interface is holding the LFA in power-down mode; the MSI_OVF bitfield will be cleared on a motion event so does not convey the same information.
4 to 3	RFU	R0/W0		Reserved for future use
2	MSI_OVF	R		Idle Timer Overflow status flag. Active High whenever the Idle timer is in its terminal count state - ie whenever count = TLIM
			0	The Idle timer counter has not reached its maximum value
			1	The idle timer counter has reached its maximum value
1	MSI_MOT_INT	R/W1->0		Motion Detected Interrupt Status Flag. Writing a “1” to this bit resets the interrupt
			0	Motion has been detected since the interrupt was last reset
			1	Motion has not been detected since the interrupt was last reset
0	MSI_OVF_INT	R/W1->0		Idle Timer Overflow Interrupt Status flag. Writing a “1” to this bit resets the interrupt
			0	The Idle timer counter has not reached its maximum value since the interrupt was last reset
			1	The idle timer counter has reached its maximum value since the interrupt was last reset

2.22 User data registers

2.22.1 User data registers 0 to 7 USRBATx

The NCF29A1 / NCF29A2 provides 8 user registers supplied by the unregulated battery supply VBAT. Each user register has a length of one byte (see Table 172).

These user registers keep their content during RISC power-down mode and can be accessed for customer applications.

Table 172. User registers USRBATx (reset values 00h)

Bit	Symbol	Access	Value	Description
7 to 0	USRB0[7:0]	R/W		User data register 0 in unregulated battery domain
7 to 0	USRB1[7:0]	R/W		User data register 1 in unregulated battery domain
7 to 0	USRB2[7:0]	R/W		User data register 2 in unregulated battery domain
7 to 0	USRB3[7:0]	R/W		User data register 3 in unregulated battery domain
7 to 0	USRB4[7:0]	R/W		User data register 4 in unregulated battery domain
7 to 0	USRB5[7:0]	R/W		User data register 5 in unregulated battery domain
7 to 0	USRB6[7:0]	R/W		User data register 6 in unregulated battery domain
7 to 0	USRB7[7:0]	R/W		User data register 7 in unregulated battery domain

2.22.2 User data registers 0 to 7 USRBATRGLx

The NCF29A1 / NCF29A2 provides 8 user registers supplied by the regulated battery supply VBATREG (see Table 173). Each user register has a length of one byte.

These user registers keep their content during RISC power-down mode and can be accessed for customer applications.

Table 173. User registers USRBATRGLx (reset values xxh)

Bit	Symbol	Access	Value	Description
7 to 0	USRBRGL0[7:0]	R/W		User data register 0 in regulated battery domain
7 to 0	USRBRGL1[7:0]	R/W		User data register 1 in regulated battery domain
7 to 0	USRBRGL2[7:0]	R/W		User data register 2 in regulated battery domain
7 to 0	USRBRGL3[7:0]	R/W		User data register 3 in regulated battery domain
7 to 0	USRBRGL4[7:0]	R/W		User data register 4 in regulated battery domain
7 to 0	USRBRGL5[7:0]	R/W		User data register 5 in regulated battery domain
7 to 0	USRBRGL6[7:0]	R/W		User data register 6 in regulated battery domain
7 to 0	USRBRGL7[7:0]	R/W		User data register 7 in regulated battery domain

2.23 Device modes

The NCF29A1 / NCF29A2 features the Device Modes

- VIRGIN
- INIT
- PROTECTED
- TAMPERED

The Device Modes affect the overall device behavior, the Monitor and Download Interface operation and the user ability to access the EEPROM and EROM. A Device Mode is controlled by a set of configuration bytes, which are located in the EEPROM.

The configuration bytes may not be altered by the user directly, instead the corresponding Monitor and Download Interface command has to be used.

2.23.1 VIRGIN

After manufacturing, the device operates in VIRGIN mode, enabling extended device test and device configuration. Finally, NXP forces the device into INIT mode and the VIRGIN mode is irreversibly locked in order to ensure it cannot be activated again.

2.23.2 INIT

When the device is supplied from NXP, it is configured in INIT mode by default.

The INIT mode shall be used during software development only. The Monitor and Download Interface is fully operational, enabling the customer to initialize the EEPROM and EROM as desired for the application.

To protect the EEPROM and EROM from readout and to disable the debug features, the device shall be forced into PROTECTED mode.

Leaving the device in INIT mode may cause the device to execute a software break, in case a LOW pulse is detected at pin MSDA. This pulse would terminate execution of the application program and would call the built-in debug program. In this case, execution of the application program is interrupted until a proper debug command is issued or a device reset is applied.

2.23.3 PROTECTED

In the moment the device is set into PROTECTED mode, the EEPROM and EROM are protected against altering and readout via the Monitor and Download Interface, and the debug features are disabled. The PROTECTED mode has to be used during system testing and in the final application.

The device may be forced into INIT mode again by issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device enters TAMPERED mode.

2.23.4 TAMPERED

The TAMPERED mode is entered temporarily during the sequence that forces the device from PROTECTED mode back into INIT mode. If this sequence does not complete successfully, the TAMPERED mode is entered.

The device may be forced into INIT mode by again issuing a corresponding command via the Monitor and Download Interface. This command sets the EEPROM and the EROM to a predefined state first, before the INIT mode is resumed. Hence, all application related EEPROM data and the EROM based application program are discarded. In case this sequence does not complete successfully, the device remains in TAMPERED mode until a new attempt is made.

2.24 System routines

2.24.1 Boot routine

The ROM based boot (see Figure 77) is called immediately after a device reset. A device reset can be forced either by a Port Wake Up condition or a LF Field Reset or can be interrogated by the application program.

The boot routine executes a sequence of instructions to evaluate the device mode and configures the device, e.g. determines the supply condition, evaluates device protection flags, calls transponder emulation modes according to the EEPROM configuration and passes control to the application code accordingly.

The boot routine has to process information about the presence of LF field and battery supply. Further, the boot routine evaluates wake-up events initiated by pressed buttons or interval timer.

The boot routine checks the setting for LFFLDDIS and handles the bit IE_LFNMI. The NMI is always handled in the application.

In case the field supply is available, but no LF field detect signal is active (weak supply field), a part of the boot routine is executed again because the source of the wake-up event cannot be determined. If the LF field supply is available but operation with corresponding field supply is disabled in the settings (LFFLDDIS), the boot routine polls for new wake-up events.

2.24.2 Transponder emulation

The NCF29A1 / NCF29A2 features a set of functions to emulate the NXP transponder families HT2-E, HT3, HT-AES or HT-Pro2. Each device supports specific transponder emulation. The corresponding functions are called from the application program by system calls (SYS instructions), which pass back control to the application program, when completed.

2.24.3 Monitor and download interface

The in-circuit Monitor and Download Interface is intended for non-intrusive debugging during application program development. The interface allows manipulating the embedded peripherals and provides means to initialize the EEPROM and EROM. It is implemented as two-wire serial interface using the dedicated pins MSDA and MSCL.

The Monitor and Download Interface provide 16 Bit Real Time Monitor containing Watches. Besides several HW/SW Break Points and single step operation, the interface contains an HW accelerator and allows autonomous operation.

The majority of the features provided by the Monitor and Download Interface are available only, if the device is set into INIT mode, which is the factory default setting. When performing system tests and field trials, the device shall be set to PROTECTED mode. Latter one locks the EEPROM and EROM content, protecting it against alteration and read out, as well as disables the debug features. The device may be forced back into INIT mode by a dedicated monitor command, which will set the EEPROM and EROM to a predefined state.

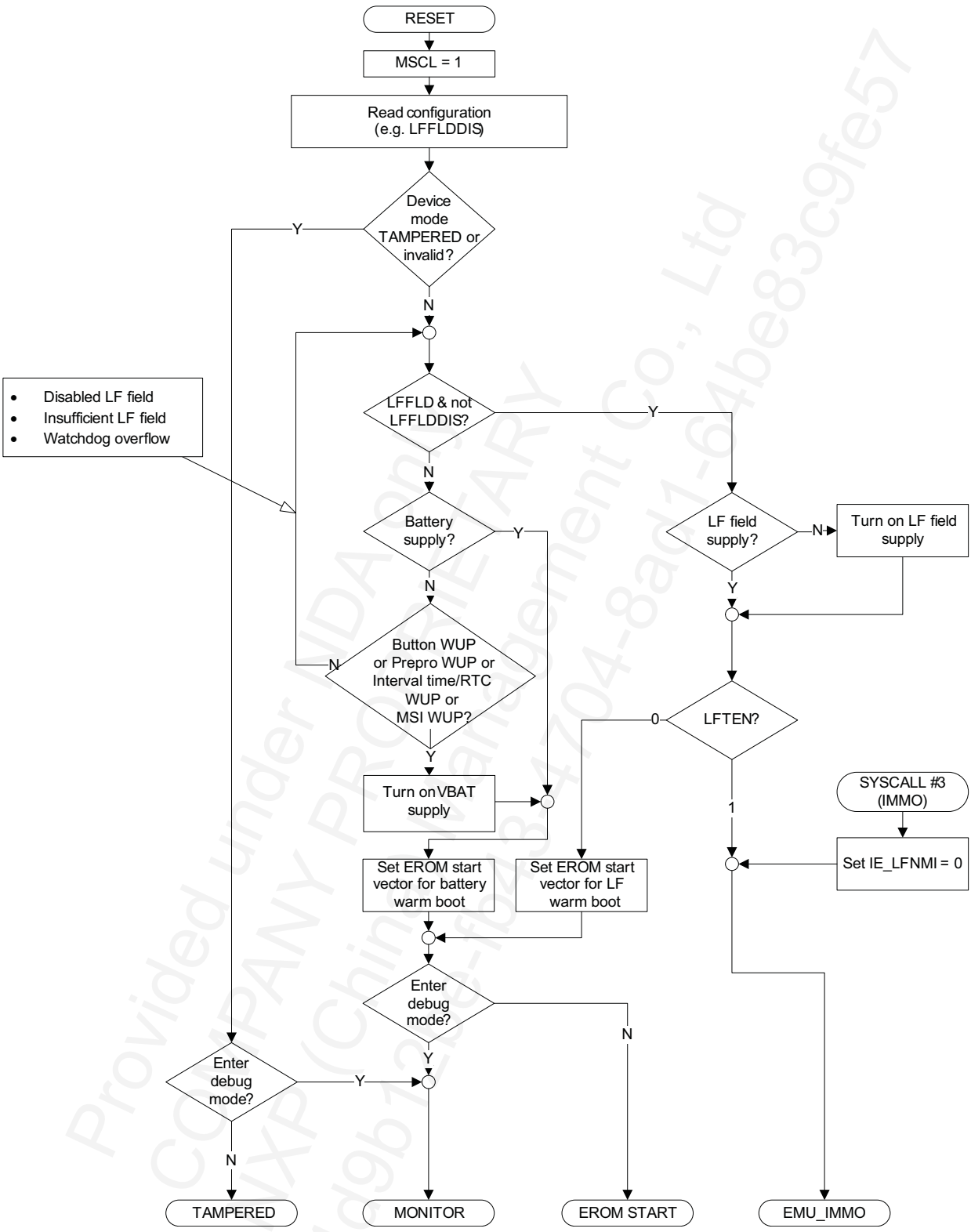


Fig 77. Boot routine flow chart

2.25 SPI 0 and 1

The NCF29A1 / NCF29A2 provides two identical synchronous, full duplex or half duplex serial peripheral interfaces SPI 0 and SPI 1 (SPI 0/1) with a baud rate selectable between 125 kHz and 4 MHz (with 8 MHz clock). The SPI 0/1 interfaces can be used to connect the PCx7900 (FraNTIC), PQx7980/81 (LoPSTer) or NCK2984 (MantraF). In full duplex mode, each interface uses three port pins, SCKx (serial clock), SDOx (serial data output master) and SDIx (serial data input master). Configuring the SPI 0/1 interfaces in half duplex mode, each interface requires two port pins SCKx and SD(I)Ox by sharing the data line for serial data input and output.

The SPI 0/1 interfaces allow 1 to 8 bit data transfer and provide double buffered operation with separate receive and transmit registers. The clock polarity, clock phase and shift direction (left or right) is configurable. The SPI 0/1 data transfer can be controlled via interrupt processing.

The SPI 0/1 controller supports a master mode, where the master provides the serial clock SCKx. An SPI 0/1 slave mode is not provided. It is possible to connect different slaves to the single bus, but only one slave at the time can communicate with the master. Hence, different slaves shall be enabled with separate control signals.

The controller supports also a modified SPI 0/1 communication in a pseudo slave mode or externally clocked master mode. In this mode the clock is derived from the slave, while theNCF29A1 / NCF29A2 communication control is still in the responsibility of the master device. The pseudo slave mode supports either full duplex or half duplex mode. This mode can be used to implement a software controlled SPI 0/1slave mode and is optimized for interfacing with PCx7900 (FraNTIC) and PQx7980/81 (LoPSTer).

2.25.1 Modes

In all modes described below only the flag SPxBUSY should be used during transmit or receive, instead of using the transmit or receive buffer flags. Flag SPxBUSY should be checked to be 0 before starting a new data transfer.

2.25.1.1 Master mode, full duplex

The following sequence describes the processing of an SPI 0/1 data transfer when configured to be the master in full duplex mode. This process assumes that any prior data transfer has already been completed and that the receive buffer is empty.

Single byte transfer (see Figure 78):

1. Reset the SPI block and set the SPI 0/1 control registers
2. Write the data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
3. Wait until the SPIxBUSY is cleared. This indicates that the current data transfer has been completed.
4. Optional: Read the received data from the SPI 0/1 data register.

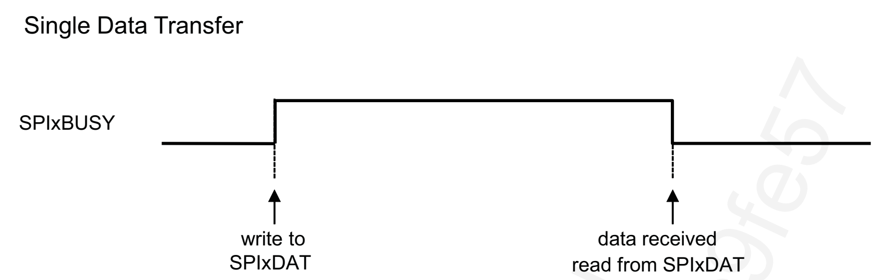


Fig 78. SPI 0/1 single data transfer

Multiple byte transfer (see Figure 79):

1. Reset the SPI block and set the SPI 0/1 control registers
2. Write the first data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
3. Wait until the SPI 0/1 busy flag SPIxBUSY is cleared. This indicates that the current data transfer has been completed.
4. Optional: Read the received data from the SPI 0/1 data register.
5. Write the next data to be transmitted to the SPI 0/1 data register. This write access transfers the content of the transmit buffer into the shift register and starts the data transfer. The SPI 0/1 busy flag SPIxBUSY is set.
6. Go to step 3 if more data shall be transmitted.
7. Wait until the last transfer is completed. The SPI 0/1 busy flag SPIxBUSY is cleared after completion.
8. Optional: Read the last received data from the SPI 0/1 data register.

Please note that the application can skip reading the SPI 0/1 data register, if received data is not desired.

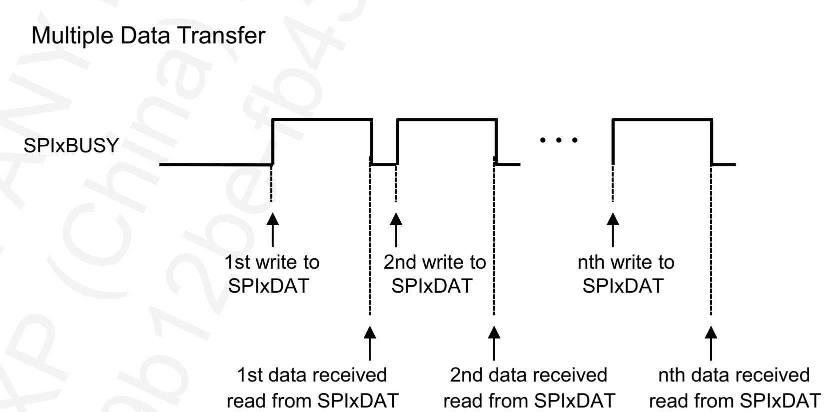


Fig 79. SPI 0/1 multiple data transfer

Dependent on the application, variations of the SPI data transfer sequence might be advantageous.

2.25.1.2 Master mode, half duplex

In half duplex mode the application shall select whether a transmit or receive transfer shall be accomplished.

The transmit mode behaves in the same way as the full duplex mode except that the received data is equal to the transmitted data.

In the receive mode every data transfer is requested by writing dummy data to the SPI 0/1 data register. If several bytes are requested the SPI 0/1 data register shall be written once for every byte.

2.25.1.3 Pseudo slave mode

In pseudo slave mode the clock is generated by the slave while the master has full control. In full duplex as well as in half duplex mode the master determines the number of transfers to be accomplished by the number of successive write accesses to the SPI 0/1 data register. Even in half duplex receive mode the master shall request every byte separately.

The transfer is synchronized according to the selected SPIxCLKPOL and SPIxCLKPHA settings with regard to the provided clock at SCKx. All clock edges before the start or after transfer completion will be ignored.

The application shall assure that the clock at SCKx is at the right state when starting a new data transfer. If the slave provides a continuous clock, the application can check the state of SCKx by reading the corresponding port pin input flag.

If the slave stops the SCKx generation during data transmission the application can trigger the bit SPIxSTOP to stop data reception. This request transfers the current content of the shift register into the receive buffer, while the status register holds the number of received bits.

The pseudo slave mode can be used to implement a software controlled SPI 0/1 slave mode. The software shall check the I/O port pin assigned as slave select input and shall control the SPI 0/1 block accordingly.

2.25.1.4 Pseudo slave initiation mode

The SPI 0/1 block supports a dedicated mode allowing a seamless hand-over of the clock from the master mode to the pseudo slave mode. If data transfer is started in this mode, SCKx is driven for half a clock period by the master and switches to slave mode thereafter. The further communication employs the clock from the slave. This mode supports PCx7900 (FraNTIC) TRANSMIT command and PQx7980/81 (LoPSTer) TRANSMIT and RECEIVE commands. These devices exploit the ninth clock pulse to enable the UHF transmitter/receiver.

The master generates only the first clock edge of the clock signal (rising/falling edge for SPIxCLKPOL = 0/1). Thereafter the port is configured for input and, if selected, the internal pull-up/pull-down resistor becomes active. In order to prevent that a false edge is detected on port SCKx until the slave drives the line, it is recommended to program the internal resistors correspondingly to the last driven state of SCKx. If PQx7980/81 (LoPSTer) is used, it is recommended to select a proper delay time (CLK2SCLK_DELAY) to avoid bus conflicts.

2.25.1.5 Shift register operation

The SPI 0/1 block has an 8 bit internal shift register, which is not directly accessible. Transmit data is transferred from the register TXBUFx into the shift register prior to the transfer and the content of the shift register is copied to RXBUFx upon completion of the transfer. The shift register holds transmit and receive data. For every bit shifted out of the shift register one received bit is shifted in. The most recent output bit is held in a separate output flip-flop. The content of this output flip-flop defines the state of the SDOx line after transfer completion. This behavior is advantageous, if SPI 0/1 is used to generate a TRANSMIT command for FraNTIC or LoPSTer. In some modes the data value on SDOx is latched in FraNTIC or LoPSTer, if the slave is deselected (see Figure 80). After a reset of the SPI 0/1 block the output flip-flop holds the value '0'.

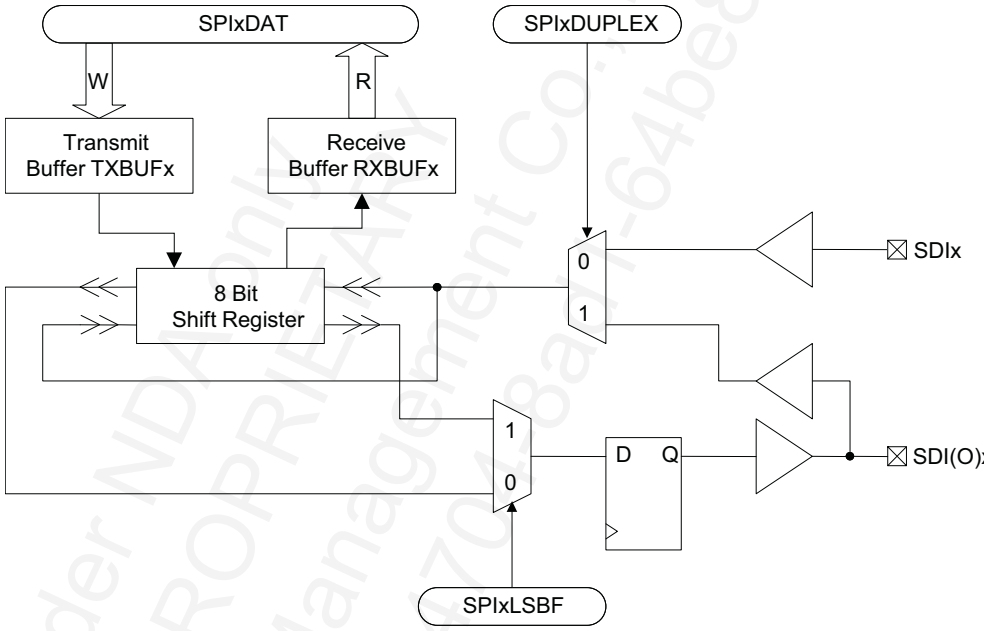


Fig 80. SPI 0/1 shift register organization

The internal shift register can work either in left shift or right shift mode dependent on whether data shall be transferred MSB first or LSB first. The common SPI 0/1 transfer mode is MSB first. Transmit data is shifted out to the left and received data is fed in on the right side of the shift register. Alternatively the SPI 0/1 block supports also transfers with LSB first. In this case transmit data is shifted out to the right and receive data is shifted in on the left side of the shift register.

Usually the SPI 0/1 transfer is byte oriented, thus all transfers are organized as 8 bit transfers. For the use as synchronous serial port controller also other bit granularities are supported (e.g. for FraNTIC and LoPSTer). For this, the SPI 0/1 block supports a selectable number of bits per transfer from 1 to 8. If less than 8 bits are selected for a single transfer the application has to consider the behavior of the shift register when writing to or reading from the SPI 0/1 data register.

During transfer with MSB first, transmit data shall always be left aligned as the leftmost bit is shifted out first. Transmit data shall be properly preprocessed by left shifts before it is written to the SPI 0/1 data register. Receive data is always right aligned with the LSB at the rightmost position.

Table 174. SPI data transfer example with 3 bits in full duplex mode, alignment of transmit and receive data

Transfer bit order	Transfer direction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB first	Transmit data	T2	T1	T0	X	X	X	X	X
	Receive data	X	X	X	X	X	R2	R1	R0
LSB first	Transmit data	X	X	X	X	X	T2	T1	T0
	Receive data	R2	R1	R0	X	X	X	X	X

During transfer with LSB first, transmit data shall be always right aligned with the LSB at the rightmost position. Receive data is left aligned with the MSB at the leftmost position. The application has to perform proper right shifts after reading data from the SPI 0/1 data register.

2.25.2 Interaction with I/O port interface

The SPI 0/1 block interacts with 2 or 3 I/O pins, when enabled.

SDIx

In full duplex mode, the SDIx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

In half duplex mode, the SDIx port is not controlled by the SPI 0/1 block and can be used as standard I/O.

SDOx and SD(I)Ox

In both full duplex mode and half duplex transmit mode, the SDOx and SD(I)Ox ports are configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value stored in the output flip-flop, which in general corresponds to the last transmitted bit.

In half duplex receive mode, the SDOx and SD(I)Ox ports are configured as input. If an internal pull-up/pull-down resistor is selected, it is active. If the application switches between half duplex transmit mode and receive mode the port direction is changed automatically.

SCKx

In master mode, the SCKx port is configured as output. The values of the corresponding port output and direction flags are ignored. If no transfer is active the port drives the value selected with the clock polarity bit SPIxCLKPOL.

In pseudo slave mode, the SCKx port is configured as input. If an internal pull-up/pull-down resistor is selected, it is active.

In pseudo slave initiation mode, the SCKx port is configured as output prior to the first data transfer. At this stage the behavior is the same as in master mode configuration. With start of the first data transmission the port drives one clock edge. The port is driven for one internal SPI 0/1 clock cycle to the opposite state of SPIxCLKPOL before it is switched to input. Once the port is switched to input it behaves like the pseudo slave mode even if a new data transfer is started. The SPI 0/1 shall be switched to master mode to re-trigger the SCKx switching behavior. It is sufficient to change the mode, thus a data transfer in master mode is not needed.

2.25.3 Registers

2.25.3.1 SPI 0/1 data register SPIxDAT

The SPI 0/1 data register gives write access to the transmit buffer and read access to the receive buffer. Read access to the transmit buffer and write access to the receive buffer is not supported.

Table 175. SPI 0/1 data register SPIxDAT (reset value xxh)

Bit	Symbol	Access	Value	Description
7 to 0	SPIxDATA[7:0]	R/W		SPI 0/1 data

Transmitted and received data is buffered. Writing data to the SPI data register transfers them into the transmit buffer, while reading the SPI data register returns the value of the read data buffer, where it is transferred to when a transfer is complete. An internal shift register is used for the transmission and reception of the serial data.

2.25.3.2 SPI 0/1 control register SPIxCON0

SPI 0/1 control register 0 provide means to select the desired SPI operating mode. It is recommended to change these settings prior to activation of the SPI 0/1 block by setting SPIxEN. The settings in SPIxCON0 shall not be changed when a SPI 0/1 transfer is active. Otherwise this can result in unpredictable behavior.

Table 176. SPI 0/1 control register SPIxCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	R0/W0		Reserved for future use
6	SPIxLSBF	R/W		SPI 0/1 shift direction
			0	Left shift, MSB (bit 7) first
			1	Right shift, LSB (bit 0) first
5 and 4	SPIxCLKPOL SPIxCLKPHA	R/W		SPI 0/1 clock polarity (bit 5), SPI 0/1 clock phase (bit 4)
			00	First data driven prior to first SCKx rising edge Other data driven at SCKx falling edge Data sampled at SCKx rising edge
			01	First data driven at first SCKx rising edge Other data driven at SCKx rising edge Data sampled at SCKx falling edge
			10	First data driven prior to first SCKx falling edge Other data driven at SCKx rising edge Data sampled at SCKx falling edge
			11	First data driven at first SCKx falling edge Other data driven at SCKx falling edge Data sampled at SCKx rising edge
3 and 2	SPIxMODE[1:0]	R/W		SPI 0/1 operating mode
			00	Master mode
			01	Reserved for future use
			10	Pseudo slave mode
			11	Pseudo slave initiation mode

Table 176. SPI 0/1 control register SPIxCON0 (reset value 00h)

Bit	Symbol	Access	Value	Description
1 and 0	SPIxDUPLEX[1:0]	R/W		SPI 0/1 duplex mode
			00	Full duplex mode (affecting SCKx, SDOx, SDIx)
			01	Reserved for future use
			10	Half duplex mode – transmission (affecting SCKx, SD(I)Ox)
			11	Half duplex mode – reception (affecting SCKx, SD(I)Ox)

SPIxLSBF, SPI 0/1 shift direction:

This bit selects the shift direction of the internal shift register and hence whether data is transferred LSB or MSB first.

SPIxCLKPOL, SPIxCLKPHA, SPI 0/1 clock polarity and clock phase:

The polarity and phase of port SCKx is selected with the bits SPIxCLKPOL and SPIxCLKPHA. The setting of SPIxCLKPOL defines the logic level of SCKx, if the master mode is selected and no transfer is active. The pin SCKx is then driven to the same value as SPIxCLKPOL.

Figure 81 shows the timing diagram for the four SPI 0/1 data transfer formats available at the example of a single 8 bit data transfer. SSELx denotes an active low slave select signal that has to be generated by the application, e.g. with the help of a standard I/O port.

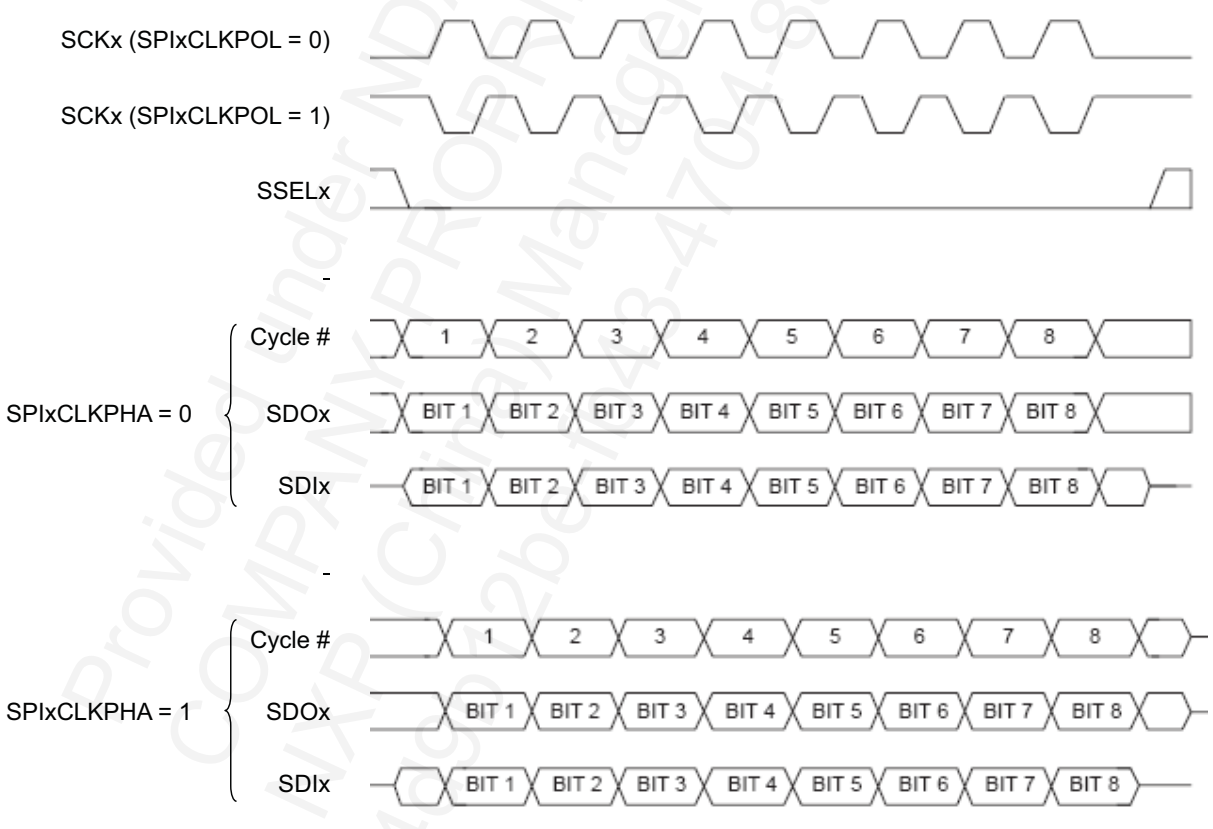


Fig 81. SPI 0/1 data transfer in full duplex mode

SPIxDUPLEX[1:0], SPI 0/1 duplex mode

The SPI 0/1 duplex mode selection configures the SPI 0/1 block either for full or half duplex mode. In full duplex mode the three port pins SCKx, SDOx and SDIx are assigned with special functions. In half duplex mode the two port pins SCKx and SD(I)Ox are assigned, while the application has to select whether transmission or reception is activated.

2.25.3.3 SPI 0/1 control register SPIxCON1

SPI 0/1 control register 1 provide means to select the SPI 0/1 baudrate, the SPI 0/1 interrupt source and bits to enable, reset and stop the SPI 0/1 block.

Table 177. SPI 0/1 control register SPIxCON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
7	RFU	R0/W0		Reserved for future use
6 to 4	SPIxCLK[2:0]	R/W		SPI 0/1 clock
			000	Internal SPI 0/1 clock rate:PCLK Transfer baudrate (master mode):PCLK/2 Max. transfer baudrate (pseudo slave mode):PCLK/8
			001	Internal SPI 0/1 clock rate:PCLK/2 Transfer baudrate (master mode):PCLK/4 Max. transfer baudrate (pseudo slave mode):PCLK/16
			010	Internal SPI 0/1 clock rate:PCLK/4 Transfer baudrate (master mode):PCLK/8 Max. transfer baudrate (pseudo slave mode):PCLK/32
			011	Internal SPI 0/1 clock rate:PCLK/8 Transfer baudrate (master mode):PCLK/16 Max. transfer baudrate (pseudo slave mode):PCLK/64
			100	Internal SPI 0/1 clock rate:PCLK Transfer baudrate (master mode):PCLK/8 Max. transfer baudrate (pseudo slave mode):PCLK/8
			101	Internal SPI 0/1 clock rate:PCLK/2 Transfer baudrate (master mode):PCLK/16 Max. transfer baudrate (pseudo slave mode):PCLK/16
			110	Internal SPI 0/1 clock rate:PCLK/4 Transfer baudrate (master mode):PCLK/32 Max. transfer baudrate (pseudo slave mode):PCLK/32
			111	Internal SPI 0/1 clock rate:PCLK/8 Transfer baudrate (master mode):PCLK/64 Max. transfer baudrate (pseudo slave mode):PCLK/64
3	SPIxINTSS	R/W		SPI 0/1 interrupt source
			0	Transmit buffer empty flag SPIxTXBE
			1	Receive buffer full flag SPIxRXBF
2	SPIxSTOP	R0/W		Stop SPI 0/1 communication
			0	No effect
			1	Stop SPI 0/1 transfer

Table 177. SPI 0/1 control register SPIxCON1 (reset value 00h)

Bit	Symbol	Access	Value	Description
1	SPIxRST	R0/W		SPI 0/1 reset
			0	No effect
			1	Reset SPI 0/1 block
0	SPIxEN	R/W		SPI 0/1 enable
			0	SPI 0/1 block disabled
			1	SPI 0/1 block enabled

SPIxCLK[2:0], SPI 0/1 clock:

The SPI 0/1 clock selection bits SPIxCLK allow setting of the internal clock rate and the transfer baudrate. The timings shall be set prior to a transfer taking place.

In master mode the transfer baudrate can be set either to 1/2 or 1/8 of the internal clock rate. The first setting is intended for maximum communication speed. The second setting can be used in an environment where the baudrate in the master mode and the pseudo slave mode should be aligned.

In pseudo slave mode the clock at SCKx is sampled with the internal SPI 0/1 clock rate, which shall be selected at least 8 times higher than the expected SPI 0/1 baudrate. Hence, the baudrate in the pseudo slave mode shall not exceed 1/8 of the internal clock rate.

The clock for the SPI 0/1 block is derived from the peripheral clock PCLK.

The setting of SPIxCLK shall not be changed when a SPI 0/1 transfer is active. Otherwise this can result in unpredictable behavior.

SPIxINTSS, SPI 0/1 interrupt source:

The application can select the source of the SPI 0/1 interrupt with the interrupt source selection bit SPIxINTSS. The interrupt request signal is statically disabled, if the SPI 0/1 block is disabled (Figure 82). The interrupt request is cleared if SPIxBUSY has changed to ‘0’.

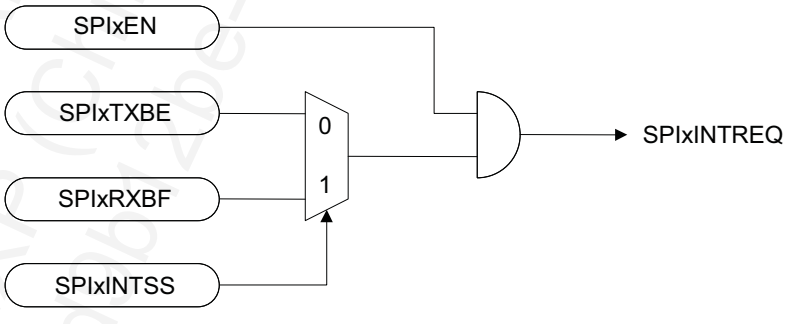


Fig 82. SPI 0/1 interrupt request generation

SPIxSTOP, stop SPI 0/1 communication:

A running SPI 0/1 transfer can be interrupted by setting the bit SPIxSTOP to '1'. This stops the internal state machine and transfers the current content of the shift register into the receive buffer. The SPI 0/1 status flags are updated accordingly. The number of received bits can be retrieved by reading the value SPIxBIT in the SPI 0/1 status register.

Bit SPIxSTOP can be used to finish a SPI 0/1 transfer in pseudo slave mode without losing the last received bits.

After stopping a communication with SPIxSTOP, the SPI 0/1 shall be reset with bit SPIxRST.

Reading of bit SPIxSTOP always yields '0'.

SPIxRST, SPI 0/1 reset:

The SPI 0/1 reset bit can be used to reset the internal state machine. The reset is accomplished, if a '1' is written to bit SPIxRST. Reading of bit SPIxRST always yields '0'.

The reset bit influences the internal state machine, the bit counter, the output flip-flop, the status flags and some other control flip-flops. The configuration of the port pins is not influenced. The only exception is the pseudo slave initiation mode. After a reset it is configured to its initial state, hence the port pin SCKx is configured as output.

If the reset is accomplished when a transfer is ongoing the current transfer is interrupted immediately.

SPIxEN, SPI 0/1 enable:

The SPI 0/1 enable bit enables the entire SPI 0/1 block. If the SPI 0/1 is disabled all blocks except the control registers are reset to their initial state and the internal clock generation is stopped. When the SPI 0/1 block is enabled the assigned I/O port pins are reconfigured.

2.25.3.4 SPI 0/1 status register SPIxSTAT

The SPI 0/1 status register holds mainly status information of the SPI 0/1 block in order to detect e.g. completion of a data transfer. The status bits are read-only.

Any write access to these bits is ignored and does not alter the state of a status bit. It has to be noted that the status register also contains some control bits.

Table 178. SPI 0/1 status register SPIxSTAT (reset value 00h)

Bit	Symbol	Access	Value	Description
7	SPIxBUSY	R		SPI 0/1 busy flag
			0	SPI 0/1 block does not transfer data
			1	SPI 0/1 transfer is currently active
6	SPIxTXBE	R		SPI 0/1 transmit buffer empty, the next data may be written to SPIxDAT after SPIxBUSY has changed from 1 to 0.
			0	Buffer full
			1	Buffer empty
5	SPIxRXBF	R		SPI 0/1 receive buffer full, the data may be read from SPIxDAT after SPIxBUSY has changed from 1 to 0.
			0	Buffer empty
			1	Buffer full
4	SPIxRXBOVF	R		SPI 0/1 receive buffer overflow
			0	No overflow
			1	Receive buffer is overwritten and previous data is lost
3	RFU	R0/W0		Reserved for future use
2 to 0	SPIxBIT[2:0]	R/W		Number of bits per SPI 0/1 transfer and transfer bit counter
			000	Write access:8 bit transfer Read access (after stop with SPIxSTOP): 0 bit received (SPIxRXBF = 0) or 8 bit received (SPIxRXBF = 1)
			001	Write access:1 bit transfer Read access (after stop with SPIxSTOP): 1 bit received
			010	Write access:2 bit transfer Read access (after stop with SPIxSTOP): 2 bit received
			011	Write access:3 bit transfer Read access (after stop with SPIxSTOP): 3 bit received
			100	Write access:4 bit transfer Read access (after stop with SPIxSTOP): 4 bit received
			101	Write access:5 bit transfer Read access (after stop with SPIxSTOP): 5 bit received
			110	Write access:6 bit transfer Read access (after stop with SPIxSTOP): 6 bit received
			111	Write access:7 bit transfer Read access (after stop with SPIxSTOP): 7 bit received

SPIxTXBE, SPI 0/1 transmit buffer empty:

SPIxTXBE = '1' signals that the transmit buffer is empty. This bit is automatically cleared by any write access to the SPI 0/1 data register. The next data may be written to SPIxDAT after SPIxBUSY has changed from 1 to 0.

If no SPI 0/1 transfer is active, hence SPIxBUSY = '0', SPIxTXBE is always '0'.

Note: The behavior of this flag does not depend on the settings of SPIxMODE and SPIxDUPLEX.

SPIxRXBF, SPI 0/1 receive buffer full:

SPIxRXBF = '1' signals that the receive buffer is full. This bit is automatically cleared by any read access to the SPI 0/1 data register. The data may be read from SPIxDAT after SPIxBUSY has changed from 1 to 0.

This bit is always '0' after a reset of the SPI 0/1 block.

Note: The behavior of this flag does not depend on the settings of SPIxMODE and SPIxDUPLEX.

SPIxRXBOVF, SPI 0/1 receive buffer overflow:

If the SPI 0/1 data register has not been read by the application when the next data transfer completes, the receive buffer is overwritten with the new data byte and the previous data is lost. This buffer overflow is signaled by setting the receive buffer overflow flag SPIxRXBOVF to '1'.

The bit SPIxRXBOVF is automatically cleared by any read access to the SPI 0/1 data register.

SPIxBIT[2:0], number of bits per SPI 0/1 transfer and transfer bit counter:

The sub-register SPIxBIT has two different meanings dependent on whether it is written or read.

For write access, the sub-register SPIxBIT determines the number of bits per SPI 0/1 transfer. The values 1 to 7 correspond directly to the requested number of transmitted/received bits. The value 0 shall be selected for an 8 bit transfer. The sub-register SPIxBIT is double buffered. If a transfer is active and the content of SPIxBIT is changed, the new value becomes effective at the beginning of the next transfer, hence it is loaded at the same time when data is transferred from the transmit buffer into the internal shift register.

During read access, the sub-register SPIxBIT gives access to the internal SPI 0/1 bit counter. If a transfer is stopped with bit SPIxSTOP, the application can retrieve the number of received bits. The value SPIxBIT = 0 can have two different meanings: If the flag SPIxRXBF is '0', no bit was received whereas SPIxRXBF = '1' indicates that 8 bits were received (provided that SPIxRXBOVF = '0'). No decision can be taken in case of a receive buffer overflow.

2.26 EEPROM content at delivery

The ULP EEPROM content is initialized with default values during device manufacturing (Table 179). The device is configured for the respective transponder emulation (HT2-E, HT3, HT-AES or HT-Pro2, one emulation per device) and set to INIT mode, providing full support regarding the monitor and download interface (MDI).

Table 179. EEPROM content upon delivery

Content (hex)[1]	ULP Module	Page
xx xx xx xx	0	0, 16 to 63
00 00 00 00		1 to 15
xx xx xx xx	1	64 to 119, 124 to 126
00 00 00 00		120 to 123
xx xx xx 00		127
xx xx xx xx	2	128 to 191
xx xx xx xx	3	192 to 255
xx xx xx xx	4	256 to 319
xx xx xx xx	5	320 to 383
xx xx xx xx	6	384 to 447
xx xx xx xx	7	448 to 487, 489, 491, 493, 495, 497, 499, 501, 503
00 00 00 xx		488, 490, 492, 494, 496, 498, 500
FF FF F5 xx		502
00 00 00 00		504 to 511
xx xx xx xx	15	960 to 975, 992 to 1015, 1017 to 1021
00 00 00 90		976
00 00 00 01		977
00 00 00 00		978 to 991
00 00 xx 00		999
00 00 xx xx		1016
xx xx 00 00		1022
xx xx xx Ex		1023

[1] Locations marked 'x' are undefined and may hold any pattern

The EEPROM content may be changed as desired by the application, except for the pages 960 to 975 and 992 to 1023.

Bit 7 to 4 of page 1023 serve the function of a product type identifier (PI) and are set to '1110'. During transponder emulation, the content of page 1023 (ULP module 15) is mapped to page 0 (ULP module 0).

Bit 16 to 23 of page 1022 serve the function of an enhanced product type identifier (EPI) and are set dependent on the product type:

EPI = 01h for NCF29A1 and EPI = 02h for NCF29A2.

3. Characterization information

3.1 Limiting values

Table 180. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134) [5].

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	Operating temperature			-40	+85	°C
T_{sto}	Storage temperature			-55	+125	°C
$V_{max,Bat}$	Voltage at any VBAT pin to VSS			-0.3	3.6	V
$V_{max,IO}$	Voltage at any I/O pin to VSS			-0.3	V_{BAT}+0.3	V
$V_{max,In}$	Voltage at INx to VSS		[1]	-0.5	7.5	V
$V_{max,xtal}$	Voltage at pins XTAL1, XTAL2			-0.3	1.95	V
$I_{Peak,In}$	Peak input current for pins IN1P, IN1N, IN2P, IN2N, IN3P and IN3N				30	mA
$I_{Peak,Out}$	Peak output current for port pins P1x, P2x				15	mA
$I_{latch-up}$	Latch-up current		[2]	100		mA
$V_{ESD,HBM}$	ESD, human body model		[3]	2		kV
$V_{ESD,CDM}$	ESD, charged device model	all pins	[4]	500		V
P_{Diss}	Power dissipation				120	mW
$V_{max,VPA}$	Maximum VPA voltage regulator output voltage	PA_POWER =PA_POWER_MAX	[6]		2.0	V

[1] Due to device concept and design, VDDC, IN1P, IN1N, IN2P, IN2N, IN3P and IN3N may show a higher voltage during normal device operation, caused by a corresponding input signal applied to the LF input pins.

[2] According to AEC-Q100-004

[3] According to AEC-Q100-002

[4] According to AEC-Q100-011

[5] Proper device operation outside the characteristic values specified under Section 3.2 “Static characteristics” and Section 3.3 “Dynamic characteristics”, is not implied and may lead to unpredictable device behavior, causing permanent alterations of the device state, memory content or characteristics.

[6] PA_POWER values must not be set to higher values than PA_POWER_MAX to avoid damage of the IC.

3.2 Static characteristics

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
LF FIELD state (transponder operation)							
V_{BAT}	Battery supply voltage		[1]	0		3.6	V
I_{IN_LF}	Coil input peak current	$\|I_{IN}\|$				15	mA
f_{c_LF}	LF field carrier frequency				125		kHz
MI_{WR_LF}	Minimum modulation index, write direction	$V_{IN\text{-}HIGH} = 5V_p$, $T_{TMOD} = 8T_0$	[2]		100	95	%
V_{DDC_LF}	Rectified supply voltage	$\|I_{IN}\|$= 150 µA				5.5	V
$V_{THR,FDLF\text{-}VIN}$	LF field detect threshold voltage, (V_{IN}, peak), rising threshold, flagged in VDD domain	$\|V_{IN1+,peak}\|$, $\|V_{IN1-,peak}\|$		2.1	2.45	2.8	V
$V_{THR,FDLF\text{-}VIN\_HYST}$	LF field detect threshold voltage, (V_{IN}, peak), hysteresis, flagged in VDD domain	$\|V_{IN1+,peak}\|$, $\|V_{IN1-,peak}\|$	[23]		500		mV
$V_{THR,FD\_ATIC\text{-}VIN}$	LF field detect threshold voltage, (V_{IN}, peak), rising threshold, flagged in VFLDLF domain	$\|V_{IN1+,peak}\|$, $\|V_{IN1-,peak}\|$		2.2	2.55	2.97	V
$V_{THR,FD\_ATIC\text{-}VIN\_HYST}$	LF field detect threshold voltage, (V_{IN}, peak), hysteresis, flagged in VFLDLF domain	$\|V_{IN1+,peak}\|$, $\|V_{IN1-,peak}\|$	[24]		150		mV
Device executes from ROM (transponder emulation), V_{DDC_LF} = 3.0V							
$I_{CC\_LF\_R}$	Supply current (wait for command)		[3]		20	28	µA
Device executes from EROM (transponder application), V_{DDC_LF} = 3.0V							
$I_{CC\_LF\_2M}$	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2 MHz	CPUCLKSEL[1:0] = 01 CPUCLKCYC[4:0] = 06h	[3]		310	360	µA
$I_{CC\_LF\_500k}$	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h	[3]		80	102	µA
$I_{CC\_LF\_IDLE}$	IDLE mode, auxiliary RC oscillator as clock source, f_{CPU} = 500 kHz	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h	[3]		35	50	µA
POWER-OFF state (battery supply for LF active receiver)							
V_{BAT}	Battery supply voltage			2.0	3.0	3.6	V
I_{QQ_OFF}	Quiescent current (VBAT regulator off)	V_{BAT} = 3.0V BATRGLEN = 0			0.67	2.1	µA
I_{QQ_PD}	Quiescent current with LF active receiver in power-down (VBAT regulator on)	BATRGLEN = 1 PDLFACT = 1 LPRC_EN = 0 IT_MODE[1:0] = 00			0.86	2.1	µA

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/$_{fC\_LF}$, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{QQ_IT}	Quiescent current with activated interval timer (VBAT regulator on, LF active receiver power-down, 180 kHz oscillator on)	BATRGLEN = 1 PDLFACT = 1 PDx_6DB = 1 LPRC_EN = 1 IT_MODE[1:0] = 10		2.0	3.0	µA
$I_{QQ\_LFACT\_G00}$	Quiescent current in application configuration (VBAT regulator on, LF active receiver on, 180 kHz oscillator on, the lowest gain enabled, baudrate 3.9 kbit/s, preprocessor and digital filter enabled)	BATRGLEN = 1 PDLFACT = 0 Gain = 00 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 -40°C, 25°C		5.0	5.5	µA
		BATRGLEN = 1 PDLFACT = 0 Gain = 00 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 85°C		5.6	7.5	µA
$I_{QQ\_LFACT\_G01}$	Quiescent current in application configuration (VBAT regulator on, LF active receiver on, 180 kHz oscillator on, additional 6 dB gain enabled, baudrate 3.9 kbit/s, preprocessor and digital filter enabled)	BATRGLEN = 1 PDLFACT = 0 Gain = 01PDx_6DB = 0 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 -40°C, 25°C		6.8	7.5	µA
		BATRGLEN = 1 PDLFACT = 0 Gain = 01 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 85°C		7.7	9.6	µA

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/$_{fC\_LF}$, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{QQ\_LFACT\_G10}$	Quiescent current in application configuration (VBAT regulator on, LF active receiver on, 180 kHz oscillator on, additional 12 dB gain enabled, baudrate 3.9 kbit/s, preprocessor and digital filter enabled)	BATRGLEN = 1 PDLFACT = 0 Gain = 10 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 -40°C, 25°C			14.1	15.7	µA
		BATRGLEN = 1 PDLFACT = 0 Gain = 10 LPRC_EN = 1 IT_MODE[1:0] = 00 BDRATE[1:0] = 01 DIGFILRST = 0 PRERST = 0 PDIREFSTUP=1 85°C			16.1	18.7	µA
$\Delta I_{QQ\_POLL\_TOFF}$	Delta quiescent current with activated polling timer (LF Active disabled by polling state-machine - TOFF interval)	BATRGLEN = 1 PDLFACT = 0 GAINCHx = 00 LPRC_EN = 1 ENPOLL=1 IT_MODE[1:0] = 00	[4]		0.21	0.3	µA
$\Delta I_{QQ\_POLL\_TON}$	Delta quiescent current with activated polling timer (LF Active enabled by polling state-machine - TON interval)	BATRGLEN = 1 PDLFACT = 0 GAINCHx = 00 LPRC_EN = 1 ENPOLL=1 IT_MODE[1:0] = 00	[4]		0.25	0.3	µA
ΔI_{QQ_MSI}	Delta quiescent current when Motion Sensor Interface is enabled	MSI_EN = 1	[4]		0.21	0.275	µA
BATTERY state (battery supply)							
V_{BAT}	Battery supply voltage			2.0	3.0	3.6	V
Device executes from ROM							
I_{BAT_R2M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2 MHz, EROM turned off	CPUCLKSEL[1:0] = 01 CPUCLKCYC[4:0] = 06h			200	255	µA
I_{BAT_R500k}	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz, EROM turned off	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h			40	52	µA
I_{BAT_RIDLE}	IDLE mode, auxiliary RC oscillator as CPU clock source, f_{CPU} = 500 kHz, EROM turned off	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h			20	27	µA
Device executes from EROM							
I_{BAT_4M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 4MHz	CPUCLKSEL[1:0] = 01 CPUCLKCYC[4:0] = 02h			480	580	µA

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{BAT_2M}	RUN mode, main RC oscillator as CPU clock source, f_{CPU} = 2MHz	CPUCLKSEL[1:0] = 01 CPUCLKCYC[4:0] = 06h			310	370	µA
I_{BAT_500k}	RUN mode, auxiliary RC oscillator as CPU clock source, f_{CPU}= 500kHz	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h			80	97	µA
I_{BAT_IDLE}	IDLE mode, auxiliary RC oscillator as CPU clock source, f_{CPU}= 500kHz	CPUCLKSEL[1:0] = 00 CPUCLKCYC[4:0] = 00h			35	48	µA
$I_{BAT\_XODIV2CLK}$	RUN mode, crystal oscillator as clock source, f_{CPU} = XODIV2CLK/4 = 3.45MHz	CPUCLKSEL[1:0] = 11 CPUCLKCYC[4:0] = 02h XODIV2CLKDIS = 1 (UHFTXCLK disabled)	[3]		800		µA
ΔI_{DD_RSSI}	Supply current RSSI		[4]		530	670	µA
$\Delta I_{DD\_RSSI\_EXT}$	Supply current RSSI, ext. range		[4]		1.45	2.1	mA
$\Delta I_{DD\_ADC\_4M}$	Battery measurement, main RC oscillator as CPU clock source, f_{CPU} = 4MHz		[4]		240	300	µA
$\Delta I_{DD\_ADC\_XO}$	Battery measurement, crystal oscillator as CPU clock source, f_{CPU} = 27.6/8 MHz		[4]		220	280	µA
ΔI_{DD_TEMP}	Supply current temperature sensor		[4]		27	40	µA
LF FIELD state or BATTERY state							
ΔI_{DD_ULPRD}	Supply current ULP-EEPROM (Read)	Single module				2.75	µA
$\Delta I_{DD\_ULPPROG}$	Supply current ULP-EEPROM (Erase/Write)	Single module	[4]		5	30	µA
ΔI_{DD_MRC}	Supply current main RC oscillator		[4]		55	60	µA
ΔI_{DD_AES}	Supply current AES calculation unit	AESCLKSEL [2:0] = 110	[4]		22	26	µA/MHz
Power-on reset (POR)							
V_{POR}	Power-on reset threshold			1.25	1.3	1.35	V
$V_{BO,VDD}$	Brown out threshold @ VDD			1.43	1.5	1.57	V
$V_{BO,VDDA}$	Brown out threshold @ VDDA	Typical value is for minimal trimming (default), Maximum value is for maximum trimming			1.3	1.72	V
$V_{BO,VBAT\_STD}$	Standard brown out threshold @ VBAT			2.02	2.1	2.15	V
$V_{BO,VBAT\_EXT}$	Extended brown out threshold @ VBAT			1.74	1.8	1.86	V
$V_{VBATIND}$	Detection threshold at falling edge			2.2	2.4	2.6	V
$V_{VBATIND\_HYST}$	Detection hysteresis			30	50	80	mV
$R_{VBATIND}$	Resistive load on VBAT			100	150	300	kΩ
Immobilizer / LF Passive interface							
C_{IN_PAS}	Input capacitance INx	125 kHz, 2 V_{rms}, Tuning capacitance disabled	[6]		25		pF

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF},
C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{x+_LIN}	Input resistance at INxP, linear (standard LF modulator)	V_{INx+} = 0.5V, V_{INx-} = 0V, V_{FLD} = 3V STRONGMOD = 0	[5]	1.4	2.0	2.6	kΩ
$R_{x+\_LIN,strong}$	Input resistance at INxP, linear (strong LF modulator)	V_{INx+} = 0.5V, V_{INx-} = 0V, V_{FLD} = 3V STRONGMOD = 1	[5]	300	550	700	Ω
R_{x+_NLIN}	Input resistance at INxP, non-linear (standard LF modulator)	V_{INx+} = 1.5V, V_{INx-} = 0V, V_{FLD} = 3V STRONGMOD = 0	[5]	0.65	1.00	1.35	kΩ
R_{x-_LIN}	Input resistance at INxN, linear (standard LF modulator)	V_{INx+} = 0V, V_{INx-} = 0.5V, V_{FLD} = 3V STRONGMOD = 0	[5]	3	4.1	5.4	kΩ
$R_{x-\_LIN,strong}$	Input resistance at INxN, linear (strong LF modulator)	V_{INx+} = 0V, V_{INx-} = 0.5V, V_{FLD} = 3V STRONGMOD = 1	[5]	300	550	700	Ω
$V_{CLP\text{-}IN}$	Input limiter clamp voltage	I_{IN} = ±15mA		6.0	7.1	7.8	V
		I_{IN} = 150µA		5.7	6.6	7.4	V
$V_{THR,CR}$	Clock recovery sensitivity				10	22	mV_p
Tuning capacitor for LF interface							
C_{STEP}					5.0		pF
LF Active interface							
C_{IN_ACT}	Input capacitance IN1, IN2, IN3	125kHz, V_{INrms} = 0.1V, Tuning cap. disabled			13.0		pF
$R_{IN\_AC\_G10}$	AC input resistance IN1, IN2, IN3	V_{IN} @ sensitivity limit Gain = 10	[6]		0.5		MΩ
$R_{IN\_AC\_G01}$	AC input resistance IN1, IN2, IN3	V_{IN} @ sensitivity limit Gain = 01	[6]		0.9		MΩ
$R_{IN\_AC\_G00}$	AC input resistance IN1, IN2, IN3, reduced gain	V_{IN} @ sensitivity limit Gain = 00	[6]		1.5		MΩ
$V_{CLP\_ACT\text{-}IN}$	Input limiter clamp voltage	I_{IN} = ±15mA		6.0	6.7	7.8	V
		I_{IN} = ±150µA		5.7	6.6	7.4	V
$V_{SENS\_ACT2k\_G10}$	Sensitivity active protocol; all three channels, 2 kbit/s	BDRATE[1:0] = 00 Gain = 10	[7]		60	130	μV_{pp}
$V_{SENS\_ACT4k\_G10}$	Sensitivity active protocol; all three channels, 4 kbit/s	BDRATE[1:0]= 01 Gain = 10	[7]		65	140	μV_{pp}
$V_{SENS\_ACT8k\_G10}$	Sensitivity active protocol; all three channels, 8 kbit/s	BDRATE[1:0]= 10 Gain = 10	[7]		80	170	μV_{pp}
$V_{SENS\_ACT2k\_G10\_SINGLE}$	Sensitivity active protocol; single channel, 2 kbit/s	BDRATE[1:0]= 00 Gain = 10	[7]		100	210	μV_{pp}
$V_{SENS\_ACT4k\_G10\_SINGLE}$	Sensitivity active protocol; single channel, 4 kbit/s	BDRATE[1:0]= 01 Gain = 10	[7]		110	240	μV_{pp}
$V_{SENS\_ACT8k\_G10\_SINGLE}$	Sensitivity active protocol; single channel, 8 kbit/s	BDRATE[1:0]= 10 Gain = 10	[7]		140	300	μV_{pp}

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{SENS\_ACT2k\_G01}$	Sensitivity active protocol; all three channels, 2 kbit/s	BDRATE[1:0] = 00 Gain = 01	[7]		100	200	µV_{pp}
$V_{SENS\_ACT4k\_G01}$	Sensitivity active protocol; all three channels, 4 kbit/s	BDRATE[1:0]= 01 Gain = 01	[7]		120	240	µV_{pp}
$V_{SENS\_ACT8k\_G01}$	Sensitivity active protocol; all three channels, 8 kbit/s	BDRATE[1:0]= 10 Gain = 01	[7]		140	280	µV_{pp}
$V_{SENS\_ACT2k\_G01\_SINGLE}$	Sensitivity active protocol; single channel, 2 kbit/s	BDRATE[1:0]= 00 Gain = 01	[7]		170	340	µV_{pp}
$V_{SENS\_ACT4k\_G01\_SINGLE}$	Sensitivity active protocol; single channel, 4 kbit/s	BDRATE[1:0]= 01 Gain = 01	[7]		200	400	µV_{pp}
$V_{SENS\_ACT8k\_G01\_SINGLE}$	Sensitivity active protocol; single channel, 8 kbit/s	BDRATE[1:0]= 10 Gain = 01	[7]		250	500	µV_{pp}
$V_{SENS\_ACT2k\_G00}$	Sensitivity active protocol reduced gain; all three channels, 2 kbit/s	BDRATE[1:0]= 00 Gain = 00	[7]		210	420	µV_{pp}
$V_{SENS\_ACT4k\_G00}$	Sensitivity active protocol reduced gain; all three channels, 4 kbit/s	BDRATE[1:0]= 01 Gain = 00	[7]		240	480	µV_{pp}
$V_{SENS\_ACT8k\_G00}$	Sensitivity active protocol reduced gain; all three channels, 8 kbit/s	BDRATE[1:0]= 10 Gain = 00	[7]		300	600	µV_{pp}
$V_{SENS\_ACT2k\_G00\_SINGLE}$	Sensitivity active protocol reduced gain; single channel, 2 kbit/s	BDRATE[1:0]= 00 Gain = 00	[7]		360	720	µV_{pp}
$V_{SENS\_ACT4k\_G00\_SINGLE}$	Sensitivity active protocol reduced gain; single channel, 4 kbit/s	BDRATE[1:0]= 01 Gain = 00	[7]		410	820	µV_{pp}
$V_{SENS\_ACT8k\_G00\_SINGLE}$	Sensitivity active protocol reduced gain; single channel, 8 kbit/s	BDRATE[1:0]= 10 Gain = 00	[7]		520	1040	µV_{pp}
Fg_{HP_2k}	Baseband amplifier high-pass filter cutoff frequency, 2 kbit/s	BDRATE[1:0]= 00		60	160	280	Hz
Fg_{LP_2k}	Baseband amplifier low-pass filter cutoff frequency, 2 kbit/s	BDRATE[1:0]= 00		3.3	5.2	7.2	kHz
Fg_{HP_4k}	Baseband amplifier high-pass filter cutoff frequency, 4 kbit/s	BDRATE[1:0]= 01		60	240	420	Hz
Fg_{LP_4k}	Baseband amplifier low-pass filter cutoff frequency, 4 kbit/s	BDRATE[1:0]= 01		6.0	9.4	13.0	kHz
Fg_{HP_8k}	Baseband amplifier high-pass filter cutoff frequency, 8 kbit/s	BDRATE[1:0]= 10		50	410	800	Hz
Fg_{LP_8k}	Baseband amplifier low-pass filter cutoff frequency, 8 kbit/s	BDRATE[1:0]= 10		10.5	16.6	24.0	kHz
$R1_{QLIM}$	Resistor 1 for Q-factor limitation			420	600	780	kΩ
$R2_{QLIM}$	Resistor 2 for Q-factor limitation			280	400	520	kΩ
$R3_{QLIM}$	Resistor 3 for Q-factor limitation			140	200	260	kΩ

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RSSI							
R_{IN_RSSI}	RSSI input resistance IN1, IN2, IN3	V_{IN} <=100 mV_{pp} All Rx_Q off		1			MΩ
R_{short}	RSSI shorting resistance IN1, IN2, IN3	V_{IN} = 200 mV_{DC} V_{BAT} = 1.8 V Resistance to ground			90	130	Ω
$aACC_{54dB}$	Absolute accuracy	Measured @ 0.75 mV_{pp}	[8]			± 20	%
$rACC_{54dB}$	Relative accuracy (deviation)	Measured @ 0.75 mV_{pp}	[9]			± 10	%
$aACC_{36dB}$	Absolute accuracy	Measured @ 3 mV_{pp}	[8]			± 20	%
$rACC_{36dB}$	Relative accuracy (deviation)	Measured @ 3 mV_{pp}	[9]			± 10	%
$aACC_{18dB}$	Absolute accuracy	Measured @ 24 mV_{pp}	[8]			± 20	%
$rACC_{18dB}$	Relative accuracy (deviation),	Measured @ 24 mV_{pp}	[9]			± 10	%
$aACC_{0dB}$	Absolute accuracy	Measured @ 300 mV_{pp}	[8]			± 20	%
$rACC_{0dB}$	Relative accuracy (deviation)	Measured @ 300 mV_{pp}	[9]			± 10	%
G_{RSSI_54dB}	Typical RSSI gain 54dB range		[10]		54.7		dB
G_{RSSI_36dB}	Typical RSSI gain 36dB range		[10]		36.4		dB
G_{RSSI_18dB}	Typical RSSI gain 18dB range		[10]		18.2		dB
G_{RSSI_0dB}	Typical RSSI gain 0dB range		[10] [11]		-1.3		dB
G_{RSSI_-18dB}	Typical RSSI gain -18dB range		[10] [11]		-18.3		dB
$R1_Q$	Resistor 1 for Q factor adjustment		[25]	112.5	150	187.5	kΩ
$R2_Q$	Resistor 2 for Q factor adjustment		[25]	90	120	150	kΩ
$R3_Q$	Resistor 3 for Q factor adjustment		[25]	75	100	125	kΩ
$R4_Q$	Resistor 4 for Q factor adjustment		[25]	60	80	100	kΩ
$R5_Q$	Resistor 5 for Q factor adjustment		[25]	37.5	50	62.5	kΩ
$R6_Q$	Resistor 6 for Q factor adjustment		[25]	15	20	25	kΩ
Rx_QdT	Temperature variation of resistors for Q factor adjustment	Temperature variation over full range related to 25°C value		-5		5	%
ADC							
RES_{ADC}	Resolution ADC					10	Bit
DNL_{ADC}	Differential nonlinearity ADC		[12]		± 0.72		LSB
INL_{ADC}	Integral nonlinearity ADC		[13] [14] [15]		± 3		LSB
$V_{ADC,REF}$	Reference voltage – full scale value			1.215	1.25	1.285	V
VIN_{ADC}	Input-voltage of VINP, VINN to VSS		[15]	0.2		1.1	V

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF},
C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Battery measurement						
G_{VBAT}	Battery measurement gain		3.54	3.65	3.78	mV/$_{LSB}$
OFF_{VBAT}	Battery measurement offset at 3V	VBAT = 3.0V, INSEL = 0 (battery voltage meas.), REFSEL = 2 (external reference at P17_LED and P12), Vref_diff = 1.05V.	970	985	995	LSB
Temperature measurement						
T_{ACC_CAL}	Temperature measurement accuracy calibrated	Offset compensated T_{amb} = -40 to +85°C	-5		5	K
G_{TADC}	Temperature measurement gain			6.0262		LSB/K
OFF_{TADC}	Temperature measurement offset at 25°C		440	512	592	LSB
Battery State (UHF transmitter operating conditions)						
V_{BAT}	Supply Voltage		2.1	3.0	3.6	V
V_{BAT_ext}	Supply Voltage		1.8		2.1	V
$\Delta I_{BAT\text{-}XTAL}$	Supply current XTAL Oscillator ON	VBAT = 2.7V		450	600	µA
$\Delta I_{BAT\text{-}VCO}$	Supply current VCO ON	VBAT = 2.7V, f_{VCO} = 868 MHz crystal oscillator as CPU clock source		2.2	2.4	mA
$I_{BAT,TX}$	Supply current in Transmit mode f_{TX} = 434 MHz	VBAT = 2.7V, CWC[16], [27] PA_POWER = PA_POWER_MAX crystal oscillator as CPU clock source		12.5	15.2	mA
f_{TX}	Carrier frequency range		310		447	MHz
I_{Limit_Step}	Current limiter step	PA_IMAX = 2 to 15		2.5		mA
I_{Limit_Offset}	Current limiter Offset			1.4		mA
I_{VDDPA}	PA driver current	f_{VCO} = 315 MHz, PA_POWER=PA_POWER_MAX 10dBm mode		1.3		mA
		f_{VCO} = 434 MHz, PA_POWER=PA_POWER_MAX 10dBm mode		1.6		mA
UHF transmitter AC/DC Conditions, XTAL Oscillator,XOEN=1, NDK 3225GA (C_L = 12 pF, f = 27,6 MHz)						
R_{MARGIN}	Oscillation startup margin	T_{amb} = 25°C		1		kΩ

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/$_{fC\_LF}$, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL Synthesizer, XOEN=1, TXON=1, f_{TX}=434MHz							
PN_{PLL}	Phase noise Matched into 50 Ω	PA_POWER = PA_POWER_MAX	[27]				
		10 kHz offset				-80	dBc/Hz
		100 kHz offset^				-78	dBc/Hz
		1 MHz offset				-88	dBc/Hz
		10 MHz offset				-105	dBc/Hz
E_{REF}	Reference spurious emissions $f_{TX} \pm f_{XTAL}$	PA_POWER = PA_POWER_MAX	[27]			-32	dBc
Power Amplifier, XOEN=1, TXON=1, f_{TX}=434MHz							
P_{OUT}	Output power matched into 50 Ω	V_{BAT} = 2.7V, T_{amb} = 25°C, PA_POWER=PA_POWER_MAX 10dBm mode	[27]	10			dBm
P_{OUT}	Output power matched into 50 Ω	V_{BAT} from 2.1V – 3.6V, T_{amb} from -40°C to 85°C PA_POWER= PA_POWER_MAX 10dBm mode	[26]	8			dBm
P_{OUT}	Output power matched into 50 Ω	V_{BAT} from 1.8V – 2.0V, T_{amb} from -40°C to 85°C PA_POWER = PA_POWER_MAX 10dBm mode	[26]	5			dBm
P_{OUT}	Output power matched into 50 Ω	V_{BAT} from 2.1V – 3.6V T_{amb} from -40°C to 85°C PA_POWER = 0d 10dBm mode			-17.8	-14	dBm
P_{OUT}	Output power matched into 50 Ω	V_{BAT} from 2.1V – 3.6V T_{amb} from -40°C to 85°C PA_POWER = 0d, 0dbm mode			-22.7	-18	dBm
$P_{O\_TX\_Step}$	Output power step size matched into 50 Ω	V_{BAT} from 2.1V – 3.6V T_{amb} from -40°C to 85°C		0.1	0.25	0.5	dBm
Modulation							
$f_{MOD,ASK}$	ASK modulation frequency	Duty cycle 50%				25	kHz
$f_{MOD,FSK}$	FSK modulation frequency	Duty cycle 50%				25	kHz
f_{BRG}	Baud rate clock frequency			0.5		50	kHz

Table 181. Static characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 3.0 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF},
C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P1,P2 (General Purpose I/O), MSDA[17], MSCL[18]						
C_I	Pin capacitance	V_{IN} = 0.1V_{RMS}, f = 1MHz		9		pF
V_{IL}	Input low voltage				0.3 V_{BAT}	V
V_{IH}	Input high voltage		0.7 V_{BAT}			V
I_I	Input low current	V_{IL} = 0 [19]			0.5	µA
I_{IH}	Input high current	V_{IH} = V_{BAT} [20]			0.5	µA
V_{OL}	Output low voltage	I_O = 1 mA			0.4	V
V_{OH}	Output high voltage	I_O = -1 mA	V_{BAT} -0.4			V
I_{OL}	Current when driving output low to an external LED	T_{amb} = -40°C to +85°C, 30sec/day single I/O operation, any GPIO, P17_LED when LED Driver disabled [28]			5	mA
R_{PU_STR}	Pull-Up resistance strong	V_I = 0V, V_{BAT} from 1.8V – 3.6V	18	28	40	kΩ
R_{PU_WK}	Pull-Up resistance weak	V_I = 0V, V_{BAT} from 1.8V – 3.6V	65	115	160	kΩ
I_{PD}	Pull-down current	V_I = 3.0 V, V_{BAT} from 1.8V – 3.6V	10	50	150	µA
R_{PU_MD}	Pull-Up for Motion Sensor pin	V_I = 0V, V_{BAT} from 2.1V – 3.6V	1.5	2.0	2.5	MΩ
LED Driver						
I_{LED}	LED driving current	V_o = 100 mV to V_{BAT} (3.6V), P17_LED	0.5	1.5	2.1	mA

[1] External measures for reverse battery connection must be applied to ensure transponder operation in such case.

[2] The demodulator sensitivity applicable in write direction is defined according Figure 15.

[3] Specifies the internal chip operating current that needs to be supplied from the rectified supply voltage. Input/output current of ports (P1and P2) zero.

[4] Specifies the additional internal chip operating current caused by the corresponding circuitry, if enabled, which has to be added to the device operating current (ICC or IBAT, respectively) in order to determine the total device operating current.

[5] Measured while the internal modulator is active, thus the additional load is ON (S2 closed), according to Figure 11.

[6] Differential measurement on INxN and INxP

[7] The sensitivity can depend on the application. Especially the antenna Q factor influences the sensitivity in general. The values are anticipated for Q = 5 with a wake-up probability of 50%. For further information, please refer to the Application note.

[8] Worst-case tolerance for a differential input-signal 125 kHz, ADC with maximal resolution (10 bit). Value related to fixed typ. values for RSSI range gain and ADC input range from device specification.

[9] Variation of RSSI result over supply voltage and temperature range in relation to RSSI result measured at 3.0 V and 25°C. Value related to device dependent limits.

[10] Typical RSSI gain (together with typical ADC input range) used as reference for absolute RSSI accuracy aACC (due to peak detector architecture a factor of two has to be considered for Vpeak-peak to Vpeak conversion). For details, refer to Application Note.

[11] Measured with low ohmic input signal, damping of coil in application to be considered. For details, refer to Application Note.

[12] A typically missing code at ADC output 511 is not considered.

[13] The INL [LSB] is measured at a resolution of 10 bit.

[14] The ADC specification is valid for the specified common-mode input range. The ADC will still be operational outside the specified range but with limited linearity and accuracy.

[15] The ADC specification is valid for the specified differential input range. The ADC will still be operational outside the specified range (including VSS) but with limited linearity and accuracy.

[16] CWC - Continuous Wave Carrier

[17] MSDA features an internal pull-up resistor to VBAT

[18] MSCL is configured statically as output

[19] Not applicable if internal pull-up resistor is active.

[20] Not applicable if internal pull-down resistor is active.

[21] Parameters values are derived from characterization.

[22] Min./ Max. values includes process variation

[23] Measured based on LFFLD flag (PCON1 register) read by the CPU (in boot code) to determine that LF Passive mode has started and transponder emulation is possible. This flag can only assert after the 2ms count.

[24] Measured based on FDET flag which is the first indicator that a field is present. This flag starts the 2ms count. Internal signal, not available as SFR bit. See DS fig 16, Field Detect block on the left.

[25] Resistor values in case of weakly-coupled signals when the LF front-end rectifier has no effect and the voltages on INxP and INxN are differential with a common-mode voltage around ground.

[26] Measured with PA_POWER set to PA_POWER_MAX. PA_POWER_MAX is a trimmed valued optimized for the 10dBm mode. PA_POWER_MAX is pre-programmed during production into ULP EEPROM module 15.

[27] PA_POWER set to 116d might be beyond the allowed maximum setting of PA_POWER_MAX. This PA_POWER setting is only used for characterization purpose. The application must ensure that PA_POWER value does not exceed PA_POWER_MAX.

[28] The parameter is only valid for driving the maximum current for one GPIO for max 30 seconds per day over a field lifetime of 15 years. Simultaneous LED drive operations (up to three GPIOs) is supported, but the maximal driver on-time of 30 seconds/day has to be divided by the number of simultaneously driven GPIOs. In case of continuous LED drive operation going beyond these conditions performance degradation can not be excluded. Note that the output low voltage level VOL may exceed 0.4V as specified for 1mA output current when used as digital output.

3.3 Dynamic characteristics

Table 182. Dynamic characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 2.0 V to 3.6 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power management							
t_{POR_HLD}	Power-on reset hold time				300	1000	µs
$t_{VDDA,PON}$	VDDA regulator power-on to operation delay				10	30	µs
$t_{VBATREG,PON}$	VBATREG regulator power-on to operation delay (VBATREG)				0.45	1.2	ms
$t_{VBATMON\_SETT}$	Battery brownout detector settling time					15	µs
t_{BAT_FIRST}	Initial delay after battery insertion					1	ms
t_{VDD_STUP}	Device wake-up to POR active delay				50		µs
$t_{AUXCLK,PON}$	Auxiliary oscillator start up time					22	µs
t_{PSMF}	Port sense mono-flop duration				25	100	µs
On-chip RC oscillators							
$f_{OSC,RC}$	Main RC oscillator clock frequency			14.4	16.0	17.6	MHz
$f_{OSC,AUX}$	Auxiliary RC oscillator clock frequency			0.9	1	1.1	MHz
$t_{AUX,PON}$	Auxiliary RC oscillator power-on to operation delay				2	5	µs
On-chip low-frequency oscillators							
$f_{OSC,LPRC}$	Low power RC oscillator clock frequency			165.6	180.0	194.4	kHz
$t_{LPRCCLK,PON}$	Low power RC oscillator start up time				125	300	µs
Transponder demodulator							
t_{ADLY}	Analogue demodulator setup delay					40	µs
t_{AHDLY}	Analog output HIGH setup delay	V_{INpk} = 2.7 V / 7.0 V		4	20	40	µs
t_{ALDLY}	Analog output LOW setup delay	V_{INpk} = 2.7 V / 7.0 V			4	16	µs
t_{DSETUP}	Demodulator setup time					40	µs
t_{IDLE}	Idle time	Tamb = 25°C				80	ms
LF field power-on							
$t_{FLD,HLD}$	LF field hold time		[1]		2048		µs
t_{VDDC}	CVDDC charging time		[2]		2		ms
LF field power-on reset							
$t_{FLD,0-DLY}$	LF field low detection delay time	V_{INpk} = 6 V		1.0	2.2	5	ms
$t_{RESET,SETUP}$	LF field power-on reset setup time		[3]	10			ms
Preprocessor: Code violation (T=1/BRact)							
t_{T-CV}	T duration			T -15%	T	T +15%	µs

Table 182. Dynamic characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 2.0 V to 3.6 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{3T\text{-}CV}$	3T duration			3T -6.5%	3T	3T +6.5%	µs
$t_{8T\text{-}CV}$	8T duration			8T -50	8T	8T +50	µs
Preprocessor: Manchester decoder (T=1/BRact)							
t_T	T duration		[4]	T -32	T	T +30	µs
t_{15T}	1.5T duration		[4]	1.5T -29	1.5T	1.5T +26	µs
t_{2T}	2T duration		[4]	2T -26	2T	2T +30	µs
Active receiver							
t_{ACT_SETT}	Active receiver settling time, after LF Active enable					3.0	ms
t_{POLL_SETT}	Active receiver settling time, for Polling mode t_{ON} and t_{OFF} calc.					2.5	ms
t_{PRE_2k}	Number of preamble bits, 2 kbit/s	BDRATE[1:0]= 00		4			counts
t_{PRE_4k}	Number of preamble bits, 4 kbit/s	BDRATE[1:0]= 01		8			counts
t_{PRE_8k}	Number of preamble bits, 8 kbit/s	BDRATE[1:0]= 10		16			counts
t_{AGC_RISE}	Active receiver AGC rise time	AGCLOWBWEN = 0, 10..90% from V_{IN_BASE} to V_{IN_BURST}		40	125	260	µs
t_{AGC_FALL}	Active receiver AGC fall time	AGCLOWBWEN = 0, 90..10% from V_{IN_BASE} to V_{IN_BURST}	[5]	0.4	1	1.8	ms
$t_{AGC\_LOWBW\_RISE}$	Active receiver AGC rise time, low bandwidth	AGCLOWBWEN = 1, 10..90% from V_{IN_BASE} to V_{IN_BURST}	[5]	100	220	400	µs
$t_{AGC\_LOWBW\_FALL}$	Active receiver AGC fall time, low bandwidth	AGCLOWBWEN = 1, 90..10% from V_{IN_BASE} to V_{IN_BURST}	[5]	0.8	1.75	3	ms
$t_{AGC\_SENSRST}$	AGC sensitivity reset time			50			µs
f_{CARR}	Input carrier frequency, active protocol			122.8	125.0	126.7	kHz
BR_{ACT_2k}	Input bit rate, active protocol, 2 kbit/s	BDRATE[1:0]= 00		1.92	1.95	1.98	kbit/s
BR_{ACT_4k}	Input bit rate, active protocol, 4 kbit/s	BDRATE[1:0]= 01		3.84	3.90	3.96	kbit/s
BR_{ACT_8k}	Input bit rate, active protocol, 8 kbit/s	BDRATE[1:0]= 10		7.68	7.80	7.92	kbit/s
Active limiter							
t_{LIM_RISE}	Limiter rise time		[6]		70	180	µs
t_{LIM_FALL}	Limiter fall time		[6]		1	3	ms

Table 182. Dynamic characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 2.0 V to 3.6 V, f_{C_LF} = 125 kHz, T0 = $1/f_{C\_LF}$, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RSSI							
$t_{RSSI,PON}$	Power-on to operation delay					200	µs
t_{IND}	Range indicator settling time					20	µs
t_{RESPR}	Reset time RSSI peak-detector and indication latch					2	µs
$t_{RANGESEL}$	Range selection settling time					40	µs
$t_{PEAKDSET}$	Peak detector settling time					20	µs
$t_{CHANSEL}$	Channel selection settling time					50	µs
ULP-serial EEPROM							
t_{ULPRET}	Data retention time	T_{amb} = 50°C		20			years
$N_{ULPWR-CYL}$	Write endurance ULP EEPROM	T_{amb} = 25°C	[7]	100 k			cycles
$t_{ULP,PON}$	ULP EEPROM power-on to operation delay					100	µs
t_{ULPDLY}	ULP EEPROM access delay					1	µs
t_{ULPRD}	Read time ULP EEPROM	1 bit				2	µs
		1 byte				20	µs
t_{ULPWR}	Erase/write time ULP EEPROM	1 page	[8]		536		$T_{REF,LF}$
EROM							
t_{ERET}	Data retention time	T_{amb} = 50°C		20			years
$N_{EWR-CYL}$	Write endurance EROM	T_{amb} = 25°C	[7]	10 k			cycles
ADC							
$t_{BG,PON}$	Band gap power-on time	VDDA settled				170	µs
t_{CONV}	ADC conversion time	Measured in number of ADC clock cycles	[11]		21		$1/f_{ADC,CLK}$
P15 (XCLK)							
f_{XCLK}	External clock frequency					5	MHz
t_{XCH}	External clock high time			100			ns
t_{XCL}	External clock low time			100			ns
t_{XCR}	External clock rise time					0.5	µs
t_{XCF}	External clock fall time					0.5	µs
Temperature sensor							
$t_{TEMP,PON}$	Power-on to operation delay (settling time)					20	µs
AES calculation unit							
$t_{AES,CALC}$	Time needed for one 128 bit AES enciphering		[8]		909		$T_{REF,AES}$

Table 182. Dynamic characteristics

T_{amb} = -40 to +85°C, V_{SS} = 0 V, V_{BAT} = 2.0 V to 3.6 V, f_{C_LF} = 125 kHz, T0 = 1/f_{C_LF}, C_{VDDC} = 10 nF connected between pins VDDC and VSS. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Random Number Generator						
$t_{RNG,CALC}$	Time to compute one 16 bit random number			136		1/$f_{OSC,AUX}$
$N_{RNG,ENT15}$	Number of computations to compute a 16 bit random number with entropy factor > 15			9		counts
$t_{RNG,Sett}$	Random number generator settling time	Oscillator settling time	69	85	135	µs
Boot routine						
t_{BOOT_WUP}	Device Boot time, WakeUp event, WakeUp on Battery				1.7	ms
$t_{BOOT\_HTPRO2\_ROM}$	Device Boot time, HT-Pro2 Transponder executed in ROM	HT-Pro2 transponder emulation [9]			20	ms
$t_{BOOT\_TRP\_ROM}$	Device Boot time, Transponder executed in ROM	HT2-E, HT3, HT-AES transponder emulation [9]			9	ms
$t_{BOOT\_TRP\_EROM}$	Device Boot time, Transponder executed in EROM	[10]			12	ms
UHF Transmitter, characterized using NDK 3225GA crystal (CL = 12 pF, f = 27,6 MHz)						
t_{XO_rdy}	XTAL Oscillator Ready settling time			100	200	µs
$t_{TX,LDO}$	Transmitter regulator startup time			20	40	µs
t_{PA_set}	Settling time of the PA				80.2	µs
t_{CCO_set}	Settling time of the CCO	After PLLEN set 1			10	µs
t_{IDAC_set}	Settling time of the IDAC	After the CCO has settled			30	µs
t_{FILT_set}	Settling time of the IDAC filter	After IDAC settled, to be applied by user software only when calibration skipped			30	µs
t_{CAL}	VCO calibration time	After CAL_RUN set 1, if calibration had been performed, not skipped		100	200	µs
t_{ACQ}	PLL Acquisition time	after VCO calibration		35	100	µs

[1] $t_{FLD,HLD}$ is derived by division of the LF field clock (256 * T_0).

[2] t_{VDDC} is application dependent and mainly determined by the coupling factor and C_{VDDC}.

[3] Value holds for a theoretical capacitor value of C_{VDDC} = 47 nF and is determined by $t_{FLD,0\text{-}DLY}$ + 0.1ms * C_{VDDC}/1nF.

[4] Guaranteed by the calibration mechanism of the Manchester decoder.

[5] PDx_6DB = 0: VIN_BASE = 5 mVpp, VIN_BURST = 50 mVpp
PDx_6DB = 1: VIN_BASE = 10 mVpp, VIN_BURST = 100 mVpp

[6] Rectifier output current measured at 90% and at 10% for raising and falling time respectively, with 125kHz burst input signal.

[7] The activation energy equals 0.15eV. According to Arhennius' Law, the number of useful cycles at room temperature is about 2.5 times higher than at 85°C.

[8] The clock period is given precisely in cycle numbers, no Min/Max values suitable. The cycle time can vary.

[9] Boot time of NXP security transponder in ROM up to start of command reception, see transponder family data sheet

[10] Boot time up to invocation of transponder application in EROM

[11] ADC clock cycle $1/f_{ADC,CLK}$ depends on ADC clock selection settings in ADCCLKSEL. In case the Main RC oscillator is selected then $1/f_{ADC,CLK}$ = 250 ns. In case the 27.6 MHz crystal oscillator is selected then $1/f_{ADC,CLK}$ = 290 ns.

4. Mechanical information

4.1 Pin 1 Keep out area

For the purpose of package orientation, so called "pin 1" Identification is included. Pin 1 can be identified by a notch in the die pad as shown in Figure 83.

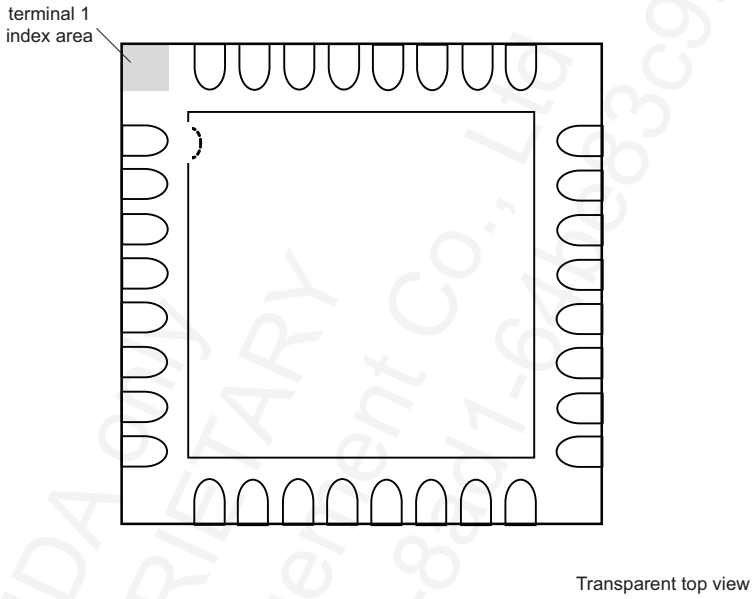
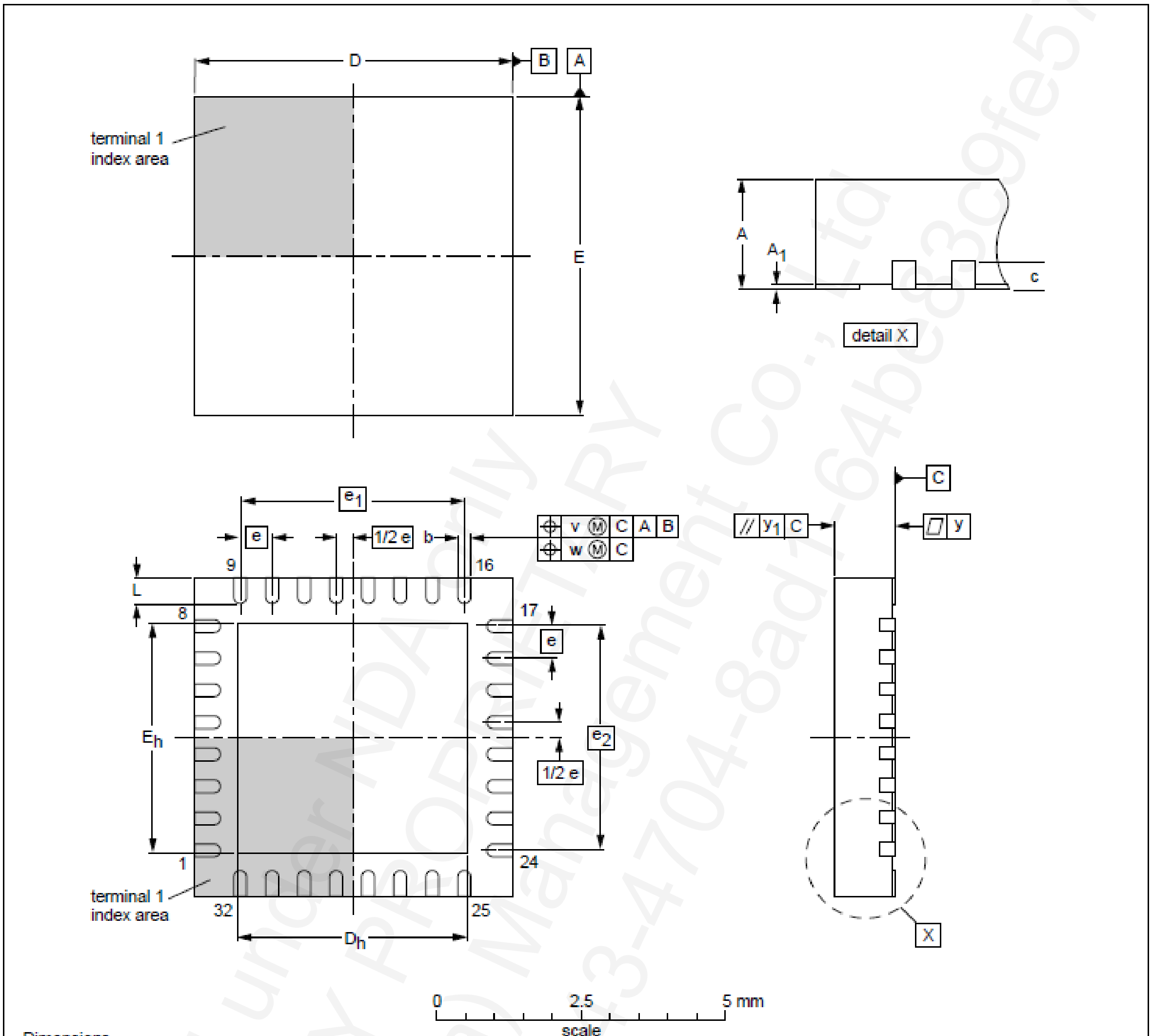


Fig 83. Pin 1 Keep out area HVQFN32

4.2 Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-3**



Dimensions

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-3		MO-220				~~11-06-14~~ 11-06-21

Fig 84. Package outline SOT617-3 (HVQFN32)

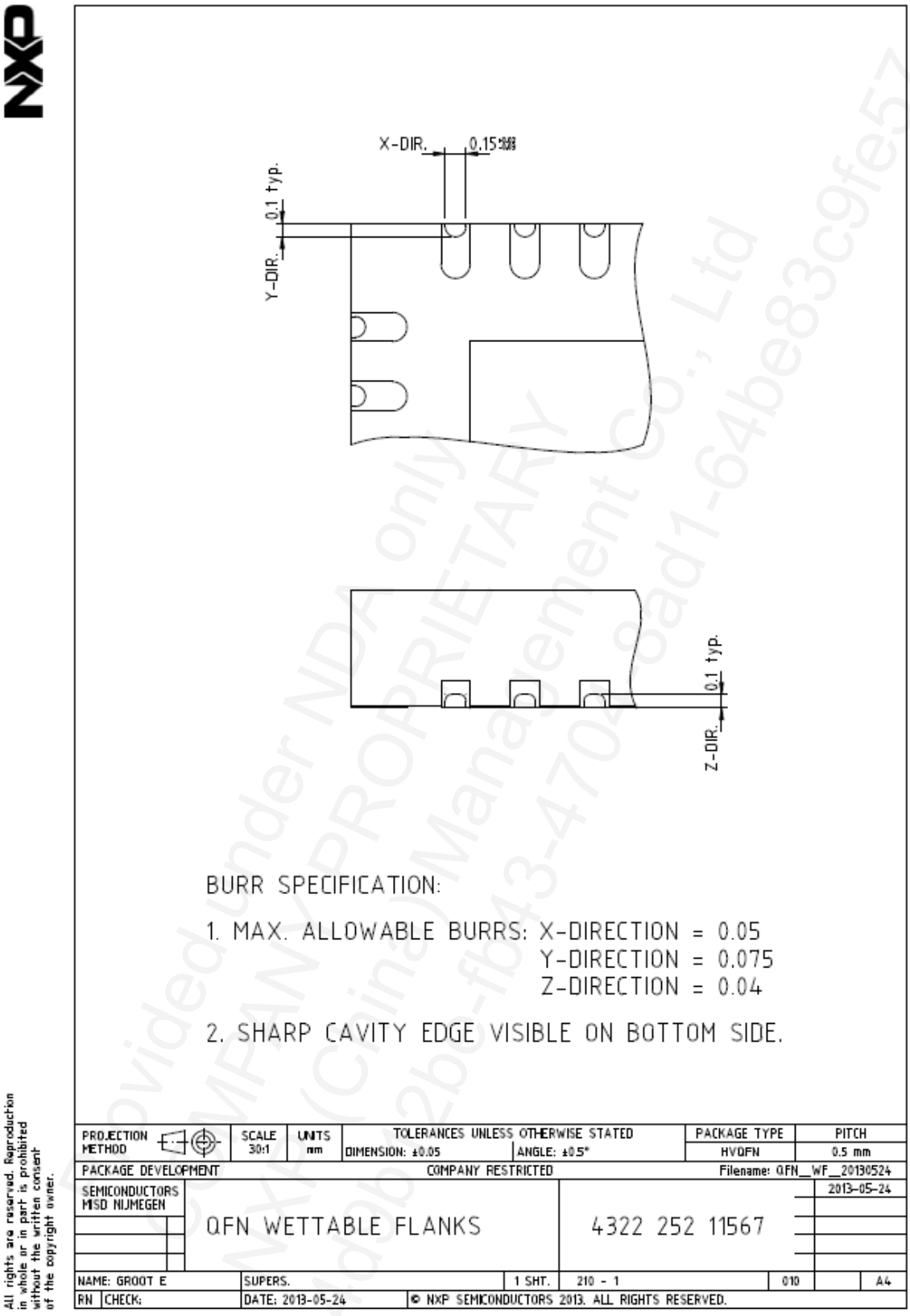


Fig 85. QFN Wettable Flanks outline

5. Handling information

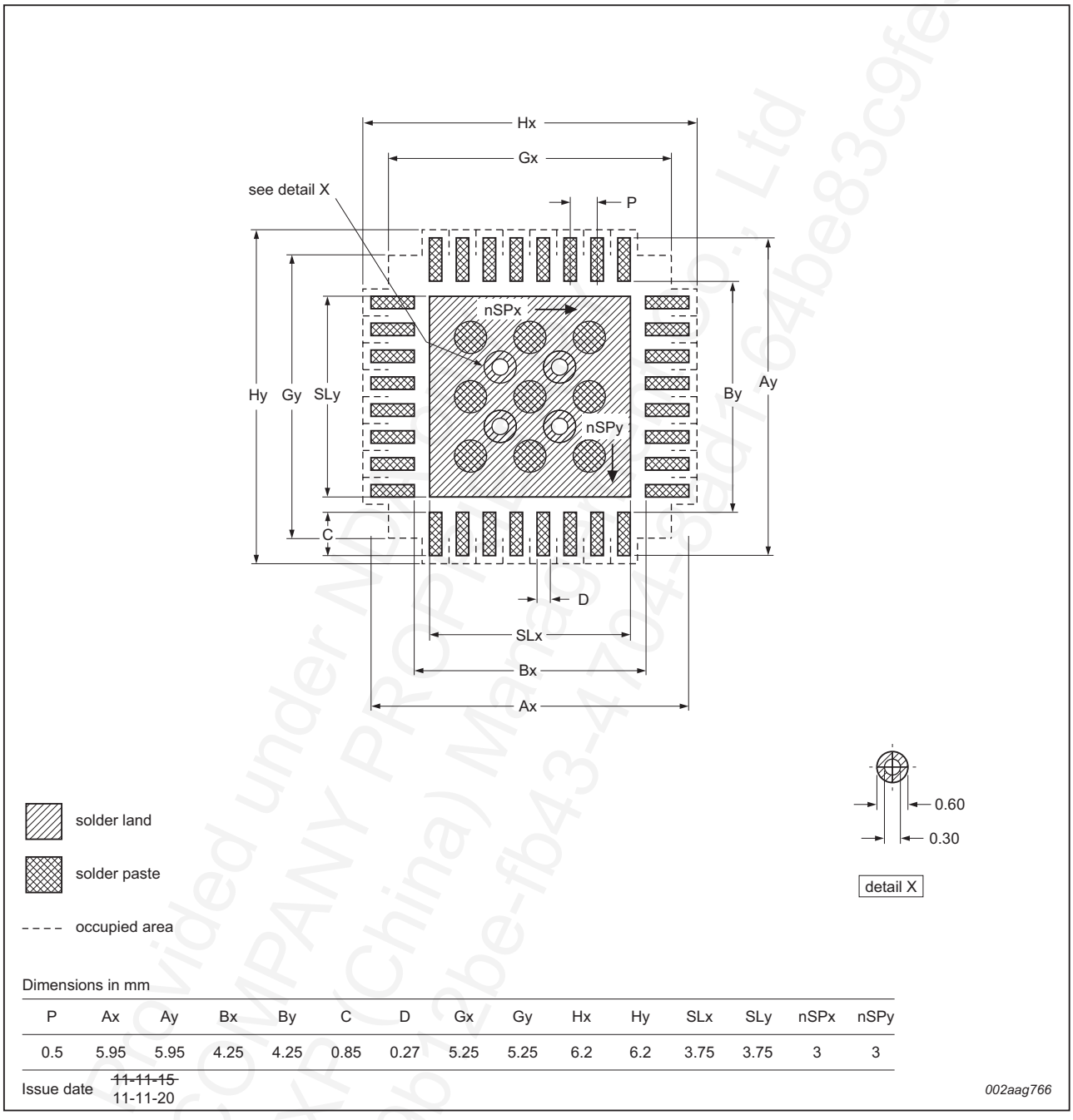
5.1 Packing information

The NCF29A1 / NCF29A2 product is available on 13” tape on reel. The minimum packing quantity is 6000 pieces per reel.

5.2 Soldering

5.2.1 Soldering footprint

Footprint information for reflow soldering of HVQFN32 package



Dimensions in mm

P	Ax	Ay	Bx	By	C	D	Gx	Gy	Hx	Hy	SLx	SLy	nSPx	nSPy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	5.25	5.25	6.2	6.2	3.75	3.75	3	3

Issue date ~~11-11-15~~ 11-11-20

Fig 86. HVQFN32 (5x5) package reflow soldering

5.3 Mounting

For detailed soldering and mounting information please refer to Ref. 3. The application note provides guidelines for the use of HVQFN Packages on printed circuit board (PCB), footprint design and reflow soldering.

This application note also provides guidelines for board mounting of surface mount semiconductor packages.

6. Anomaly Notes

This section provides additional information concerning known anomalies discovered with the device and reports changes that are subject to implementation with future device versions.

6.1 SFR reading corrupted after reading VBATREG SFRs at fCPU>=8MHz

After a VBATREG SFR read, a subsequent VDD/VBAT SFR read will fail if another code fetch is not in progress. Worst case conditions are CPUCLK=16MHz+10%, CPUCLKCYC=0, slow process, low VDD/VBATREG voltage and -40C (temperature inversion in VBATREG=0.85V domain).

The application software must ensure that a “dummy read” from VDD SFR after each VBATREG read is performed.This measure will put some non-VBATREG SFR address on bus to clear data bus and ensures that VBATREG read is performed correctly. Such a Dummy read operation is just adding one instruction.

7. Supplementary information

7.1 Abbreviations

Table 183. Abbreviations

Acronym	Description
CDP encoding	Conditional Diphase Encoding also called Differential Manchester encoding. It is a line code in which data and clock signals are combined to form a single 2-level self-synchronizing data stream. It is a differential encoding, using the presence or absence of transitions to indicate logical value.
NRZ encoding	Non-return-to-zero encoding
BPLM	Binary Pulse Length Modulation
R&C	Read and Cleared
IIU	Immobilizer Interface Unit
PA	Power amplifier

7.2 References

[1] **Application note —** Application Note for the NCF29Ax (TOKEN) Family, Document number AN-CAI 1401

[2] **Application note —** RF Power Amplifier Matching for the NCF29Ax (TOKEN) Family, Document number AN-NCF29A1

[3] **Application note —** Surface mount reflow soldering description, Rev. 6 — 30 July 2012, Document number AN10365

7.3 Revision history

Table 184. Revision history

Revision	Date	Description	Author
3.2	08.10.2015	• Editorial changes • Section 1.2.1 “General”: Single Lithium cell operation, updated typical value to 2.0, corrected typo (Changed Motion detector to Motion sensor) • Section 1.2.5 “Calculation Unit”: corrected typo (changed HT2 to HT2-E) • Section 1.2.6 “RISC Controller”: updated RAM value • Table 2 “NCF29A1 / NCF29A2 type name format” corrected typo (changed HT2 to HT2-E) • Table 4 “NCF29A1 / NCF29A2 marking codes”: corrected typo (changed HT2 to HT2-E) • Section “VBATBRNREG, VBAT brown-out detector register”: changed $V_{BAT\_BRO\_STD}$ to $V_{BO,\ VBAT\_STD}$ and $V_{BAT\_BRO\_EXT}$ to $V_{BO,\ VBAT\_EXT}$ • Figure 4 “Power Supply Domains”: updated (rewording) • moved Figure 6 “Power up timing”: from Section 2.2.2.2 to Section 2.2.2.3 • Section 2.2.4.4 “Power control register PCON1”: added explanation for VBATMONEN • Section 2.3.3.3 “Clock control register CLKCON2”: added explanation for AESCLKSEL[2:0]. • Inserted clarification regarding AES clock selection for the case that RC oscillator is not started up in Section “AESCLKSEL[2:0], AES clock selection”. • Table 19 “Clock control register CLKCON4 (reset value 0000_0x00b)”: added table note [1], changed reset value to “0000_0x00b” • Section 2.5.2.2 “LF telegram”: update in “Data reception”: changed PRESTAT to PREDAT • Editorial changes Section 2.5.3 “Polling of LF Active receiver” • Table 27 “Protocol parameter examples”: updated • Table 29 “Preprocessor control register RTCCON (reset value 80h)”: fixed typo in table header (reset value corrected to 80) • Table 40 “Preprocessor status register PRESTAT (reset value 0000h)”: Access type, description and following remark changed, updated remark about PRESTAT register • Table 52 “RSSI control register RSSICON (reset value 0000h)”: changed SFR bits RSSI_OVF[2:0] access type to “R” • Figure 21 “LF Active interface, block diagram”: figure updated (simplification) • Section 2.6.4 “Transmitter Power On/Off and Output Power Control”: updated • Section 2.6.4.2 “Maximum Current Calculation”: chapter updated • Section 2.5.2.2 “LF telegram”: added explanation • Description for “PDLFACT, power-down LF active receiver” corrected because real time clock crystal oscillator is not available. See Section 2.5.6.3 “Preprocessor control register PRECON2”. • Figure 31 “Typical timing diagram of setup and operation”: figure description updated • Equation 3, Equation 8 and Equation 9 updated (changed to floor function instead of abs function) • Equation 4 FCFRAC correction.	Frank Graeber

Table 184. Revision history

Revision	Date	Description	Author
3.2	08.10.2015	• Table 62 “Current limiter settings register, PALIMIT (reset value 4Ah)”: Updated description of Bit 4 to 0 • Table 67 “VCO calibration control in VCOCALCON (reset value 00h)”: updated • Table 68 “PLL control in PLLCON (reset value 11h)”: updated • Table 69 “Encoder control in ENCCON0 (reset value 0000h)”: updated • Section 2.6.6 “Encoding Control”: updated • Figure 33 “PA block diagram” update: Inserted VDDPA power supply labels into drawing • Figure 34 “Baud rate generator” update • Section 2.6.7 “Modulation Control”: updated • Section 2.9.2.5 “LF tuning capacitors” / Figure 43 “ULP EEPROM memory module 15” Swap of LFTUNE_IMMO with LFTUNE_ACTIVE bits corrected, page 979 inserted, UID removed • Table 88 “Device configuration page DCFG E (content upon delivery see Section 2.26)”: updated • Section 2.9.2.6 “ENWER (ENable Write EROM)”: added • Section 2.6.7.8 “Frequency Ramping Register, FSKRMP”: updated • Table 132 “Watchdog timer control register WDCON (reset value 50h)”: Added WDCON setting 11(bin) which allows transition from WDMODE=01 (fixed time-out selection) to single shot mode. Improved wording. • Section “WDMODE[1:0], watchdog mode selection” bit change correction • Section 2.17 “HT calculation unit”: updated graphics • Table 166 “CRC8 data input register CRC8DIN (reset value xxh)”: added reset value • Table 136 “Port 2 Interrupt Disable register P2INTDIS (reset value xxx0_0000b)” corrected reset value • Reset value of RTCCON corrected, see Table 29 “Preprocessor control register RTCCON (reset value 80h)” • Table 137 “Port 1 output control register P1OUT (reset value 00h)” corrected reset value • Reset value of P2INTDIS corrected, see Table 136 “Port 2 Interrupt Disable register P2INTDIS (reset value xxx0_0000b)” • Table 142 “Port pull up strength control register P2WRES (reset value xx0x_xx11b)” corrected reset value description • Table 150 “P17O port output control bit in port output control registers P1OUT (LED driver is enabled)” updated • Table 152 “ADC control register ADCCON (reset value 00000000_0000xx00b)” corrected reset value • Figure 43 “ULP EEPROM memory module 15” update • Figure 59 “LED driver combined with the general purpose digital I/O port P1.7” update	Frank Graeber

Table 184. Revision history

Revision	Date	Description	Author
3.2	08.10.2015	• Section 2.6.5.3 “Crystal Oscillator Set-up”: “The XO Ready validation circuit is not reporting the XO signal real-time status” removed. • Section 2.6.5.4 “Phase Locked Loop Set-up and VCO Calibration”: updated • Figure 74 “Random number generator block diagram” update • Figure 77 “Boot routine flow chart” updated, moved from Section 2.24.1 to Section 2.24.2 • Section 2.13.1.1 “Watchdog timer control register WDCON” added explanation to WDMODE[1:0] • Section 2.14.1 “Port wake up”: corrected typo (changed ten I/O to all I/O) • Section 2.14.2.5 “Port pull up strength control register PxWRES”: updated • Table 142 “Port pull up strength control register P2WRES (reset value xx0x_xx11b)”: updated • Section 2.15 “LED driver”: updated • Table 166 “CRC8 data input register CRC8DIN (reset value xxh)” added reset value • Table 171 “MSI Flag and Interrupt Register, MSISTAT1 (reset value 00h)”: Corrected access type of SFR bits MSI_OVF and MSI_LFA_PD to "R" instead of "R/W • Table 181 “Static characteristics” I_{PD} min. set from 9 to 10 µA, $V_{BO,VBAT\_EXT}$ max. value changed from **1.94** to **1.86**; corrected typo to be consistent with the CPUCLKCYC conditions to fCPU = XODIV2CLK/4 = 3.45MHz; I_{VDDPA} corrected conditions, added parameters for 434MHz • Table 181 “Static characteristics” $R_{IN\_AC\_Gxx}$ differential measurement, ADC INL/DNL change • Table 181 “Static characteristics” C_{IN_PAS}, C_{STEP}, C_{IN_ACT}, tolerance defined. • Table 182 “Dynamic characteristics”: changed $f_{OSC,LPRC}$ min value to **165.6 kHz** and $t_{FLD,HLD}$ typ value to **2048 µs** • Table 182 “Dynamic characteristics”: inserted battery brownout detector settling time $t_{VBATMON\_SETT}$ • Section 2.21 “Motion sensor”: corrected typo (changed Motion detector to Motion sensor) • Section 2.21.3.6 “Low Power RC Oscillator Frequency Calibration”: corrected typo (changed lw4CAL to PRECON6 LPRC_CAL[3:0]) • Table 181 “Static characteristics”: changed $I_{BAT,TX}$ from PA_POWER = 116d to PA_POWER_MAX • Table 181 “Static characteristics”: changed DNL_{ADC} from **0.65** to **0.72** and INL_{ADC} from **1** to **3** • Table 180: $V_{ESD,CDM}$ 500 V valid for all pins • Table 181 “Static characteristics”: added P2 to reference [3] • Table 182 “Dynamic characteristics”: updated, corrected typo (changed $t_{LPRC,PON}$ to $t_{LPRCLK,PON}$) • Table 182 “Dynamic characteristics”: t_{VDDC} added [2], $t_{RESET,SETUP}$ added [3], t_{CONV} added [10] • Table 183 “Abbreviations”: updated • Figure 12 “LF Field Reset Timing” updated, LF field detection threshold voltage $V_{THR,FDLF-VIN}$ is defined as peak voltage level • Table 181 “Static characteristics”: Conditions for $V_{THR,FDLF-VIN}$ and $V_{THR,FD\_ATIC-VIN}$ clarified, LF field detection threshold voltages are defined as peak voltage level	Frank Graeber

Table 184. Revision history

Revision	Date	Description	Author
3.3		• Figure 1 "Typical application schematic": changed to grey scale colors • Section 1.2.4 "UHF Transmitter": updated • Section 1.6 "Ordering information": updated table note [1] • Section 1.7 "Marking": updated table note [1] • Table 5 "Pin description": Symbol VSS (Pin 33) renamed to EP, changed description • Editorial change Figure 8 "Manual LF pre-switch control" • Table 6 "Device register set": inserted access mode R for PALMIT, bit 5 (RFU) • Table 8 "Battery system register BATSYS1 (reset value xxxx_xxx0b)": corrected typo • Table 9 "Power control register PCON0 (reset value 0100_x000b)": updated VBATRIND description of value 0 • Table 9 "Power control register PCON0 (reset value 0100_x000b)": changed reset value • Figure 63 "RSSI voltage management": updated. Vref-input of ADC changed from VSS to VSSA. • Table 64 "PA trimming register, PATRIM (reset value 2Ch)": inserted access mode R/W • Table 72 "ASK Modulation Magnitude in ASKCON (reset value 009Fh)": inserted access mode R for ASKCON bit 5 (RFU) • Table 71 "Baud rate settings in BRGCON (reset value 317fh)": inserted access mode R for BRGCON bit 14 and 15 • Section "VBATBRNIND, Weak battery indicator": updated • Table 33 "Preprocessor control register PRECON7 (reset value PRECON7 = xxxx_xxxxb)": reset value corrected • Section 2.1 "Special function register set": changed wording "Special Function Register (SFR) set" • Figure 6: changed figure • Full editorial change Section 2.6 "UHF transmitter" • Table 89 "Device configuration page DCFG D (content upon delivery see Section 2.26)": new • Table 130 "Timer 1 compare register T1CMP (reset value T1CMP = xxxx_xxxx_xxxx_xxxxb)": updated reset value • Table 141 "Port pull up strength control register P1WRES (reset value FFh)": replaced pull up resistor values by referenced symbols to static characteristics	Frank Graeber

Table 184. Revision history

Revision	Date	Description	Author
3.3		• Section 2.13.1.1 “Watchdog timer control register WDCON”: updated • Table 142 “Port pull up strength control register P2WRES (reset value xx0x_xx11b)”: replaced pull up resistor values by referenced symbols to static characteristics • Table 152 “ADC control register ADCCON (reset value 00000000_0000xx00b)”: changed description • Table 160 “Random number generator data register RNGDAT (reset value xxh)”: updated reset value • Table 154 “ADC data register ADCDAT (reset value x0xxxx00_00000000b)”: changed Access from **W0** to **R** • Section 2.21 “Motion sensor”: changed wording: The device provides the capability to operate with an external Motion Sensor component via the dedicated GPIO Pin P21_MD (rolling-ball movement sensor). • Table 137 “Port 1 output control register P1OUT (reset value 00h)”: inserted access mode for R/W for P1OUT.P110 • Table 138 “Port 2 output control register P2OUT (reset value xxxxxx00b)”: inserted access mode for R/W for P2OUT.P210 • Table 171 “MSI Flag and Interrupt Register, MSISTAT1 (reset value 00h)”: change access more from R/W to R/W1->0 for MSI_MOT_INT and MSI_OVF_INT • Table 179 “EEPROM content upon delivery”: changed Content at delivery for page 976 • Table 180 “Limiting values In accordance with the Absolute Maximum Rating System (IEC 60134) [5].”: added row for $V_{max,xtal}$ absolute maximum rating for pin XTAL1 and XTAL2 with min = -0.3V and max = 1.95V is required. • Table 181 “Static characteristics” added $V_{VBATIND}$, $V_{VBATIND\_HYST}$, $R_{VBATIND}$ I_{Limit_Offset} introduced, changed conditions of symbol PN_{PLL}, E_{REF}, and P_{OUT} • Table 181 “Static characteristics”: added conditions for ΔI_{DD_AES} • Table 182 “Dynamic characteristics” t_{PA_set} , PA settling time max. 80.2 µs • Table 182 “Dynamic characteristics”: changed Settling time of the IDAC t_{IDAC_set} to 30 µs, changed Settling time of the IDAC filter t_{FILT_set} to 30 µs • Table 152 “ADC control register ADCCON (reset value 00000000_0000xx00b)”: updated description for ADCCON.CONVSTART • Table 178 “SPI 0/1 status register SPIxSTAT (reset value 00h)”: changed Access from **W0** to **R0/W0** • Table 181 “Static characteristics”: "RTC_EN" setting removed from characteristics conditions. Condition is already sufficiently defined by “IT_MODE” setting • Clarifications inserted for all “RFU” and “RDT” SFR bits. Note that read operation to 'RFU' bits may return an undefined result. For future compatibility, a write operation shall assign a '0'. • Table 181 “Static characteristics”: deleted unused footnote [9]	Frank Graeber

Table 184. Revision history

Revision	Date	Description	Author
3.4	24.06.2016	• Table 182 “Dynamic characteristics”: changed unit of symbol $t_{VDDA,PON}$ to µs • Table 181 “Static characteristics”: removed parameter I_{OL} and I_{OH} to prevent misinterpretation because these two parameters were never meant for normal operating conditions. • Table 181 “Static characteristics”: Inserted new parameter I_{OL} as replacement for old parameter I_{OL} but using new parameter definition and conditions. • Table 182 “Dynamic characteristics”: inserted reference to NDK 3225GA crystal used for UHF transmitter characterization	Frank Graeber

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