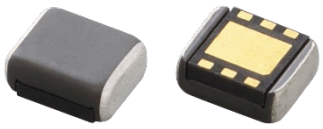
# "PicoBK™" MYRLP-F-RD/RE series

Ultra-Low Quiescent Current, Inductor Built-in Step-Down DC/DC Converter

☆Green Operation compatible

## GENERAL DESCRIPTION

The MYRLP-F-RD/RE series is a synchronous step-down mini DC/DC converter which integrates an inductor and a control IC in one tiny package.
It uses an ultra-low current consumption circuit and PFM control.
The control IC and coil are integrated to achieve miniaturization, and a space-saving power supply can be configured simply by adding two external capacitors. In addition, the ultra-low current consumption circuit and PFM control method realize high efficiency with a light load.



A operating voltage range of 1.8V to 6.0V enables support for applications that require an internally fixed output voltage from 0.5V to 3.60V. It has a built-in UVLO (Under Voltage Lock Out) function, the internal P-channel MOS driver transistor and N-channel MOS driver transistor are turned OFF when input voltage is below the UVLO detection voltage. The MYRLP-F-RD integrates CL discharge function which enables the electric charge at the output capacitor CL to be discharged via the internal discharge switch located between the VOUT and GND. When the devices enter stand-by mode, output voltage quickly returns to the VSS level as a result of this function.

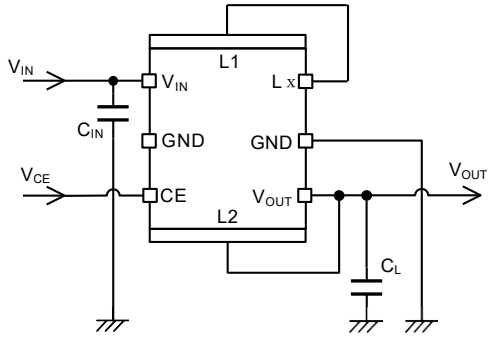
## ■APPLICATIONS

- Smart meter
- Low Power RF
- Sensor Module
- Wearable Devices
- Energy Harvest devices
- Back-up power supply circuit
- Smart card
- Devices with 1 Lithium cell

## ■FEATURES

| | | |
|---|---|---|
| Input Voltage Range | : | 1.8V ~ 6.0V |
| Output Voltage Setting | : | 0.5V ~ 3.60V |
| Output Voltage Accuracy | : | ±20mV ($V_{OUT}$ ≦ 1.0V)<br>±2.0% ($V_{OUT}$ > 1.0V) |
| Output Current | : | 150mA |
| Supply Current | : | 200nA @ $V_{OUT}$=1.8V |
| Control Method | : | PFM control |
| Function | : | $C_L$ Discharge (MYRLP-F-RD)<br>UVLO function |
| Protection Functions | : | Short Protection |
| Input / Output Capacitor | : | Ceramic Capacitor Compatible |
| Operation Ambient Temperature | : | -40 ~ 85℃ |
| Environmentally Friendly | : | EU RoHS compliant, Pb Free<br>Halogen Free |

## ■TYPICAL APPLICATION CIRCUIT

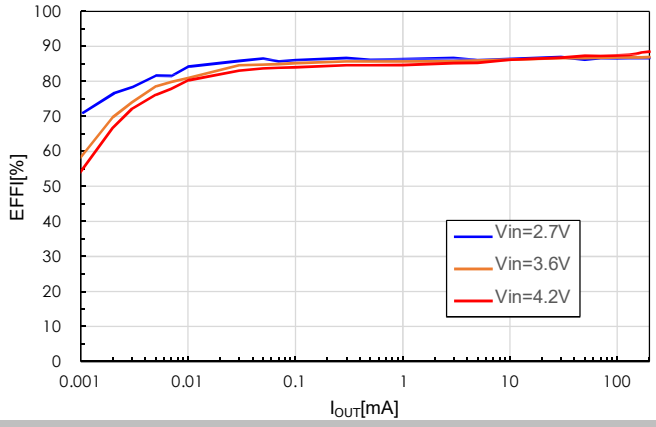



< MYRLP-F-RD/RE Series >

## ■ TYPICAL PERFORMANCE CHARACTERISTICS

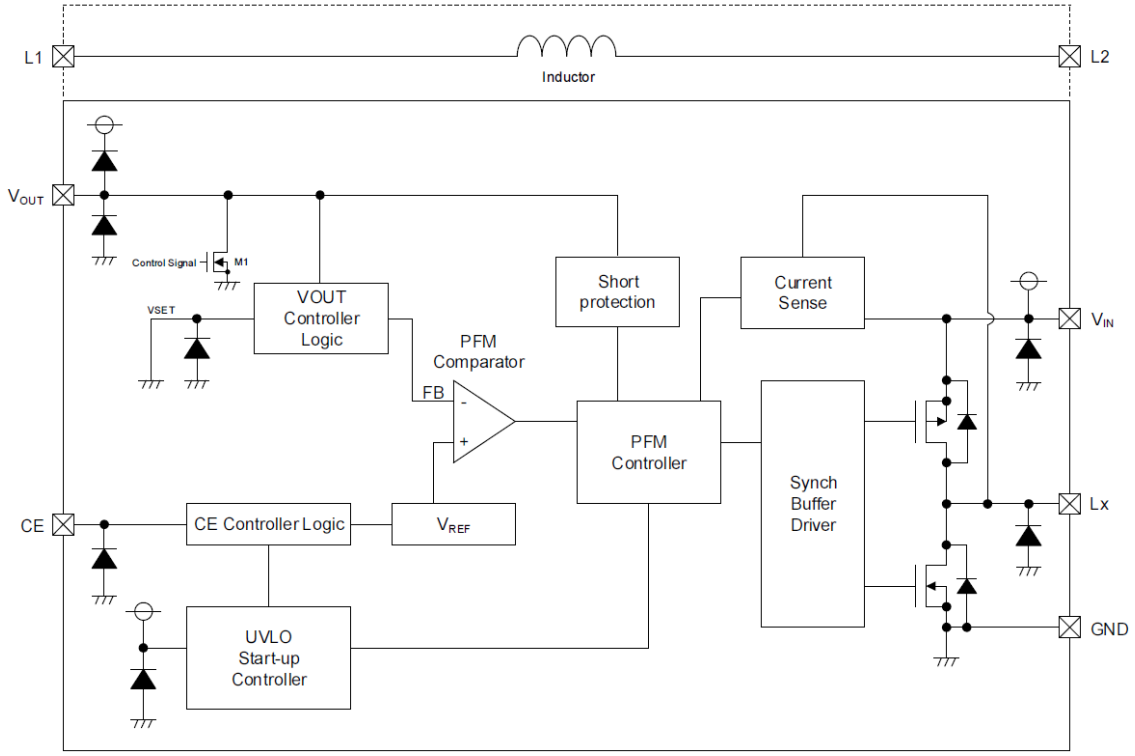
MYRLP-F-RD

$V_{OUT}$ =1.8V, $C_{IN}$ =10μF, $C_L$ =20μF, Ta=25℃



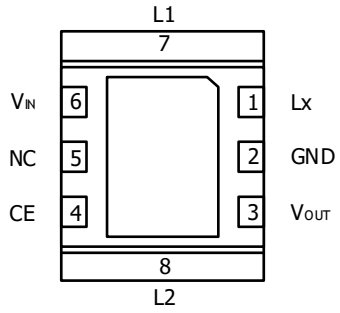
## ■ BLOCK DIAGRAM

MYRLP-F-RD/RE Series




* Diodes inside the circuits are ESD protection diodes and parasitic diodes.
MYRLP-F-RE does not have $C_L$ Discharge function.

## ■ PIN CONFIGURATION




< BOTTOM VIEW >

* The dissipation pad should be solder-plated in recommended mount pattern and metal masking to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No.2) pin.

## ■ PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTION |
|---|---|---|
| 1 | Lx | Switching |
| 2 | GND | Ground |
| 3 | $V_{OUT}$ | Output Voltage |
| 4 | CE | Chip Enable |
| 5 | GND | Ground |
| 6 | $V_{IN}$ | Input Voltage |
| 7 | L1 | Inductor Electrodes |
| 8 | L2 | Inductor Electrodes |

* The NC (No.5) pin is not connected to the chip.

## ■ FUNCTION

| PIN NAME | SIGNAL | STATUS |
|---|---|---|
| CE | H | Active |
| | L | Stand-by |

* Please do not leave the CE pin open.

## ■ PRODUCTION SUFFIX

| Product Series Name | Output voltage | Output Current | Switched Type | Product Size | | Package | Function |
|---|---|---|---|---|---|---|---|
| MYRLP | 180 | 015 | F | 2 | 1 | R | E/D |
| Ultra-Low Quiescent Current | 120=1.2V<br>180=1.8V<br>330=3.3V | 015=150mA | PFM Control | 2=2mm<br>*Please see tolerance | 1=1mm<br>*Please see tolerance | Tape & Reel | E= Without CL Discharge<br>D=Wit CL Discharge |

## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATINGS | UNITS |
|---|---|---|---|
| $V_{IN}$ Pin Voltage | $V_{IN}$ | -0.3 ~ 7.0 | V |
| Lx Pin Voltage | $V_{LX}$ | -0.3 ~ $V_{IN}$ + 0.3 or 7.0 (*1) | V |
| $V_{OUT}$ Pin Voltage | $V_{OUT}$ | -0.3 ~ $V_{IN}$ + 0.3 or 7.0 (*1) | V |
| CE Pin Voltage | $V_{CE}$ | -0.3 ~ 7.0 | V |
| Power Dissipation (Ta=25℃) | Pd | TBD (JESD51-7board) (*2) | mW |
| Operating Ambient Temperature | Topr | -40 ~ 85 | ℃ |
| Storage Temperature | Tstg | -55 ~ 125 | ℃ |

* All voltages are described based on the GND pin.
(*1) The maximum value should be either $V_{IN}$+0.3V or 7.0V in the lowest.
(*2) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

# ■ ELECTRICAL CHARACTERISTICS

MYRLP-F-RD/RE Series

Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|---|
| Output Voltage(*1) | $V_{OUT}$ | When connected to external components, $I_{OUT}$ = 30mA | | - | <T-1> | - | V | ① |
| Output Voltage1-2 | $V_{OUT1-2}$ | Voltage which Lx pin changes "H" to "L" level while $V_{OUT}$ is increase. (*5) | | <E-1> | <E-2> | <E-3> | V | ② |
| Operating Voltage Range | $V_{IN}$ | - | | <C-1> | - | 6.0 | V | ① |
| Maximum Output Current | $I_{OUTMAX}$ | When connected to external components (*2) | | 150 | - | - | mA | ① |
| UVLO Release Voltage | $V_{UVLOR}$ | $V_{OUT}$ = 0.0V , $V_{CE}$ = 1.8V<br>Voltage which Lx pin holding "H" level(*5) | Ta=25℃<br>Ta=-40~85℃ (*3) | - | 1.50 | 1.78 | V | ② |
| UVLO Detect Voltage | $V_{UVLOD}$ | $V_{OUT}$ = 0.0V , $V_{CE}$ = 1.8V<br>Voltage which Lx pin holding "L" level(*5) | Ta=25℃<br>Ta=-40~85℃ (*3) | 1.00 | 1.40 | - | V | ② |
| Quiescent Current | Iq | $V_{IN}$ = $V_{CE}$ =<C-1>, $V_{OUT}$ = $V_{OUT}$×1.05 | | - | <E-4> | <E-5> | nA | ③ |
| Stand-by Current | $I_{STB}$ | $V_{IN}$ = $V_{OUT}$ = 6.0V | | - | 0.0 | 0.1 | μA | ③ |
| PFM Switching Current | $I_{PFM}$ | When connected to external components, $V_{IN}$ = $V_{OUT(T)}$ + 2.0V, $I_{OUT}$ = 10mA | | - | 400 | 600 | mA | ① |
| Efficiency | EFFI | $I_{OUT}$ = 30mA | | - | <E-6> | - | % | ① |
| Lx SW "H" ON Resistance | $R_{LXH}$ | $V_{OUT}$ = 0.0V, $V_{IN}$ = $V_{CE}$ = 5.0V, ILx = 50mA | | - | 0.35 | 0.45 | Ω | ④ |
| Lx SW "L" ON Resistance(*3) | $R_{LXL}$ | $V_{IN}$ = 5.0V | | - | 0.32 | 0.42 | Ω | - |
| Lx SW "H" Leakage Current | $I_{LeakH}$ | $V_{IN}$ = 6.0V , $V_{OUT}$ = $V_{CE}$ = 0.0V , VLx = 6.0V | | - | 0.0 | 0.1 | μA | ④ |
| Lx SW "L" Leakage Current | $I_{LeakL}$ | $V_{IN}$ = 6.0V , $V_{OUT}$ = $V_{CE}$ = 0.0V , VLx = 0.0V | | - | 0.0 | 0.1 | μA | ④ |
| Output Voltage Temperature Characteristics | $\Delta V_{OUT}/(\Delta V_{OUT} \cdot \Delta Topr)$ | $I_{OUT}$ = 30mA<br>-40℃ ≦ Topr ≦ 85℃ | | - | ±100 | - | ppm/℃ | ① |
| CE "H" Voltage | $V_{CEH}$ | $V_{OUT}$ = 0.0V,<br>Voltage which Lx pin holding "H" level(*5) | Ta=25℃<br>Ta=-40~85℃ (*3) | 1.2 | - | 6.0 | V | ② |
| CE "L" Voltage | $V_{CEL}$ | $V_{OUT}$ = 0.0V,<br>Voltage which Lx pin holding "L" level(*5) | Ta=25℃<br>Ta=-40~85℃ (*3) | GND | - | 0.3 | V | ② |
| CE "H" Current | $I_{CEH}$ | $V_{IN}$ = 6.0V, $V_{OUT}$ = 0.0V , $V_{CE}$ = 6.0V | | -0.1 | 0.0 | 0.1 | μA | ⑤ |
| CE "L" Current | $I_{CEL}$ | $V_{IN}$ = 6.0V, $V_{OUT}$ = 0.0V , $V_{CE}$ = 0.0V | | -0.1 | 0.0 | 0.1 | μA | ⑤ |
| Short Protection Threshold Voltage (*4) | $V_{SHORT}$ | Voltage which Lx pin holding "L" level(*5) | Ta=25℃<br>Ta=-40~85℃ (*3) | 0.10 | 0.54 | 0.80 | V | ② |
| $C_L$ Discharge (MYRLP-F-RD) | $R_{DCHG}$ | $V_{IN}$ = 5.0V, $V_{CE}$ = 0.0V, $V_{OUT}$=0.1V | | 29 | 45 | 60 | Ω | ② |
| Inductance Value | L | Test Frequency=1MHz | | - | 2.2 | - | μH | |
| Inductor Rated Current | $I_{DC\_L}$ | ΔT=+40℃<br>Current value that raises the temperature by 40℃<br>With DC current | | - | 850 | - | mA | |

Unless otherwise stated, $V_{IN}$=5V, $V_{CE}$=5V, $V_{OUT(T)}$=Nominal Value

(*1) $V_{OUT}$ are the average values of the output voltage considering the ripple voltage and they are set so that they can be a setting output voltage with this evaluation condition.

(*2) The maximum output current performance varies based on a voltage difference between an input voltage and an output voltage, and external components and so on. Regarding detail of this variation, please refer to OPERATIONAL EXPLANATION and NOTE ON USE section.

(*3) Design value

(*4) SHORT PROTECTION with LATCH is not available if $V_{OUT1}$ is 1.2V or less.

(*5) "H" = $V_{IN}$ ~ $V_{IN}$ -1.2V, "L" = 0.1V ~ -0.1V

# ■ ELECTRICAL CHARACTERISTICS

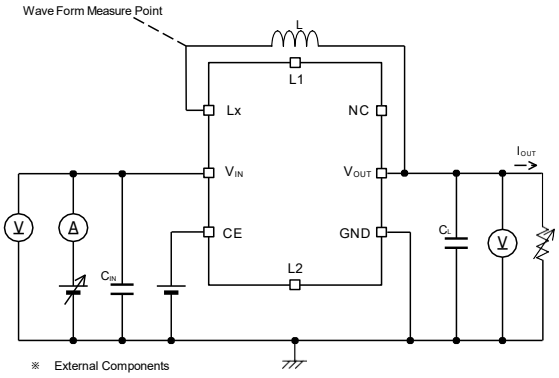
SPEC Table

| Part Number | NOMINAL OUTPUT VOLTAGE | $V_{OUT}$(V) | $V_{OUT1-2}$(V) | | | $V_{IN}$(V) | Iq(nA) | |
|---|---|---|---|---|---|---|---|---|
| | | <T-1> | <E-1> | <E-2> | <E-3> | <C-1> | <E-4> | <E-5> |
| | $V_{OUT(T)}$ | TYP. | MIN. | TYP. | MAX. | $V_{IN}$ | TYP. | MAX. |
| MYRLP060015F21RD | 0.60 | 0.600 | 0.560 | 0.580 | 0.600 | 1.80 | 200 | 600 |
| MYRLP080015F21RD | 0.80 | 0.800 | 0.760 | 0.780 | 0.800 | 1.80 | 200 | 600 |
| MYRLP090015F21RD | 0.90 | 0.900 | 0.860 | 0.880 | 0.900 | 1.80 | 200 | 600 |
| MYRLP100015F21RD | 1.00 | 1.000 | 0.960 | 0.980 | 1.000 | 1.80 | 200 | 600 |
| MYRLP120015F21RD | 1.20 | 1.200 | 1.156 | 1.180 | 1.204 | 1.80 | 200 | 600 |
| MYRLP180015F21RD | 1.80 | 1.800 | 1.744 | 1.780 | 1.816 | 2.30 | 200 | 600 |
| MYRLP200015F21RD | 2.00 | 2.000 | 1.940 | 1.980 | 2.020 | 2.50 | 210 | 630 |
| MYRLP250015F21RD | 2.50 | 2.500 | 2.430 | 2.480 | 2.530 | 3.00 | 220 | 660 |
| MYRLP300015F21RD | 3.00 | 3.000 | 2.920 | 2.980 | 3.040 | 3.50 | 230 | 690 |
| MYRLP330015F21RD | 3.30 | 3.300 | 3.214 | 3.280 | 3.346 | 3.80 | 240 | 720 |
| MYRLP060015F21RE | 0.60 | 0.600 | 0.560 | 0.580 | 0.600 | 1.80 | 200 | 600 |
| MYRLP080015F21RE | 0.80 | 0.800 | 0.760 | 0.780 | 0.800 | 1.80 | 200 | 600 |
| MYRLP090015F21RE | 0.90 | 0.900 | 0.860 | 0.880 | 0.900 | 1.80 | 200 | 600 |
| MYRLP100015F21RE | 1.00 | 1.000 | 0.960 | 0.980 | 1.000 | 1.80 | 200 | 600 |
| MYRLP120015F21RE | 1.20 | 1.200 | 1.156 | 1.180 | 1.204 | 1.80 | 200 | 600 |
| MYRLP180015F21RE | 1.80 | 1.800 | 1.744 | 1.780 | 1.816 | 2.30 | 200 | 600 |
| MYRLP200015F21RE | 2.00 | 2.000 | 1.940 | 1.980 | 2.020 | 2.50 | 210 | 630 |
| MYRLP250015F21RE | 2.50 | 2.500 | 2.430 | 2.480 | 2.530 | 3.00 | 220 | 660 |
| MYRLP300015F21RE | 3.00 | 3.000 | 2.920 | 2.980 | 3.040 | 3.50 | 230 | 690 |
| MYRLP330015F21RE | 3.30 | 3.300 | 3.214 | 3.280 | 3.346 | 3.80 | 240 | 720 |

With regard to other voltage, please contact our sales representative.

# ■ TEST CIRCUITS

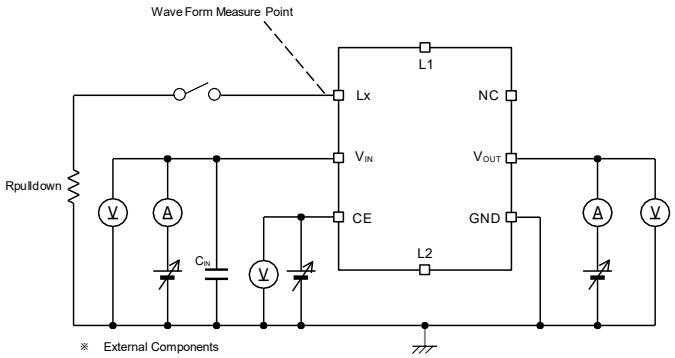
< Test Circuit No.① >




※ External Components

L : 2.2μH(For test process)
$C_{IN}$ : 10μF
$C_L$ : 10μF

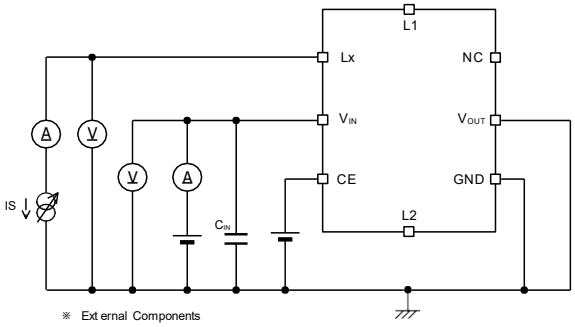
< Test Circuit No.② >




※ External Components

$C_{IN}$ : 10μF
Rpulldown : 100Ω

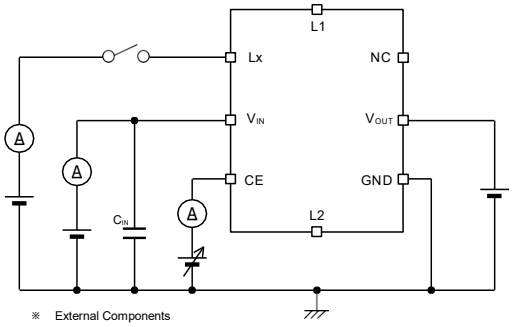
< Test Circuit No.③ >




※ Ext ernal Components

$C_{IN}$ : 10μF

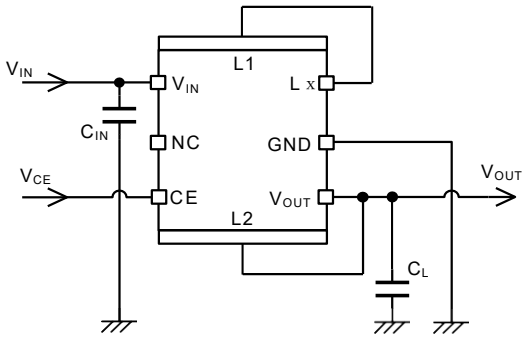
< Test Circuit No.④ >




※ External Components

$C_{IN}$ : 0.1μF

# TYPICAL APPLICATION CIRCUIT




(NOTES):
The coil is exclusively for this product.
Please do not use it for any purpose other than this product.

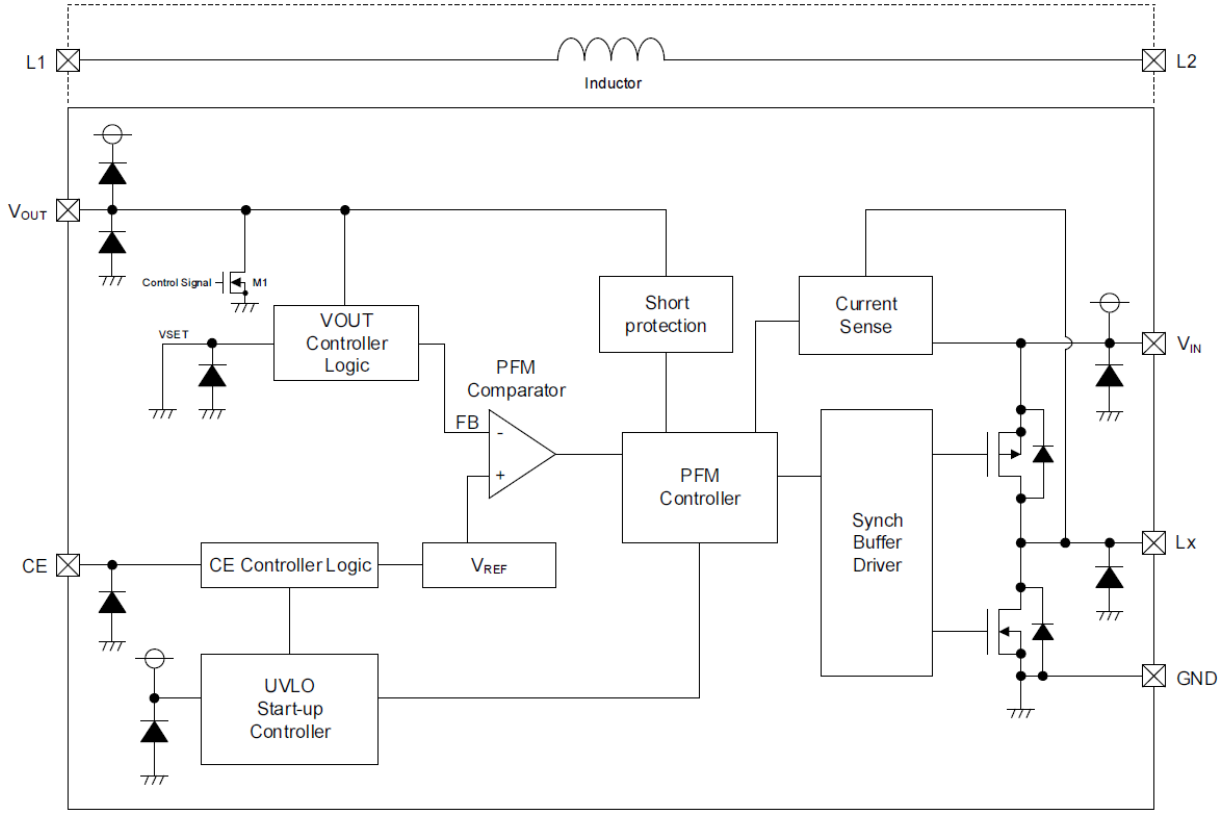
【Typical Examples】

| | Manufacture | Product Number | Value | Size |
|---|---|---|---|---|
| $C_{IN}$ | Murata | GRM188R61A106ME69 | 10µF/10V | 1.6 x 0.8 x 1.0mm |
| $C_L$ | Murata | GRM188R61A106ME69 | 10µF/10V | 1.6 x 0.8 x 1.0mm |
| | | GRM188R61A226ME15 | 22µF/10V | |

Please select the components taking into consideration the rated voltage, rated current, and ceramic capacitor DC bias characteristics, etc.
Use a ceramic capacitor with an execution capacitance value equal to or higher than the recommended component.
If a capacitor with a low effective capacitance value is used, the output voltage may become unstable.
Please increase a capacitance value for $C_L$ in order to reduce output ripple voltages.
$C_L$ such as tantalum capacitors which have a larger ESR value can increase output ripple voltages.
If large-capacity capacitors such as electrolytic capacitors are connected in parallel, the inrush current may increase at startup and the output voltage may become unstable.

## ■ OPERATIONAL EXPLANATION

The MYRLP-F-RD/RE series consists of a reference voltage supply, PFM comparator, Pch driver FET, Nch driver FET, current sensing circuit, PFM control circuit, CE control circuit, and others.




< BLOCK DIAGRAM >

The efficiency performance at a light load current is significantly improved compared to existing Murata products by implementing a current limit PFM as a control method and reducing a consumption current by IC itself.

## ■OPERATIONAL EXPLANATION (Continued)

<Normal operation>

This IC controls the output voltage by adjusting the following ①~③ operation intervals in response to the output current.
The $V_{OUT}$ output voltage average values during actual operation depend on $V_{OUT}$ and the ripple voltage during actual operation and are calculated as follows. For this reason, if the ripple voltage changes due to the influence of the input voltage, output voltage, or peripheral components, etc., the output voltage average value will change.

$$V_{OUT} = V_{OUT1\text{-}2} + \text{Ripple Voltage} \times 1/2$$

①The feedback voltage (FB voltage) is the voltage that results from dividing the output voltage with the VOUT Controller logic circuit. The PFM comparator compares this FB voltage to $V_{REF}$. When the FB voltage is lower than $V_{REF}$, the PFM comparator sends a signal to the PFM control circuit to turn on the Pch driver FET.

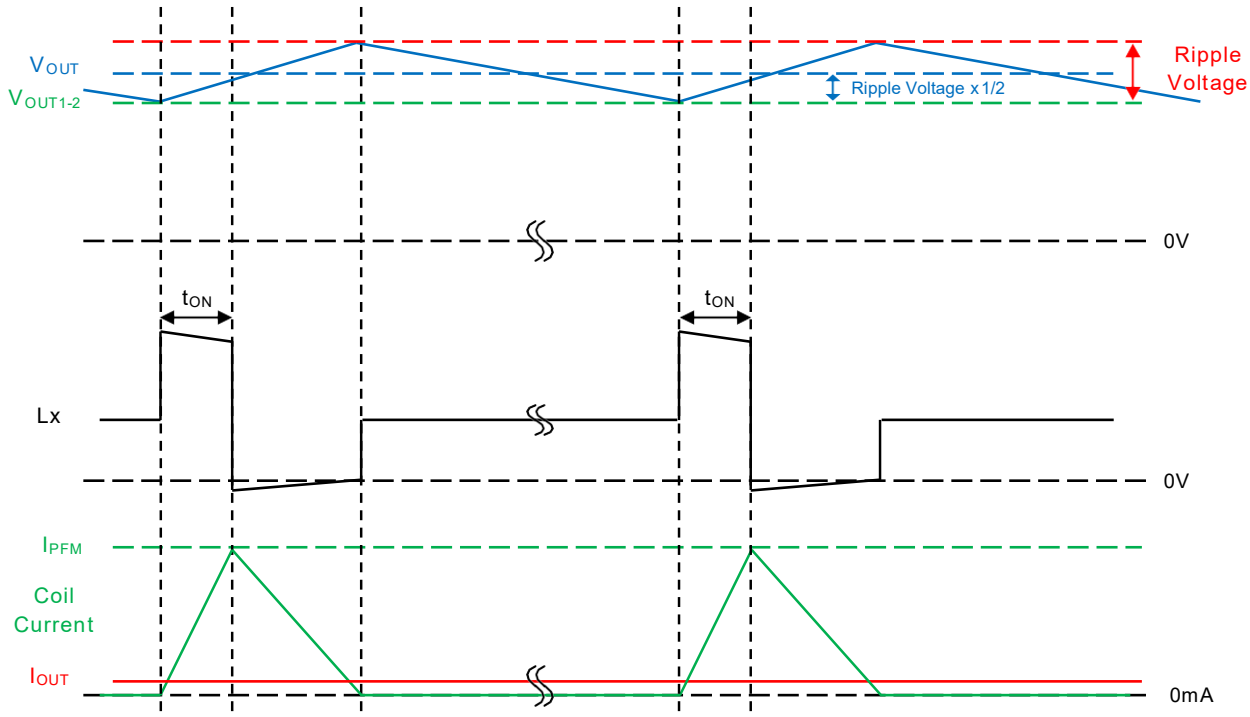
The On Time to Pch driver FET can be obtained by the following equation.

$$t_{ON} = L \times I_{PFM} / (V_{IN} - V_{OUT})$$

②When the Pch driver FET turns on, the coil current increases until the coil current reaches PFM Switching Current ($I_{PFM}$). When the coil current reaches $I_{PFM}$, the Pch driver FET turns off and then the Nch driver FET turns on.

③ After the Nch driver FET turns on, the coil current will decrease and when the coil current goes down to approx. 0mA, the Nch driver FET will turn off.
The Pch driver FET and Nch driver FET remain off until the FB voltage becomes lower than the reference voltage $V_{REF}$.

The above ①~③ switching operations increase the FB voltage accompanying the output voltage increase, but if the PFM comparator determines the FB voltage is lower than the reference voltage $V_{REF}$ before the coil current reaches 0mA, the Nch driver FET turns off and the status moves to ①.



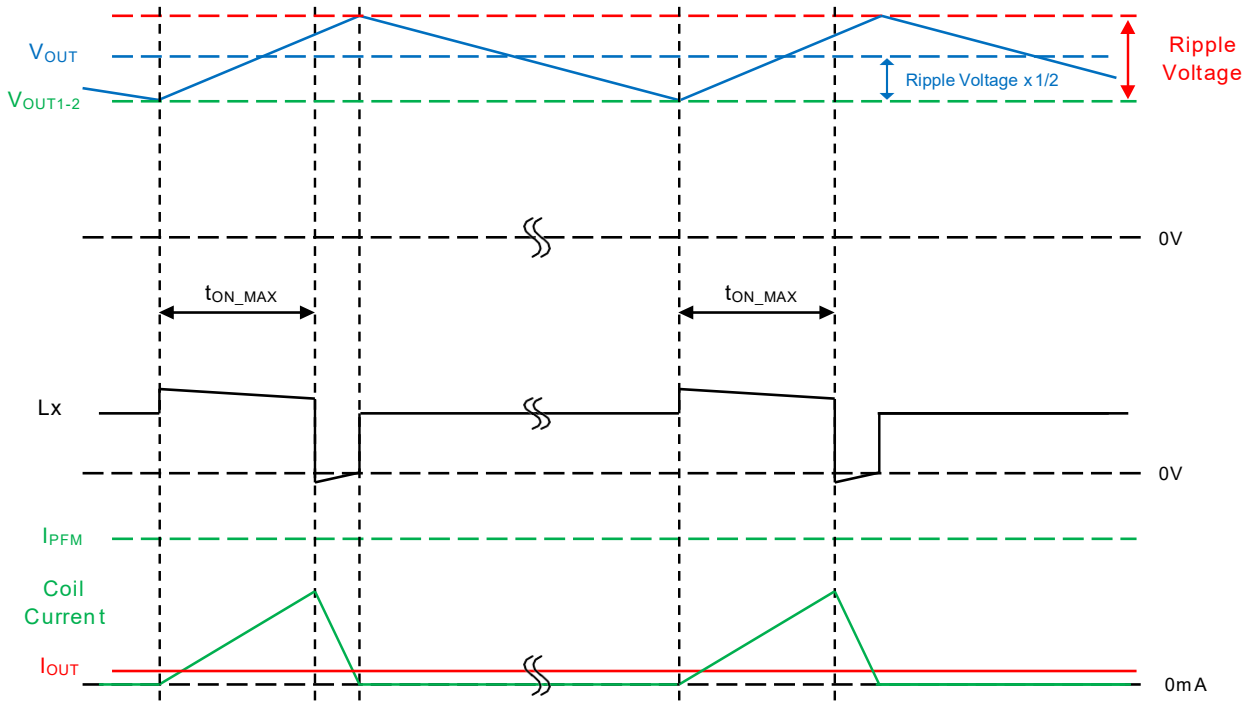
## ■ OPERATIONAL EXPLANATION (Continued)

< Maximum on-time function, 100% Duty operation>

When the input / output potential difference decreases, the on-time required for the coil current to reach $I_{PFM}$ increases, and the output ripple voltage tends to increase. Therefore, under conditions where the input / output potential difference is small, excessive ripple voltage is suppressed by limiting the maximum on-time that the Pch driver FET can turn on after the FB voltage becomes higher than the reference voltage $V_{REF}$ to 3.0µs (TYP.).

If the input / output potential difference is further reduced, the FB voltage is always lower than the reference voltage $V_{REF}$, so the 100% duty operation is performed and the Pch driver FET is always on.

At 100% duty, the current consumption of the IC increases compared to normal operation.



## ■OPERATIONAL EXPLANATION (Continued)

<CE function>

When "H" voltage ($V_{CEH}$) is fed to the CE pin, normal operation starts after raising the output voltage with Start-up Mode. When the "L" voltage ($V_{CEL}$) is fed to the CE pin, it enters the stand-by state and the current consumption is suppressed to 0.0μA (TYP.). Additionally, Pch MOS driver FET and Nch MOS driver FET are turned off.

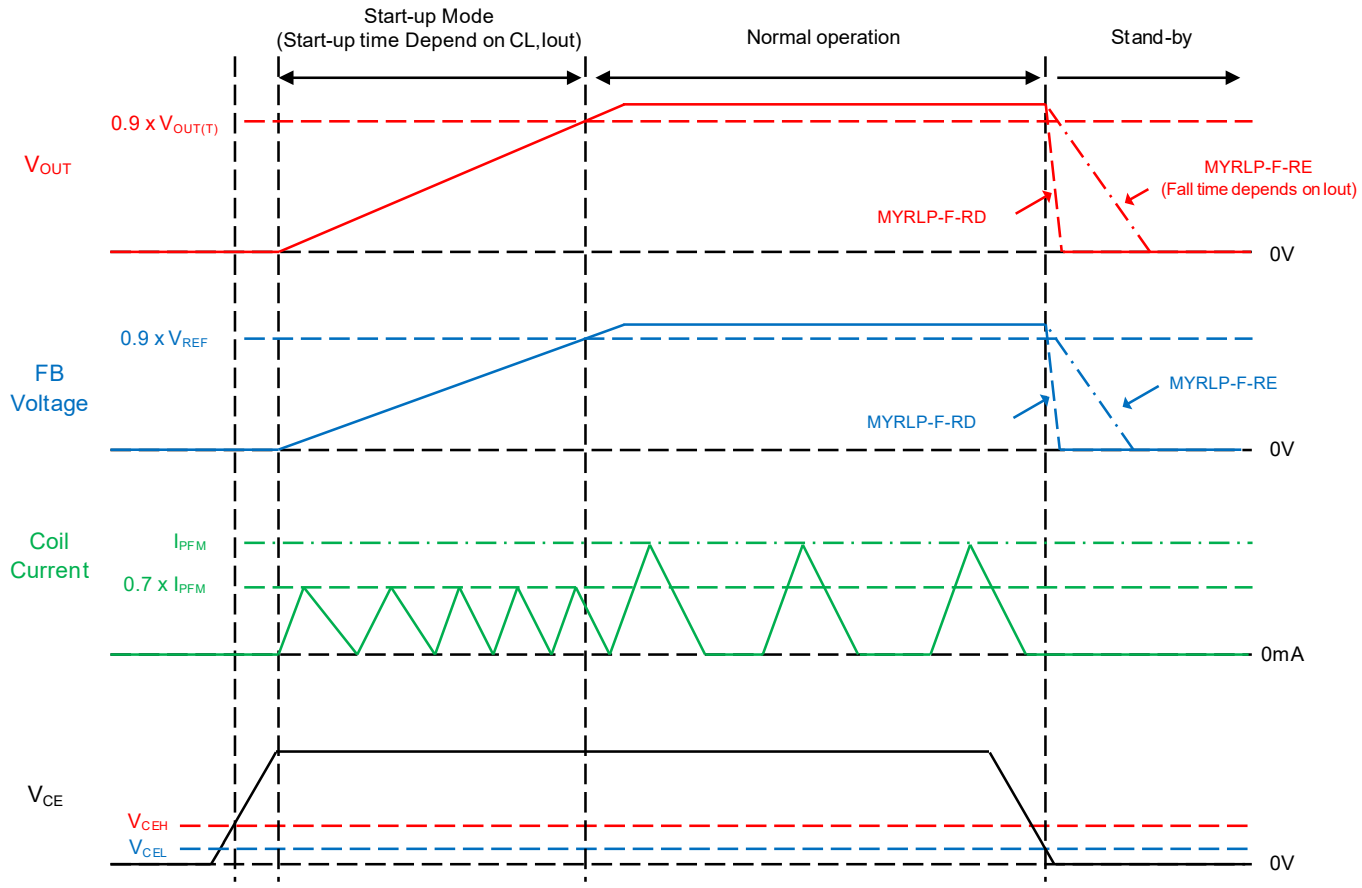
<Start-up Mode>

After “H” voltage ($V_{CEH}$) is fed to CE pin and UVLO function is released, by the time when FB voltage goes up to 0.9 x $V_{REF}$, the startup mode operates.

Unlike the normal operation, the start-up mode stops the operation of the short-circuit protection function and prevents the IC from being inadvertently stopped.

In order to suppress the inrush current, the peak current of the coil is limited to 0.7 x $I_{PFM}$, and the Nch driver FET does not turn on and the coil current flows through the parasitic diode of the Nch driver FET.

The rise time of the output voltage depends on the output capacitance and output current.




<UVLO function>

When the $V_{IN}$ voltage becomes UVLO Detect Voltage ($V_{UVLOD}$) or less, the UVLO function operates to forcibly turn off the Pch MOS driver FET to prevent erroneous pulse output due to operation instability of the internal circuit.

During the UVLO function, the Pch driver FET and Nch driver FET turn off, and the Nch FET M1 between the $V_{OUT}$ pin and GND pin turns on to discharge the output capacitance and make the output voltage be lower.

When the $V_{IN}$ voltage becomes UVLO Release Voltage ($V_{UVLOR}$) or more, the UVLO function is canceled. After the UVLO function is canceled, the output voltage rises with the startup mode, and then the normal operation is performed.

Moreover, during the UVLO operation, the current consumption increases because the internal circuit is operating and the switching operation is stopped, not the stand-by state.

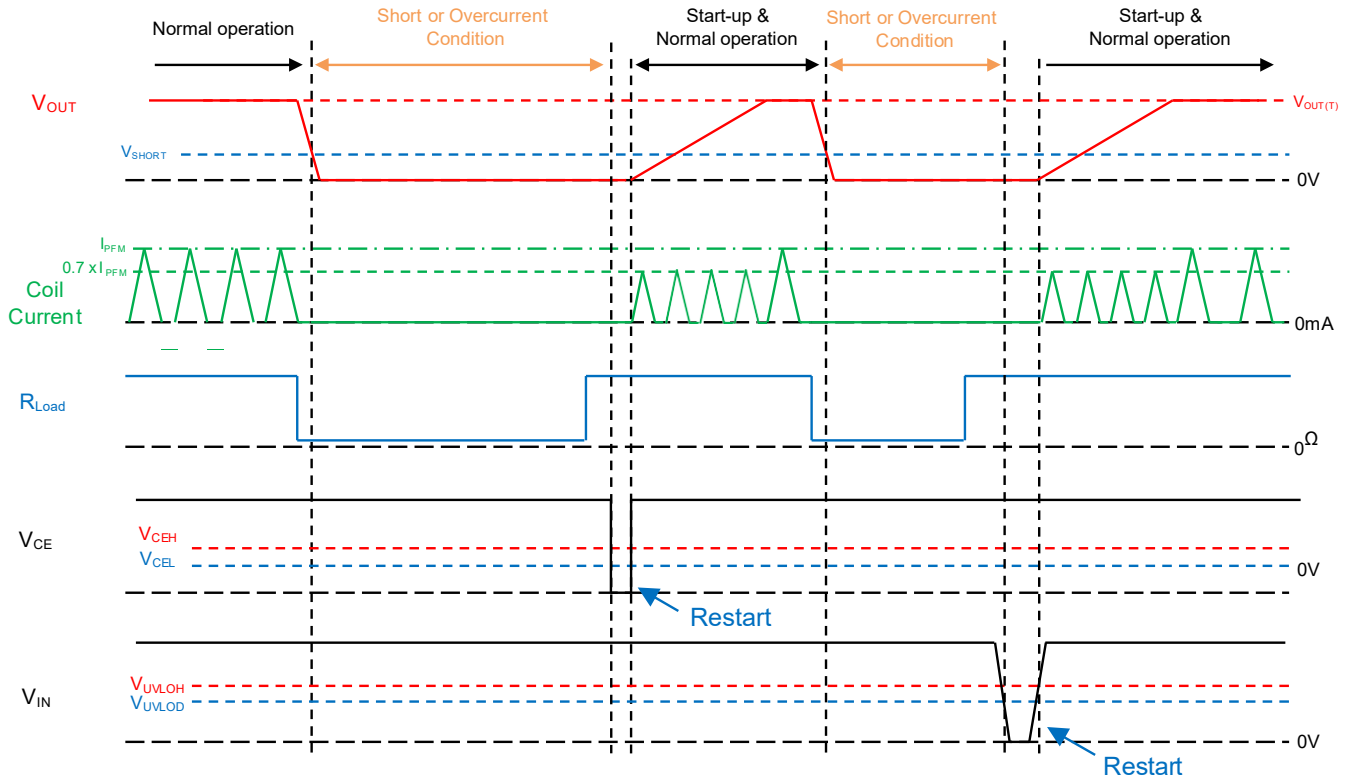
# ■ OPERATIONAL EXPLANATION (Continued)

・Case (a) : $V_{OUT}$ ≧1.2V

The short-circuit protection function monitors the $V_{OUT}$ pin voltage, and if the $V_{OUT}$ pin voltage drops below the Short Protection Threshold Voltage ($V_{SHORT}$) due to a short circuit or overcurrent, the short circuit protection function operates.

When the short-circuit protection function is activated, the Pch driver FET and Nch driver FET are held off. If the $V_{OUT}$ pin voltage exceeds the Short Protection Threshold Voltage ($V_{SHORT}$) after the short-circuit protection function is activated, normal operation resumes.

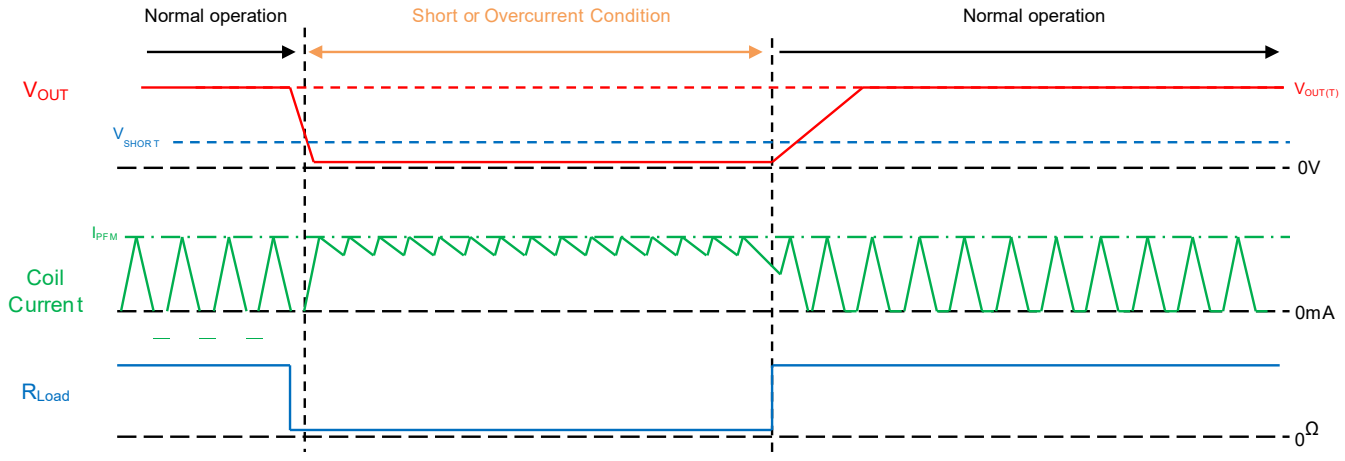
To cancel the short-circuit protection function, it is necessary to start the IC after putting the IC in the standby state with the CE function, or to raise the input voltage after setting the input voltage below the UVLO detection voltage ($V_{UVLOD}$).




・Case (b) : $V_{OUT}$ < 1.2V

The short-circuit protection function is not implemented in the part numbers where $V_{OUT}$ is less than 1.2V. If a short circuit or overcurrent occurs, the output voltage will drop and switching operation will continue.

When the short-circuit state or excessive output current is released, the output voltage rises quickly to the set output voltage.



# ■OPERATIONAL EXPLANATION (Continued)

< $C_L$ Discharge function (MYRLP-F-RD)>

On the MYRLP-F-RD/RE series, a $C_L$ discharge function is available as an option.

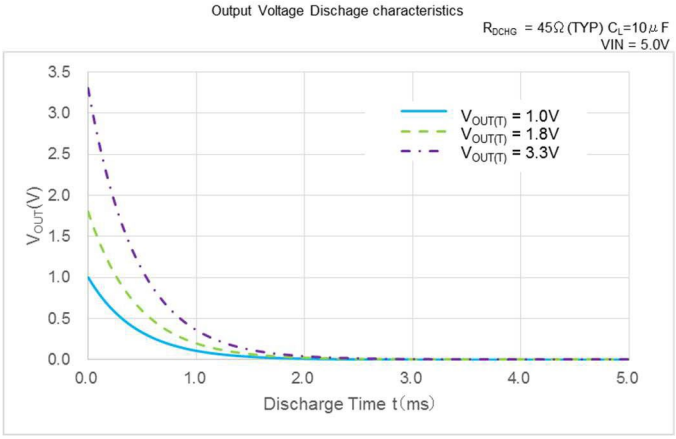
$C_L$ discharge function turns on the Nch FET M1 between the $V_{OUT}$ pin and GND pin when the stand-by condition in order to discharge the output capacitance quickly and make the output voltage be lower.

This prevents malfunctioning of the application in the event that a charge remains on $C_L$ when the IC is stand-by state.

The discharge time is determined by $C_L$ and the $C_L$ discharge resistance $R_{DCHG}$, including the Nch FET M1.
the discharge time of the output voltage is calculated by means of the equation below.

$$V = V_{OUT(T)} \times e^{-t/\tau}$$
$$t = \tau \ln(V_{OUT(T)} / V)$$

| | |
|---|---|
| V | : Output voltage during discharge |
| $V_{OUT(T)}$ | : Output voltage |
| t | : Discharge time |
| $C_L$ | : Effective capacitance of Output capacitor |
| $R_{DCHG}$ | : $C_L$ auto-discharge resistance |
| τ | : $C_L \times R_{DCHG}$ |



## ■ NOTE ON USE

1. Be careful not to exceed the absolute maximum ratings for externally connected components and this IC.

2. The DC/DC converter characteristics greatly depend not only on the characteristics of this IC but also on those of externally connected components, so refer to EXTERNAL COMPONENTS SELECTION and the specifications of each component and be careful when selecting the components. Be especially careful of the characteristics of the capacitor used for the load capacity $C_L$ and use a capacitor with B characteristics (JIS Standard) or an X7R/X5R (EIA Standard) ceramic capacitor.

3. The CE pin and VSET pin does not have an internal pull-up or pull-down, etc. Apply the prescribed voltage to the CE pin and VSET pin.
   If an intermediate voltage is fed to the CE and VSET pins, a through current will flow through the input stage of the CE and VSET pins, increasing current consumption.

4. At light loads or when IC operation is stopped, leakage current from the Pch driver FET may cause the output voltage to rise.

5. Switching operation may be performed continuously due to internal delay or input offset of the PFM comparator circuit.
   If the switching operation continues, the output ripple voltage increases and the output voltage rises as the ripple voltage increases.

6. When the input / output potential difference is small, the ripple voltage increases and the output voltage may increase.

7. Since the short-circuit protection function is not implemented in the part number where both of or either VOUT is less than 1.2V, the coil current may be superposed under the condition of high input voltage and excessive output current.

8. During start-up mode, the peak current of the coil is set lower than in normal operation, so the output voltage may not rise under conditions where the output current is large during start-up.

9. To suppress current consumption, UVLO detection is performed only for a certain period after the Pch driver FET is turned on. For this reason, the UVLO function may not operate if the VIN pin voltage instantaneously drops below the UVLO detection voltage ($V_{UVLOD}$).

10. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

11. Murata places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Murata products in their systems.

## ■NOTE ON USE (Continued)

12. Instructions of pattern layouts

(1)In order to stabilize $V_{IN}$ voltage level, we recommend that a by-pass capacitor ($C_{IN}$) be connected as close as possible to the $V_{IN}$ & GND pins.

(2) Please mount each external component as close to the IC as possible.

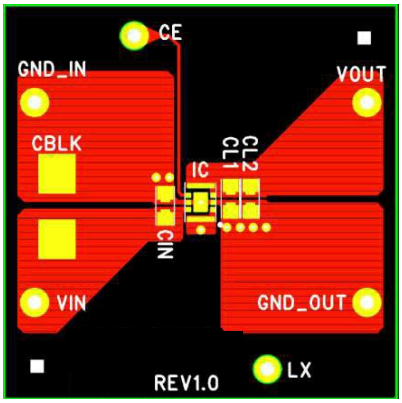
(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

(4) Make sure that the PCB GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

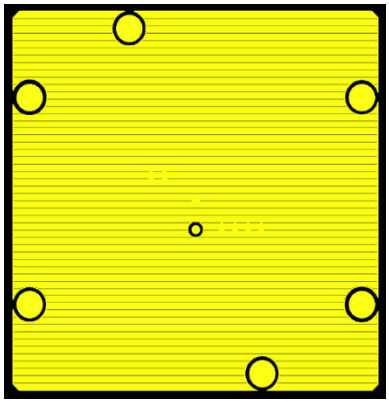
(5) This series' internal driver FET bring on heat because of the output current and ON resistance of Pch driver FET.

< Reference pattern layout >

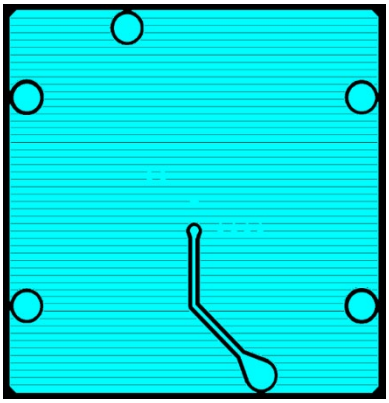
Layer 1



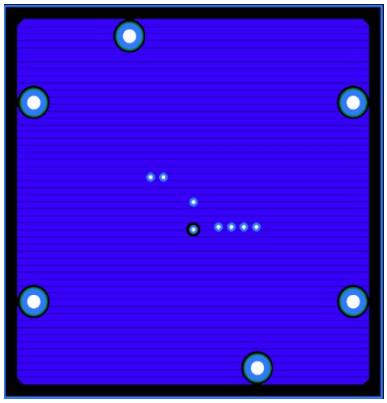

Layer 2



Layer 3



Layer 4



## ■ Notes on handling of product

(1) The coil mounted on this product complies with the general surface mount type chip inductor specifications, and may have scratches, flux stains, etc.

(2) Do not use this product in the following environments. Places exposed to water or salt water, places where condensation occurs, places where toxic gases (hydrogen sulfide, zinc acid, chlorine, ammonia, etc.) are present.

(3) Please do not wash this product with solvent.

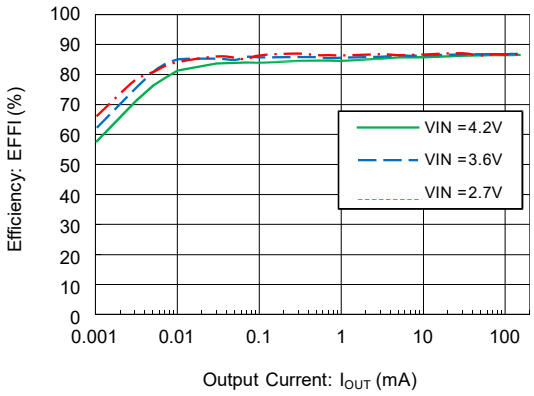
## ■ Notes on mounting

(1) Please set the mounting position accuracy within 0.05 mm.

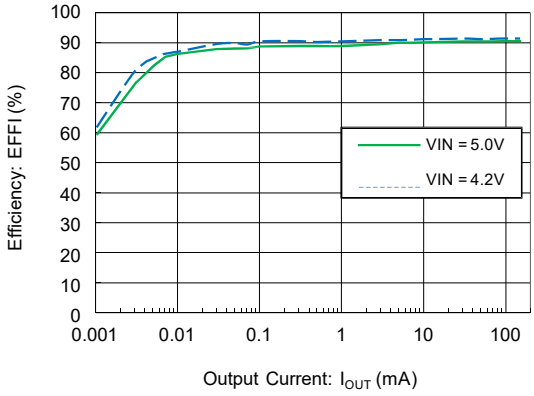
# ■ TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output Current

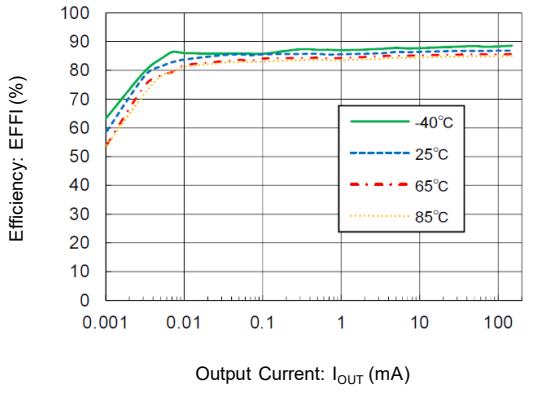
MYRLP-F-RD/RE (VOUT=1.8V)



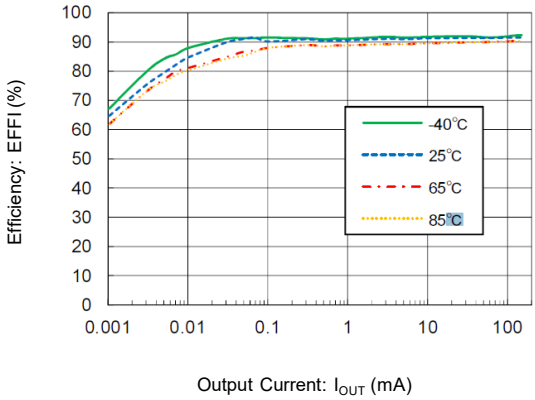

MYRLP-F-RD/RE (VOUT=3.0V)



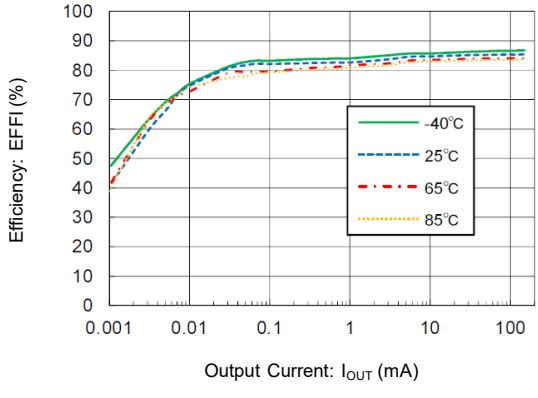

MYRLP-F-RD/RE (VOUT=1.8V)



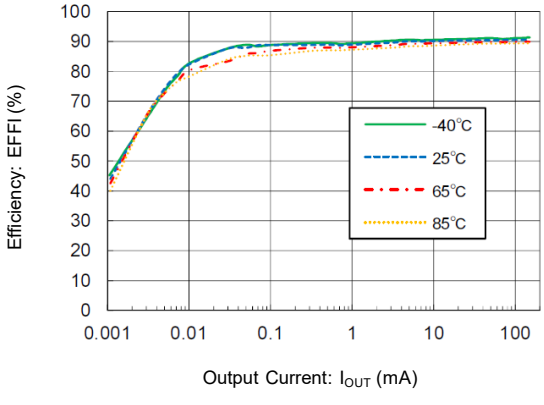

MYRLP-F-RD/RE (VOUT=3.0V)




MYRLP-F-RD/RE (VOUT=1.8V)



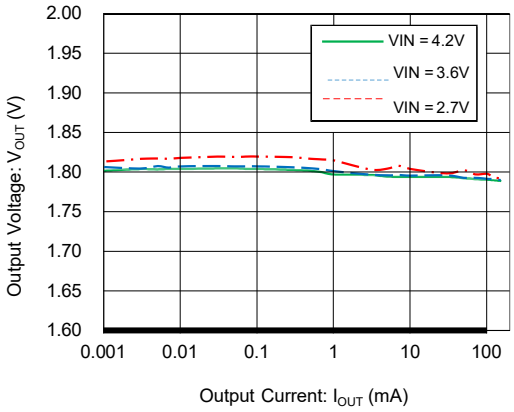

MYRLP-F-RD/RE (VOUT=3.0V)



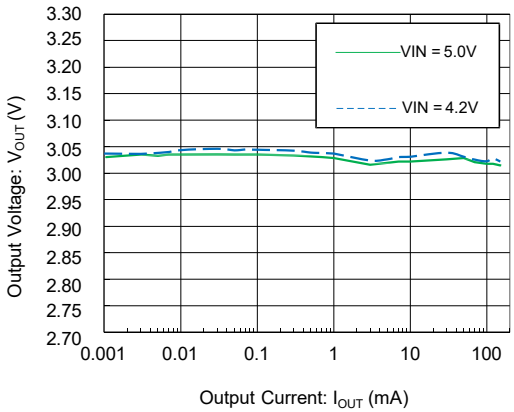
# ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(2) Output Voltage vs. Output Current

MYRLP-F-RD/RE (VOUT=1.8V)

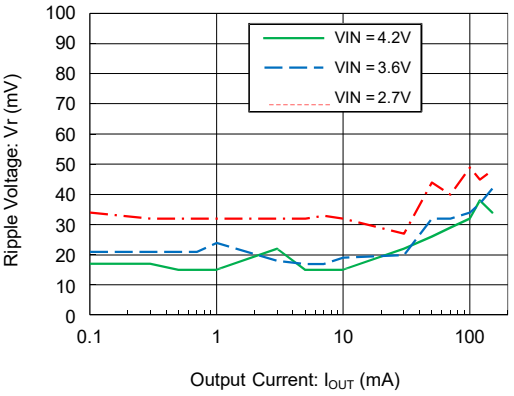



MYRLP-F-RD/RE (VOUT=3.0V)

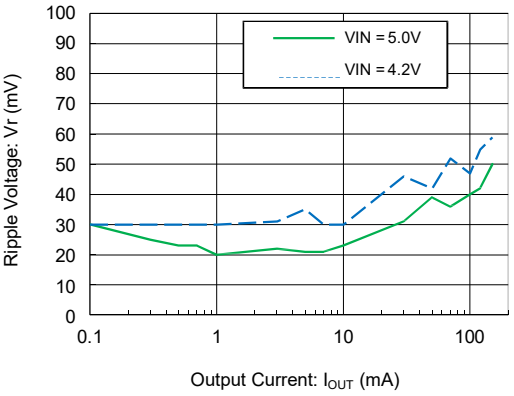



(3) Ripple Voltage vs. Output Current

MYRLP-F-RD/RE (VOUT=1.8V)

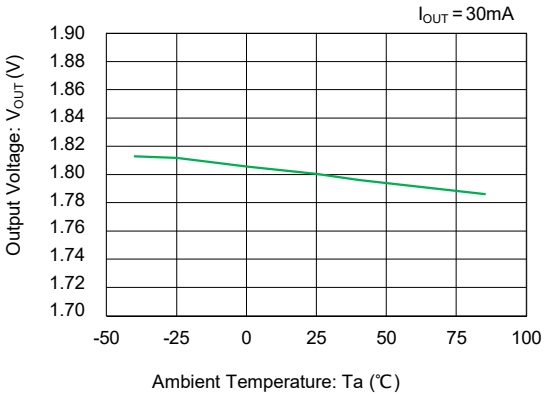



MYRLP-F-RD/RE ($V_{OUT}$=3.0V)



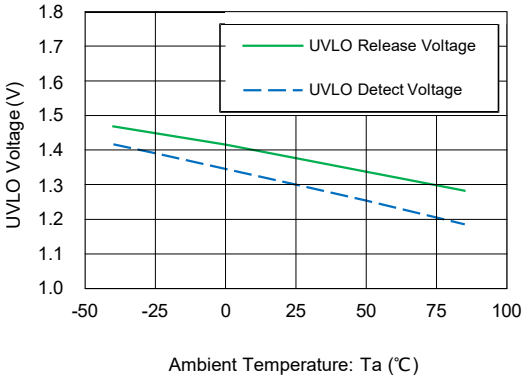

(4) Output Voltage vs. Ambient Temperature

MYRLP-F-RD/RE (VOUT=1.8V)



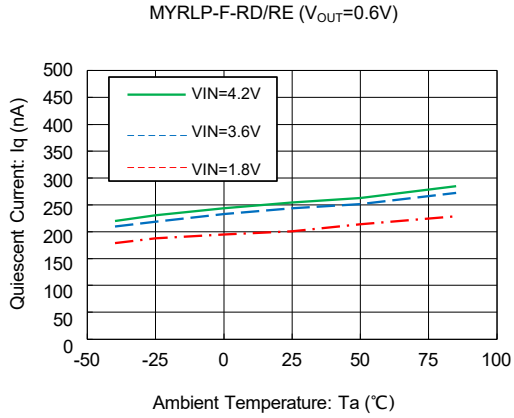

(5) UVLO Voltage vs. Ambient Temperature

MYRLP-F-RD/RE

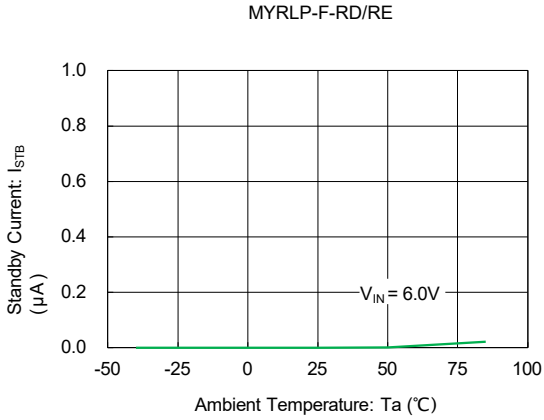


## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

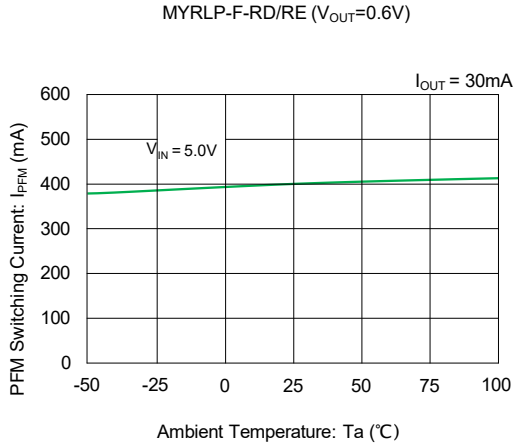
(6) Quiescent Current vs. Ambient Temperature



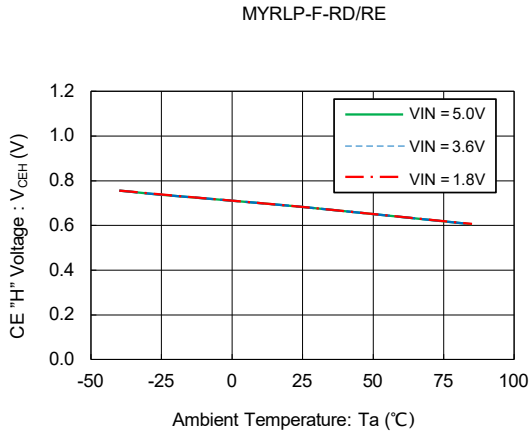

(7) Stand-by Current vs. Ambient Temperature



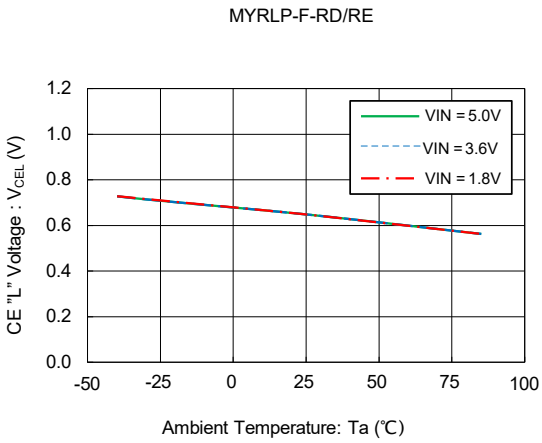

(8) PFM Switching Current vs. Ambient Temperature



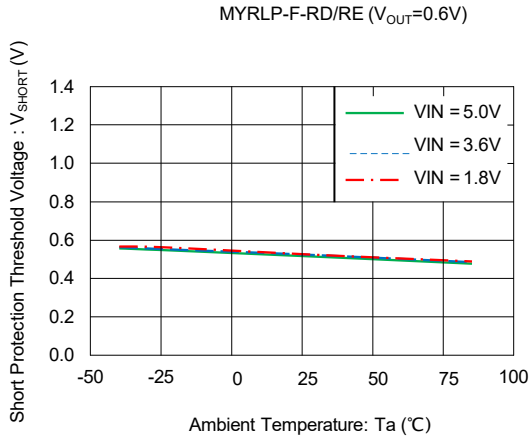

(9) CE ”H” Voltage vs. Ambient Temperature




(10) CE ”L” Voltage vs. Ambient Temperature



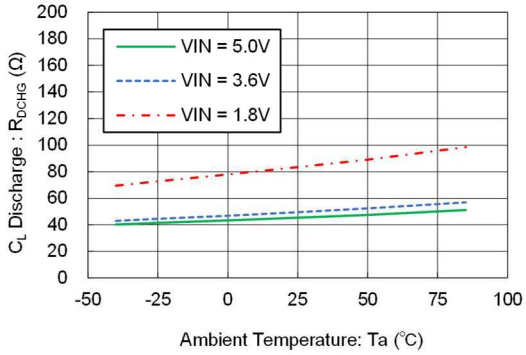

(11) Short Protection Threshold vs. Ambient Temperature



# ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(12) CL Discharge Resistance vs. Ambient Temperature

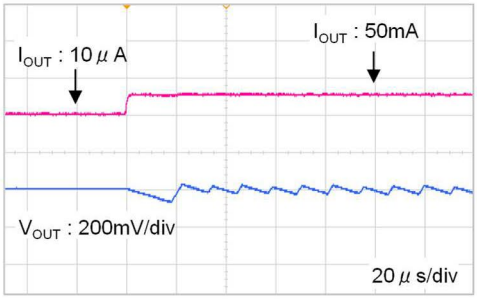
MYRLP-F-RD/RE




(13) Load Transient Respones

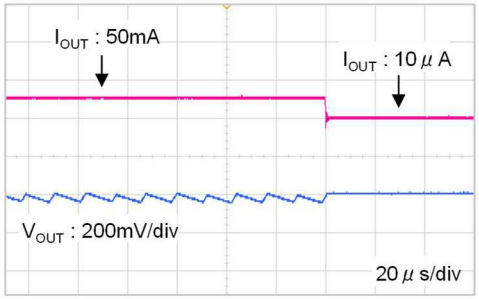
MYRLP-F-RD

$V_{IN}$ = 3.6V $V_{OUT}$ = 1.8V $I_{OUT}$ = 10 μA ⇒ 50mA tr = 5 μs



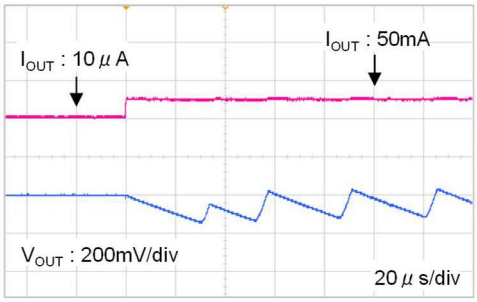

MYRLP-F-RD

$V_{IN}$ = 3.6V $V_{OUT}$ = 1.8V $I_{OUT}$ = 50mA ⇒ 10 μA tf = 5 μs



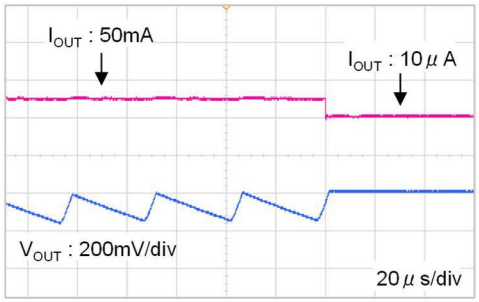

MYRLP-F-RD

$V_{IN}$ = 3.6V $V_{OUT}$ = 3.0V $I_{OUT}$ = 10 μA ⇒ 50mA tr = 5 μs




MYRLP-F-RD

$V_{IN}$ = 3.6V $V_{OUT}$ = 3.0V $I_{OUT}$ = 50mA ⇒ 10 μA tf = 5 μs

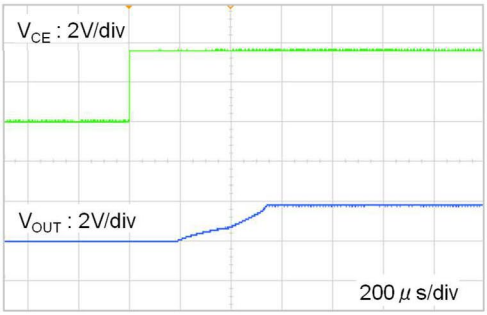


# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(14) Startup Mode

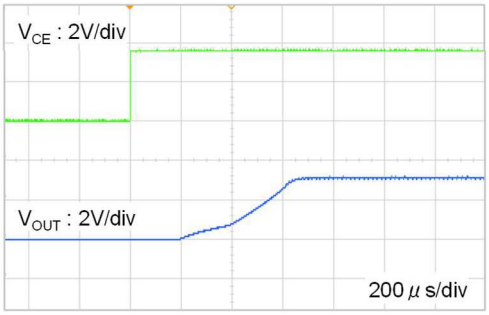
MYRLP-F-RD

$V_{IN}$ = 3.6V , $V_{OUT}$=1.8V , $V_{CE}$ = 0.0V ⇒ 3.6V , $I_{OUT}$ = 50mA
tr = 5 μ s



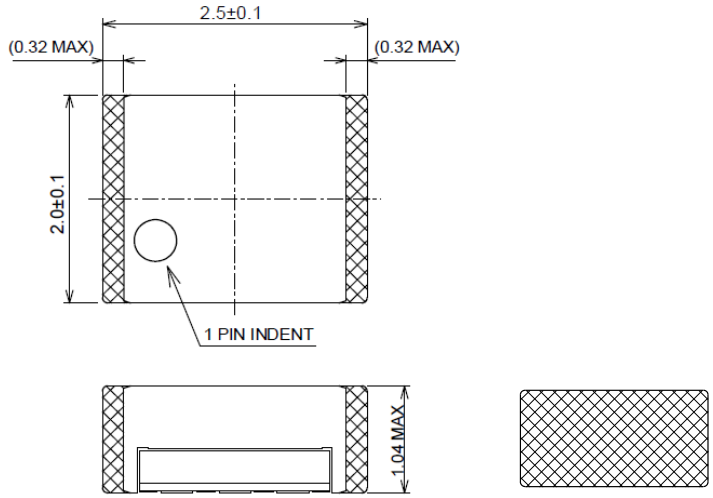

MYRLP-F-RD

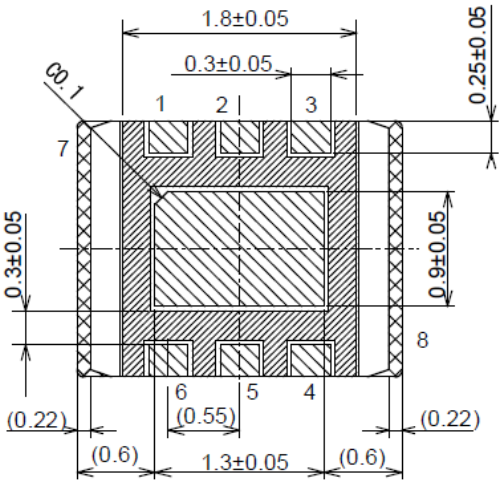
$V_{IN}$ = 3.6V , $V_{OUT}$=3.0V , $V_{CE}$ = 0.0V ⇒ 3.6V , $I_{OUT}$ = 50mA
tr = 5 μ s



# ■ PACKAGING INFORMATION

●Packaging (2.0mm × 2.5mm, h=1.0mm)

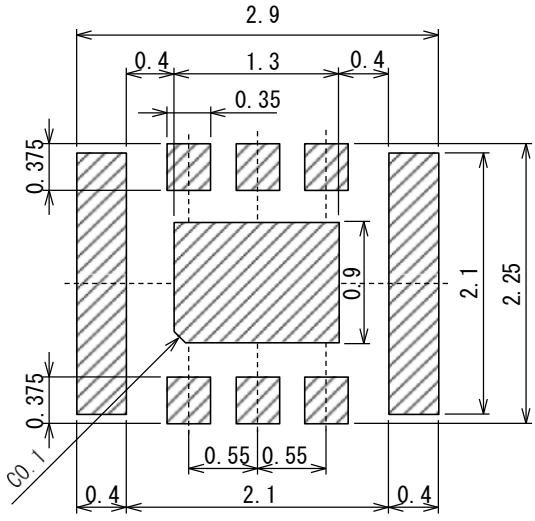


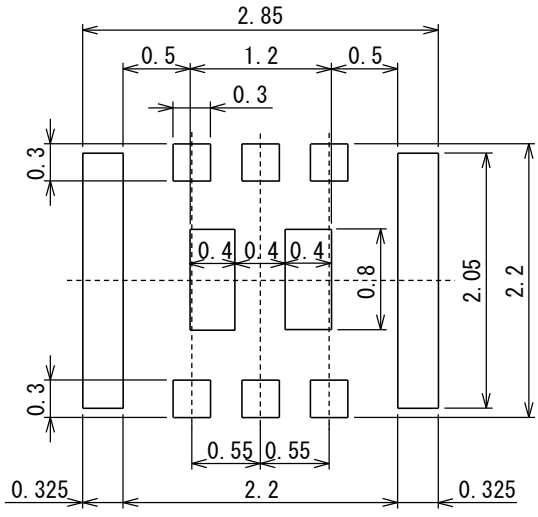

(unit: mm)

Terminal material : Copper foil
Terminal plating : 1～6 Gold plating
7～8 Lead(Pb) free Solder plating

●Reference Pattern Layout (unit:mm)




●Reference Metal Mask Design (unit:mm)




*Please use the above mount pad dimensions and metal mask design as reference data.

# ■ PACKAGING INFORMATION

Power Dissipation

Power dissipation data for the package is shown in this page.
The value of power dissipation varies with the mount board conditions.
Please use this data as one of reference data taken in the described condition.

1. Measurement Condition (Reference data)

Condition: Mount on a board

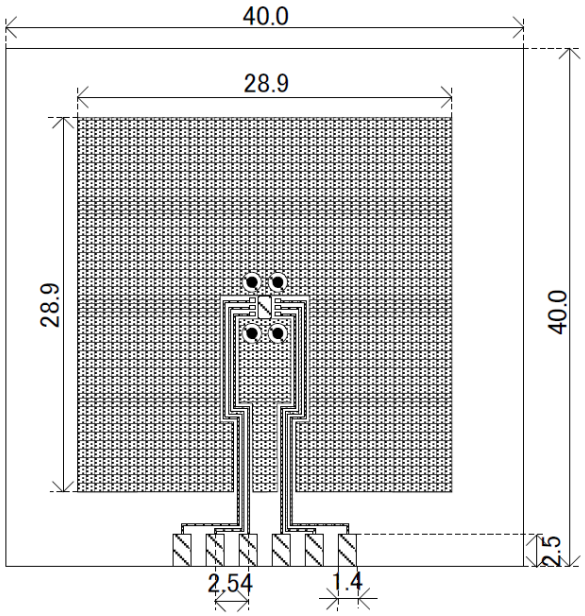
Ambient: Natural convection

Soldering: Lead (Pb) free

Board Dimensions: 40 x 40 mm (1600mm² in one side)
Copper (Cu) traces occupy 50% of the board area
In top and back faces Package heat-sink is tied to the copper traces

Material: Glass Epoxy (FR-4)
Thickness: 1.6 mm
Through-hole: 4 x 0.8 Diameter

Copper foil thickness: Front 35um, Back 35um

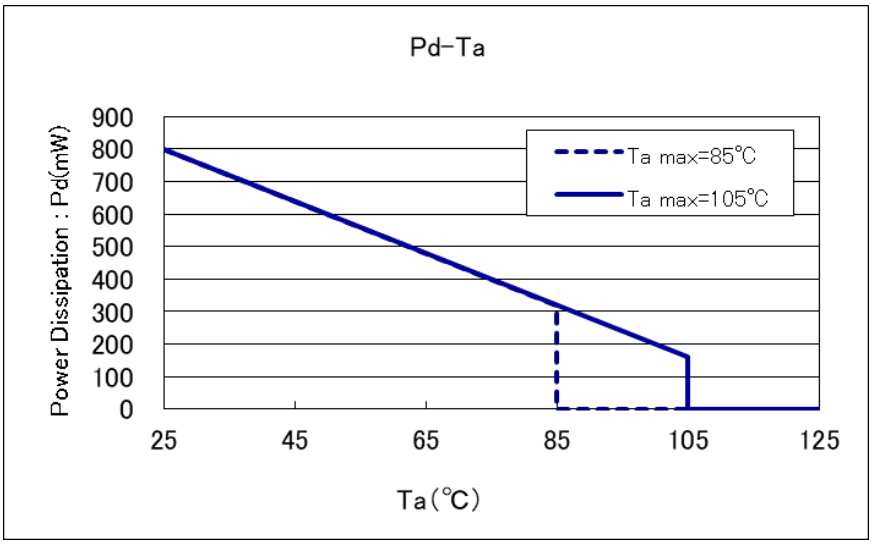


Evaluation Board (Unit:mm)

2. Power Dissipation vs. Ambient Temperature

Board Mount ( Tjmax=125℃)

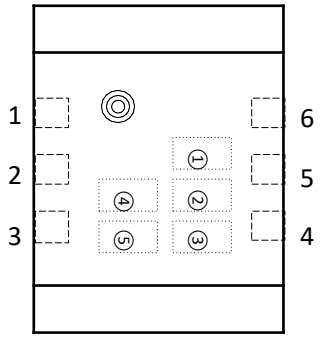
| Ambient Temperature (℃) | Power Dissipation Pd (mW) | | Thermal Resistance (℃/W) |
|---|---|---|---|
| | Ta max=85℃ | Ta max=105℃ | |
| 25 | 800 | 800 | 125.00 |
| 85 | 320 | 320 | |
| 105 | 0 | 160 | |
| 125 | 0 | 0 | |



## ■ MARKING RULE

Mark①represents product series.

| MARK | PRODUCT SERIES |
|---|---|
| A | MYRLP***015F21RD / MYRLP***015F21RE |




Mark②,③ represents the registered setting, output voltage.

| MARK | Type | OUTPUT VOLTAGE(V) | PRODUCT SERIES |
|---|---|---|---|
| 15 | E | 0.50～3.60V | MYRLP***015F21RE |
| | D | 0.50～3.60V | MYRLP***015F21RD |

Mark ④⑤ ,represents production lot number

01～09、0A～0Z、11～9Z、A1～A9、AA～ZZ、B1～ZZ in order.

(G, I, J, O, Q, W excluded) * No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9. 

Murata Manufacturing Co., Ltd