

# 74LVT16244B; 74LVTH16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 13 — 12 August 2021

Product data sheet

## 1. General description

The 74LVT16244B; 74LVTH16244B is a 16-bit buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1OE, 2OE, 3OE and 4OE), each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

## 2. Features and benefits

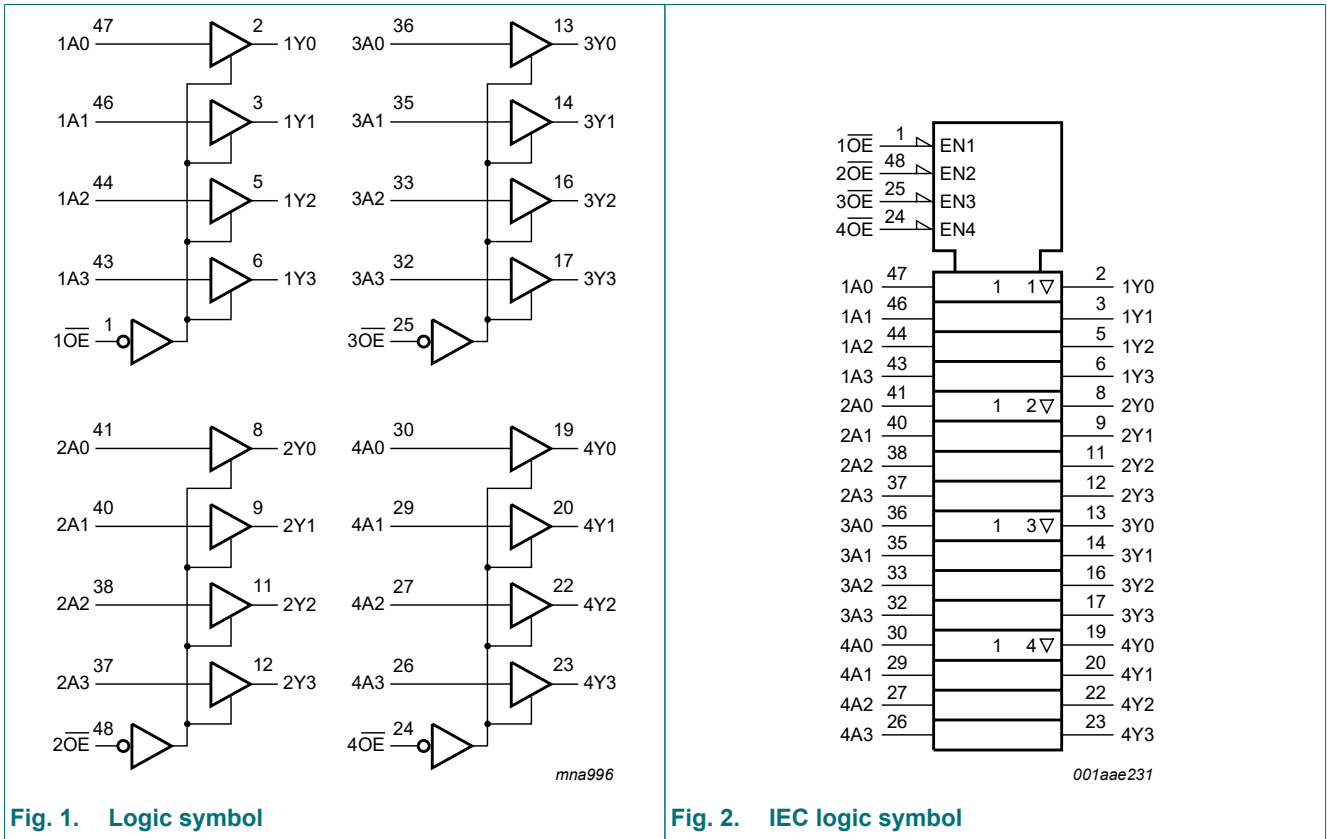
- 16-bit bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JEDEC standard JESD8C (2.7 V to 3.6 V)
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVT16244BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVTH16244BDGG				

4. Functional diagram



## 5. Pinning information

### 5.1. Pinning

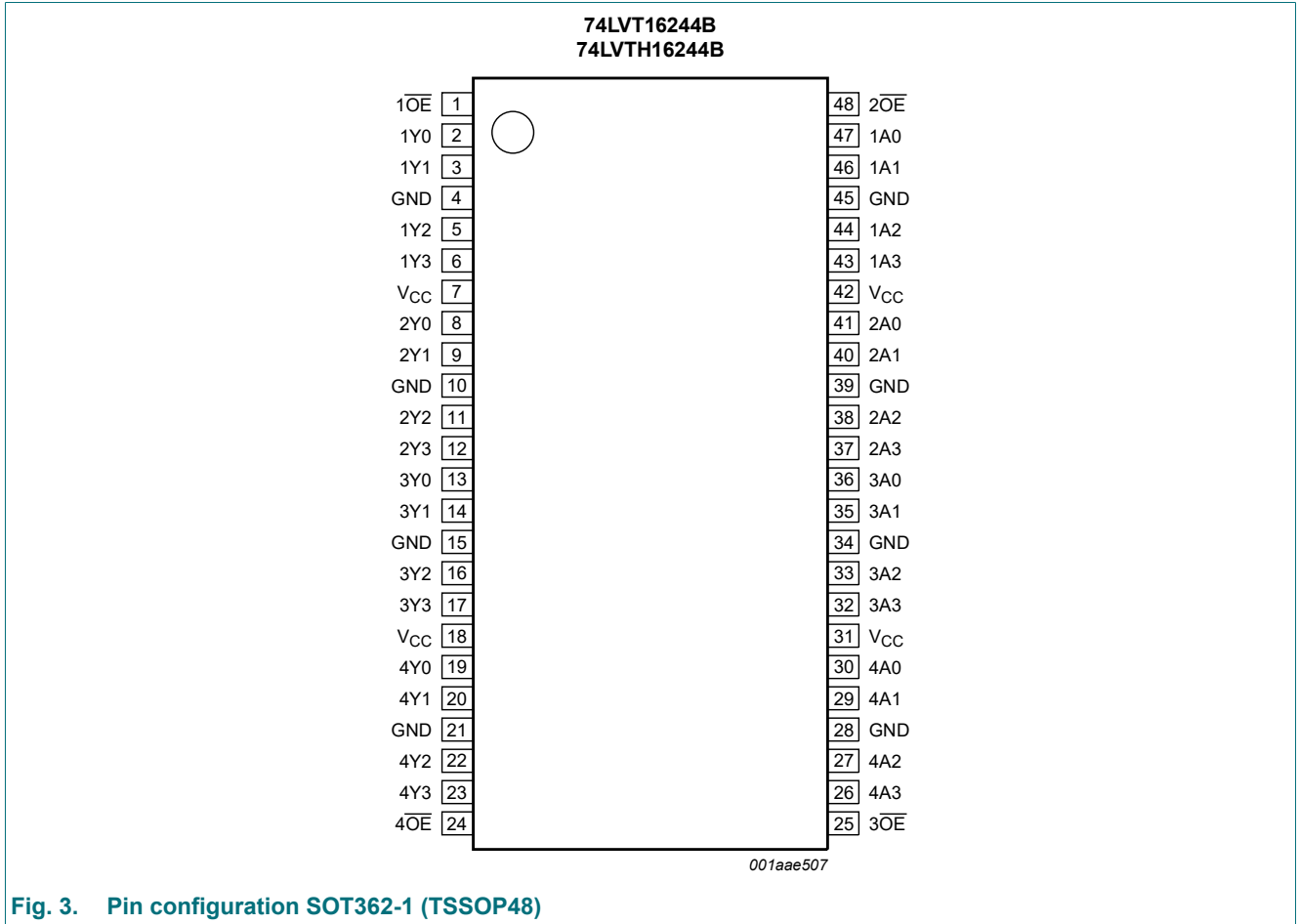


Fig. 3. Pin configuration SOT362-1 (TSSOP48)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	output enable input (active LOW)
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data output
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data output
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data output
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data input
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data input

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[2] -	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C;	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-32	-	-	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz	-	-	64	mA
T <sub>amb</sub>	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-1.2	-0.85	-	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -100\text{ }\mu\text{A}$ ; $V_{CC} = 2.7\text{ V to }3.6\text{ V}$	$V_{CC} - 0.2$	$V_{CC}$	-	V
		$I_{OH} = -8\text{ mA}$ ; $V_{CC} = 2.7\text{ V}$	2.4	2.5	-	V
		$I_{OH} = -32\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$	2.0	2.3	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$				
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V
		$I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$				
		$I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
$I_I$	input leakage current	all input pins; $V_{CC} = 0\text{ V or }3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
		control pins; $V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1.0$	$\mu\text{A}$
		data pins; $V_{CC} = 3.6\text{ V}$ [2]				
		$V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$
	$V_I = 0\text{ V}$	-5	-0.1	-	$\mu\text{A}$	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V to }4.5\text{ V}$	-	0.1	$\pm 100$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 3\text{ V}$ ; $V_I = 0.8\text{ V}$ [3]	75	135	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 3\text{ V}$ ; $V_I = 2.0\text{ V}$	-	-135	-75	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V to }3.6\text{ V}$	500	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	nAn input; $V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V to }3.6\text{ V}$	-	-	-500	$\mu\text{A}$
$I_{LO}$	output leakage current	output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.0\text{ V}$	-	50	125	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/ power-down output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V to }V_{CC}$ ; $V_I = \text{GND or }V_{CC}$ ; nOE = don't care [4]	-	1	$\pm 100$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{IH}$ or $V_{IL}$				
		output HIGH: $V_O = 3.0\text{ V}$	-	0.5	5	$\mu\text{A}$
		output LOW: $V_O = 0.5\text{ V}$	-5	+0.5	-	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6\text{ V}$ ; $V_I = \text{GND or }V_{CC}$ ; $I_O = 0\text{ A}$				
		output HIGH	-	0.07	0.12	mA
		output LOW	-	4.0	6.0	mA
		outputs disabled [5]	-	0.07	0.12	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND [6]	-	0.1	0.2	mA

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	3	-	pF
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or 3.0 V	-	9	-	pF

- [1] Typical values are measured at V<sub>CC</sub> = 3.3 V and at T<sub>amb</sub> = 25 °C.  
 [2] Unused pins at V<sub>CC</sub> or GND.  
 [3] This is the bus hold overdrive current required to force the input to the opposite logic state.  
 [4] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T<sub>amb</sub> = 25 °C only.  
 [5] I<sub>CC</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.  
 [6] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); T<sub>amb</sub> = -40 °C to +85 °C; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn; see Fig. 4				
		V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.7	3.2	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{O}E$ to nYn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{O}E$ to nYn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Fig. 5				
		V <sub>CC</sub> = 2.7 V	-	-	4.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

- [1] Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

10.1. Waveforms and test circuit

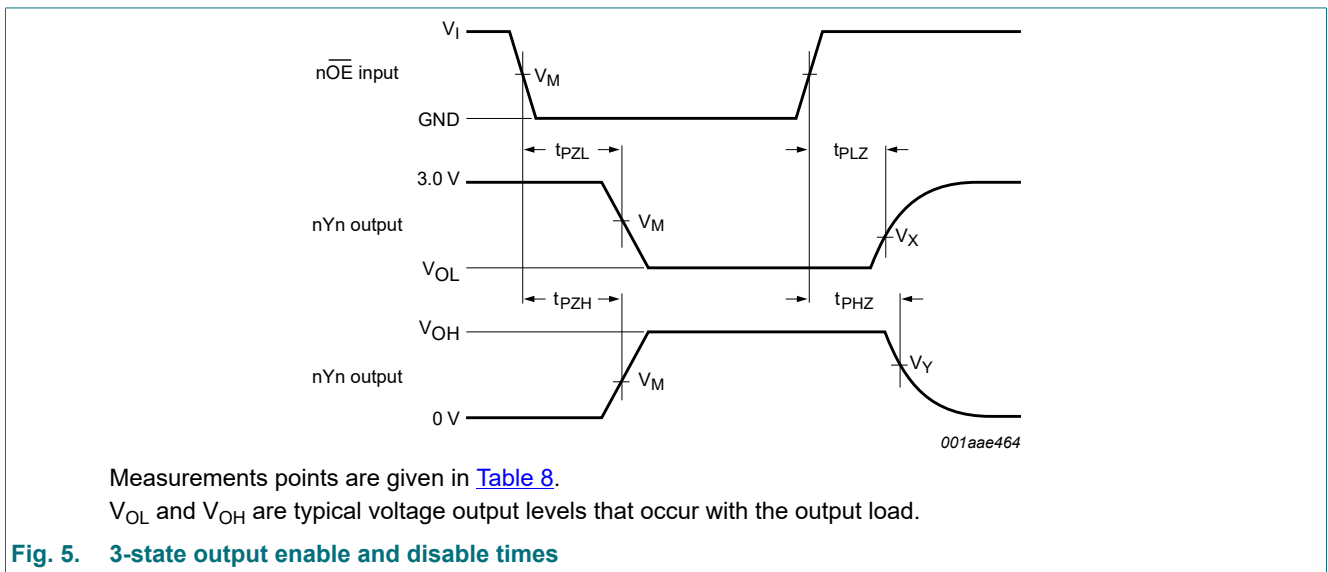
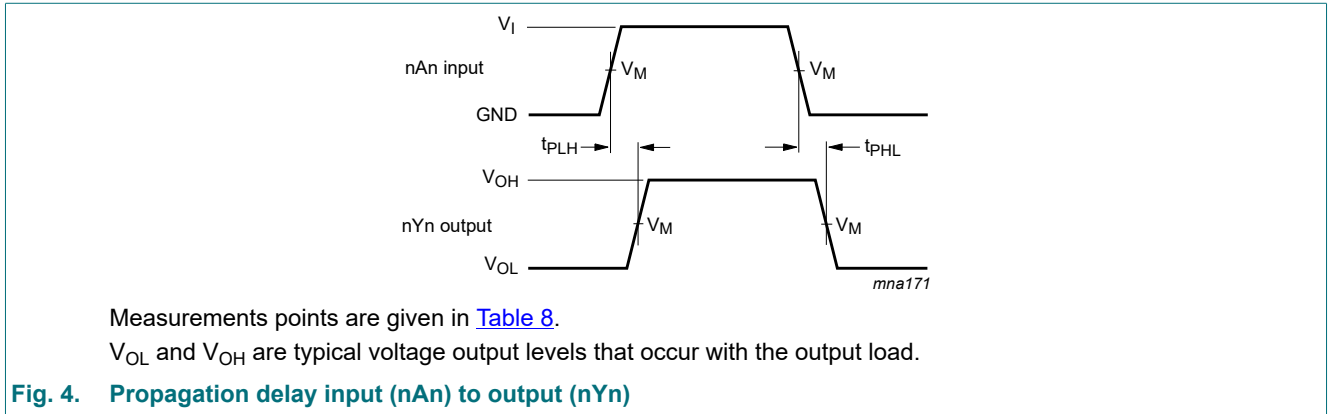
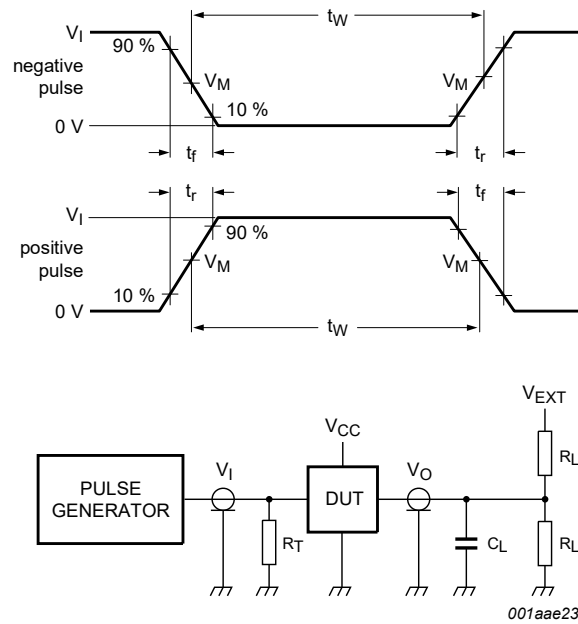


Table 8. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open



11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

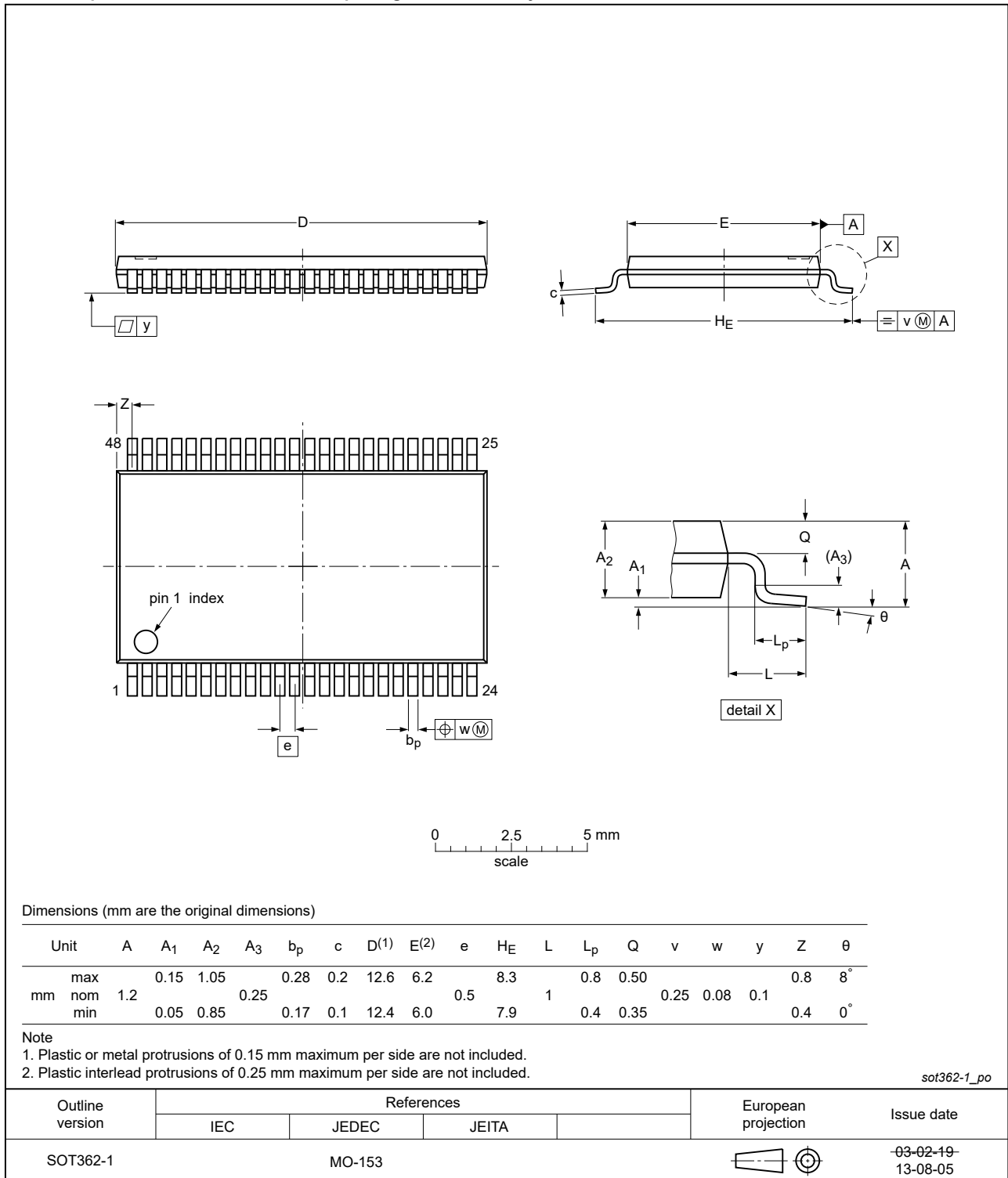


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16244B v.13	20210812	Product data sheet	-	74LVT_LVTH16244B v.12
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• Type numbers 74LVT16244BDL and 74LVTH16244BDL (SOT370-1/SSOP48) removed.</li> <li>• <a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation removed.</li> </ul>			
74LVT_LVTH16244B v.12	20181019	Product data sheet	-	74LVT_LVTH16244B v.11
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type numbers 74LVT16244BEV (SOT702-1), 74LVT16244BBX (SOT1134-2) and 74LVTH16244BBX (SOT1134-2) removed.</li> <li>• Package outline drawing <a href="#">SOT362-1</a> updated</li> </ul>			
74LVT_LVTH16244B v.11	20120301	Product data sheet	-	74LVT_LVTH16244B v.10
Modifications:	<ul style="list-style-type: none"> <li>• For type number 74LVT16244BBX and 74LVTH16244BBX the sot code has changed to SOT1134-2.</li> </ul>			
74LVT_LVTH16244B v.10	20111122	Product data sheet	-	74LVT_LVTH16244B v.9
Modifications:	<ul style="list-style-type: none"> <li>• Legal pages updated.</li> </ul>			
74LVT_LVTH16244B v.9	20110620	Product data sheet	-	74LVT_LVTH16244B v.8
74LVT_LVTH16244B v.8	20100322	Product data sheet	-	74LVT_LVTH16244B v.7
74LVT_LVTH16244B v.7	20090326	Product data sheet	-	74LVT_LVTH16244B v.6
74LVT_LVTH16244B v.6	20081113	Product data sheet	-	74LVT_LVTH16244B v.5
74LVT_LVTH16244B v.5	20060321	Product data sheet	-	74LVT16244B v.4
74LVT16244B v.4	20021031	Product specification	-	74LVT16244B v.3
74LVT16244B v.3	19981007	Product specification	-	74LVT16244B v.2
74LVT16244B v.2	19980219	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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