



60V +175°C N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI5060-8

Product Summary

BV _{DSS}	Rds(on) max	I _{D MAX} T _C = +25°C
60V	$14m\Omega @ V_{GS} = 10V$	50.5A
	$21m\Omega$ @ $V_{GS} = 4.5V$	41.2A

Features

- Rated to +175°C Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching (UIS) Test in Production— Ensures More Reliable and Robust End Application
- Low R_{DS(ON)} Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspection
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

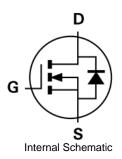
- Engine Management Systems
- Body Control Electronics
- DC-DC Converters

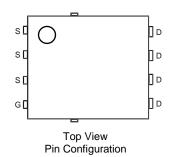
PowerDI5060-8 (SWP) (Type Q)



Mechanical Data

- Case: PowerDI[®] 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish Matte Tin Annealed over Copper Leadframe;
 Solderable per MIL-STD-202, Method 208 [®]
- Weight: 0.097 grams (Approximate)





Ordering Information (Note 4)

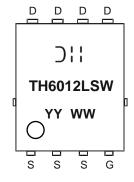
Part Number	Case	Packaging	
DMTH6012LPSW-13	PowerDI5060-8 (SWP) (Type Q)	2,500 / Tape & Reel	

Notes:

- 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Bottom View

Marking Information



DII = Manufacturer's Marking
TH6012LSW = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 19 = 2019)
WW = Week Code (01 to 53)

July 2019

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Maximum Ratings ($@T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage		V_{DSS}	60	V	
Gate-Source Voltage		V_{GSS}	±20	V	
Continuous Prain Current V 40V (Note 5)	$T_A = +25^{\circ}C$	I _D	11.5	- A	
Continuous Drain Current, V _{GS} = 10V (Note 5)	T _A = +100°C		8.1		
Continuous Pusis Coment V 40V (Note C)	T _C = +25°C	ID	50.5	Α	
Continuous Drain Current, V _{GS} = 10V (Note 6)	T _C = +100°C		35.7		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	200	Α		
Maximum Continuous Body Diode Forward Current (Note 6)	I _S	50	Α		
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle	I _{SM}	200	Α		
Avalanche Current, L=0.1mH		I _{AS}	12.6	Α	
Avalanche Energy, L=0.1mH		E _{AS}	7.9	mJ	

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	P_{D}	2.8	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{ heta JA}$	54	°C/W
Total Power Dissipation (Note 6)	T _C = +25°C	P_{D}	53.6	W
Thermal Resistance, Junction to Case (Note 6)		$R_{ heta JC}$	2.8	°C/W
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)					•		
Drain-Source Breakdown Voltage	BV _{DSS}	60	_	_	٧	$V_{GS} = 0V$, $I_D = 1mA$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 48V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)						•	
Gate Threshold Voltage	V _{GS(TH)}	1	_	2.3	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance		_	10.6	14	_	$V_{GS} = 10V, I_D = 20A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	14.8	21	mΩ	$V_{GS} = 4.5V, I_D = 10A$	
Diode Forward Voltage	V _{SD}	_	0.7	1.2	V	V _{GS} = 0V, I _S = 1A	
DYNAMIC CHARACTERISTICS (Note 8)		•	•	•		•	
Input Capacitance	C _{iss}	_	785	_		V _{DS} = 30V, V _{GS} = 0V, f = 1MHz	
Output Capacitance	Coss	_	281	_	pF		
Reverse Transfer Capacitance	C _{rss}	_	27	_			
Gate Resistance	R_g	_	1.5	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	7.3	_			
Total Gate Charge (V _{GS} = 10V)	Qg	_	13.6	_	nC	V _{DS} = 30V, I _D = 10A	
Gate-Source Charge	Qgs	_	2.2	_	nc		
Gate-Drain Charge	Q_{gd}	_	3.4	_			
Turn-On Delay Time	t _{D(ON)}	_	3.2	_		$V_{DD} = 30V, V_{GS} = 10V,$ $I_{D} = 10A, R_{q} = 6\Omega$	
Turn-On Rise Time	t _R	_	4.4	_	20		
Turn-Off Delay Time	t _{D(OFF)}	_	14.7	_	ns		
Turn-Off Fall Time	t _F	_	8.5	_		_	
Body Diode Reverse Recovery Time	t _{RR}	_	23.0	_	ns	1 400 41/44 4000///	
Body Diode Reverse Recovery Charge	Q _{RR}	_	14.1	_	nC	I _F = 10A, di/dt = 100A/μs	

Notes: 5. Device mounted on FR-4 substrate PCB, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

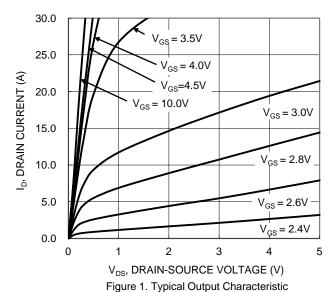
6. Thermal resistance from junction to soldering point (on the exposed drain pad). 7. Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to product testing.

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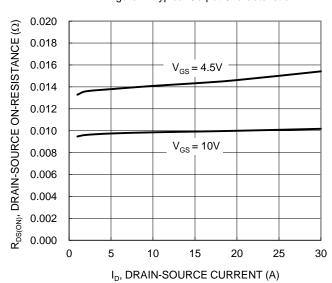


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

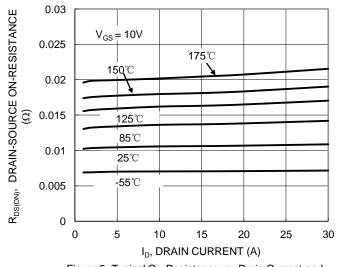


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

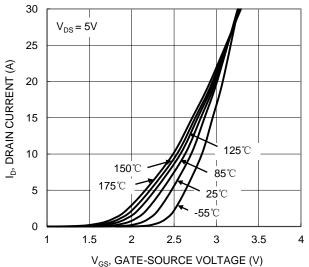


Figure 2. Typical Transfer Characteristic

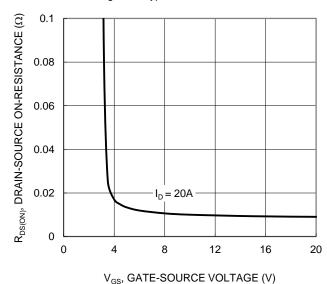


Figure 4. Typical Transfer Characteristic

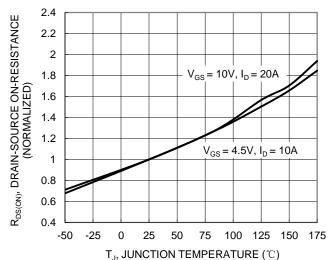


Figure 6. On-Resistance Variation with Temperature





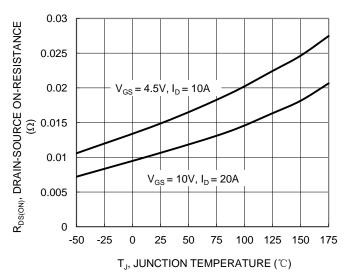


Figure 7. On-Resistance Variation with Temperature

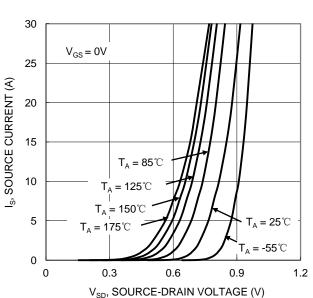


Figure 9. Diode Forward Voltage vs. Current

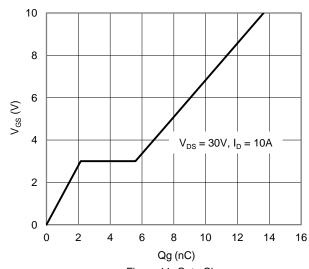


Figure 11. Gate Charge

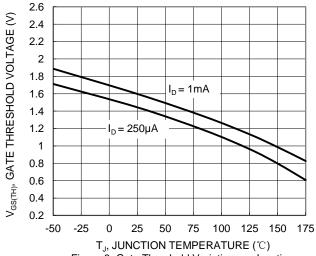


Figure 8. Gate Threshold Variation vs. Junction Temperature

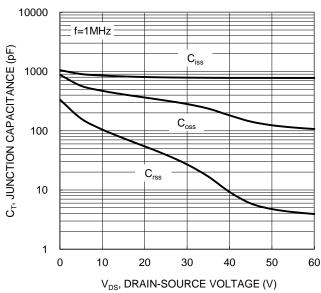


Figure 10. Typical Junction Capacitance

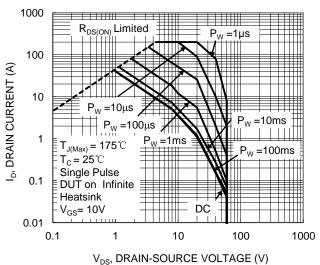


Figure 12. SOA, Safe Operation Area



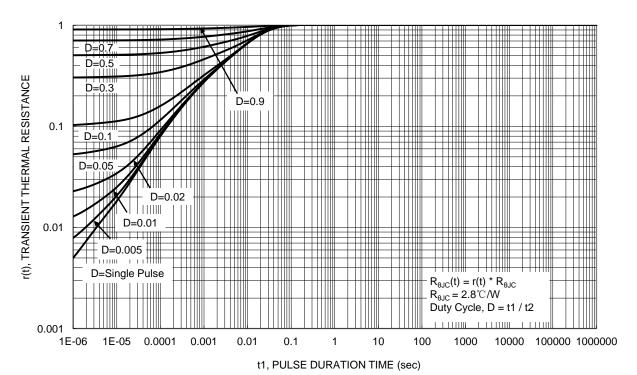


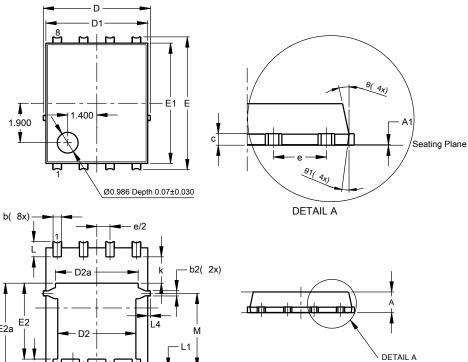
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type Q)

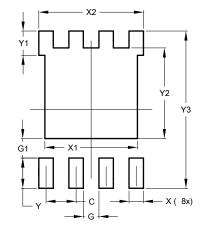


PowerDI5060-8 (SWP)					
(Type Q)					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0	0.05			
b	0.30	0.50	0.41		
b2	0.20	0.35	0.25		
b4).25REF	-		
С	0.230	0.330	0.277		
D		.15 BS0			
D1	4.70	5.10	4.90		
D2	3.56	3.96	3.76		
D2a	3.78	4.18	3.98		
Е	6	.40 BS0	\sim		
E1	5.60	6.00	5.80		
E2	3.46	3.86	3.66		
E2a	4.195	4.595	4.395		
е	1	.27BSC)		
k	1.05				
L	0.635	0.835	0.735		
La	0.635	0.835	0.735		
L1	0.200	0.400	0.300		
L1a	0.050REF				
L4	0.025	0.225	0.125		
М	3.205	4.005	3.605		
θ	10°	12°	11°		
θ1	6°	8°	7°		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (SWP) (Type Q)



Dimensions	Value (in mm)		
С	1.270		
G	0.660		
G1	0.820		
Х	0.610		
X1	4.100		
X2	4.420		
Y	1.270		
Y1	1.020		
Y2	3.810		
Y3	6.610		



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