

Product Summary

BV _{DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
40V	21mΩ @ V _{GS} = 10V	8.6A
	28mΩ @ V _{GS} = 4.5V	6.9A

Features and Benefits

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm²
- Low Gate Threshold Voltage
- Low On-Resistance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free. “Green” Device (Note 3)**
- **The DMN4020LFDEQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

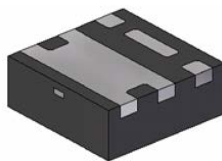
<https://www.diodes.com/quality/product-definitions/>

Description and Applications

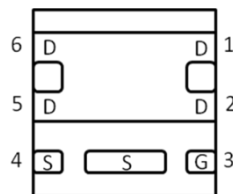
This MOSFET is designed to meet the stringent requirements of automotive applications. It is AEC-Q101 qualified, supported by a PPAP, and is ideal for use in:

- General Purpose Interfacing Switch
- Power Management Functions

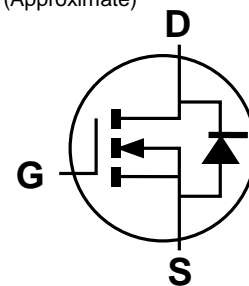
U-DFN2020-6 (Type E)



Bottom View



Pin Out



Equivalent Circuit

Mechanical Data

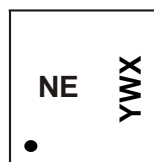
- Case: U-DFN2020-6
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Lead-Frame. Solderable per MIL-STD-202, Method 208 ④
- Weight: 0.0065 grams (Approximate)

Ordering Information (Note 4)

Part Number	Case	Quantity Per Reel
DMN4020LFDEQ-7	U-DFN2020-6 (Type E)	3,000
DMN4020LFDEQ-13	U-DFN2020-6 (Type E)	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



NE = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 0 = 2020)
 W = Week (ex: a = week 27; z represents week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
Code	0	1	2	3	4	5	6	7	8	9	0	1
Week	1-26				27-52				53			
Code	A-Z				a-z				z			
Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat					
Code	T	U	V	W	X	Y	Z					

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	40	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$	I_D	8.6	A
		$T_A = +70^\circ\text{C}$		6.9	
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	40	A
Maximum Body Diode Continuous Current			I_S	8.6	A
Pulsed Body Diode Forward Current (10 μs Pulse, Duty Cycle = 1%)			I_{SM}	40	A
Avalanche Current (Note 7) $L = 0.1\text{mH}$			I_{AS}	22.4	A
Avalanche Energy (Note 7) $L = 0.1\text{mH}$			E_{AS}	25	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	0.85	W
	$T_A = +70^\circ\text{C}$		0.54	
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	147.6	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.35	W
	$T_A = +70^\circ\text{C}$		1.5	
Thermal Resistance, Junction to Ambient (Note 6)		$R_{\theta JA}$	53.3	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	6.9	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.4	—	2.4	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	15	21	m Ω	$V_{GS} = 10\text{V}, I_D = 8\text{A}$
			20	28		$V_{GS} = 4.5\text{V}, I_D = 4\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{ISS}	—	1201	—	pF	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{OSS}	—	87	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	58	—	pF	
Gate Resistance	R_g	—	1.3	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	12.7	—	nC	
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_g	—	25.3	—	nC	
Gate-Source Charge	Q_{gs}	—	5.6	—	nC	
Gate-Drain Charge	Q_{gd}	—	4.4	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	8	—	ns	$V_{DS} = 20\text{V}, R_L = 2.5\Omega$ $V_{GS} = 10\text{V}, R_G = 3\Omega$
Turn-On Rise Time	t_R	—	2.6	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	17	—	ns	
Turn-Off Fall Time	t_F	—	8.9	—	ns	
Reverse Recovery Time	t_{RR}	—	17.5	—	ns	$I_F = 8\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	8.9	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square pad layout.
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

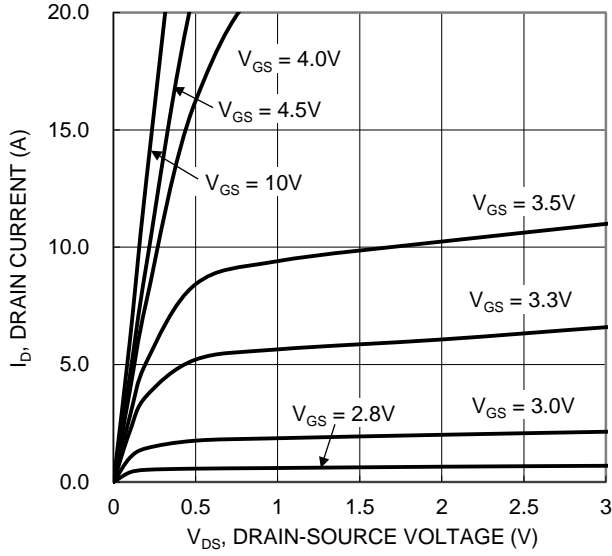


Figure 1. Typical Output Characteristic

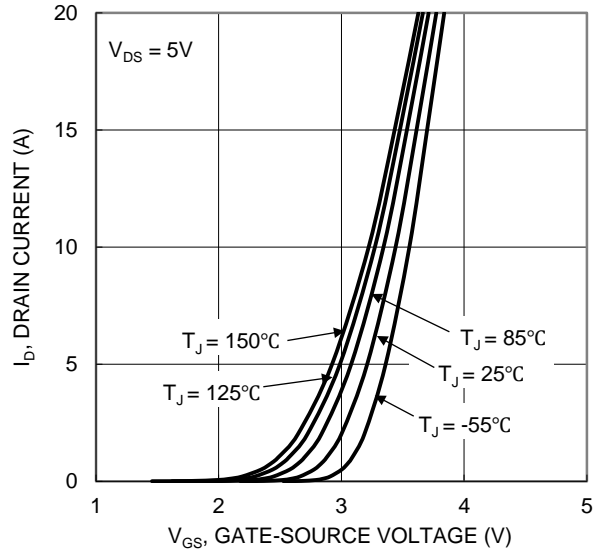


Figure 2. Typical Transfer Characteristic

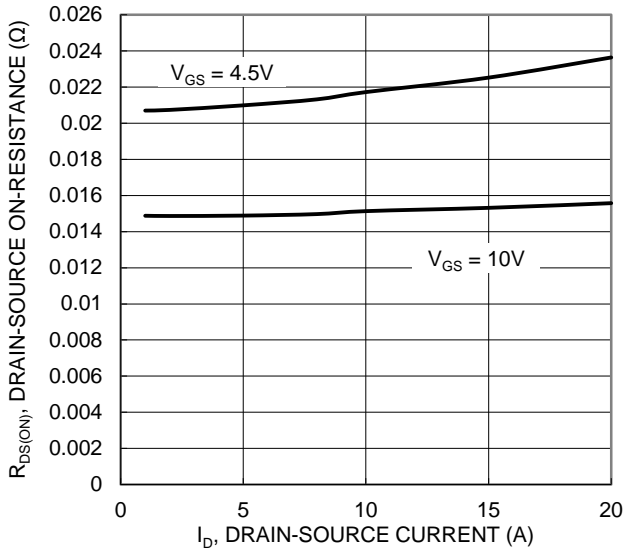


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

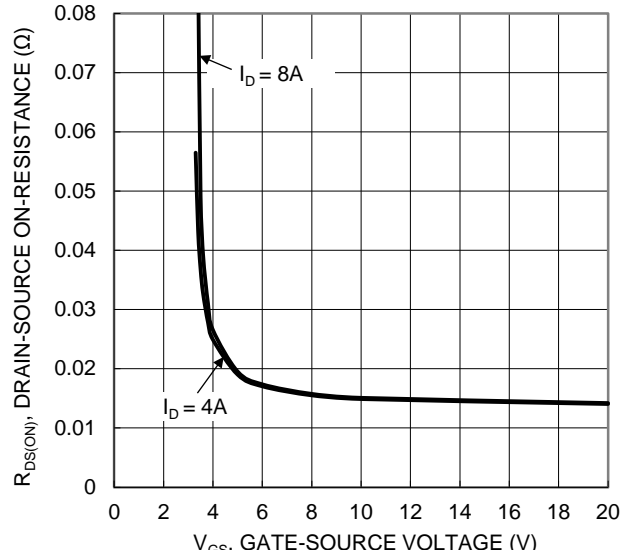


Figure 4. Typical Transfer Characteristic

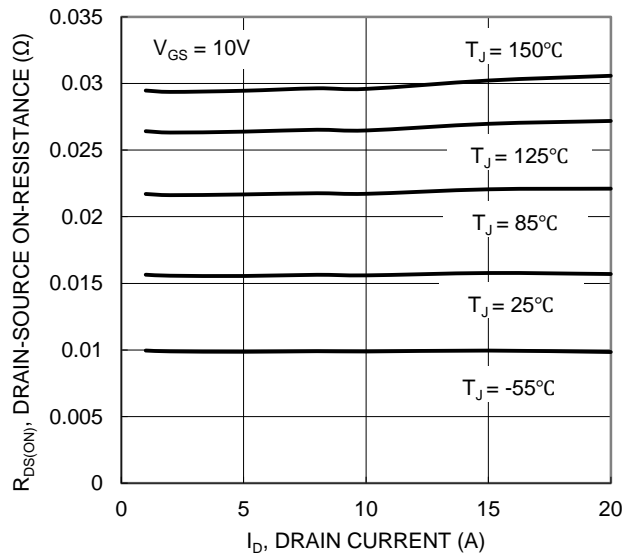


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

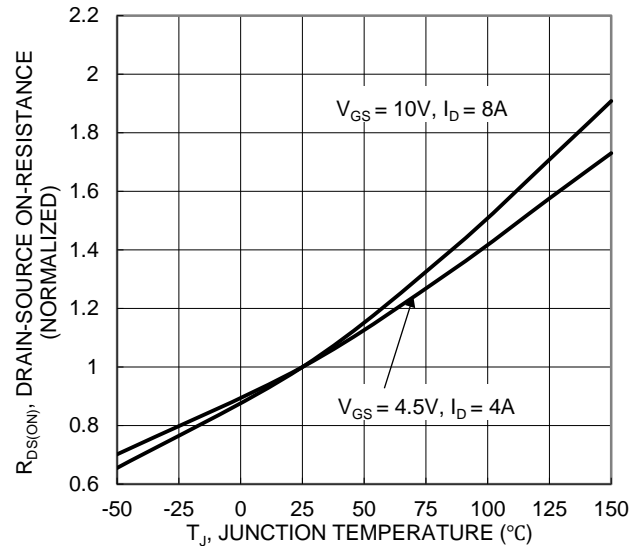


Figure 6. On-Resistance Variation with Junction Temperature

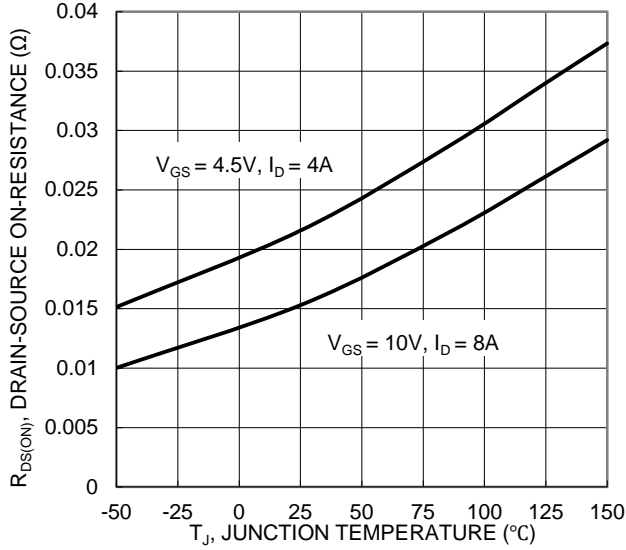


Figure 7. On-Resistance Variation with Junction Temperature

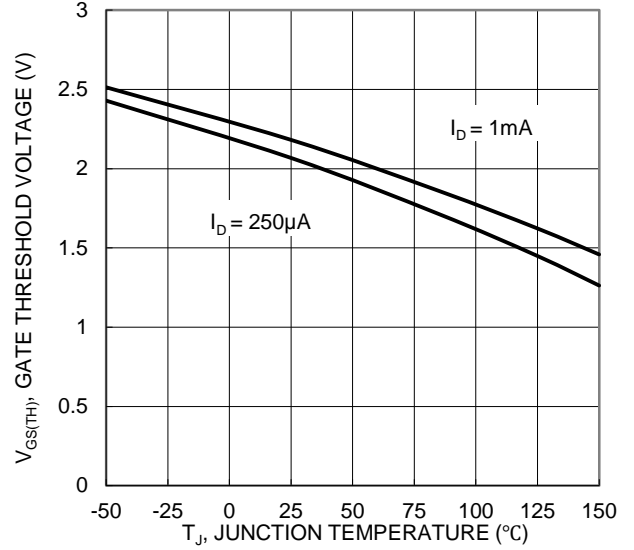


Figure 8. Gate Threshold Variation vs. Junction Temperature

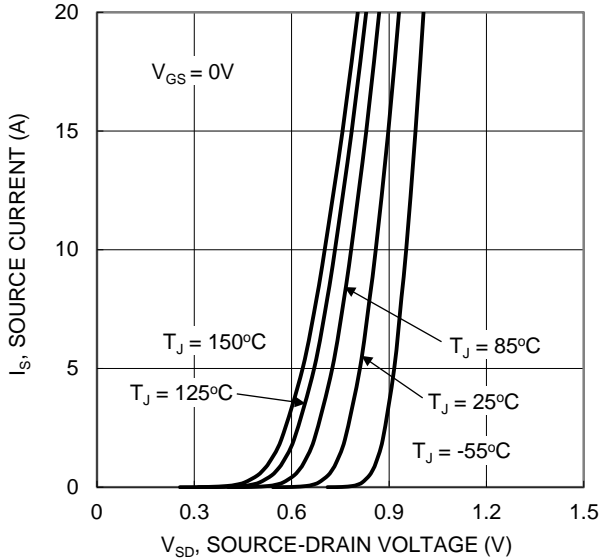


Figure 9. Diode Forward Voltage vs. Current

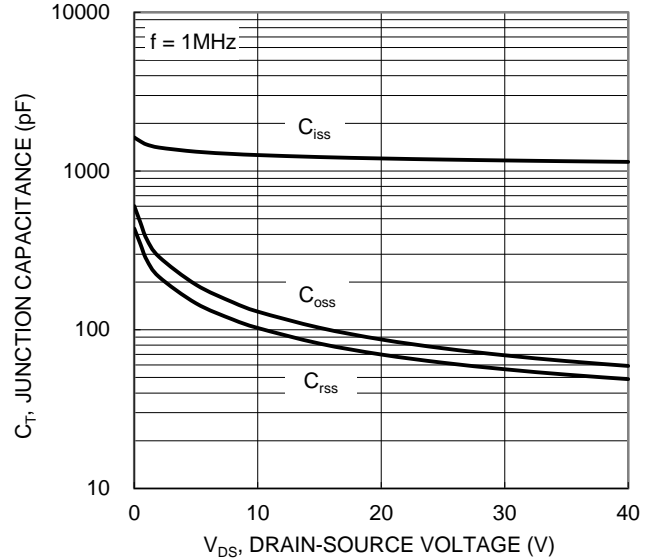


Figure 10. Typical Junction Capacitance

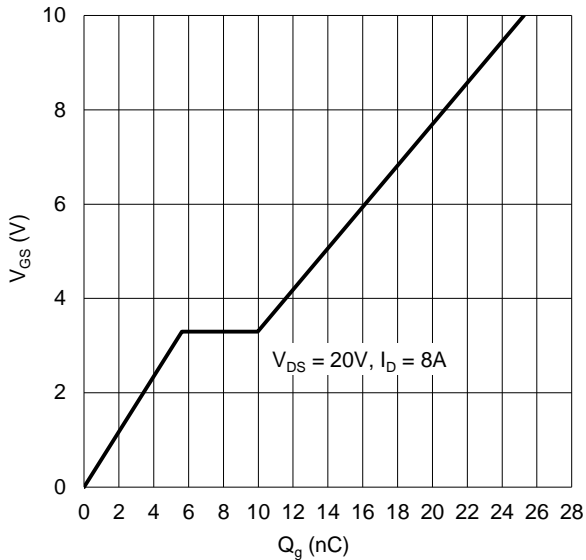


Figure 11. Gate Charge

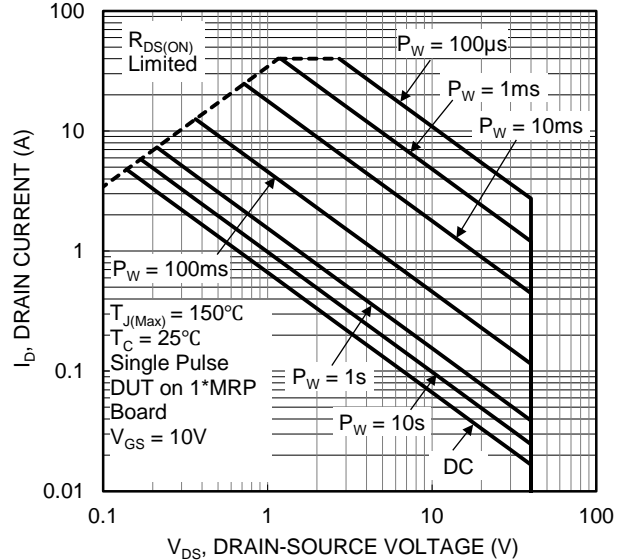


Figure 12. SOA, Safe Operation Area

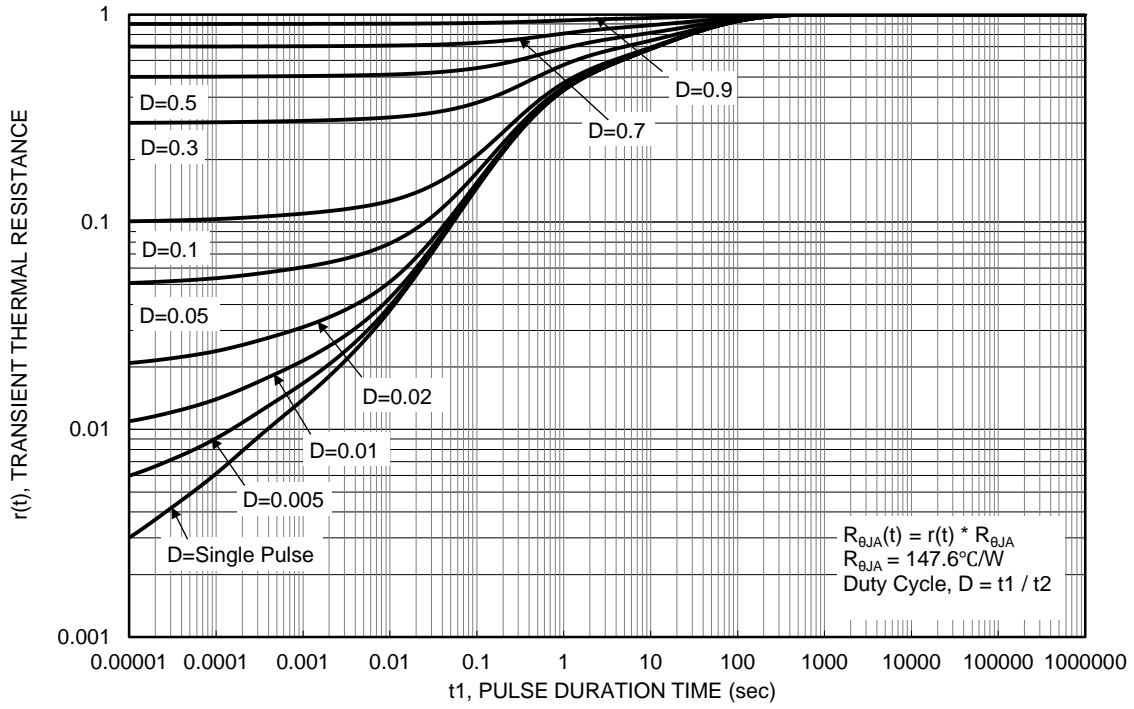
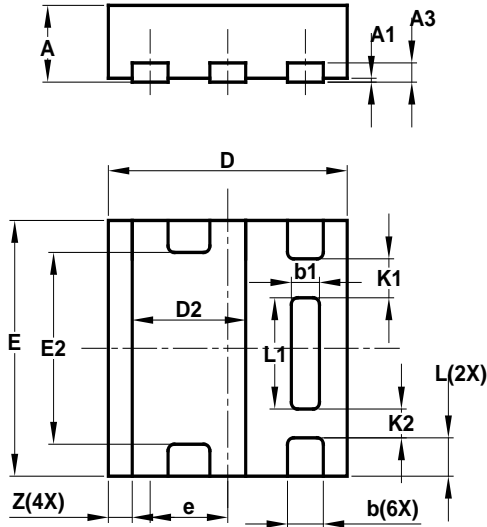


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

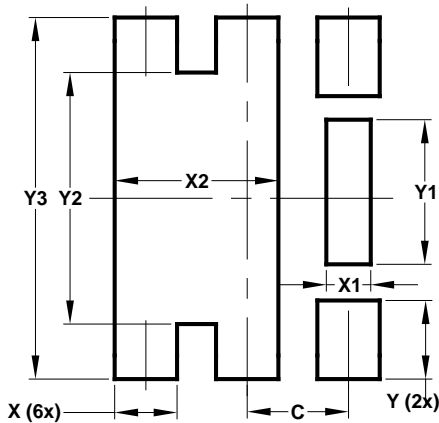


U-DFN2020-6 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
L(2X)	—	—	0.305
K1	—	—	0.225
K2	—	—	0.20
Z	—	—	0.20

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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