

Product Summary

BV_{DSS}	R_{DS(ON)} Max	I_D Max T_C = +25°C (Note 9)
100V	4.3mΩ @ V _{GS} = 10V	100A

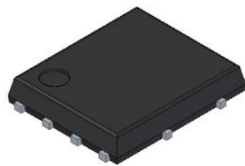
Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize R_{DS(ON)}, yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

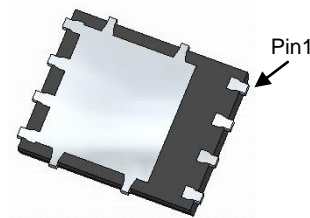
Applications

- Motor Control
- DC-DC Converters
- Power Management

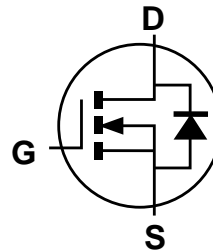
PowerDI5060-8 (Standard)



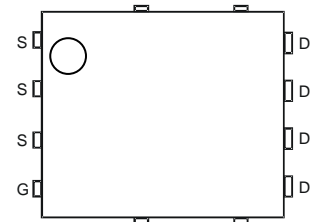
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

Features

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- High Conversion Efficiency
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

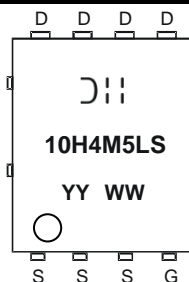
- Case: PowerDI[®]5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.097 grams (Approximate)

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT10H4M5LPS-13	PowerDI5060-8 (Standard)	2,500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <100ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



- **⌋** = Manufacturer's Marking
- 10H4M5LS = Product Type Marking Code
- YYWW = Date Code Marking
- YY or YY = Last Two Digits of Year (ex: 19 = 2019)
- WW or WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 5)	Steady State	$T_A = +25^\circ\text{C}$	19	A
		$T_A = +70^\circ\text{C}$	15	
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6)	Steady State	$T_C = +25^\circ\text{C}$	100	A
		$T_C = +70^\circ\text{C}$ (Note 9)	100	
Pulsed Drain Current (10 μs Pulse, $T_C = +25^\circ\text{C}$, Package Limited)		I_{DM}	400	A
Maximum Continuous Body Diode Forward Current (Note 6)		I_S	100	A
Pulsed Body Diode Forward Current (10 μs Pulse, $T_C = +25^\circ\text{C}$, Package Limited)		I_{SM}	400	A
Avalanche Current (Note 7) $L = 0.3\text{mH}$		I_{AS}	40	A
Avalanche Energy (Note 7) $L = 0.3\text{mH}$		E_{AS}	240	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	2.3	W
Thermal Resistance, Junction to Ambient (Note 5)		$R_{\theta JA}$	54	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_C = +25^\circ\text{C}$	P_D	113	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	100	—	—	V	$V_{GS} = 0\text{V}, I_D = 10\text{mA}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	—	2.5	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	3.5	4.3	m Ω	$V_{GS} = 10\text{V}, I_D = 30\text{A}$
		—	4.7	6.2		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$
Diode Forward Voltage	V_{SD}	—	—	1.2	V	$V_{GS} = 0\text{V}, I_S = 30\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{ISS}	—	4843	—	pF	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{OSS}	—	1302	—		
Reverse Transfer Capacitance	C_{RSS}	—	25.5	—		
Gate Resistance	R_g	—	2.1	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_g	—	80	—	nC	$V_{DD} = 50\text{V}, I_D = 30\text{A},$ $V_{GS} = 10\text{V}$
Gate-Source Charge	Q_{GS}	—	14	—		
Gate-Drain Charge	Q_{GD}	—	18	—		
Turn-On Delay Time	$t_{D(ON)}$	—	9	—	ns	$V_{DD} = 50\text{V}, V_{GS} = 10\text{V},$ $I_D = 30\text{A}, R_g = 4.7\Omega, R_L = 1.1\Omega$
Turn-On Rise Time	t_R	—	26	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	76	—		
Turn-Off Fall Time	t_F	—	50	—		
Reverse Recovery Time	t_{RR}	—	63	—	ns	$I_F = 22.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	133	—	nC	

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.
 - Package limited.

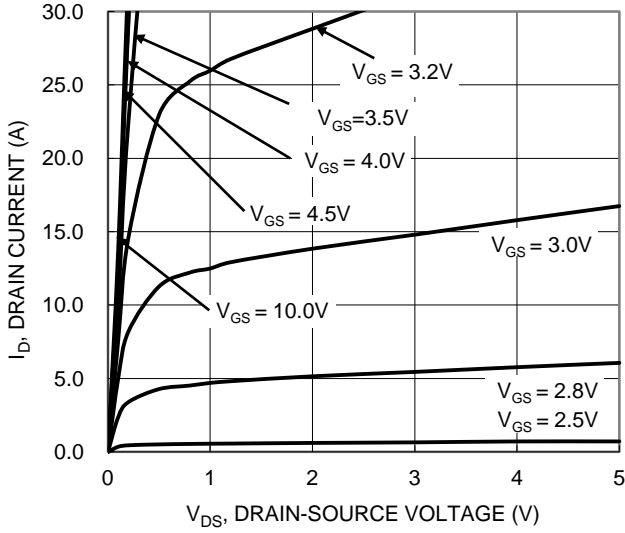


Figure 1. Typical Output Characteristic

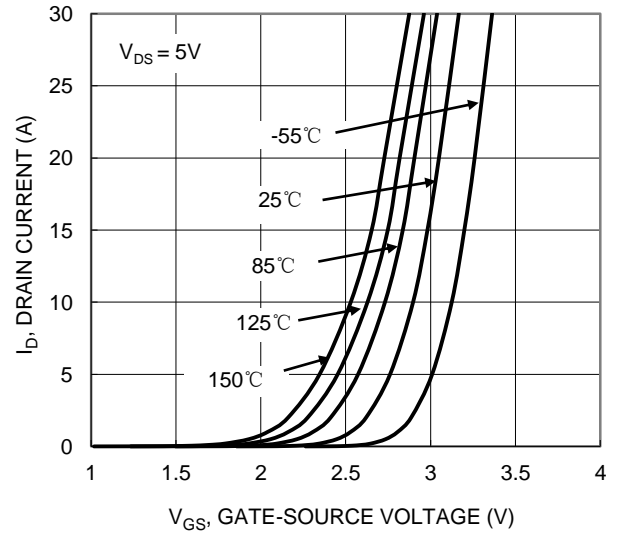


Figure 2. Typical Transfer Characteristic

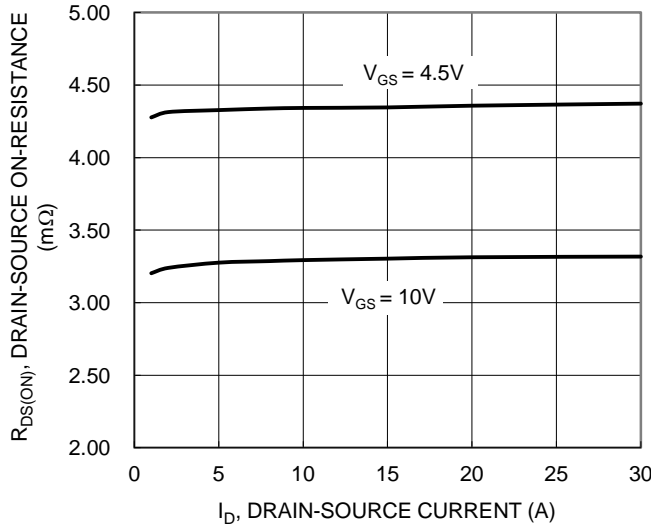


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

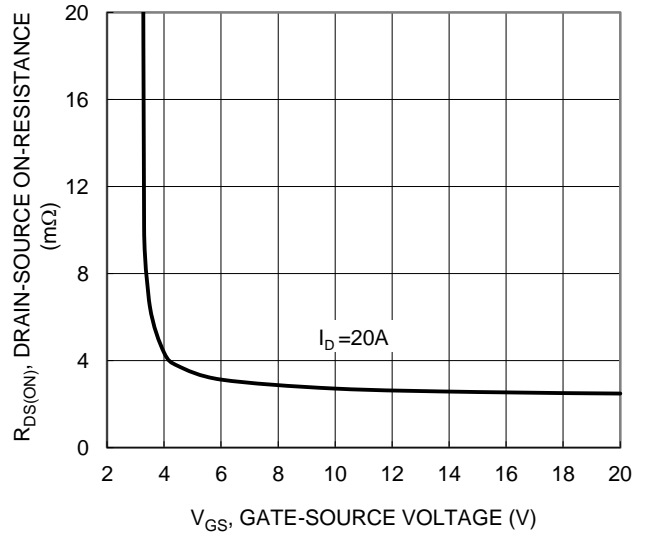


Figure 4. Typical Transfer Characteristic

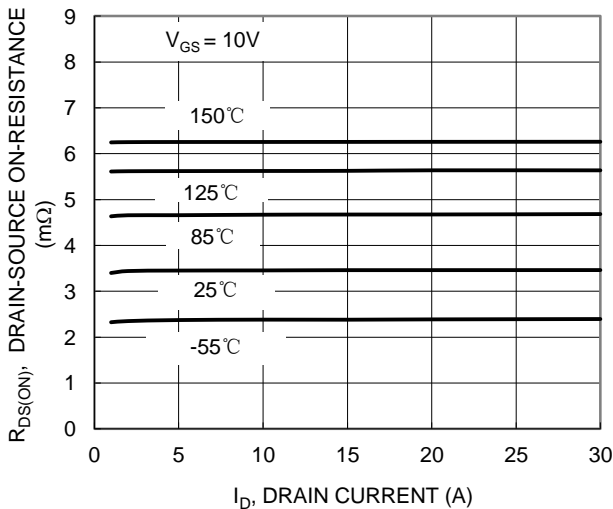


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

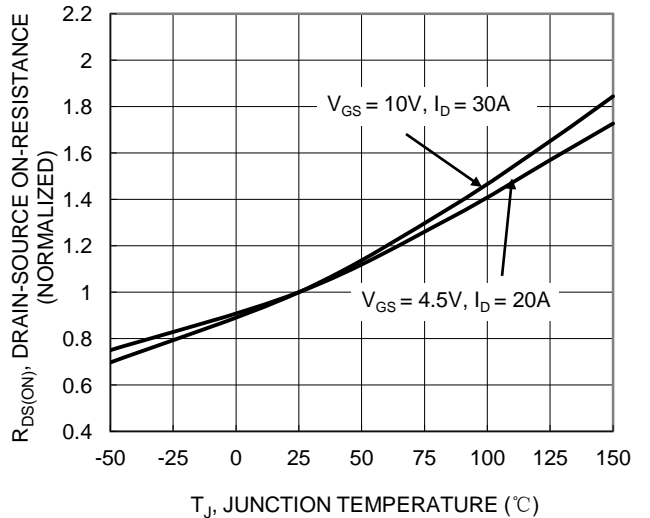


Figure 6. On-Resistance Variation with Temperature

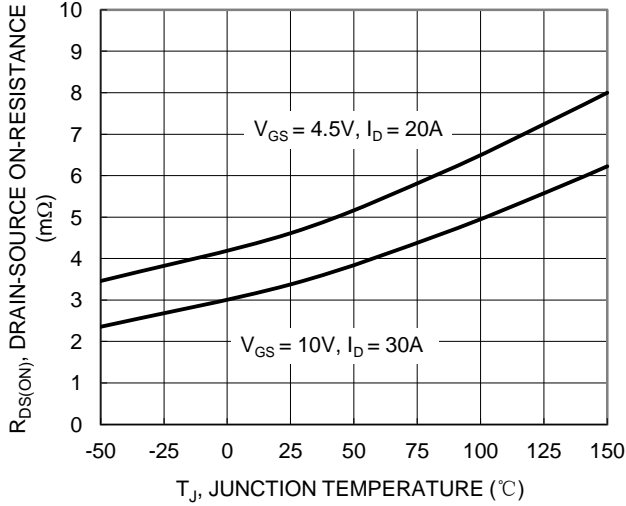


Figure 7. On-Resistance Variation with Temperature

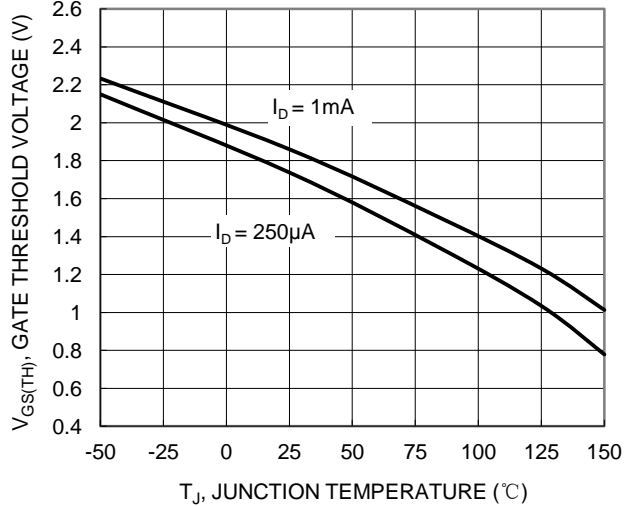


Figure 8. Gate Threshold Variation vs. Junction Temperature

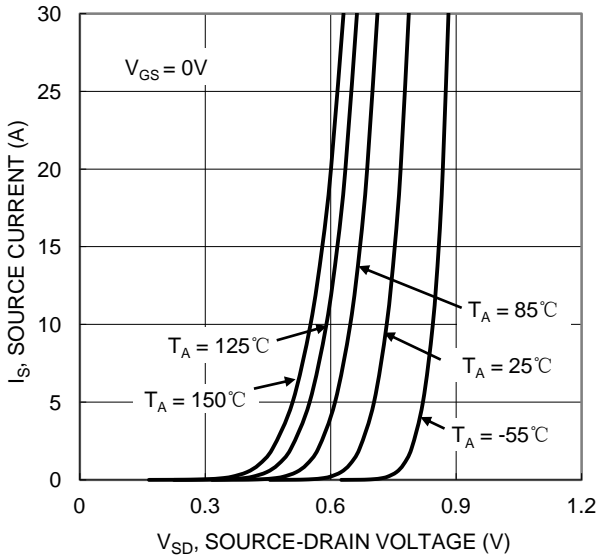


Figure 9. Diode Forward Voltage vs. Current

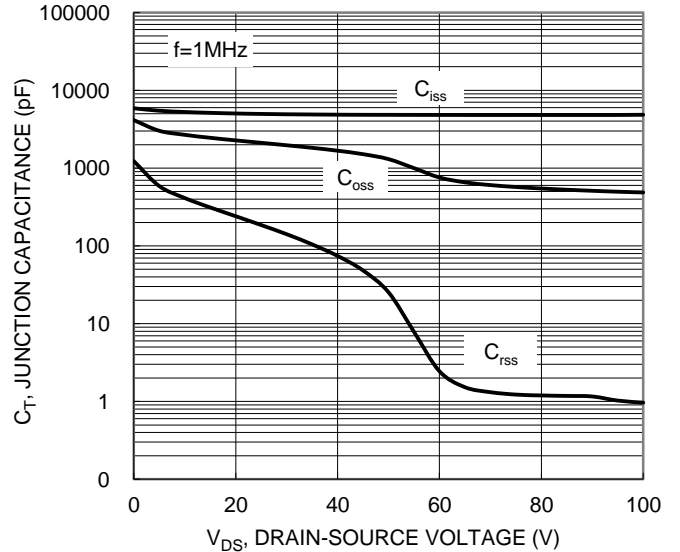


Figure 10. Typical Junction Capacitance

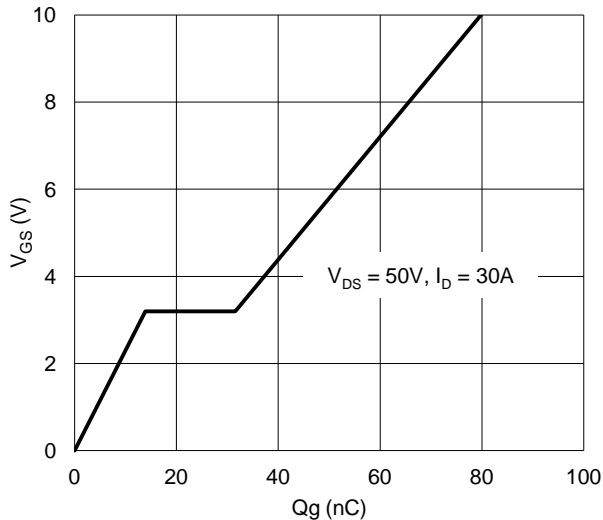


Figure 11. Gate Charge

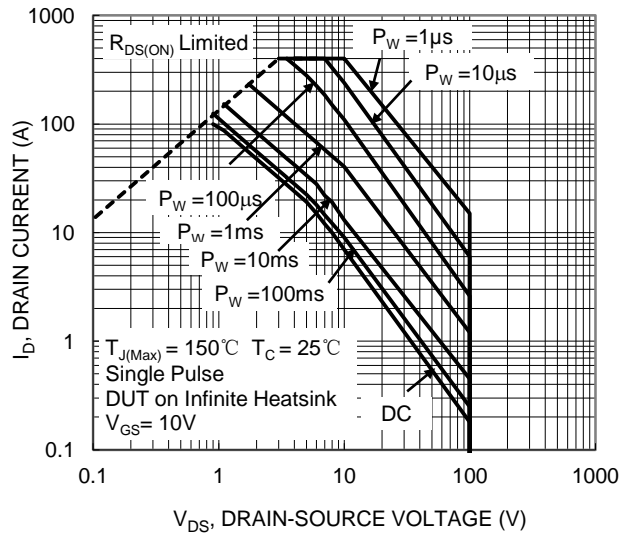


Figure 12. SOA, Safe Operation Area

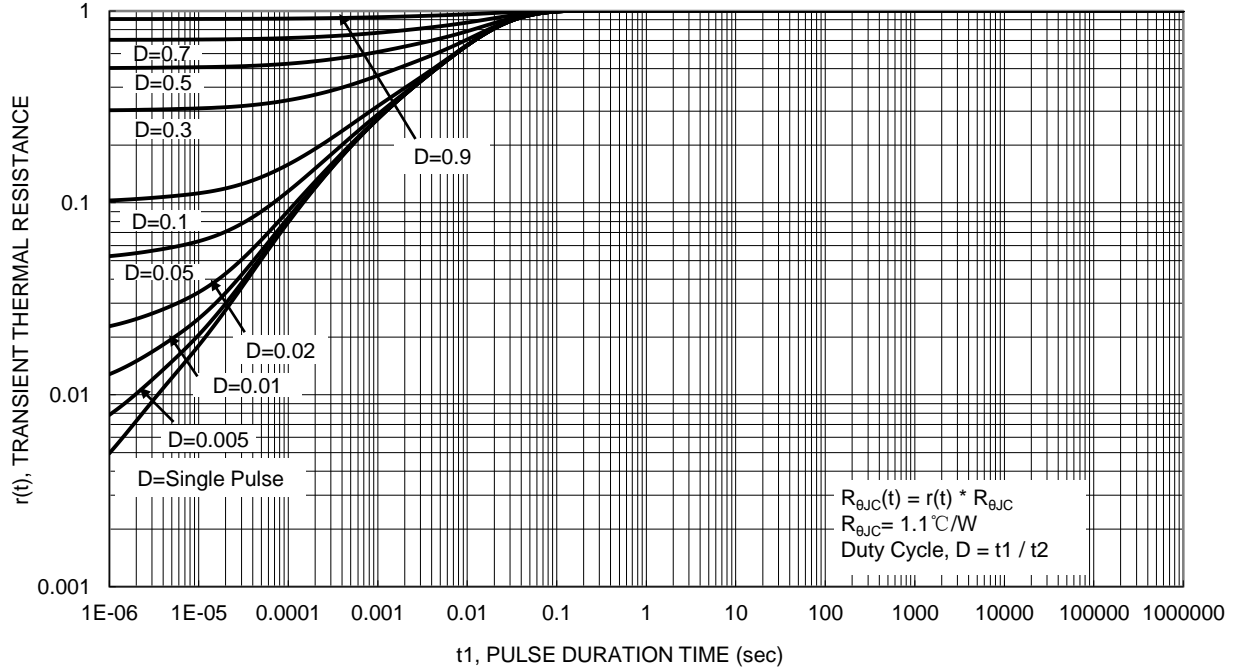
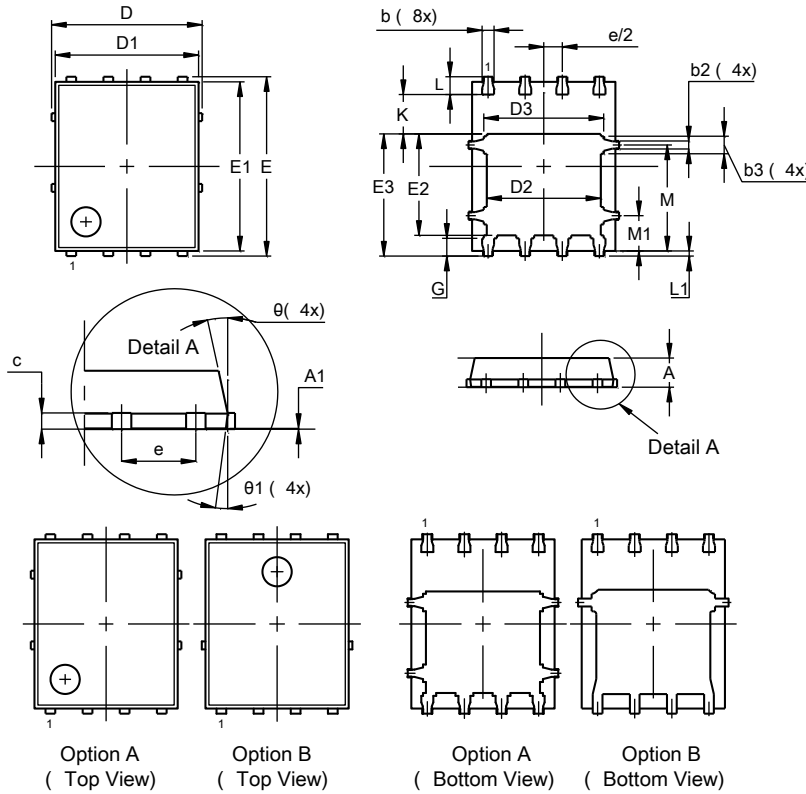


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (Standard)

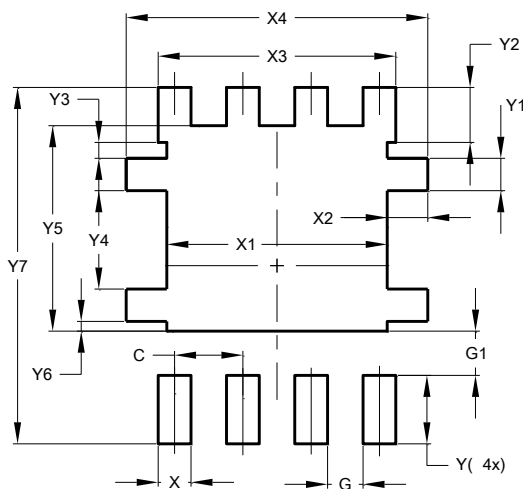


PowerDI5060-8 (Standard)			
Dim	Min	Max	Typ
A	0.90	1.20	--
A1	0.00	0.05	--
b	0.33	0.51	--
b2	0.200	0.350	--
b3	0.40	0.80	0.60
c	0.230	0.354	--
D (Option A)	5.15 BSC		
D (Option B)	5.30 BSC		
D1	4.70	5.40	--
D2	3.70	4.25	--
D3	3.90	4.70	--
E	6.15 BSC		
E1	5.60	6.06	--
E2	3.28	3.92	--
E3	3.99	4.39	--
e	1.27 BSC		
G	0.40	0.71	--
K	0.51	1.45	--
L	0.38	0.71	--
L1	0.100	0.200	--
M	3.235	4.035	--
M1	1.00	1.40	1.21
θ	8°	12°	--
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8 (Standard)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.300
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	4.100
Y6	0.180
Y7	6.610

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