



40V N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
40V	$8.5 \text{m}\Omega @ V_{GS} = 10V$	12.8A
	12.5mΩ @ $V_{GS} = 4.5V$	10.6A

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}), maintain superior switching performance, making it ideal for high efficiency power management applications.

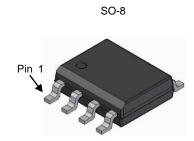
- DC-DC Converters
- Synchronous Rectification
- Power Supplies

Features and Benefits

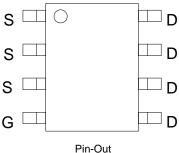
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Mechanical Data

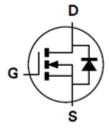
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.076 grams (Approximate)



Top View



Pin-Out Top View



Equivalent Circuit

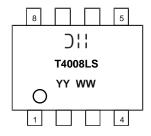
Ordering Information (Note 4)

Part Number	Case	Packaging
DMT4008LSS-13	SO-8	2,500/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



☐ Sill = Manufacturer's Marking
☐ T4008LS = Product Type Marking Code
☐ YYWW = Date Code Marking
☐ YY or YY = Year (ex: 19 = 2019)
☐ WW or WW = Week (01 to 53)



Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	40	V	
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Note 6)	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I _D	12.8 10.3	А
Continuous Drain Current, $V_{GS} = 10V$ (Note 5) $T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$		I _D	10.2 8.2	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	90	Α	
Maximum Continuous Body Diode Forward Current (Note 6)	Is	2.6	Α	
Avalanche Current, L = 0.1mH	I _{AS}	23.4	А	
Avalanche Energy, L = 0.1mH	E _{AS}	27.3	mJ	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

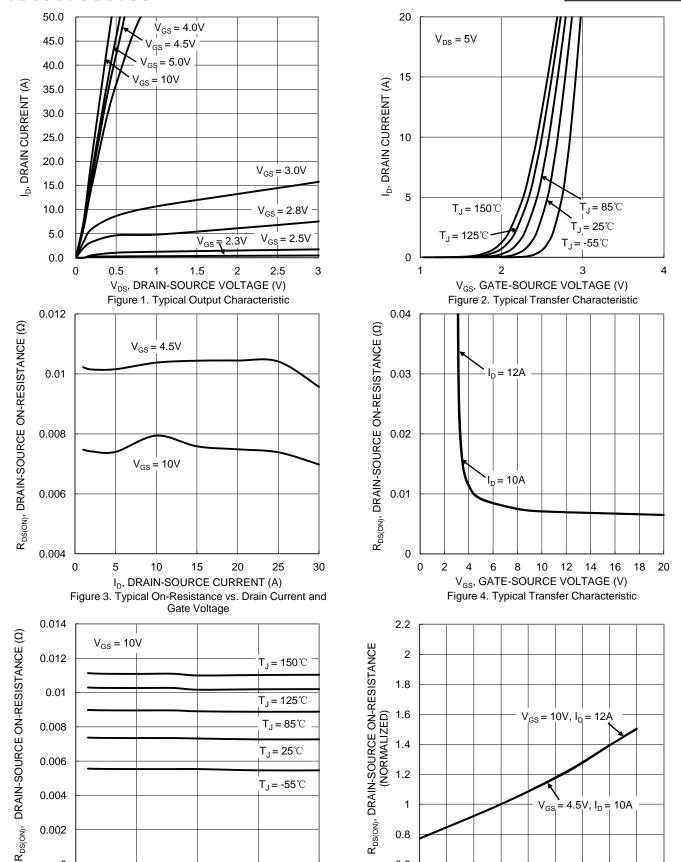
Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	P_{D}	1.32	W	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{0JA}	94	°C/W
Total Power Dissipation (Note 6)	P_{D}	2.09	W	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{0JA}	59.2	°C/W
Thermal Resistance, Junction to Case	R ₀ JC	7.6	°C/W	
Operating and Storage Temperature Range		T_J , T_STG	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	40	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μΑ	$V_{DS} = 32V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(TH)}	1	1.56	3	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance		_	6.8	8.5	mΩ	$V_{GS} = 10V, I_D = 12A$	
Static Dialii-Source Off-Resistance	R _{DS(ON)}	_	9.6	12.5		$V_{GS} = 4.5V, I_D = 10A$	
Diode Forward Voltage	V_{SD}	_	0.8	1.2	V	$V_{GS} = 0V, I_{S} = 10A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	1,143	_		V _{DS} = 20V, V _{GS} = 0V, f = 1MHz	
Output Capacitance	Coss	-	320	_	pF		
Reverse Transfer Capacitance	C_{rss}	_	24.9	_			
Gate Resistance	R_{G}	_	0.91	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 10V)	Q_{G}	_	18.6	_			
Total Gate Charge (V _{GS} = 4.5V)	Q_{G}	_	9.4	_	nC	V 20V L 40A	
Gate-Source Charge	Q _{GS}	_	1.9	_	nc	$V_{DS} = 20V, I_{D} = 10A$	
Gate-Drain Charge	Q_{GD}	_	3.3	_			
Turn-On Delay Time	t _{D(ON)}	_	4.9	_		$V_{GS} = 10V, V_{DS} = 20V,$ $R_G = 6\Omega, I_D = 10A$	
Turn-On Rise Time	t _R	_	5.9	_			
Turn-Off Delay Time	t _{D(OFF)}	_	26.2	_	ns		
Turn-Off Fall Time	t _F	_	10.9	_			
Reverse Recovery Time	t _{RR}	_	14.5	_	ns L 40A III/II 400A/		
Reverse Recovery Charge	Q_{RR}	_	13.0	_	nC	$I_F = 10A$, di/dt = 400A/ μ s	

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
- 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.





ID, DRAIN CURRENT (A) Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

10

75

50

25

= 4.5_V, I_D = 10A

100 125

0.002

0

0

20

1

0.8

0.6

-50 -25 150 175





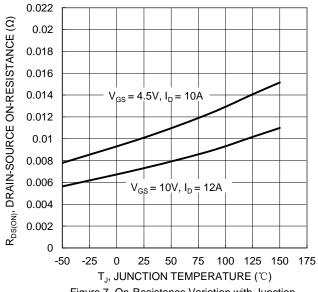
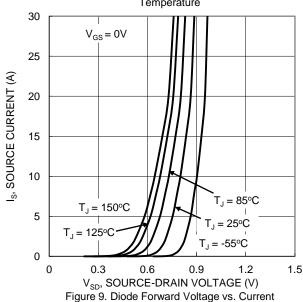


Figure 7. On-Resistance Variation with Junction Temperature

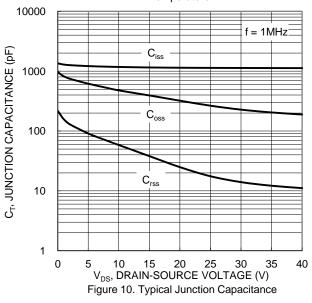


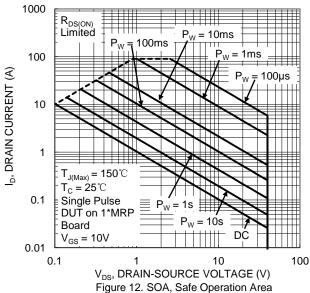
10 9 8 7 6 5 4 3 $V_{DS} = 20V, I_{D} = 10A$ 2 1 0 0 12 16 20 Q_q (nC)

Figure 11. Gate Charge

3 $V_{GS(TH)}, \text{ GATE THRESHOLD VOLTAGE }(V)$ 2.5 2 $I_D = 1mA$ 1.5 1 $I_{D} = 250 \mu A$ 0.5 0 -50 -25 0 25 50 75 100 125 150 175 T_J, JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature







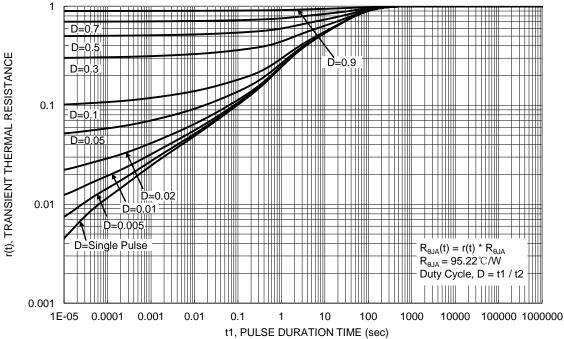


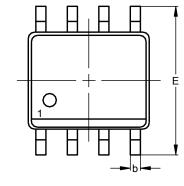
Figure 13. Transient Thermal Resistance

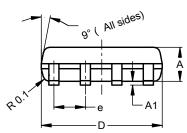


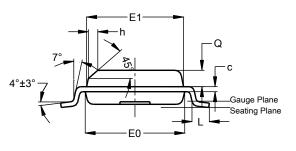
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8





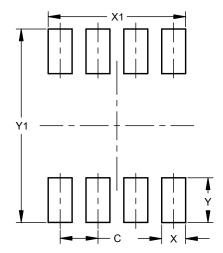


SO-8					
Dim	Min	Max	Тур		
Α	1.40	1.50	1.45		
A1	0.10	0.20	0.15		
b	0.30	0.50	0.40		
С	0.15	0.25	0.20		
D	4.85	4.95	4.90		
Е	5.90	6.10	6.00		
E1	3.80	3.90	3.85		
E0	3.85	3.95	3.90		
е			1.27		
h	-		0.35		
L	0.62	0.82	0.72		
Q	0.60	0.70	0.65		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)		
C	1.27		
Х	0.802		
X1	4.612		
Y	1.505		
Y1	6.50		



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