

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D $T_C = +25^\circ C$
100V	9.5mΩ @ $V_{GS} = 10V$	48A

Features and Benefits

- 100% Unclamped Inductive Switch (UIS) Test in Production
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

Description and Applications

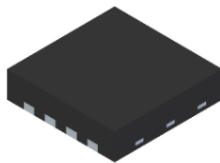
This new generation N-channel enhancement mode MOSFET is designed to minimize $R_{DS(ON)}$ yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

- Backlighting
- Power Management Functions
- DC-DC Converters

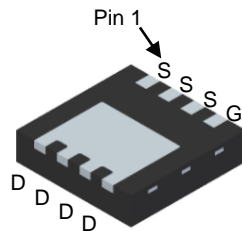
Mechanical Data

- Case: V-DFN3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Below Diagram
- Terminals: Finish –NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^(e4)
- Weight: 0.03 grams (Approximate)

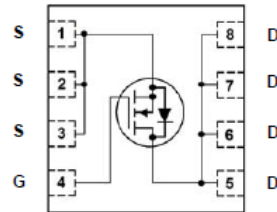
V-DFN3333-8 (Type B)



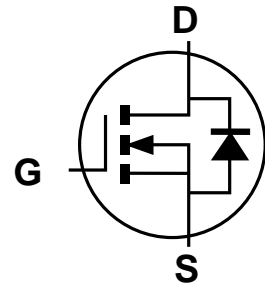
Top View



Bottom View



Top View
Internal Schematic



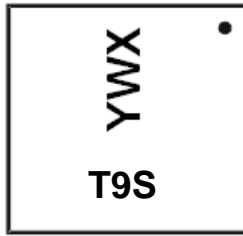
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT10H009SCG-7	V-DFN3333-8 (Type B)	2000/Tape & Reel
DMT10H009SCG-13	V-DFN3333-8 (Type B)	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



T9S = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 0 = 2020)
 W = Week (ex: a = Week 27; z Represents Week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Code	9	0	1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Note 6)	Steady State	T _A = +25°C	14
		T _A = +70°C	11
Continuous Drain Current, V _{GS} = 10V	Steady State	T _C = +25°C	48
		T _C = +70°C	38
Maximum Continuous Body Diode Forward Current (Note 6)	I _S	48	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	198.5	A
Pulsed Body Diode Continuous Current (10µs Pulse, Duty Cycle = 1%)	I _{SM}	198.5	A
Avalanche Current, L = 0.3mH (Note 8)	I _{AS}	27	A
Avalanche Energy, L = 0.3mH (Note 8)	E _{AS}	109.4	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P _D	1.3	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	99	°C/W
Total Power Dissipation (Note 6)	P _D	2.7	W
Thermal Resistance, Junction to Ambient (Note 6)	R _{θJA}	46	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	3.7	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	100	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 80V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	2	—	4	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	7.5	9.5	mΩ	V _{GS} = 10V, I _D = 20A
Diode Forward Voltage	V _{SD}	—	0.8	1.2	V	V _{GS} = 0V, I _S = 20A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{ISS}	—	2085	—	pF	V _{DS} = 50V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{OSS}	—	609	—		
Reverse Transfer Capacitance	C _{rss}	—	13	—	nC	V _{DD} = 50V, I _D = 13A, V _{GS} = 10V
Gate Resistance	R _g	—	1.7	—		
Total Gate Charge	Q _g	—	30	—		
Gate-Source Charge	Q _{gs}	—	9.5	—		
Gate-Drain Charge	Q _{gd}	—	7.3	—	ns	V _{DD} = 50V, V _{GS} = 10V, I _D = 13A, R _g = 6Ω
Turn-On Delay Time	t _{D(ON)}	—	9.7	—		
Turn-On Rise Time	t _R	—	13.7	—		
Turn-Off Delay Time	t _{D(OFF)}	—	25.1	—		
Turn-Off Fall Time	t _F	—	17.3	—	ns	I _F = 13A, di/dt = 100A/μs
Reverse Recovery Time	t _{RR}	—	45	—		
Reverse Recovery Charge	Q _{RR}	—	68	—	nC	

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

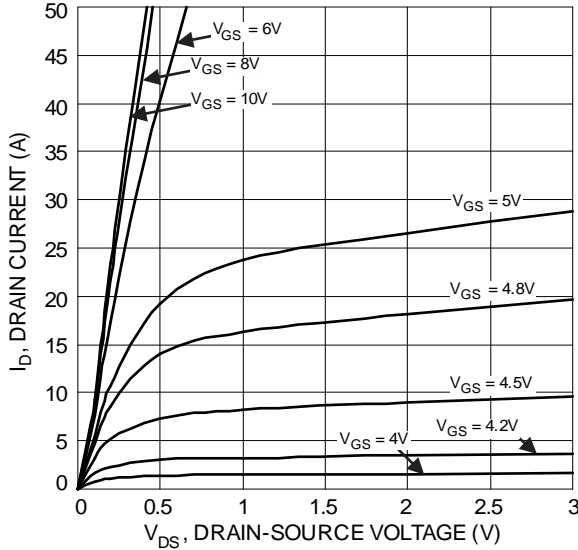


Figure 1 Typical Output Characteristic

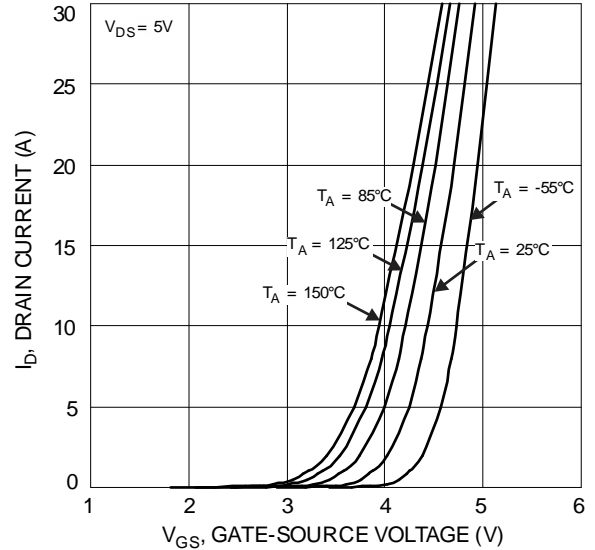


Figure 2 Typical Transfer Characteristics

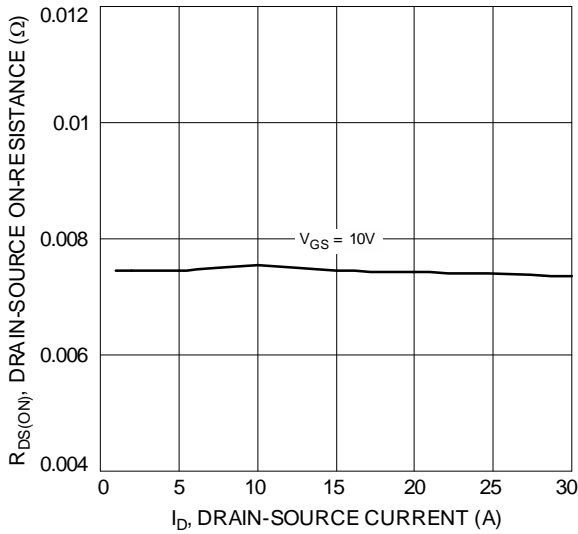


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

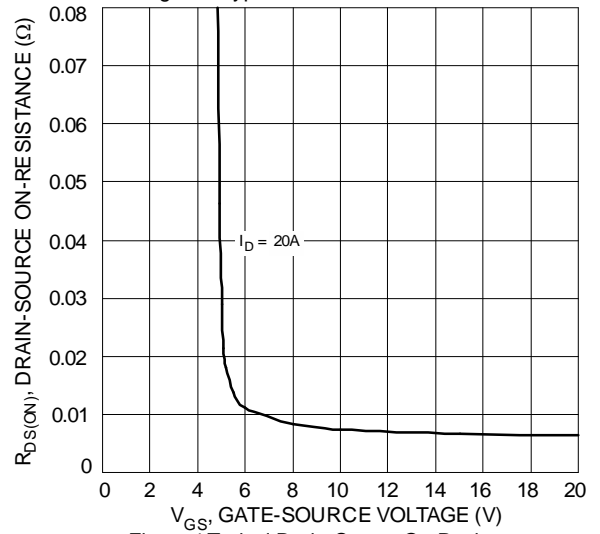


Figure 4 Typical Drain-Source On-Resistance vs. Gate-Source Voltage

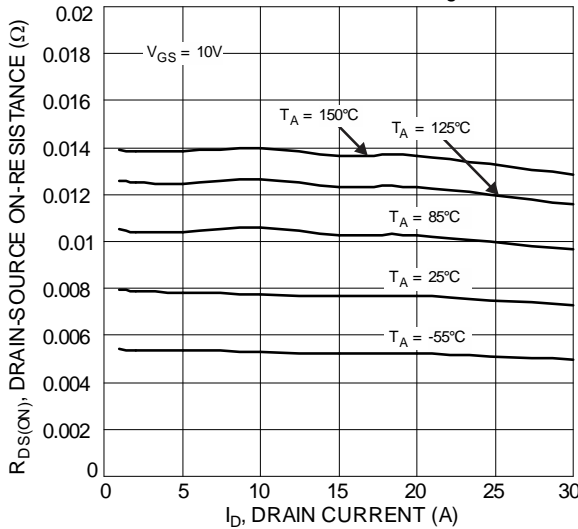


Figure 5 Typical On-Resistance vs. Drain Current and Temperature

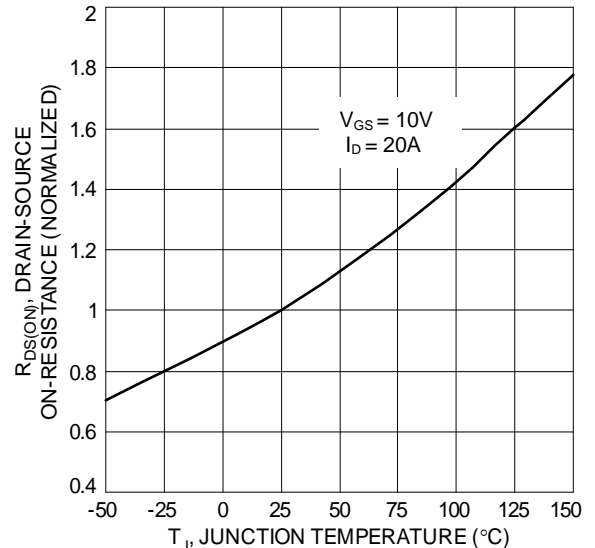


Figure 6 On-Resistance Variation with Temperature

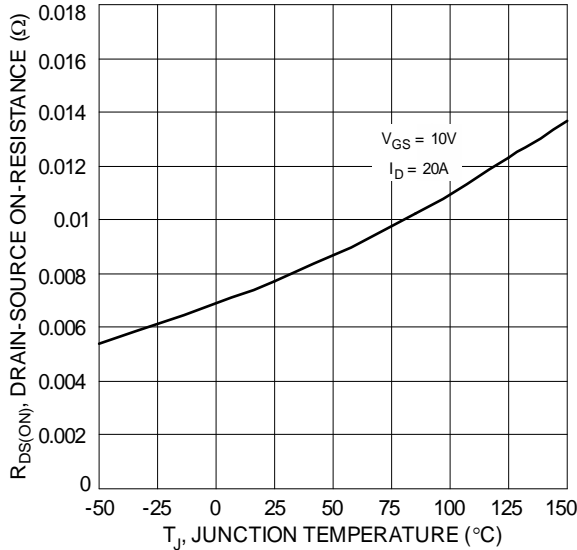


Figure 7 On-Resistance Variation with Temperature

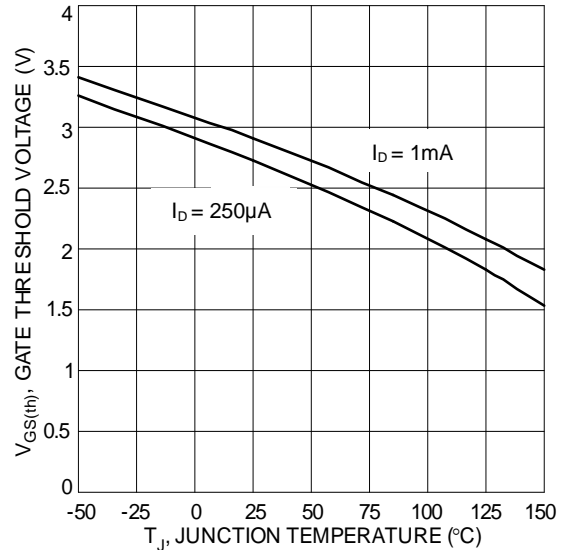


Figure 8 Gate Threshold Variation vs. Junction Temperature

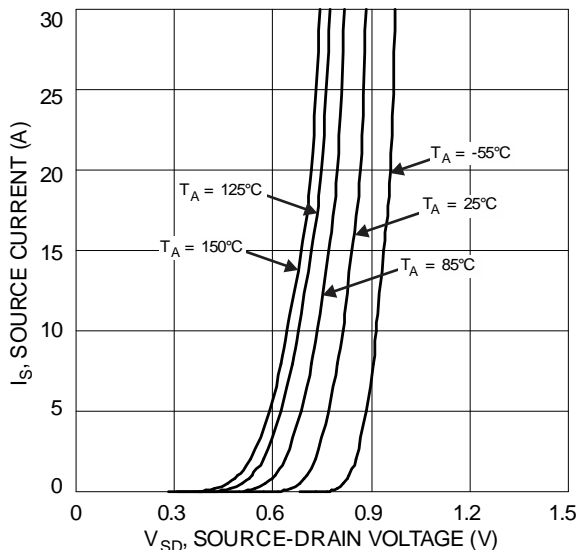


Figure 9 Diode Forward Voltage vs. Current

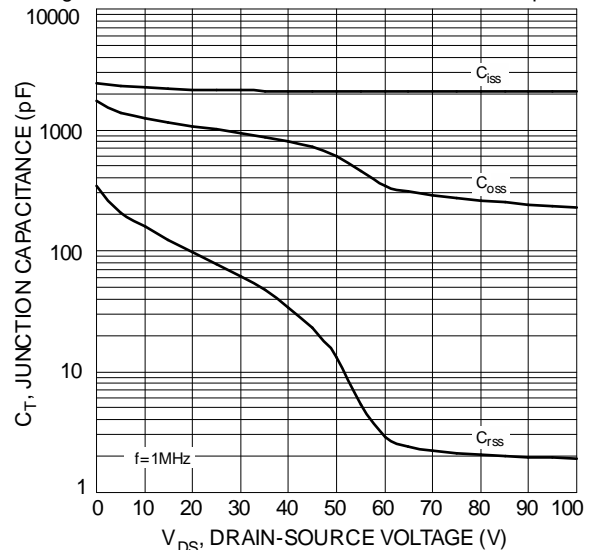


Figure 10 Typical Junction Capacitance

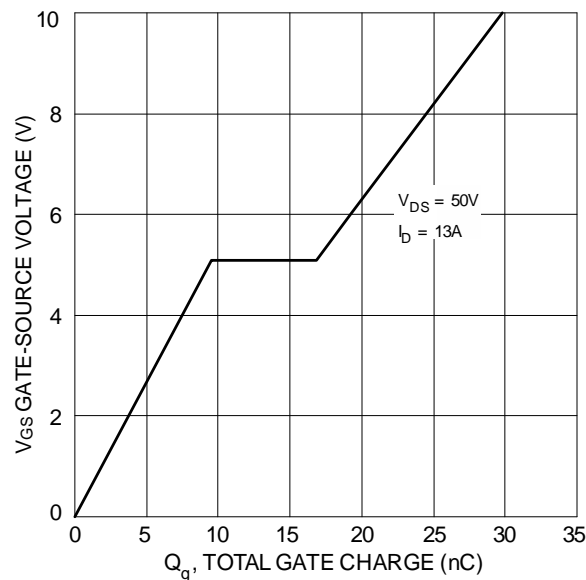


Figure 11 Gate Charge

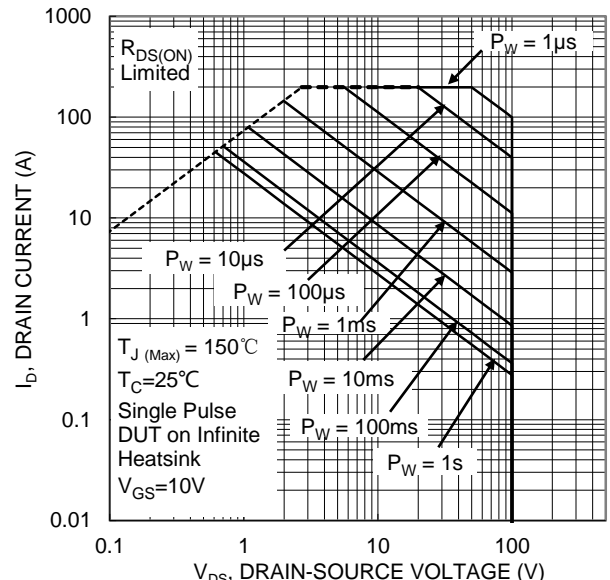
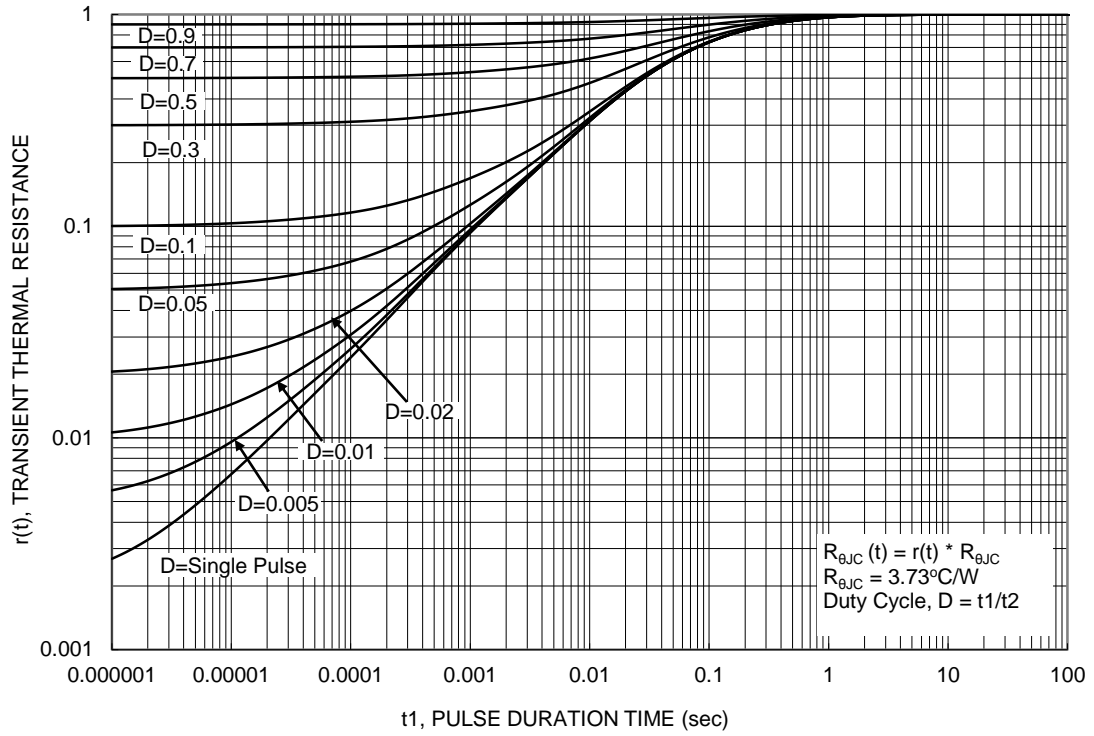


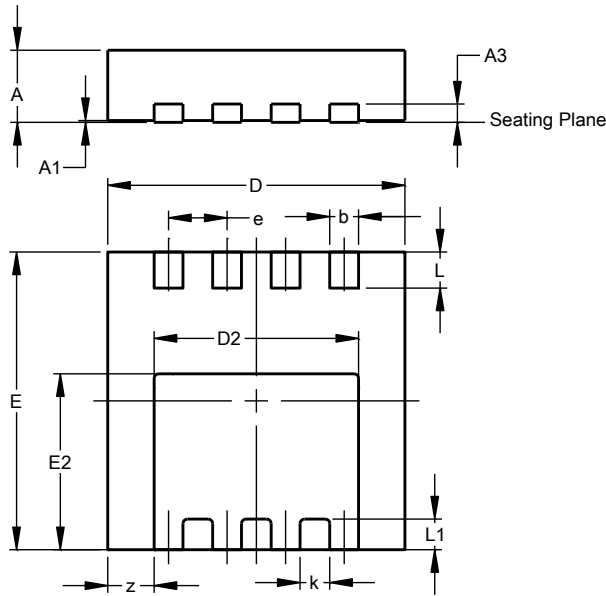
Figure 12 SOA, Safe Operation Area



Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3333-8 (Type B)

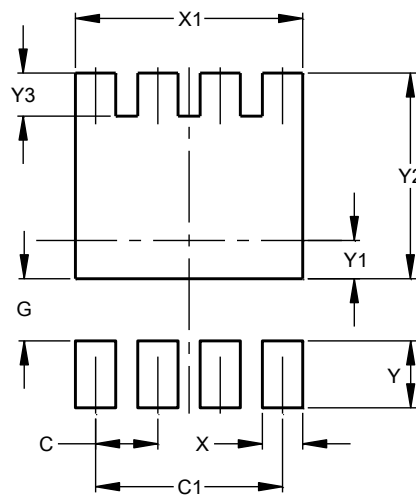


V-DFN3333-8 (Type B)			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	--	--	0.203
b	0.27	0.37	0.32
D	3.25	3.35	3.30
D2	2.17	2.37	2.27
E	3.25	3.35	3.30
E2	1.85	2.05	1.95
e	--	--	0.65
k	--	--	0.33
L	0.35	0.45	0.40
L1	--	--	0.34
z	--	--	0.515
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3333-8 (Type B)



Dimensions	Value (in mm)
C	0.650
C1	1.950
G	0.650
X	0.420
X1	2.370
Y	0.700
Y1	0.400
Y2	2.150
Y3	0.450

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