

Voltage Detector with Adjustable Delay Time

Features

- Operate from VCC of 1.2V to 5.5V
- Capacitor-Adjustable Delay
- Active-High/-Low Output Options
- Open-Drain /Push-Pull Output Options
- Detect Voltage Threshold Accurate: 2.5% in full Temperature from -40 °C to +85 °C
- Low Supply Current (2µA, Typ.)
- Ultra-Small 4-Pin UDFN Package or SOT23-5 Package or SC70-4 package

Applications

- Computers/Servers/Networking
- Medical Equipment
- Critical µP Monitoring
- Intelligent Instruments
- Set-Top Boxes/Portable Equipment

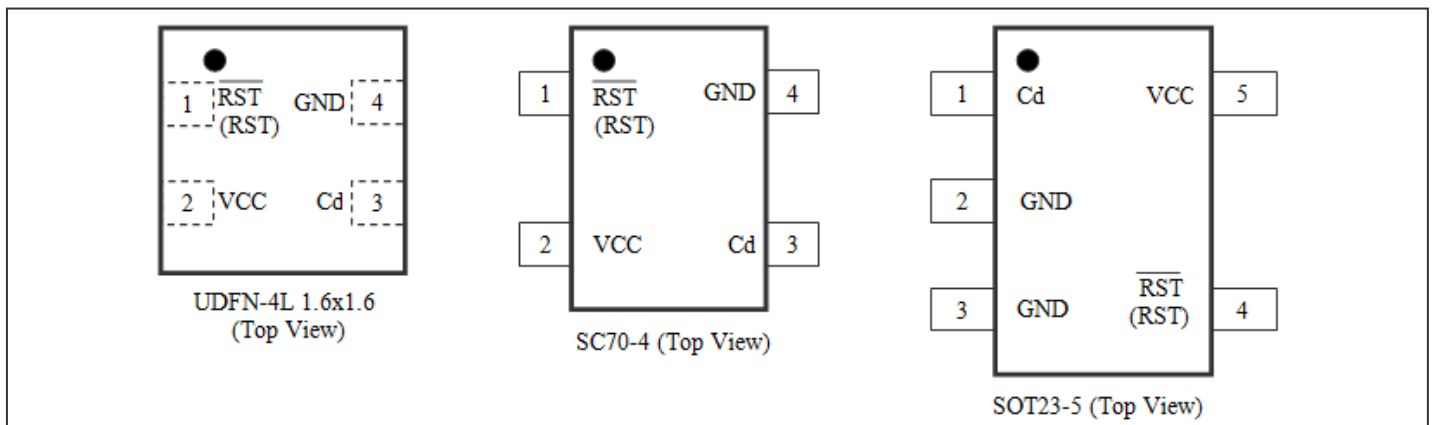
Description

The PT7M6518-6550 is a family of small, low-power, voltage-monitoring circuits with adjustable delay time capability. PT7M65xx series features a highly accurate under voltage detector with hysteresis and an externally programmable time delay generator. This combination of features prevents erratic system reset operation.

PT7M65xx series provide external capacitor to adjust for set up delay time.

All series operate from a 1.2V to 5.5V supply voltage and are fully specified over the -40 °C to +85 °C operating temperature range. This family is available in ultra-small 4-pin UDFN (1.6mm x 1.6mm) and SC70-4 and SOT23-5 packages.

Pin Configuration



Pin Description

Name	Type	Description
$\overline{\text{RST}}$	O	Active Low Reset Output: $\overline{\text{RST}}$ is asserted to LOW when V_{CC} drops below voltage threshold V_{TH-} value (PT7M65xxCL/NL). PT7M65xxCL output with push-pull. PT7M65xxNL output with open-drain which requires external pullup resistance.
RST	O	Active High Reset Output. RST is asserted High when V_{CC} drops below voltage threshold V_{TH-} voltage (PT7M65xxCH). PT7M65xxCH output with push-pull.
GND	P	Ground.
V_{CC}	P	Supply Voltage. Operation voltage from 1.2V to 5.5V. By pass 0.1µF ceramic capacitor to GND for noise decoupling.
Cd	I/O	Capacitor Delay. Adjustable. Connect an external capacitor from Cd pin to GND to set the Reset inactive delay time (timeout period) after V_{CC} rise over voltage threshold V_{TH+} . Do not short Cd pin to GND directly. The delay time equation as $t_{\text{delay}} = \text{Cd}(\mu\text{F}) \times 4 \times 10^6 \mu\text{s} + 40 \mu\text{s}$.

Table 1 Function comparison

Item	Part No.	Reset Output				Threshold
		Open-Drain		Push-Pull		
		Active high	Active low	Active high	Active low	
1	PT7M65xxCL	-	-	-	√	1.8V to 5.0V in 100mV increments
2	PT7M65xxCH	-	-	√	-	
3	PT7M65xxNL	-	√	-	-	

Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND)	-0.3V to +6.0V
DC Input Voltage (All inputs except V _{CC} and GND).....	-0.3V to V _{CC} +0.3V
DC Output Current (All outputs)	20mA
Power Dissipation	320mW (Depend on package)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

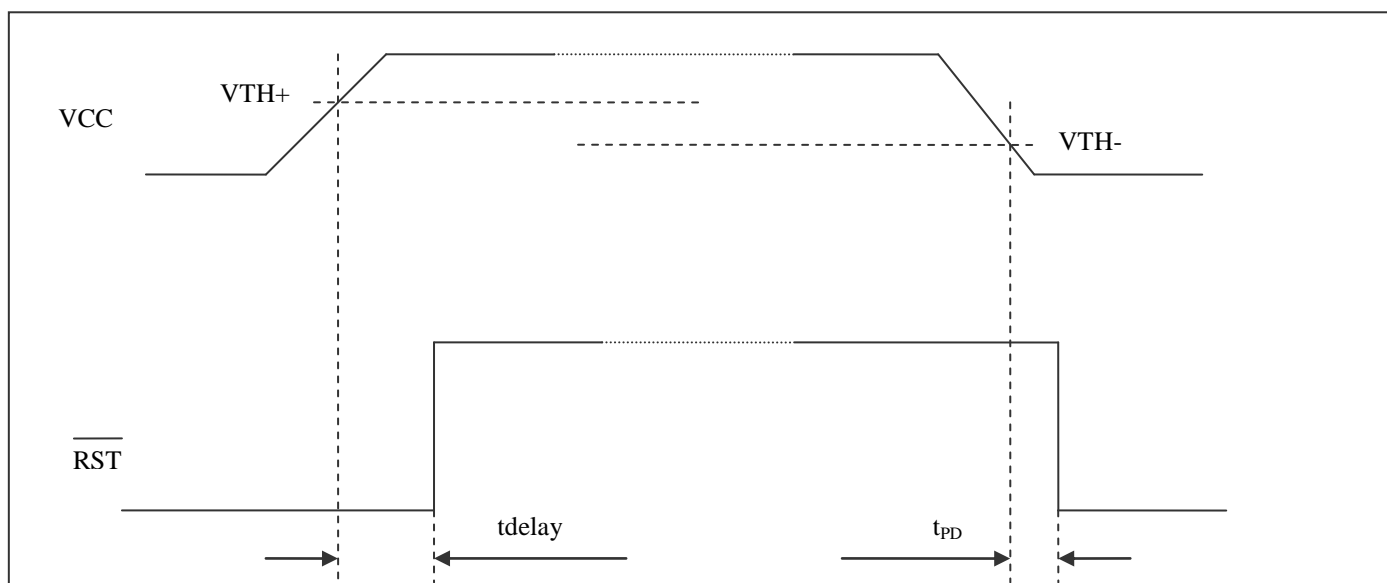
(V_{CC} = 1.2V to 5.5V, T_A = -40~85 °C, unless otherwise noted. Typical values are at T_A = +25 °C)

Description		Sym.	Test Conditions	Min	Typ.	Max.	Unit
Supply Voltage		V _{CC}	T _A = 0~70 °C	1.0	-	5.5	V
			T _A = -40~85 °C	1.2	-	5.5	
Supply Current		I _{CC}	V _{CC} = 3.6V. No load.	-	1.3	3.6	μA
			V _{CC} = 5V. No load.	-	2.0	5.0	μA
Output Driving	Output high (push-pull)	V _{OH}	V _{CC} ≥ 1.8V, I _{source} = 1mA	0.8×V _{CC}	-	-	V
			V _{CC} ≥ 2.5V, I _{source} = 3mA	0.8×V _{CC}	-	-	
			V _{CC} ≥ 4.5V, I _{source} = 8mA	0.8×V _{CC}	-	-	
	Output low (open-drain or push-pull)	V _{OL}	V _{CC} ≥ 1.2V, I _{sink} = 1mA	-	-	0.3	V
			V _{CC} ≥ 2.5V, I _{sink} = 4mA	-	-	0.3	
			V _{CC} ≥ 4.5V, I _{sink} = 9mA	-	-	0.4	
Open-Drain Output Leakage Current		I _{LKG}	-	-	-	1	μA
VCC Detect Voltage Threshold		V _{TH-}	+25°C	(V _{TH-}) × 0.985	V _{TH-}	(V _{TH-}) × 1.015	V
			-40°C~85°C	(V _{TH-}) × 0.975	V _{TH-}	(V _{TH-}) × 1.025	
		V _{TH+}	+25°C	(V _{TH+}) × 0.985	V _{TH+}	(V _{TH+}) × 1.015	
			-40°C~85°C	(V _{TH+}) × 0.975	V _{TH+}	(V _{TH+}) × 1.025	
Delay charge current		I _{cd}	-	200	250	300	nA
Delay voltage Threshold		V _{tcd}	C _{delay} rising	0.95	1.00	1.05	V
C _{delay} pulldown Resistance		R _{cdelay}	-	-	200	500	Ω

Note: V_{TH+} = 1.05 × V_{TH-}. V_{TH-} is voltage threshold when V_{CC} falls from high to low. V_{TH+} is voltage threshold when V_{CC} rises from low to high.

AC Electrical Characteristics

PT7M65xxNL Timing diagram



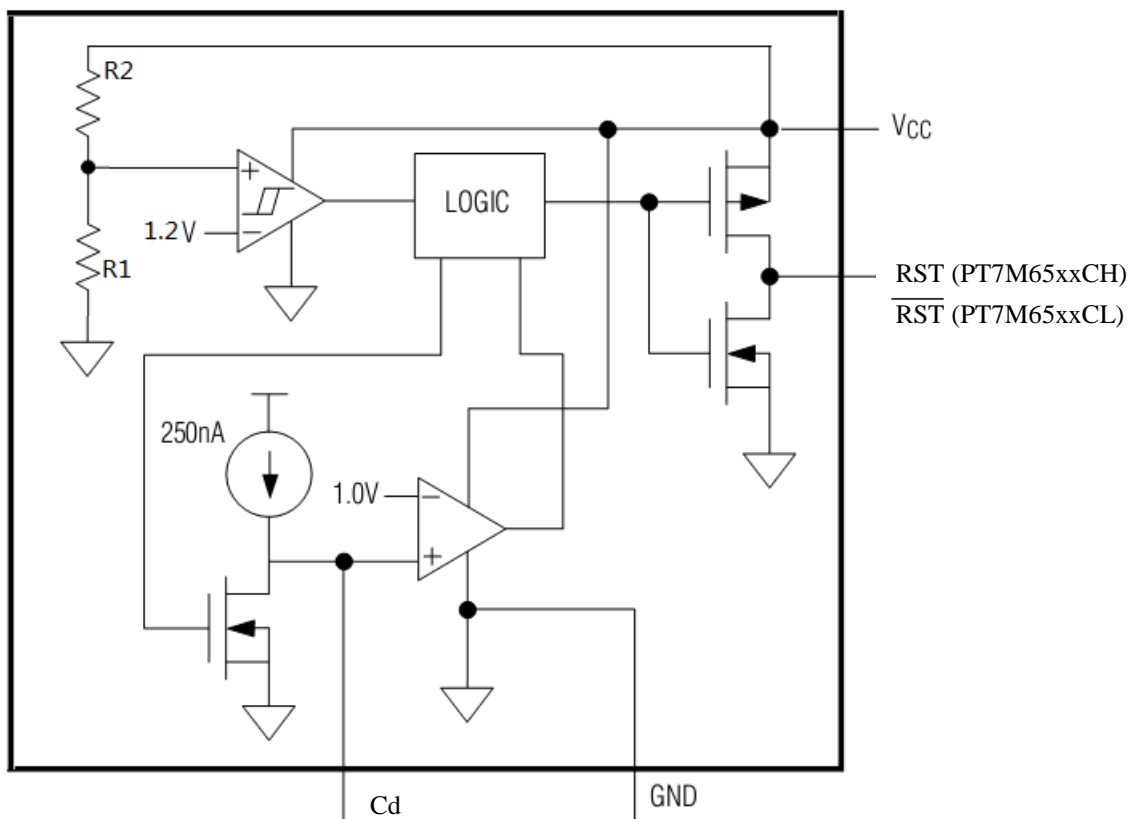
(V_{CC} = 1.2V to 5.5V, T_A = -40~85 °C, unless otherwise noted. Typical values are at T_A = +25 °C)

Sym.	Description	Test Conditions	Min.	Typ.	Max.	Unit
t _{PD}	Reset active Propagation Delay		-	50	-	μs
t _{delay}	Reset inactive delay time after VCC > V _{TH+} (Reset Timeout Period).		-	Cd(μF) × 4 × 10 ⁶ + 40	-	μs

Function Description

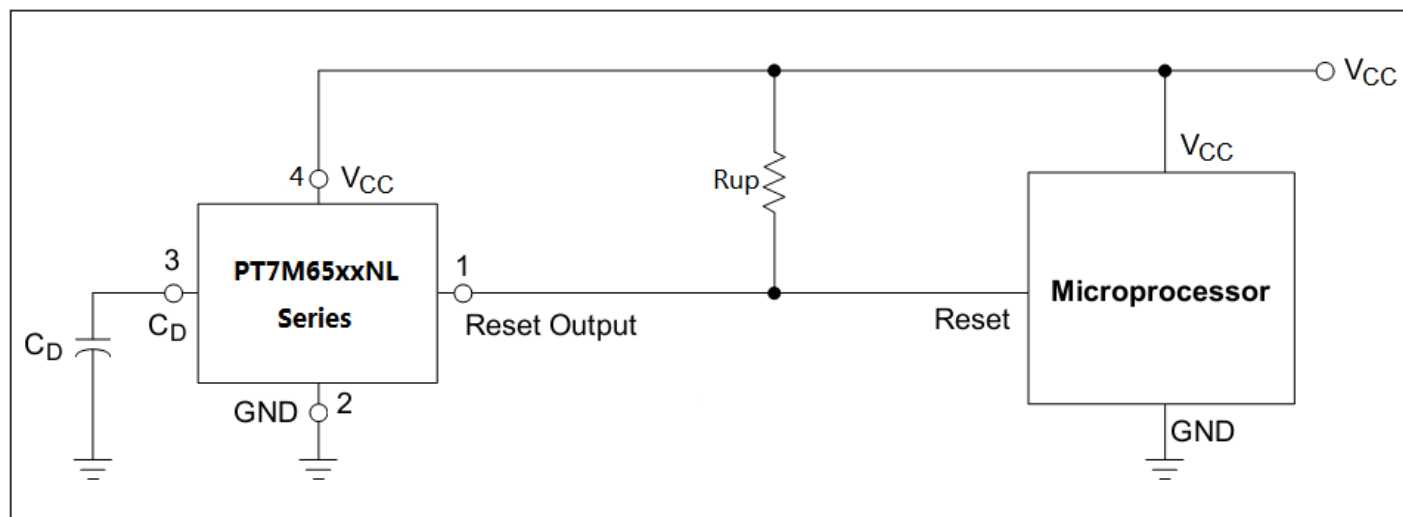
PT7M65xx has adjustable reset output delay time function through Cd pin with cap. Internal 250nA sourcing will charge the external cap through Cd pin when VCC is rise above V_{TH+}, and reset output will disalert after Cd pin voltage reaches 1V. This delay time is t_{delay} = Cd (μF) × 4 × 10⁶ μs + 40 μs. For example, if Cd = 1nF, the t_{delay} = 0.001 × 4 × 10⁶ μs + 40 μs = 4040 μs. Cd pin voltage will be discharged when reset output is assert ok at Vcc falls below V_{th-}, the discharge resistance is about 200Ω.

Block Diagram



Typical Operation Circuit

PT7M65xxNL Application Example



Note: Capacitor-Adjustable Delay application.

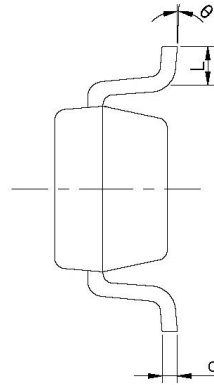
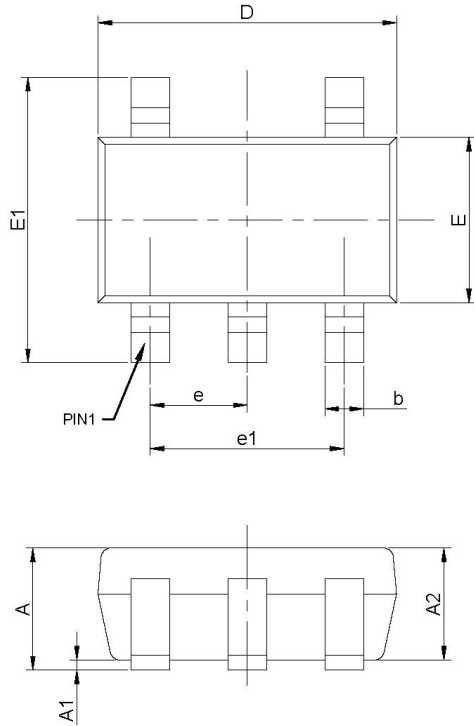
Connect an external capacitor (C_{cd}) from Cd to GND delay period.

$$t_{delay} = C_d(\mu f) \times 4 \times 10^6 \mu s + 40 \mu s$$

There is a fixed short delay ($40 \mu s$, typ.) for the output deasserting when V_{in} falls below V_{th} .

Mechanical Information:

TA5 (SOT23-5)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	1.50	1.70
E1	2.65	2.95
e	0.95 BSC	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°

Note:

1. Ref. JEDEC MO-178C/AA



DATE: 06/18/13

DESCRIPTION: 5-Pin, Small Outline Transistor Plastic Package (SOT23)

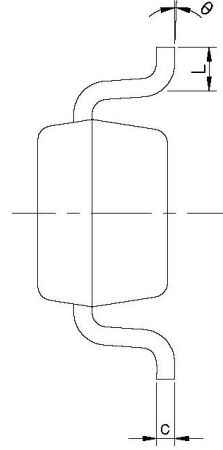
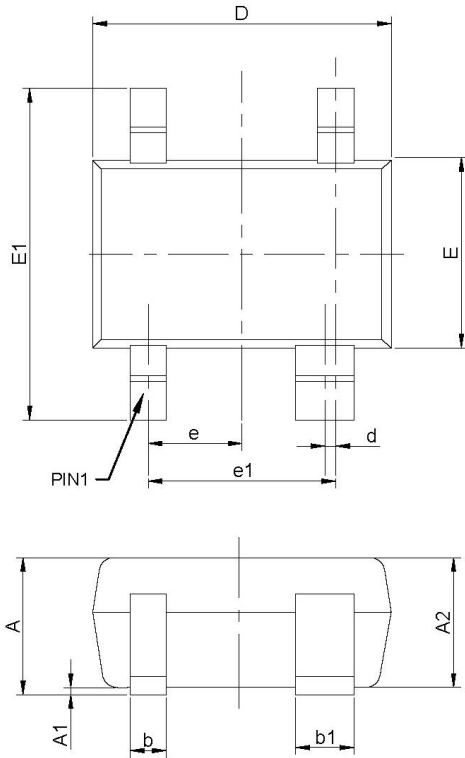
PACKAGE CODE: TA (TA5)

DOCUMENT CONTROL #: PD-2144

REVISION: --

13-0183

C4 (SC70-4)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.25	0.40
b1	0.35	0.50
c	0.08	0.15
D	2.00	2.20
d	0.05 TYP	
E	1.15	1.35
E1	2.15	2.45
e	0.65 TYP	
e1	1.20	1.40
L	0.26	0.46
θ	0°	8°

Notes:

1. Ref: JEDEC MO-203B



DATE: 06/18/13

DESCRIPTION: 4-Pin, SOT343 (SC70)

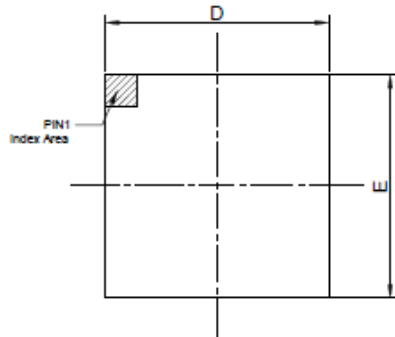
PACKAGE CODE: C (C4)

DOCUMENT CONTROL#: PD-2148

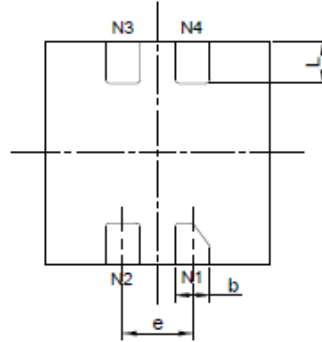
REVISION: --

13-0187

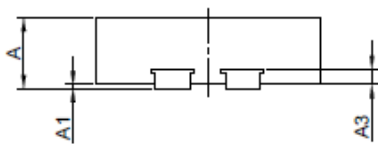
XV (UDFN1.6x1.6-4L)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.11 REF	
D	1.55	1.65
E	1.55	1.65
b	0.20	0.30
e	0.50 TYP	
L	0.25	0.35

Notes:
1. Ref. JEDEC MO-287A



DATE: 06/18/13

DESCRIPTION: 4-Pin, UDFN, 1.6X1.6, MIS

PACKAGE CODE: XV (XV4)

DOCUMENT CONTROL #: PD-2130

REVISION: --

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Part Number	Package Code	Package
PT7M65xxCLTA5E	TA5	Lead free and Green SOT23-5
PT7M65xxCLC4E	C4	Lead free and Green SC70-4
PT7M65xxCLXVE	XV	Lead Free and Green DFN1.6X1.6-4L
PT7M65xxNLTA5E	TA5	Lead free and Green SOT23-5
PT7M65xxNLXVE	XV	Lead Free and Green DFN1.6X1.6-4L
PT7M65xxNLC4E	C4	Lead free and Green SC70-4
*PT7M65xxCHTA5E	TA5	Lead free and Green SOT23-5
*PT7M65xxCHXVE	XV	Lead Free and Green DFN1.6X1.6-4L
*PT7M65xxCHC4E	C4	Lead free and Green SC70-4

Notes:

- “xx” refer to voltage range, see below table 2.
- E = Pb-Free and Green
- Adding X Suffix= Tape/Reel
- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- “*” for CH part, please check the storage with related sales.

Table 2 Suffix “xx” definition of PT7M65xx

Suffix xx	V _{TH-} (V)	Suffix xx	V _{TH-} (V)	Suffix xx	V _{TH-} (V)	Suffix xx	V _{TH-} (V)	Suffix xx	V _{TH-} (V)
18	1.8	25	2.5	32	3.2	39	3.9	46	4.6
19	1.9	26	2.6	33	3.3	40	4.0	47	4.7
20	2.0	27	2.7	34	3.4	41	4.1	48	4.8
21	2.1	28	2.8	35	3.5	42	4.2	49	4.9
22	2.2	29	2.9	36	3.6	43	4.3	50	5.0
23	2.3	30	3.0	37	3.7	44	4.4		
24	2.4	31	3.1	38	3.8	45	4.5		

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