## 1. General description

The 74ABT00 is a quad 2-input NAND gate. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

### 2. Features and benefits

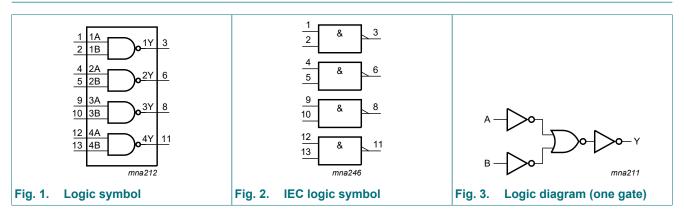
- Supply voltage range from 4.5 V to 5.5 V
- · BiCMOS high speed and output drive
- · Direct interface with TTL levels
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

**Table 1. Ordering information** 

Type number	Package	Package							
	Temperature range	Name	Description	Version					
74ABT00D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1					
74ABT00PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					

## 4. Functional diagram

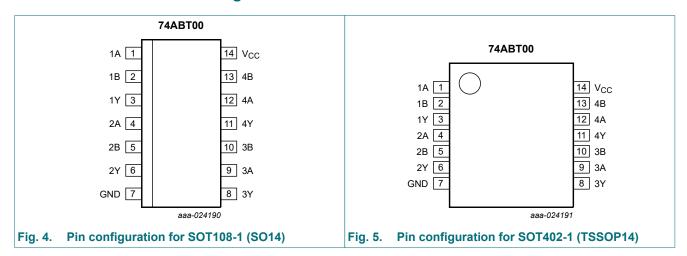




**Quad 2-input NAND gate** 

# 5. Pinning information

### 5.1. Pinning



## 5.2. Pin description

### Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

# 6. Functional description

### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input	Output	
nA	nB	nY
L	X	Н
X	L	Н
Н	Н	L

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**Quad 2-input NAND gate** 

# 7. Limiting values

### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-1.2	+7.0	V
Vo	output voltage	output HIGH or LOW [1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	40	mA
Tj	junction temperature		-	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

### **Table 5. Operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-15	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	20	mA
Δt/ΔV	input transition rise and fall rate		0	-	5	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

**Quad 2-input NAND gate** 

## 9. Static characteristics

**Table 6. Static characteristics** 

Symbol	Parameter	Conditions			25 °C		-40 °C to	o +85 °C	Unit
			ı	Min	Тур	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-1.2	-0.9	-	-1.2	-	V
V <sub>OH</sub>	HIGH-level output voltage	$V_{CC}$ = 4.5 V; $I_{OH}$ = -15 mA; $V_{I}$ = $I_{IL}$ or $V_{IH}$		2.5	2.9	-	2.5	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_{CC}$ = 4.5 V; $I_{OL}$ = 20 mA; $V_I$ = $V_{IL}$ or $V_{IH}$		-	0.35	0.5	-	0.5	V
I <sub>I</sub>	input leakage current	$V_{CC} = 5.5 \text{ V}; V_{I} = \text{GND or } 5.5 \text{ V}$		-	±0.01	±1.0	-	±1.0	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μΑ
I <sub>CEX</sub>	output high leakage current	HIGH-state; $V_O$ = 5.5 V; $V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$		-	5.0	50	-	50	μA
Io	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	1]	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	supply current	$V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$		-	2	50	-	50	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V; other inputs at V <sub>CC</sub> or GND	2]	-	0.25	500	-	500	μA
Cı	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>		-	3	-	-	-	pF

<sup>[1]</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# 10. Dynamic characteristics

**Table 7. Dynamic characteristics** 

GND = 0 V; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	25 °	C; V <sub>CC</sub> = (	5.0 V	-40 °C to V <sub>CC</sub> = 5.0	Unit	
			Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA, nB to nY; see Fig. 6	1.0	2.5	3.6	1.0	4.1	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA, nB to nY; see Fig. 6	1.0	2.0	2.8	1.0	3.4	ns
t <sub>sk(o)</sub>	output skew time	[1]	-	0.4	0.5	-	0.5	ns

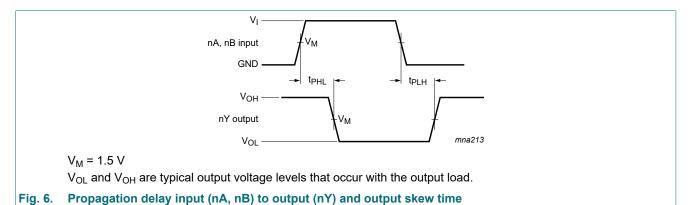
<sup>[1]</sup> Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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<sup>[2]</sup> This is the increase in supply current for each input at 3.4 V.

### **Quad 2-input NAND gate**

### 10.1. Waveforms and test circuit



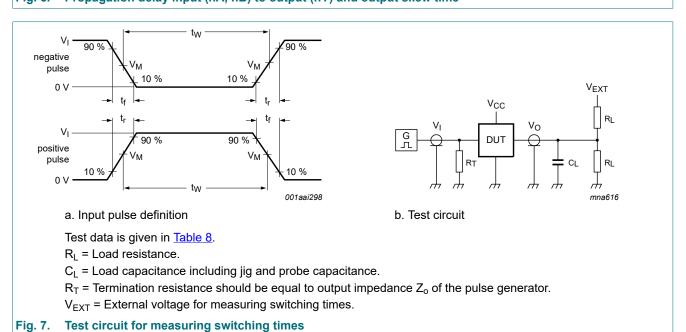


Table 8. Test data

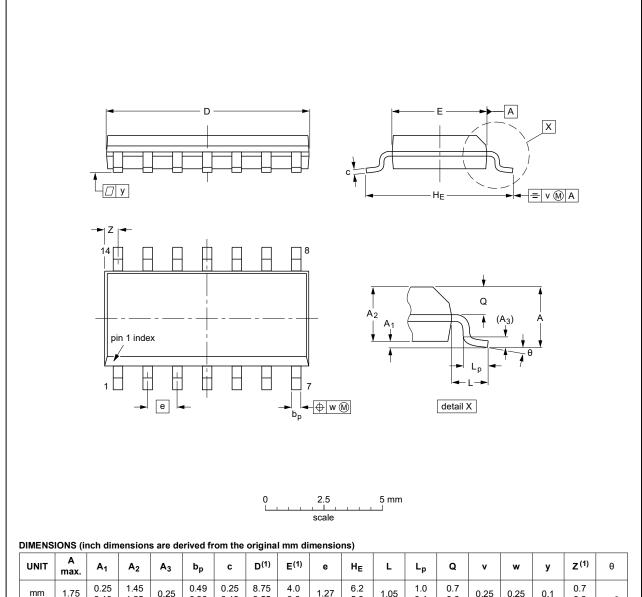
Input			Load	V <sub>EXT</sub>		
V <sub>I</sub>	f <sub>i</sub>	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open

**Quad 2-input NAND gate** 

# 11. Package outline

### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

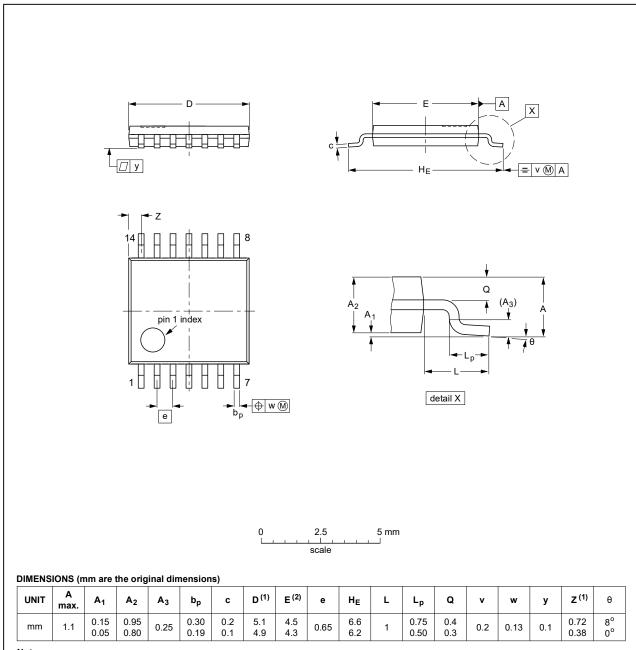
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012			<del>99-12-27</del> 03-02-19

Package outline SOT108-1 (SO14)

### **Quad 2-input NAND gate**

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



## Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT402-1		MO-153			<del>99-12-27</del> 03-02-18	

Fig. 9. Package outline SOT402-1 (TSSOP14)

**Quad 2-input NAND gate** 

## 12. Abbreviations

### **Table 9. Abbreviations**

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 13. Revision history

### Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74ABT00 v.4	20201005	Product data sheet	-	74ABT00 v.3	
Modifications:	guidelines c  Legal texts  Section 1 a	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Type number 74ABT00DB (SOT337-1 / SSOP14) removed.</li> </ul>			
74ABT00 v.3	20160811	Product data sheet	-	74ABT00 v.2	
Modifications:	guidelines o	the format of this data sheet has been redesigned to comply with the new identity uidelines of NXP Semiconductors.  egal texts have been adapted to the new company name where appropriate.			
74ABT00 v.2	19950918	Product specification	-	-	

### **Quad 2-input NAND gate**

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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