

Features

- ★ Super Low Gate Charge
- ★ Green Device Available
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology
- ★ 100% EAS Guaranteed

Product Summary

RoHS

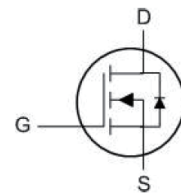
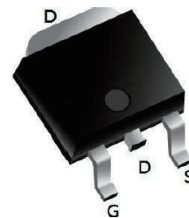
BVDSS	RDS(ON)	ID
100V	13.5mΩ	60A

Description

The S60N10 is the highest performance trench Nc-h MOSFETs with extreme high cell density, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications .

The S60N10 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units	
V _{DSS}	Drain-Source Voltage	100	V	
V _{GSS}	Gate-Source Voltage	±20	V	
I _D	Continuous Drain Current	T _C = 25°C	60	A
		T _C = 100°C	28.5	A
I _{DM}	Pulsed Drain Current <small>note1</small>	180	A	
EAS	Single Pulsed Avalanche Energy <small>note2</small>	80	mJ	
P _D	Power Dissipation	T _C = 25°C	67.5	W
R _{θJC}	Thermal Resistance from Junction-to-Lead	1.85	°C/W	
R _{θJA}	Thermal Resistance from Junction-to-Ambient <small>note3</small>	45	°C/W	
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to 150	°C	

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Static Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	-	-	1	μA
		$T_J = 100^\circ\text{C}$	-	-	100	
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	2.5	V
$R_{DS(on)}$	Drain-Source on-Resistance ⁴	$V_{GS} = 10V, I_D = 20A$	-	13.5	17	m Ω
		$V_{GS} = 4.5V, I_D = 10A$	-	17	20	
g_{fs}	Forward Transconductance ⁴	$V_{DS} = 10V, I_D = 20A$	-	54	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	1208	-	μF
C_{oss}	Output Capacitance		-	144	-	
C_{rss}	Reverse Transfer Capacitance		-	11.3	-	
R_G	Gate Resistance	$f = 1\text{MHz}$	-	1.8	-	Ω
Switching Characteristics						
Q_g	Total Gate Charge	$V_{GS} = 10V, V_{DS} = 50V,$ $I_D = 20A$	-	22.7	-	nC
Q_{gs}	Gate-Source Charge		-	3	-	
Q_{gd}	Gate-Drain Charge		-	5	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 10V, V_{DD} = 50V,$ $R_G = 3\Omega, I_D = 20A$	-	9.2	-	ns
t_r	Rise Time		-	3.6	-	
$t_{d(off)}$	Turn-off Delay Time		-	25.6	-	
t_f	Fall Time		-	4.4	-	
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 20A,$	-	30	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$dI/dt = 100A/\mu s$	-	42	-	nC
Drain-Source Body Diode Characteristics						
V_{SD}	Diode Forward Voltage ⁴	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V
I_S	Continuous Source Current	-	-	-	60	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.4\text{mH}, I_{AS} = 20A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

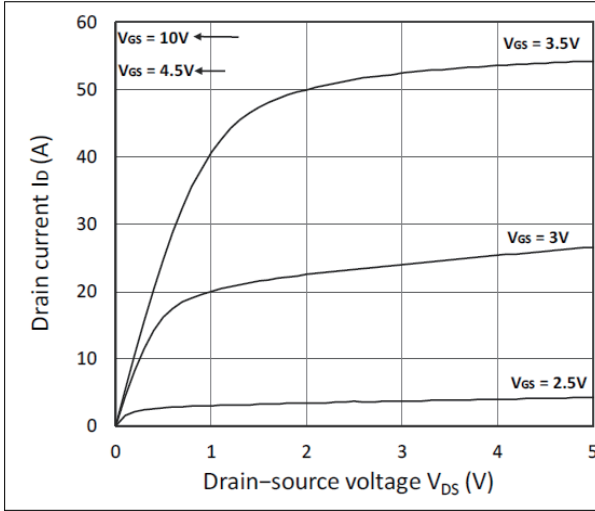


Figure 2: Typical Transfer Characteristics

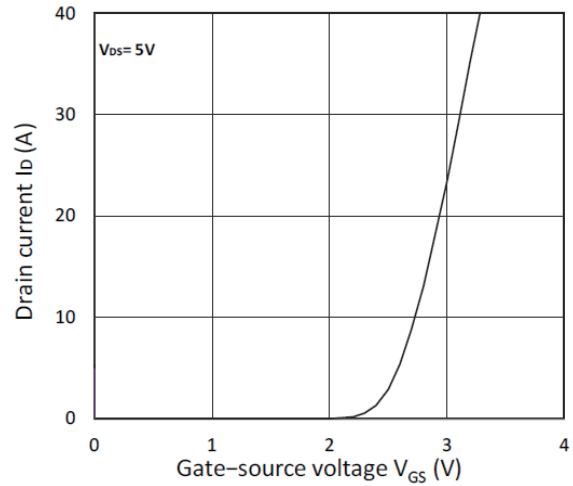


Figure 3: Forward Characteristics of Reverse

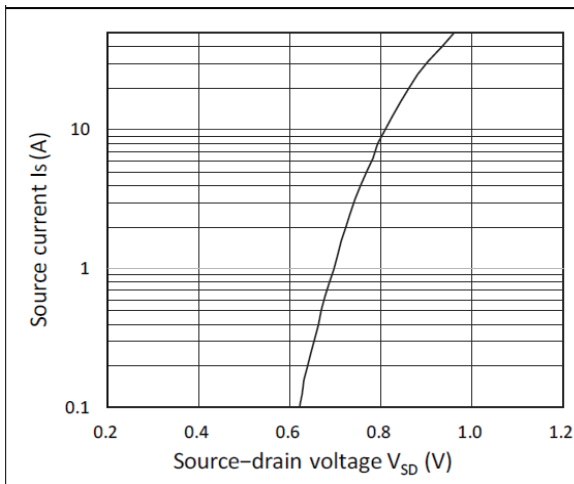


Figure 4: RDS(ON) vs. VGS

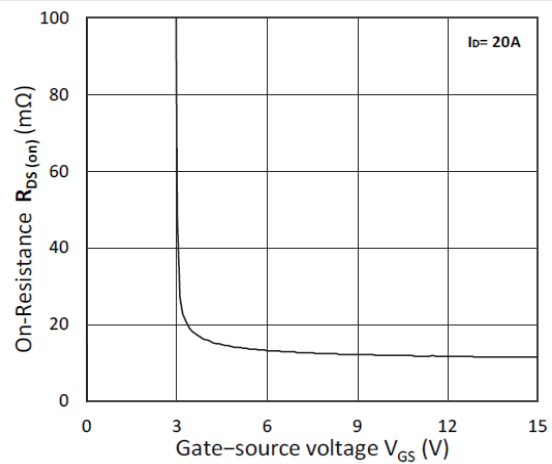
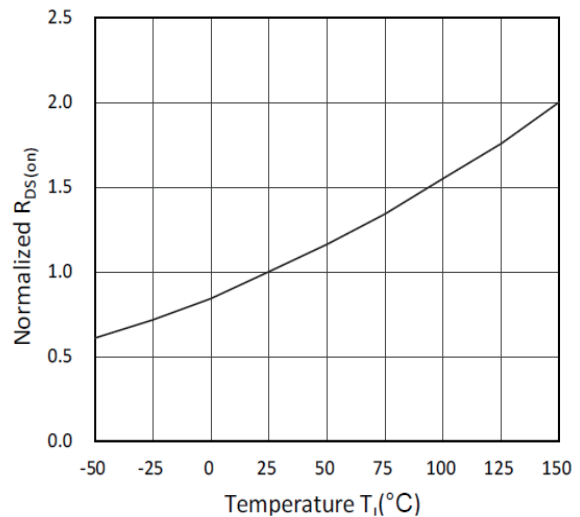
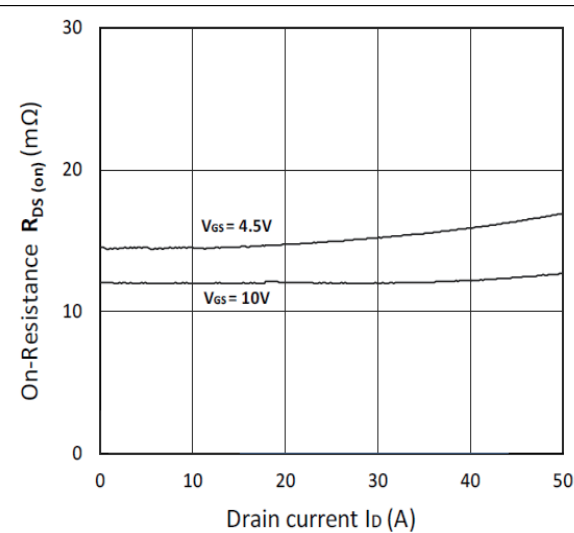


Figure 5: RDS(ON) vs. ID Figure 6. Normalized

Figure 6: Normalized RDS(on) vs. Temperature



Typical Performance Characteristics

Figure 7: Capacitance Characteristics

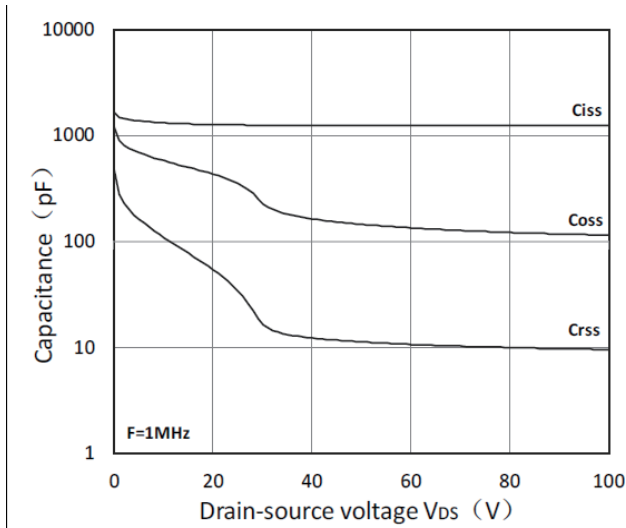


Figure 8: Gate Charge Characteristics

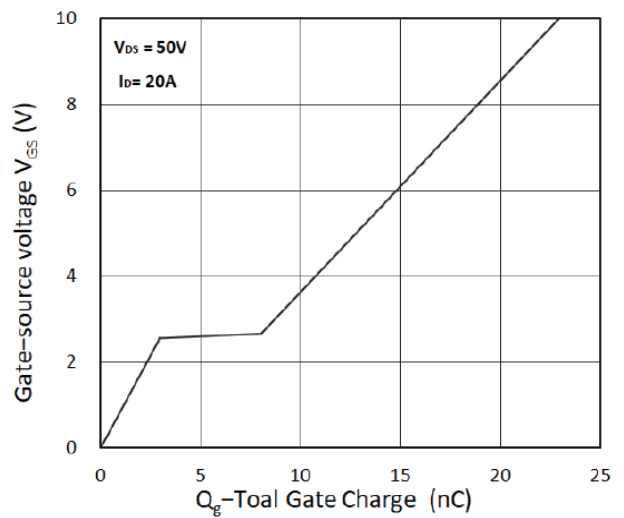


Figure 9: Power Dissipation

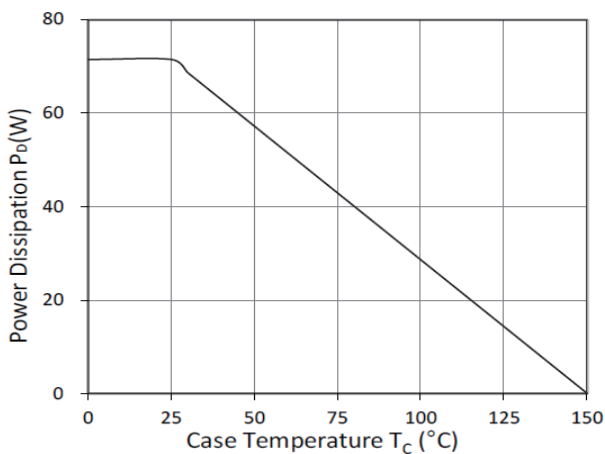


Figure 10: Safe Operating Area

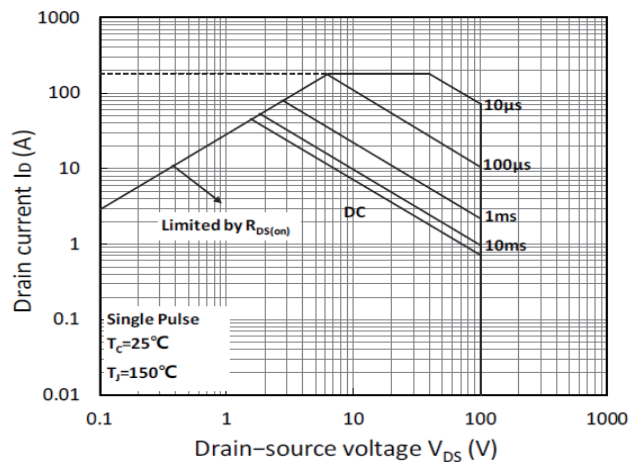
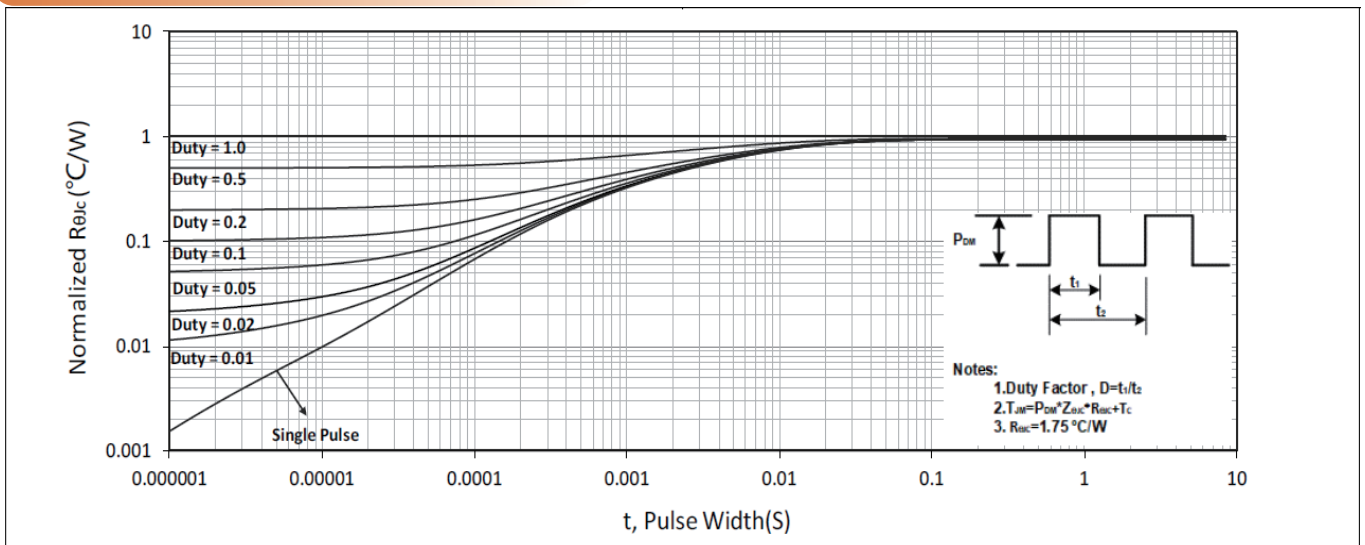


Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit

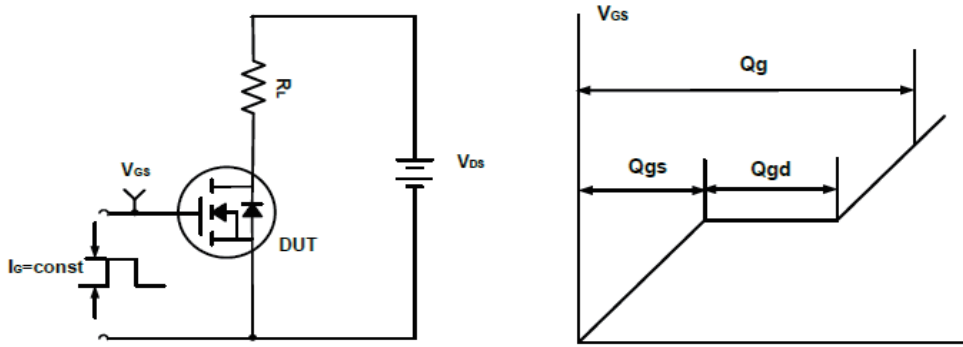


Figure A. Gate Charge Test Circuit & Waveforms

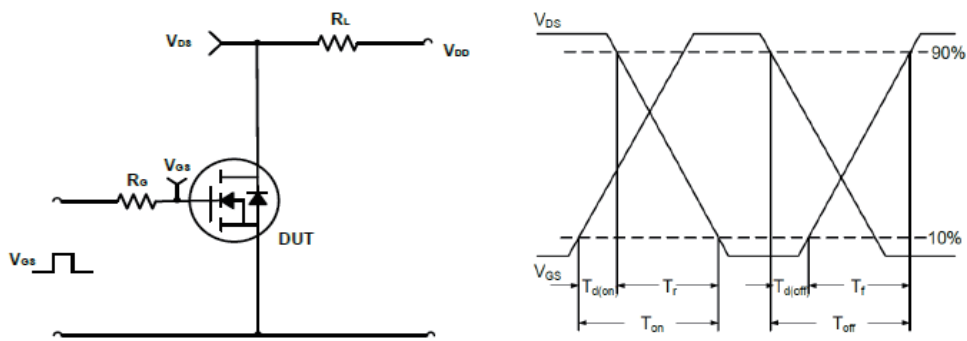


Figure B. Switching Test Circuit & Waveforms

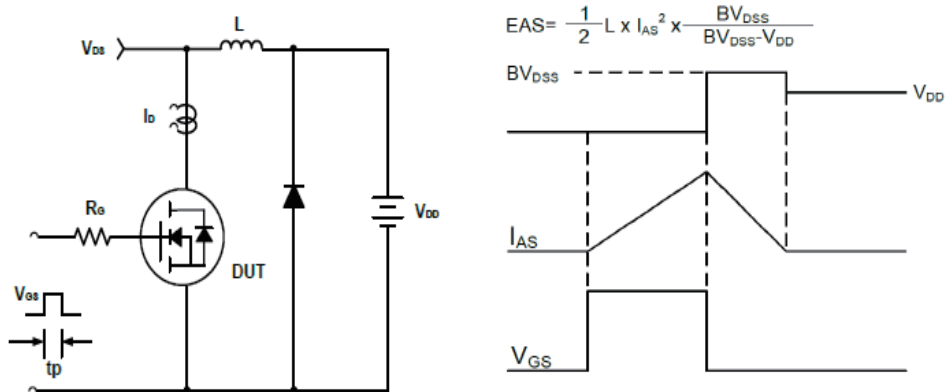
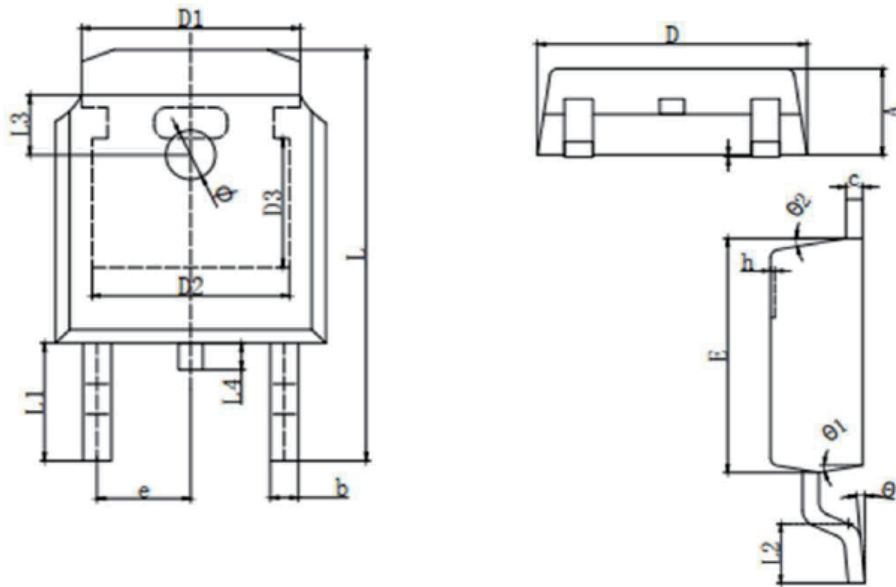


Figure C. Unclamped Inductive Switching Circuit & Waveforms

TO-252 Package outline



SYMBOL	MILLIMETER		SYMBOL	MILLIMETER	
	MIN	MAX		MIN	MAX
A	2.200	2.400	h	0.000	0.200
A1	0.000	0.127	L	9.900	10.30
b	0.640	0.740	L1	2.888 REF	
c	0.460	0.580	L2	1.400	1.700
D	6.500	6.700	L3	1.600 REF	
D1	5.334 REF		L4	0.600	1.000
D2	4.826 REF		φ	1.100	1.300
D3	3.166 REF		θ	0°	8°
E	6.000	6.200	θ 1	9° TYP2	
e	2.286 TYP		θ 2	9° TYP	