NL17SH125

Non-Inverting 3-State Buffer

The NL17SH125 MiniGate[™] is an advanced high-speed CMOS non-inverting buffer in ultra-small footprint.

The NL17SH125 requires the 3-state control input (\overline{OE}) to be set High to place the output in the high impedance state.

The NL17SH125 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.8 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1.0 \ \mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- These are Pb–Free and Halide–Free Devices



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http://onsemi.com

MARKING DIAGRAM



Т



= Specific Device Code

SOT-953

(Rotated 90°) Month Code

PIN ASSIGNMENT					
1	IN A				
2	GND				
3	OE				
4	OUT Y				
5	V _{CC}				

FUNCTION TABLE

Input A	Input OE	Output Y
L	L	L
н	L	н
x	н	z

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

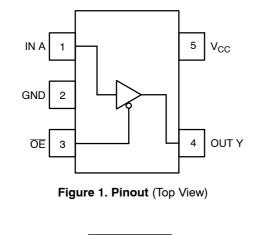




Figure 2. Logic Symbol

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{IN}	DC Input Voltage		-0.5 to +7.0	V
V _{OUT}	DC Output Voltage		–0.5 to V _{CC} + 0.5	V
Ι _{ΙΚ}	DC Input Diode Current	V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current V _{OUT}	< GND, V _{OUT} > V _{CC}	±20	mA
I _{OUT}	DC Output Source/Sink Current		±12.5	mA
I _{CC}	DC Supply Current per Supply Pin		±25	mA
I _{GND}	DC Ground Current per Ground Pin		±25	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
TJ	Junction Temperature Under Bias		+150	°C
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating Ox	ygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	Mad	Body Model (Note 2) chine Model (Note 3) evice Model (Note 4)	>3000 >150 N/A	V
ILATCHUP	Latchup Performance Above V _{CC} and Below GN	ID at 125°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability. 1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.

Tested to EIA/JESD22-A114-A.
Tested to EIA/JESD22-A115-A.

Tested to JESD22–C101–A.
Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V	
V _{IN}	Digital Input Voltage	0.0	5.5	V	
V _{OUT}	Output Voltage		0.0	V _{CC}	V
T _A	Operating Temperature Range		-55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fail Rate	$V_{\rm CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{\rm CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0	100 20	ns/V

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DC ELECTRICAL CHARACTERISTICS

			V _{cc}	1	Γ _A = 25°	С	$T_A \le 85^{\circ}C$		-55°C to 125°C		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	High-Level Input Voltage		1.65 to 2.0	0.75 x V _{CC}			0.75 x V _{CC}				V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}				
V _{IL}	Low-Level Input Voltage		1.65 to 2.0			0.25 x V _{CC}		0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 to 5.5			0.30 x V _{CC}		0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \ \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V _{OL}	Low-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \ \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I _{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5 \ V$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I _{CC}	Quiescent Supply Current	$0 \leq V_{IN} \leq V_{CC}$	5.5			1.0		10		40	μΑ
I _{OZ}	3-State Leakage Current	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	0.0			±0.25		±2.5		±2.5	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

		V _{CC}	Test	٦	r _A = 25°0	2	T _A ≤	85°C	−55°C t	o 125°C	
Symbol	Parameter	(V)	Conditions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Propagation Delay, A to Y	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0		12.0 16.0	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5		8.5 10.5	
t _{PZL} , t _{PZH}	Output Enable Time, OE to Y	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0		11.5 15.0	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0		7.5 9.5	
t _{PLZ} , t _{PHZ}	Output Enable Time, OE to Y	3.0 to 3.6	C _L = 15 pF C _L = 50 pF		6.5 8.0	9.7 13.2	1.0 1.0	11.5 15.0		14.5 18.5	ns
		4.5 to 5.5	C _L = 15 pF C _L = 50 pF		4.8 7.0	6.8 8.8	1.0 1.0	8.0 10		10.0 12.0	
C _{IN}	Input Capacitance				5.5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	5.0			11						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

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ORDERING INFORMATION

Device	Package	Shipping [†]
NL17SH125P5T5G	SOT-953 (Pb-Free)	8000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

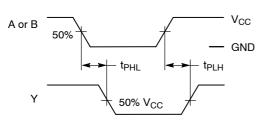
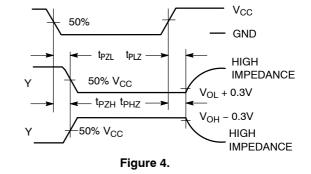
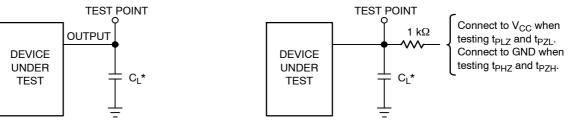


Figure 3. Switching Waveform





*Includes all probe and jig capacitance.

Figure 5. Test Circuit

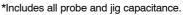


Figure 6. Test Circuit

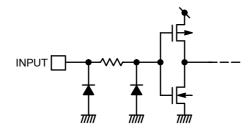


Figure 7. Input Equivalent Circuit

MiniGate is a trademark of Semiconductor Components Industries, LLC (SCILLC).

SCALE 4:1

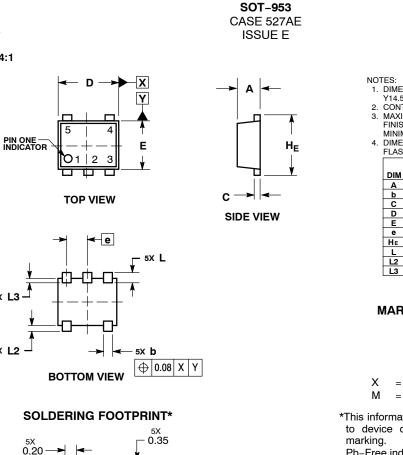
5X L3

5X L2

PACKAGE OUTLINE

0.35 PITCH





DATE 02 AUG 2011

NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL. 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	МІ	LIMETE	RS				
DIM	MIN NOM MAX						
Α	0.34	0.37	0.40				
b	0.10	0.15	0.20				
С	0.07	0.12	0.17				
D	0.95	1.00	1.05				
E	0.75	0.80	0.85				
е		0.35 BS	С				
ΗE	0.95	1.00	1.05				
L	(0.175 RE	F				
L2	0.05	0.10	0.15				
L3			0.15				

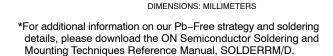
GENERIC **MARKING DIAGRAM***

= Specific Device Code

= Month Code

*This information is generic. Please refer to device data sheet for actual part

Pb-Free indicator, "G" or microdot " .", may or may not be present.



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