

Dual N-Channel 80 V (D-S) MOSFETs



FEATURES

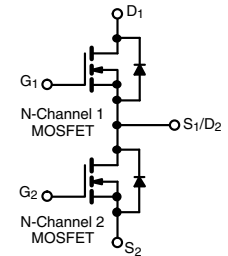
- TrenchFET® Gen IV power MOSFETs
- 100 % R_g and UIS tested
- Integrated MOSFET half bridge power stage
- Optimized Q_{gs}/Q_{gs} ratio improves switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- POL
- Synchronous buck converter
- Telecom DC/DC
- Resonant converters
- Motor drive control



| PRODUCT SUMMARY | | |
|---|-----------|-----------|
| | CHANNEL-1 | CHANNEL-2 |
| V _{DS} (V) | 80 | 80 |
| R _{DS(on)} max. (Ω) at V _{GS} = 10 V | 0.0245 | 0.0247 |
| R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V | 0.0310 | 0.0310 |
| Q _g typ. (nC) | 6.2 | 6.3 |
| I _D (A) ^a | 24.7 | 24.6 |
| Configuration | Dual | |

| ORDERING INFORMATION | |
|---------------------------------|------------------|
| Package | PowerPAIR 3 x 3S |
| Lead (Pb)-free and halogen-free | SiZ260DT-T1-GE3 |

| ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted) | | | | | |
|---|-----------------------------------|------------------------|---------------------|---------------------|---|
| PARAMETER | SYMBOL | CHANNEL-1 | CHANNEL-2 | UNIT | |
| Drain-source voltage | V _{DS} | 80 | 80 | V | |
| Gate-source voltage | V _{GS} | ± 20 | ± 20 | | |
| Continuous drain current (T _J = 150 °C) | I _D | T _C = 25 °C | 24.7 ^a | 24.6 ^a | A |
| | | T _C = 70 °C | 19.8 | 19.7 | |
| | | T _A = 25 °C | 8.9 ^{b, c} | 8.9 ^{b, c} | |
| | | T _A = 70 °C | 7.2 ^{b, c} | 7.1 ^{b, c} | |
| Pulsed drain current (100 μs pulse width) | I _{DM} | 60 | 60 | | |
| Continuous source drain diode current | I _S | T _C = 25 °C | 27 | 27 | |
| | | T _A = 25 °C | 3.6 ^{b, c} | 3.6 ^{b, c} | |
| Single pulse avalanche current | I _{AS} | 12 | 12 | | |
| Single pulse avalanche energy | E _{AS} | 7.2 | 7.2 | mJ | |
| Maximum power dissipation | P _D | T _C = 25 °C | 33 | 33 | W |
| | | T _C = 70 °C | 21 | 21 | |
| | | T _A = 25 °C | 4.3 ^{b, c} | 4.3 ^{b, c} | |
| | | T _A = 70 °C | 2.8 ^{b, c} | 2.8 ^{b, c} | |
| Operating junction and storage temperature range | T _J , T _{stg} | -55 to +150 | | °C | |
| Soldering recommendations (peak temperature) ^d | | 260 | | | |

| THERMAL RESISTANCE RATINGS | | | | | | |
|---|-------------------|-----------|------|-----------|------|------|
| PARAMETER | SYMBOL | CHANNEL-1 | | CHANNEL-2 | | UNIT |
| | | TYP. | MAX. | TYP. | MAX. | |
| Maximum junction-to-ambient ^{b, f} | R _{thJA} | 23 | 29 | 23 | 29 | °C/W |
| Maximum junction-to-case (drain) | R _{thJC} | 3 | 3.8 | 3 | 3.8 | |

Notes

- T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 64 °C/W for channel-1 and 64 °C/W for channel-2



| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | | |
|---|--------------------------------------|--|---|------|--------|--------|-------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | | |
| Static | | | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | Ch-1 | 80 | - | - | V | |
| | | V _{GS} = 0 V, I _D = 250 μA | Ch-2 | 80 | - | - | | |
| V _{DS} Temperature coefficient | ΔV _{DS} /T _J | I _D = 250 μA | Ch-1 | - | 63 | - | mV/°C | |
| | | I _D = 250 μA | Ch-2 | - | 60 | - | | |
| V _{GS(th)} Temperature coefficient | ΔV _{GS(th)} /T _J | I _D = 250 μA | Ch-1 | - | -4.8 | - | | |
| | | I _D = 250 μA | Ch-2 | - | -5.4 | - | | |
| Gate threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | Ch-1 | 1.1 | - | 2.4 | V | |
| | | V _{DS} = V _{GS} , I _D = 250 μA | Ch-2 | 1.1 | - | 2.4 | | |
| Gate source leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | Ch-1 | - | - | ± 100 | nA | |
| | | V _{DS} = 0 V, V _{GS} = ± 20 V | Ch-2 | - | - | ± 100 | | |
| Zero gate voltage drain current | I _{DSS} | V _{DS} = 80 V, V _{GS} = 0 V | Ch-1 | - | - | 1 | μA | |
| | | V _{DS} = 80 V, V _{GS} = 0 V | Ch-2 | - | - | 1 | | |
| | | V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C | Ch-1 | - | - | 5 | | |
| | | V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C | Ch-2 | - | - | 5 | | |
| On-state drain current ^b | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 10 V | Ch-1 | 10 | - | - | A | |
| | | V _{DS} ≥ 5 V, V _{GS} = 10 V | Ch-2 | 10 | - | - | | |
| Drain-source on-state resistance ^b | R _{DS(on)} | V _{GS} = 10 V, I _D = 10 A | Ch-1 | - | 0.0204 | 0.0245 | Ω | |
| | | V _{GS} = 10 V, I _D = 10 A | Ch-2 | - | 0.0206 | 0.0247 | | |
| | | V _{GS} = 4.5 V, I _D = 7 A | Ch-1 | - | 0.0243 | 0.0310 | | |
| | | V _{GS} = 4.5 V, I _D = 7 A | Ch-2 | - | 0.0246 | 0.0310 | | |
| Forward transconductance ^b | g _{fs} | V _{DS} = 10 V, I _D = 10 A | Ch-1 | - | 85 | - | S | |
| | | V _{DS} = 10 V, I _D = 10 A | Ch-2 | - | 25 | - | | |
| Dynamic ^a | | | | | | | | |
| Input capacitance | C _{iss} | Channel-1 V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz Channel-2 V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz | Ch-1 | - | 820 | - | pF | |
| | | | Ch-2 | - | 820 | - | | |
| Output capacitance | C _{oss} | | Ch-1 | - | 95 | - | pF | |
| | | | Ch-2 | - | 90 | - | | |
| Reverse transfer capacitance | C _{rss} | | Ch-1 | - | 10 | - | pF | |
| | | | Ch-2 | - | 10 | - | | |
| C _{rss} /C _{iss} ratio | | | Ch-1 | - | - | 0.024 | | |
| | | | Ch-2 | - | - | 0.024 | | |
| Total gate charge | Q _g | | V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A | Ch-1 | - | 13.1 | 27 | nC |
| | | | V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A | Ch-2 | - | 13.3 | 27 | |
| | | V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A | Ch-1 | - | 6.2 | 13 | | |
| | | V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A | Ch-2 | - | 6.3 | 13 | | |
| Gate-source charge | Q _{gs} | Channel-1 V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A | Ch-1 | - | 2.7 | - | nC | |
| | | | Ch-2 | - | 2.7 | - | | |
| Gate-drain charge | Q _{gd} | Channel-2 V _{DS} = 40 V, V _{GS} = 4.5 V, I _D = 10 A | Ch-1 | - | 1.78 | - | nC | |
| | | | Ch-2 | - | 1.9 | - | | |
| Output charge | Q _{oss} | V _{DS} = 40 V, V _{GS} = 0 V | Ch-1 | - | 12 | - | nC | |
| | | | Ch-2 | - | 12 | - | | |
| Gate resistance | R _g | f = 1 MHz | Ch-1 | 0.26 | 1.3 | 2.6 | Ω | |
| | | | Ch-2 | 0.2 | 1 | 2 | | |



| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | | |
|---|---------------------|---|------|------|------|------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
| Dynamic ^a | | | | | | | |
| Turn-on delay time | t _{d(on)} | Channel-1 V _{DD} = 40 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω | Ch-1 | - | 11 | 20 | ns |
| | | | Ch-2 | - | 12 | - | |
| Rise time | t _r | | Ch-1 | - | 6 | 12 | |
| | | | Ch-2 | - | 6 | 12 | |
| Turn-off delay time | t _{d(off)} | Channel-2 V _{DD} = 40 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω | Ch-1 | - | 25 | 50 | |
| | | | Ch-2 | - | 23 | 45 | |
| Fall time | t _f | | Ch-1 | - | 6 | 12 | |
| | | | Ch-2 | - | 5 | 10 | |
| Turn-on delay time | t _{d(on)} | Channel-1 V _{DD} = 40 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω | Ch-1 | - | 20 | 40 | |
| | | | Ch-2 | - | 20 | 40 | |
| Rise time | t _r | | Ch-1 | - | 55 | 110 | |
| | | | Ch-2 | - | 42 | 80 | |
| Turn-off delay time | t _{d(off)} | Channel-2 V _{DD} = 40 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω | Ch-1 | - | 24 | 48 | |
| | | | Ch-2 | - | - | 50 | |
| Fall time | t _f | | Ch-1 | - | 25 | 50 | |
| | | | Ch-2 | - | 20 | 40 | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I _S | T _C = 25 °C | Ch-1 | - | - | 27 | A |
| | | | Ch-2 | - | - | 27 | |
| Pulse diode forward current (t = 100 μs) | I _{SM} | | Ch-1 | - | - | 60 | |
| | | | Ch-2 | - | - | 60 | |
| Body diode voltage | V _{SD} | I _S = 5 A, V _{GS} = 0 V | Ch-1 | - | 0.8 | 1.2 | V |
| | | I _S = 5 A, V _{GS} = 0 V | Ch-2 | - | 0.8 | 1.2 | |
| Body diode reverse recovery time | t _{rr} | Channel-1 I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C | Ch-1 | - | 27 | 54 | ns |
| | | | Ch-2 | - | 28 | 56 | |
| Body diode reverse recovery charge | Q _{rr} | Channel-2 I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C | Ch-1 | - | 24 | 48 | nC |
| | | | Ch-2 | - | 29 | 58 | |
| Reverse recovery fall time | t _a | | Ch-1 | - | 17 | - | ns |
| | | | Ch-2 | - | 22 | - | |
| Reverse recovery rise time | t _b | | Ch-1 | - | 10 | - | |
| | | | Ch-2 | - | 6 | - | |

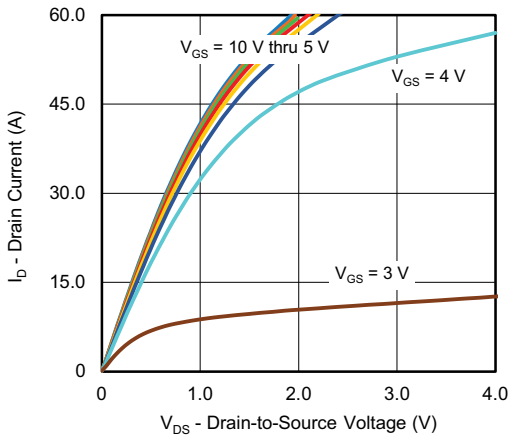
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

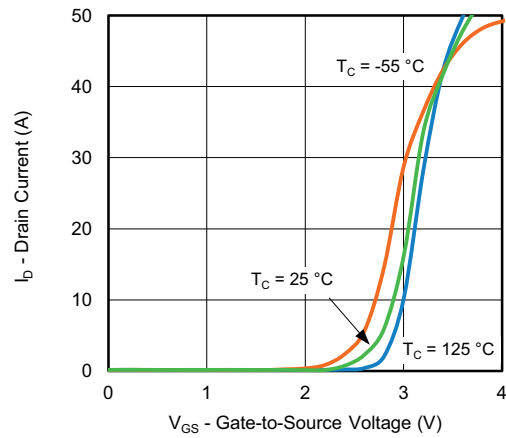
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



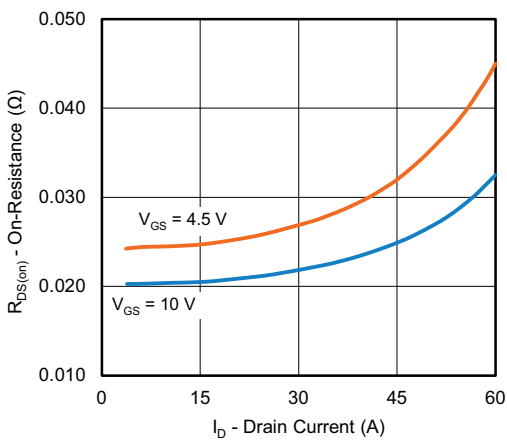
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



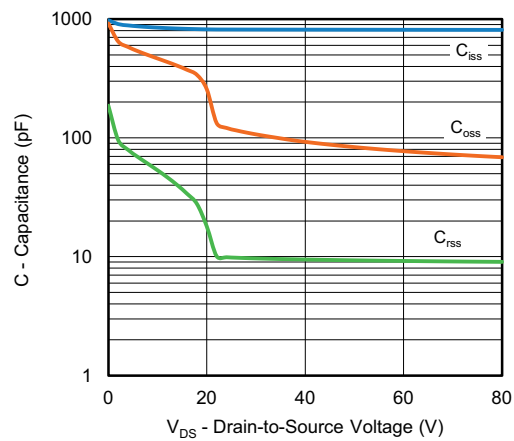
Output Characteristics



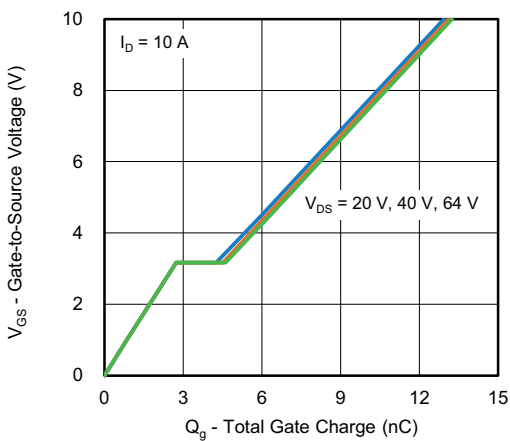
Transfer Characteristics



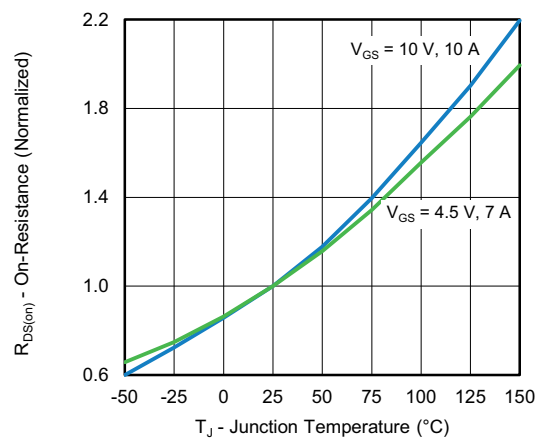
On-Resistance vs. Drain Current



Capacitance



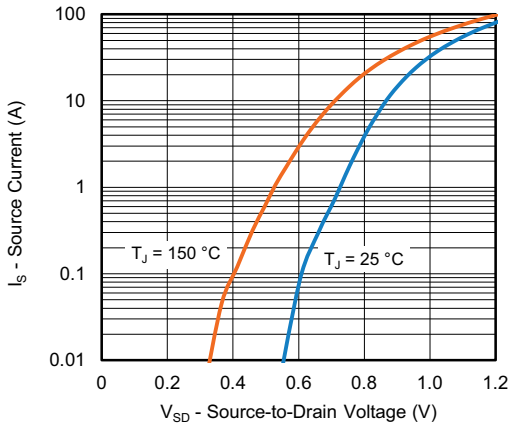
Gate Charge



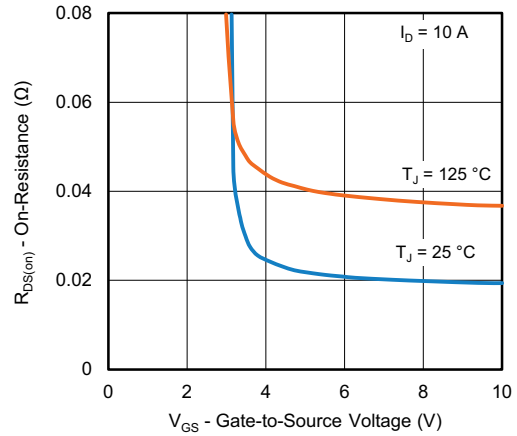
On-Resistance vs. Junction Temperature



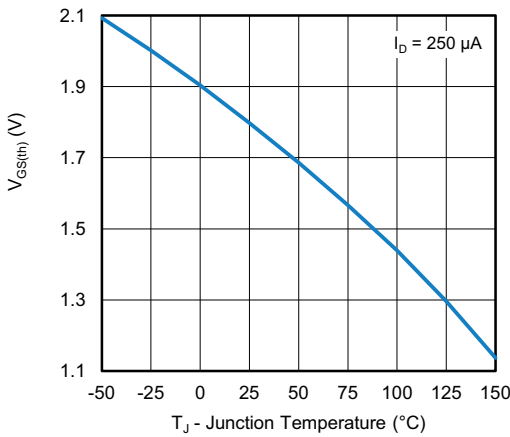
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



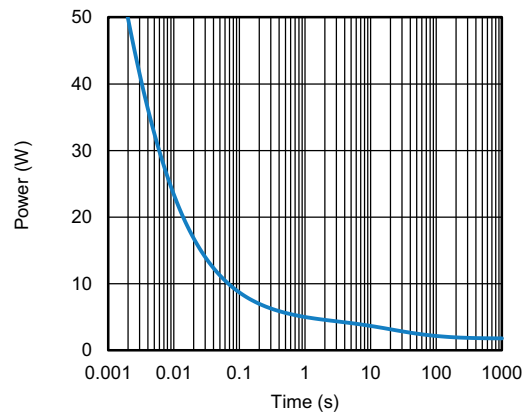
Source-Drain Diode Forward Voltage



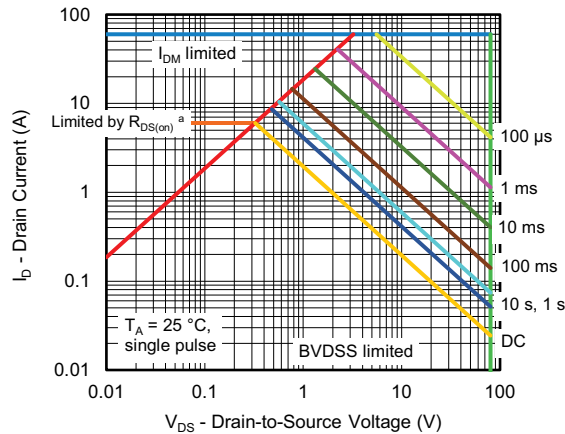
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



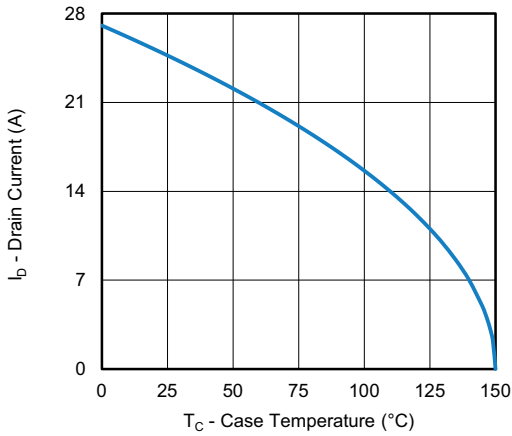
Safe Operating Area, Junction-to-Ambient

Note

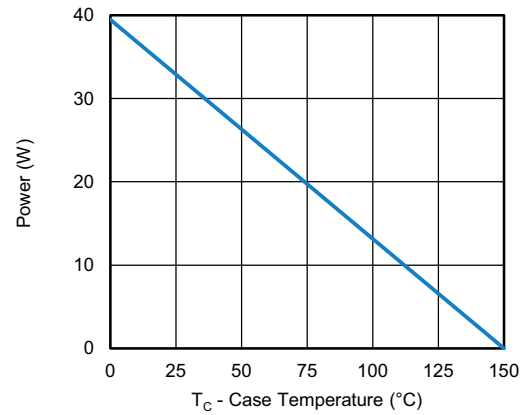
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



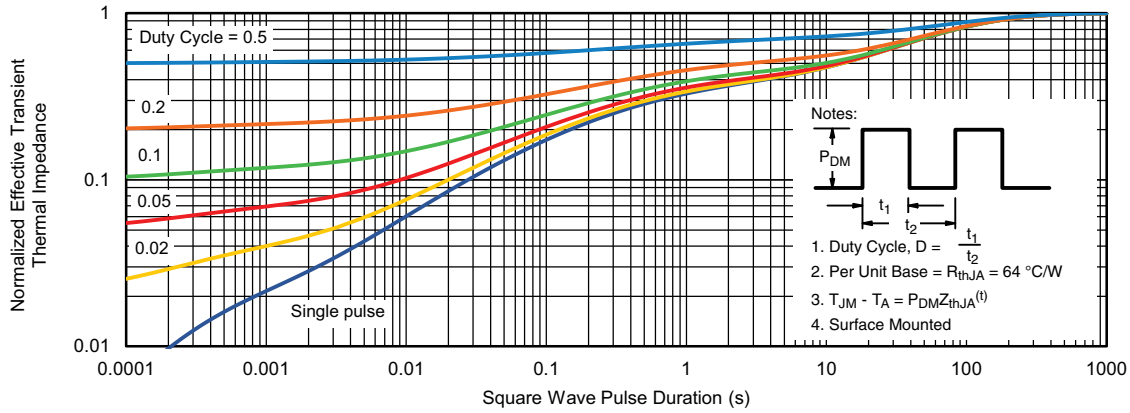
Power, Junction-to-Case

Note

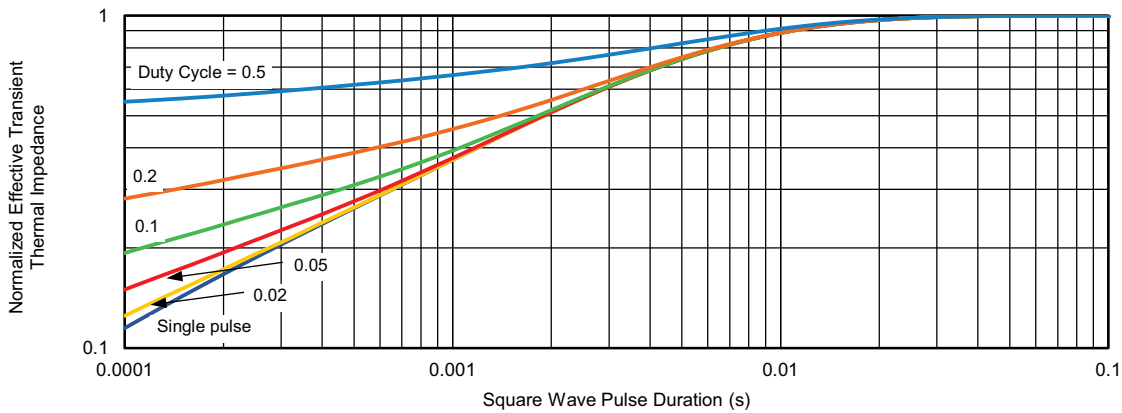
- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



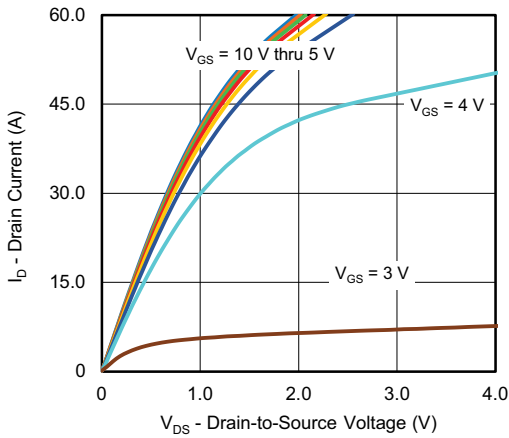
Normalized Thermal Transient Impedance, Junction-to-Ambient



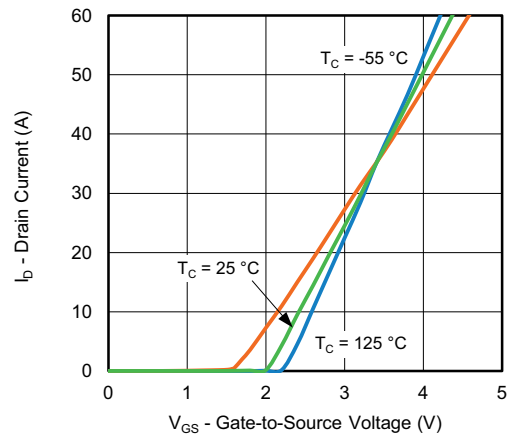
Normalized Thermal Transient Impedance, Junction-to-Case



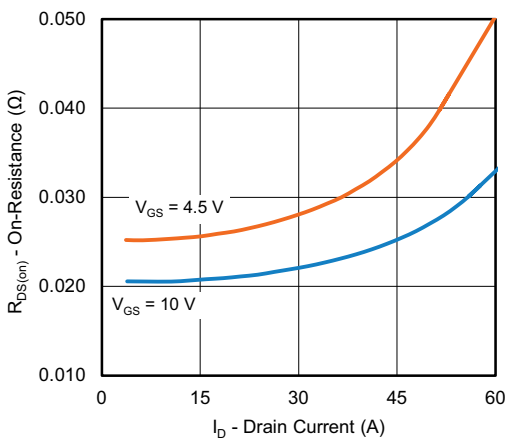
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



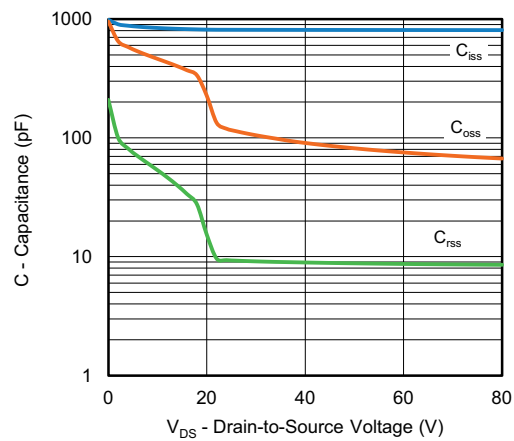
Output Characteristics



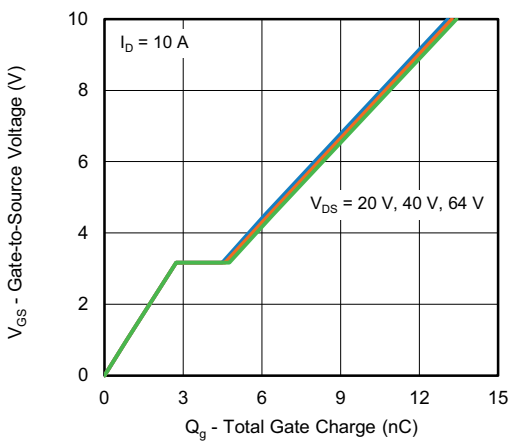
Transfer Characteristics



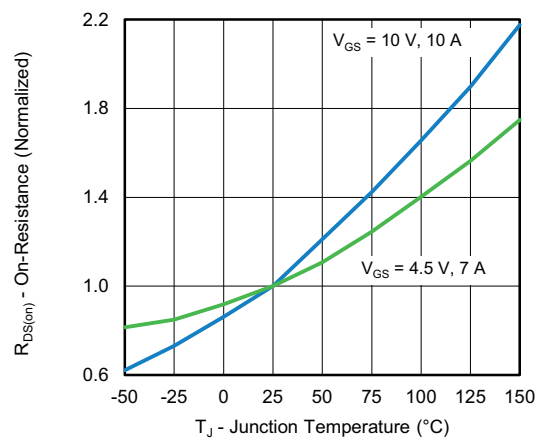
On-Resistance vs. Drain Current



Capacitance



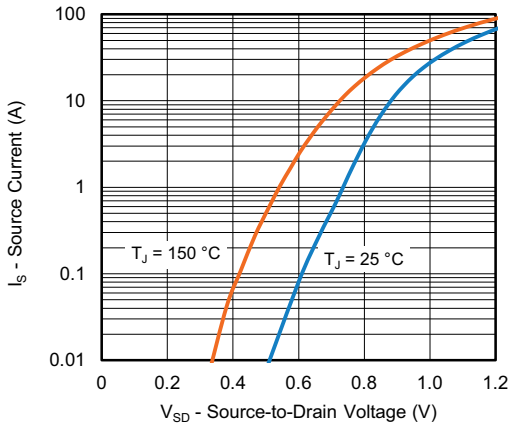
Gate Charge



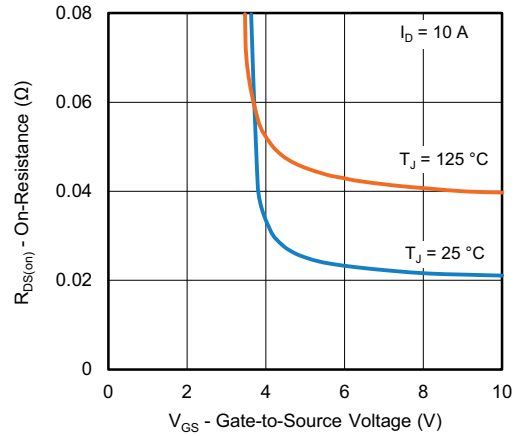
On-Resistance vs. Junction Temperature



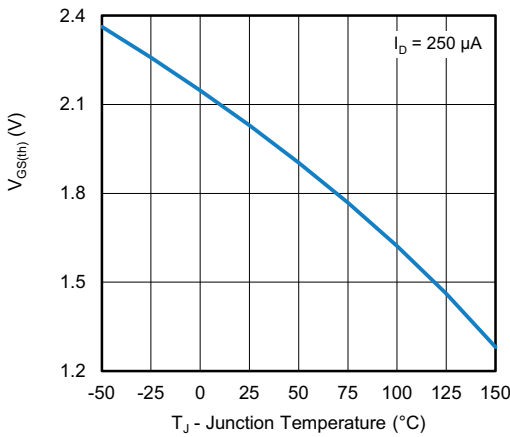
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



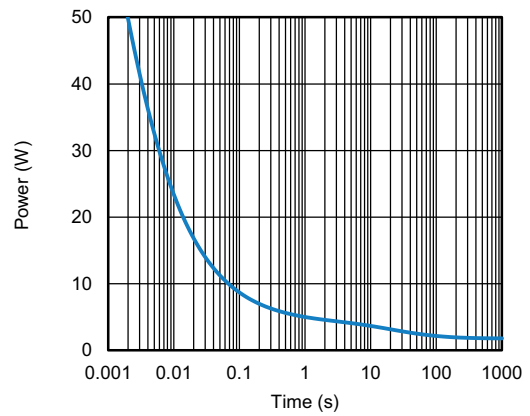
Source-Drain Diode Forward Voltage



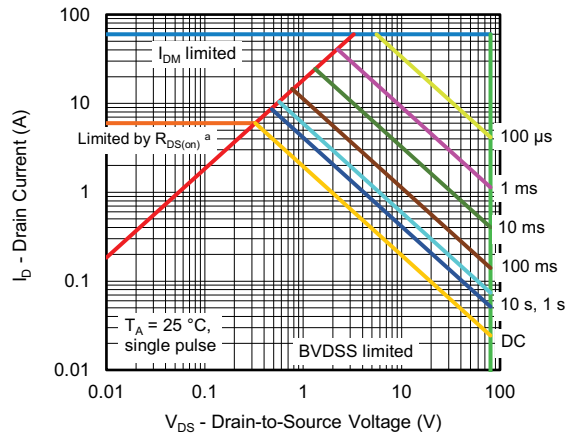
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



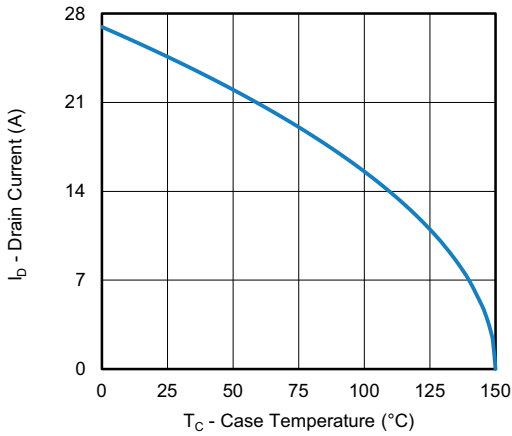
Safe Operating Area, Junction-to-Ambient

Note

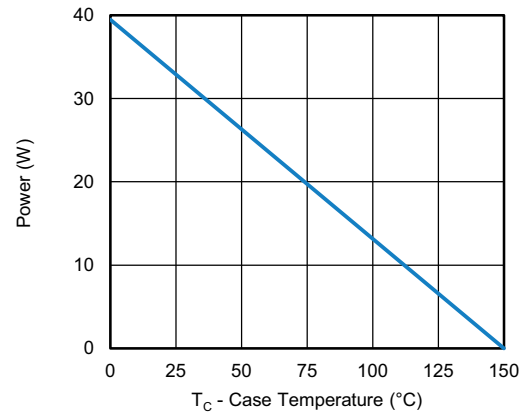
- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



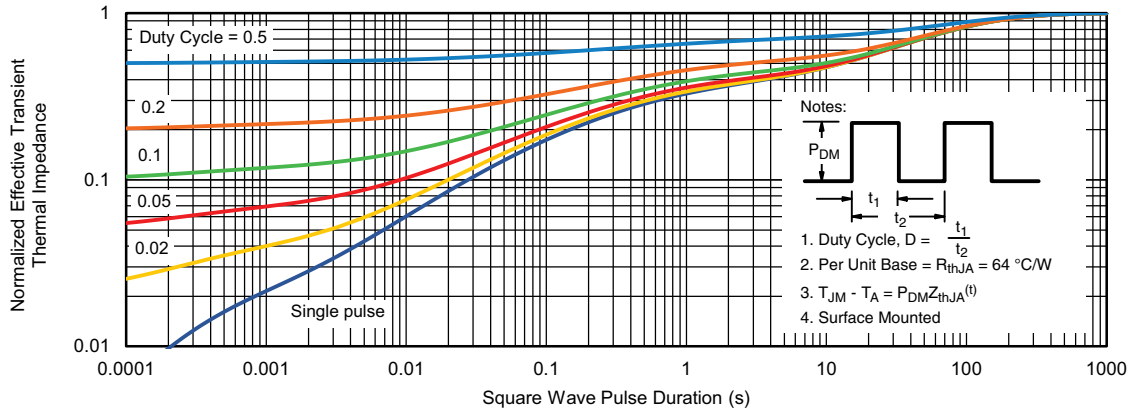
Power, Junction-to-Case

Note

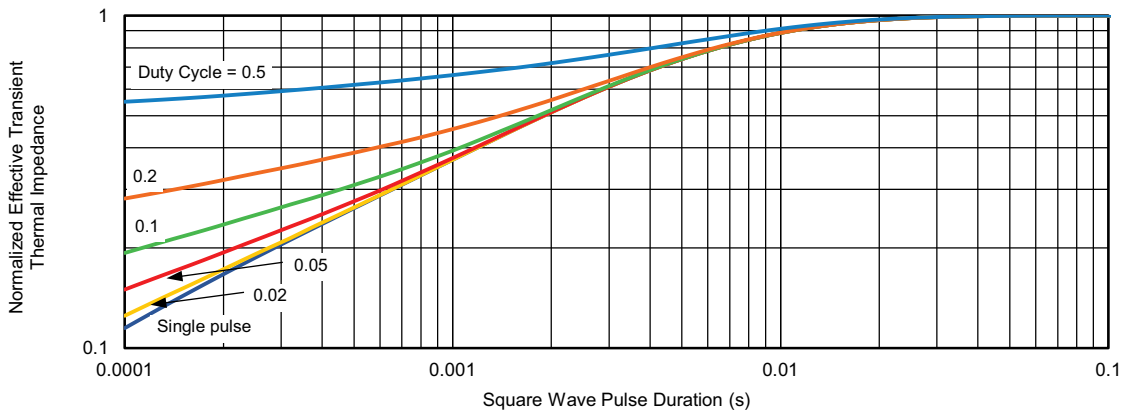
- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77236.

PowerPAIR® 3.3 x 3.3 Case Outline



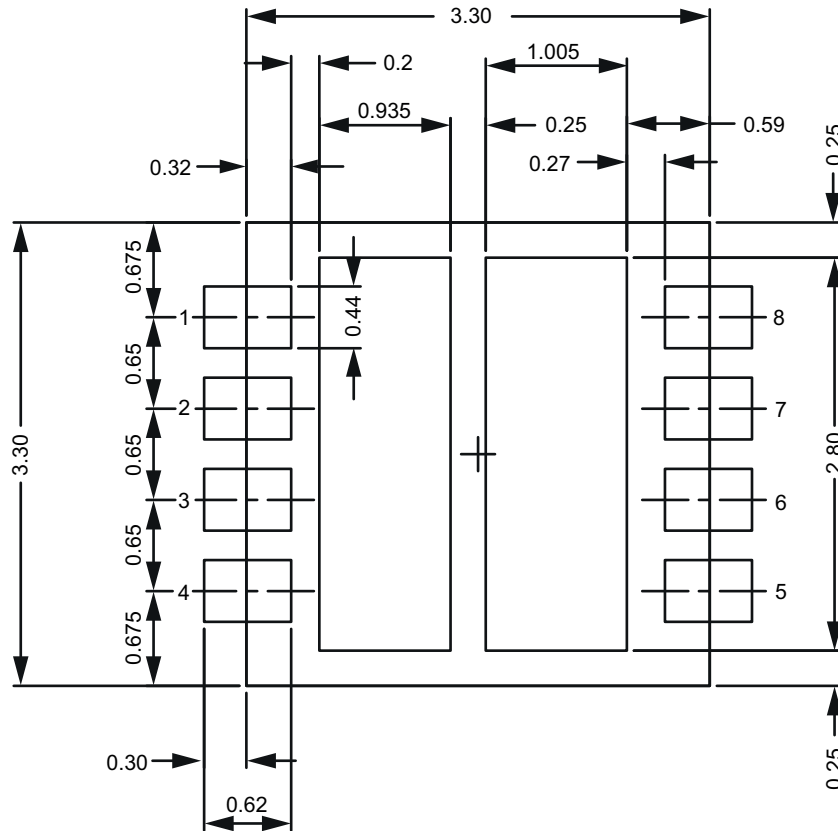
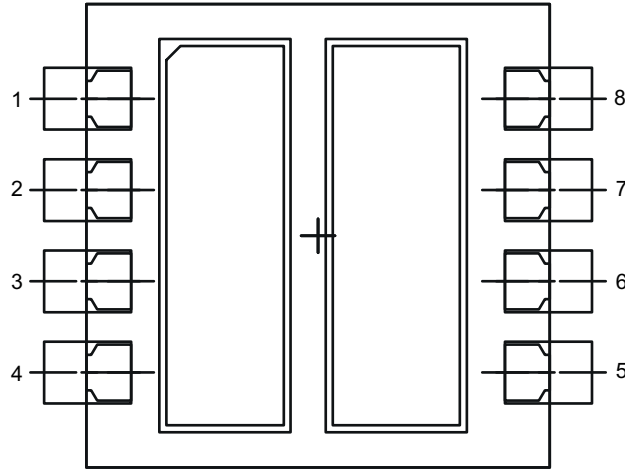
| DIM. | MILLIMETERS | | | INCHES | | |
|---|-------------|------|------|------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| b | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| b1 | 0.20 | 0.25 | 0.38 | 0.008 | 0.010 | 0.015 |
| C | 0.18 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| D | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| D1 | 0.86 | 0.91 | 0.96 | 0.034 | 0.036 | 0.038 |
| D2 | 0.79 | 0.84 | 0.89 | 0.031 | 0.033 | 0.035 |
| E | 3.20 | 3.30 | 3.40 | 0.126 | 0.130 | 0.134 |
| E1 | 2.65 | 2.70 | 2.75 | 0.104 | 0.106 | 0.108 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| K | 0.25 ref. | | | 0.010 ref. | | |
| K1 | 0.35 ref. | | | 0.014 ref. | | |
| K2 | 0.32 ref. | | | 0.013 ref. | | |
| K3 | 0.30 ref. | | | 0.012 ref. | | |
| L | 0.27 | 0.32 | 0.37 | 0.011 | 0.013 | 0.015 |
| C18-0564-Rev. A, 14-May-2018 DWG: 6066 | | | | | | |

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5M - 1994
- (3) N is the number of terminals; Nd is the number of terminals in X-direction; Ne is the number of terminals in Y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- (5) The pin # 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (6) Exact shape and size of this features is optional
- (7) Package warpage max. 0.08 mm
- (8) Applied only for terminals



Recommended Land Pattern for PowerPAIR® 3 x 3S BWL





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