

200V Half-Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 200 V max.
- $I_{\text{O}+/-}$ (min.) 130mA/270mA
- V_{OUT} 10 V - 18 V
- $t_{\text{on/off}}$ (typ.) 125 ns/125 ns
- **Deadtime** (typ.) 500 ns

GENERAL DESCRIPTION

The SLM2003E is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 200 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 18 V
- Under-voltage lockout
- 3.3 V, 5 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with $\overline{\text{HIN}}$ input
- Low-side output out of phase with $\overline{\text{LIN}}$ input
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT

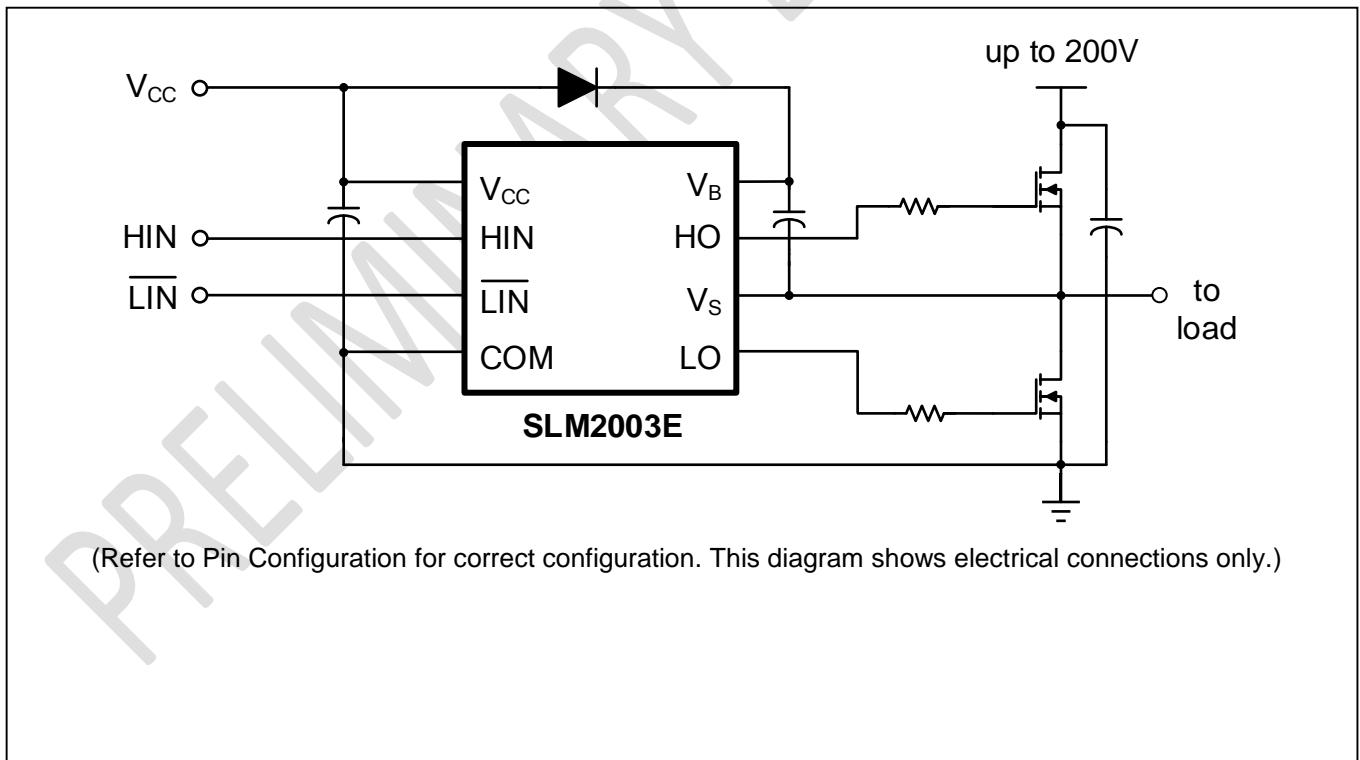
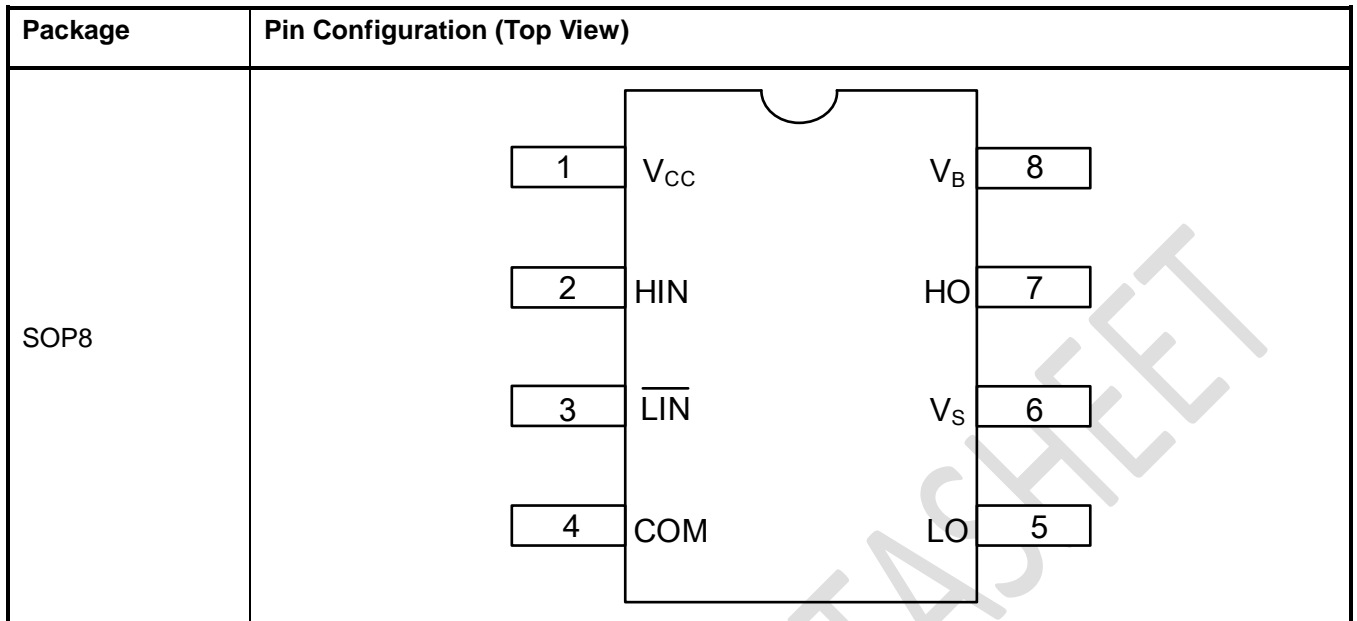


Table of Contents

| | |
|--|---|
| Product Summary | 1 |
| General Description | 1 |
| Features | 1 |
| Typical Application Circuit..... | 1 |
| PIN Configuration..... | 3 |
| PIN Description..... | 3 |
| Ordering Information..... | 3 |
| Functional Block Diagram | 4 |
| Absolute Maximum Ratings | 5 |
| Recommended Operation Conditions | 5 |
| Dynamic Electrical Characteristics | 6 |
| Static Electrical Characteristics..... | 6 |
| Package Case Outlines | 8 |
| Revision History | 9 |

PRELIMINARY DATASHEET

PIN CONFIGURATION



PIN DESCRIPTION

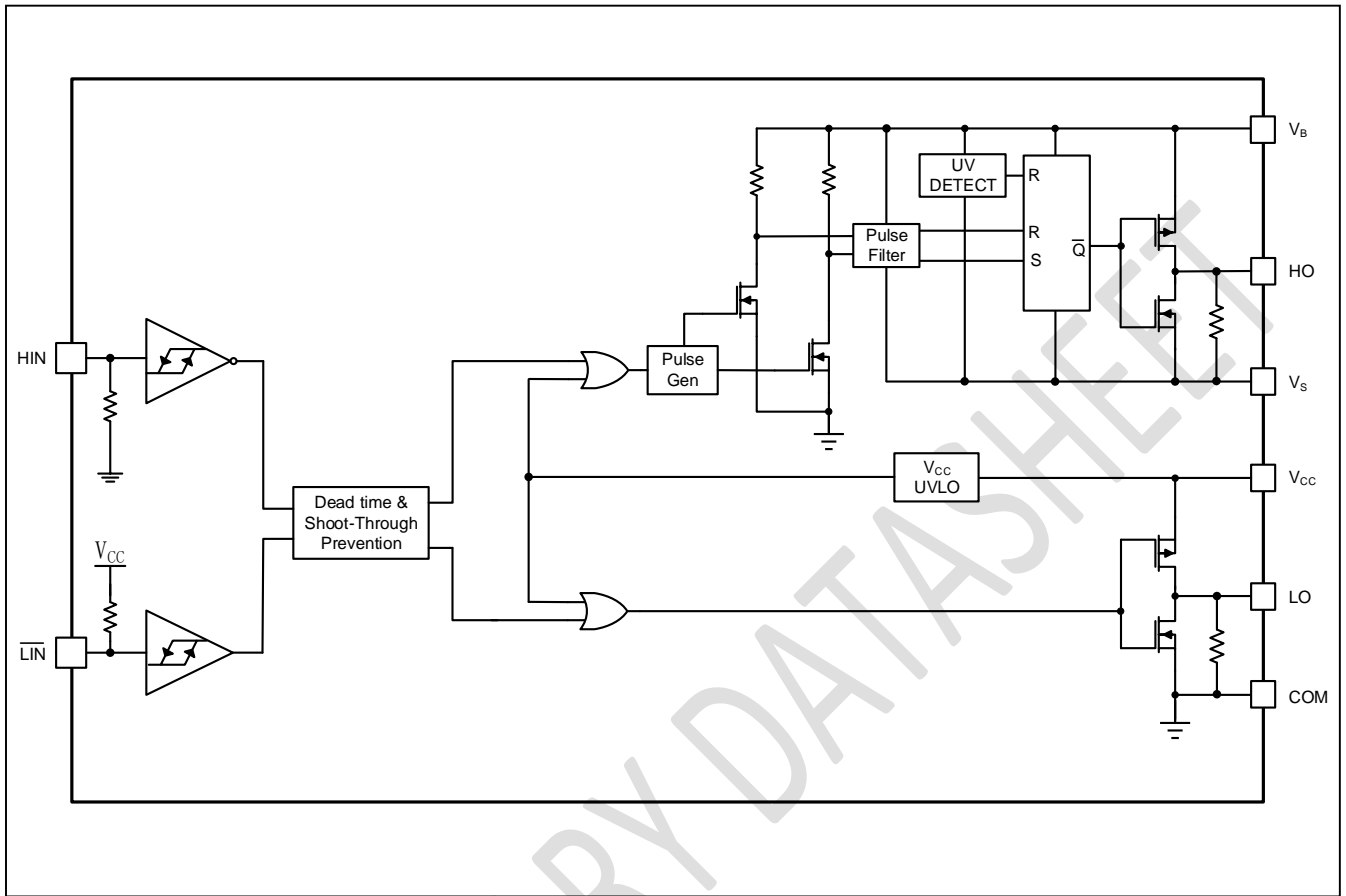
| No. | Pin | Description |
|-----|-------------------------|--|
| 1 | V _{CC} | Low-side and logic fixed supply |
| 2 | HIN | Logic input for high-side gate driver output (HO), in phase |
| 3 | $\overline{\text{LIN}}$ | Logic input for low-side gate driver output (LO), out of phase |
| 4 | COM | Low-side return |
| 5 | LO | Low-side gate drive output |
| 6 | V _s | High-side floating supply return |
| 7 | HO | High-side gate drive output |
| 8 | V _b | High-side floating supply |

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY |
|----------------|---------------|-----------|
| SLM2003ECA-DG | SOP8, Pb-Free | 2500/Reel |

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

| Symbol | Definition | Min. | Max. | Units |
|---------------------|---|----------------------|-----------------------|-------|
| V _B | High-side floating absolute voltage | -0.3 | 220 | V |
| V _S | High-side floating supply offset voltage | V _B - 20 | V _B + 0.3 | |
| V _{HO} | High-side floating output voltage | V _S - 0.3 | V _B + 0.3 | |
| V _{CC} | Low-side and logic fixed supply voltage | -0.3 | 20 | |
| V _{LO} | Low-side output voltage | -0.3 | V _{CC} + 0.3 | |
| V _{IN} | Logic input voltage (HIN & LIN) | -0.3 | 10 | |
| dV _S /dt | Allowable offset supply voltage transient | --- | 50 | V/ns |
| P _D | Package power dissipation at T _A ≤ +25°C | --- | 0.625 | W |
| θ _{JA} | Thermal resistance, junction to ambient | --- | 200 | °C/W |
| T _J | Junction temperature | --- | 150 | °C |
| T _S | Storage temperature | -55 | 150 | |
| T _L | Lead temperature (soldering, 10 seconds) | --- | 300 | |

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

| Symbol | Definition | Min. | Max. | Units |
|-----------------|--|---------------------|---------------------|-------|
| V _B | High-side floating absolute voltage | V _S + 10 | V _S + 18 | V |
| V _S | High-side floating supply offset voltage | | 200 | |
| V _{HO} | High-side floating output voltage | V _S | V _B | |
| V _{CC} | Low-side and logic fixed supply voltage | 10 | 18 | |
| V _{LO} | Low-side output voltage | 0 | V _{CC} | |
| V _{IN} | Logic input voltage (HIN & LIN) | 0 | 10 | |
| T _A | Ambient temperature | - 40 | 125 | °C |

Note: For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-----------|---|--------------------|------|------|------|------|
| t_{on} | Turn-on propagation delay | $V_S = 0\text{ V}$ | --- | 125 | 200 | ns |
| t_{off} | Turn-off propagation delay | $V_S = 0\text{ V}$ | --- | 125 | 200 | |
| t_r | Turn-on rise time | | --- | 70 | 100 | |
| t_f | Turn-off fall time | | --- | 25 | 40 | |
| DT | Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off | | --- | 500 | --- | |
| MT | Delay matching, HS & LS turn-on/off | | --- | --- | 60 | |

Note: See timing diagram in Figure 1, Figure 2, Figure 3 and Figure 4.

STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-------------|--|---------------------------------------|------|------|------|---------------|
| V_{IH} | Logic "1" (HIN) & Logic "0" (\overline{LIN}) input voltage | $V_{CC} = 10\text{ V to }18\text{ V}$ | 2.5 | --- | --- | V |
| V_{IL} | Logic "0" (HIN) & Logic "1" (\overline{LIN}) input voltage | | --- | --- | 0.8 | |
| V_{OH} | High level output voltage, $V_{BIAS} - V_O$ | $I_O = 20\text{ mA}$ | --- | 0.4 | 0.6 | |
| V_{OL} | Low level output voltage, V_O | | --- | 0.13 | 0.2 | |
| I_{LK} | Offset supply leakage current | $V_B = V_S = 200\text{ V}$ | --- | --- | 50 | μA |
| I_{QBS} | Quiescent V_{BS} supply current | $V_O = 0\text{ V}$ | --- | 105 | 160 | |
| I_{QCC} | Quiescent V_{CC} supply current | | --- | 245 | 390 | |
| I_{IN+} | Logic "1" input bias current on HIN | $HIN = 5\text{ V}$ | --- | 100 | 150 | |
| | Logic "1" input bias current on \overline{LIN} | $\overline{LIN} = 0\text{ V}$ | --- | --- | 80 | |
| I_{IN-} | Logic "0" input bias current on HIN | $HIN = 0\text{ V}$ | --- | --- | 5 | |
| | Logic "0" input bias current on \overline{LIN} | $\overline{LIN} = 5\text{ V}$ | --- | --- | -80 | |
| V_{CCUV+} | V_{CC} supply under-voltage positive going threshold | | 8 | 8.6 | 9.5 | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|-------------|--|--|------|------|------|------|
| V_{CCUV-} | V_{CC} supply under-voltage negative going threshold | | 7.6 | 8.2 | 9 | |
| V_{BSUV+} | V_{BS} supply under-voltage positive going threshold | | | 8.6 | | |
| V_{BSUV-} | V_{BS} supply under-voltage negative going threshold | | | 7.9 | | |
| I_{O+} | Output high short circuit pulsed current | $V_O = 0\text{ V}$, $V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$ | 130 | 290 | | mA |
| I_{O-} | Output low short circuit pulsed current | $V_O = 15\text{ V}$, $V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$ | 270 | 600 | | |

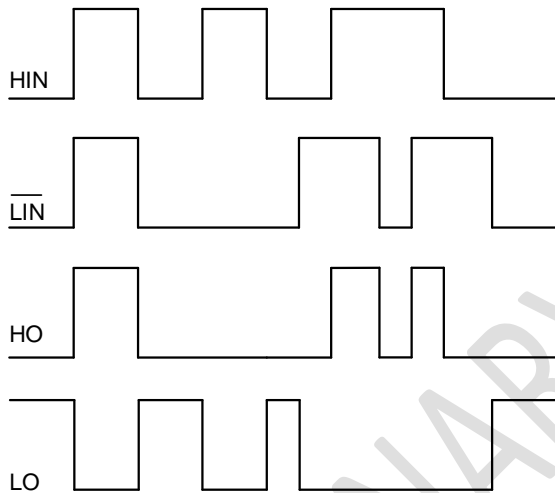


Figure 1. Input/Output Timing Diagram

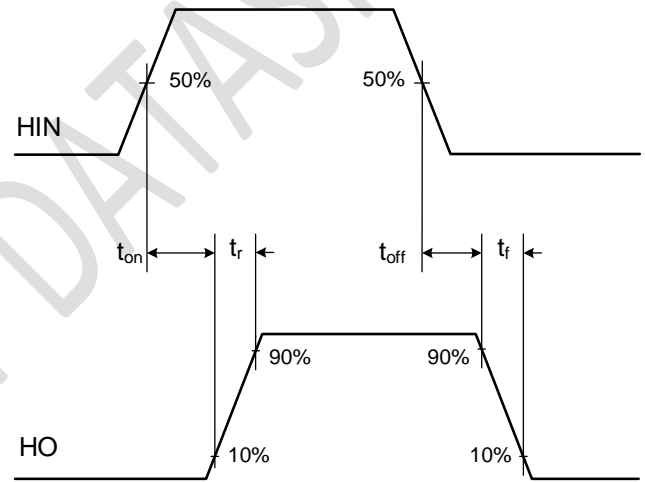


Figure 2. High Side Switching Time Waveform

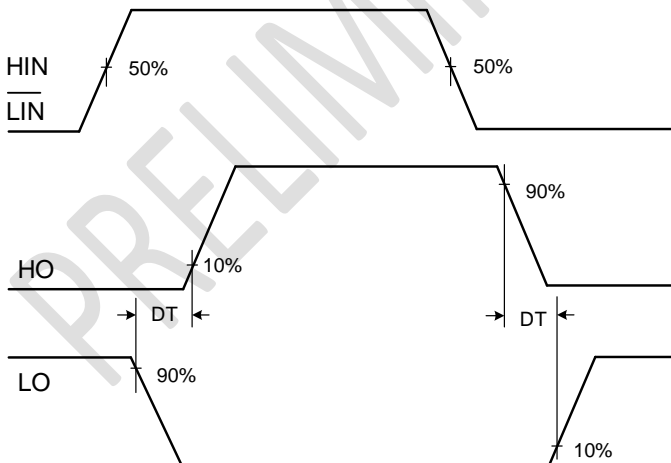


Figure 3. Dead Time Waveform

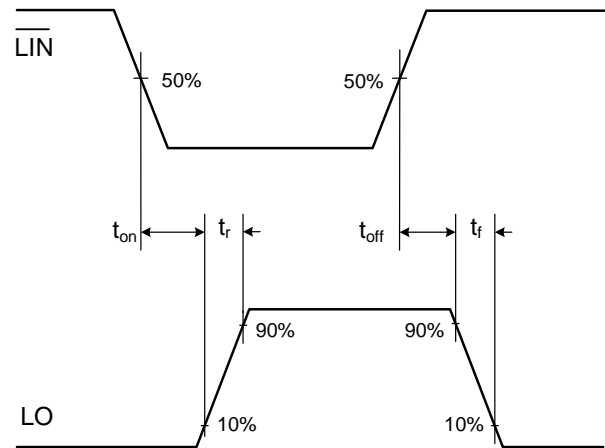


Figure 4. Low Side Switching Time Waveform

PACKAGE CASE OUTLINES

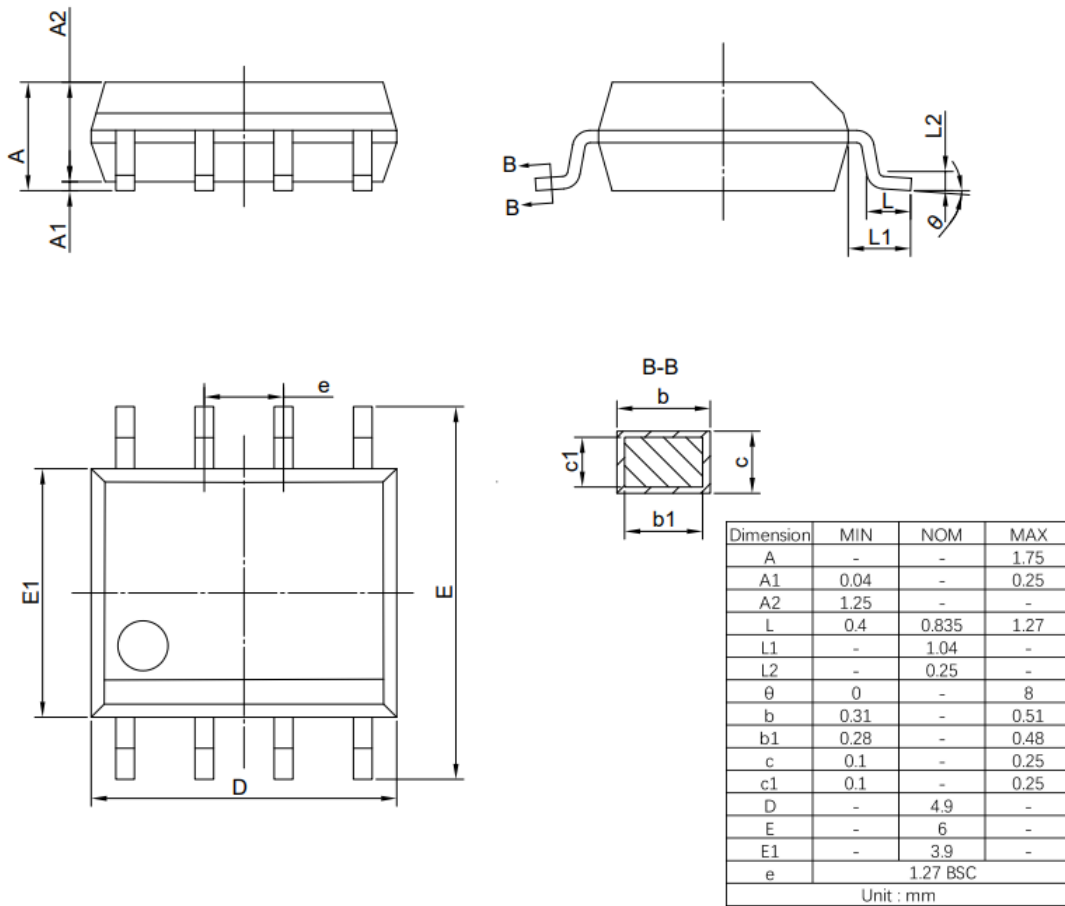


Figure 5. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

| Page or Item | Subjects (major changes since previous revision) |
|---|--|
| Rev 0.1 preliminary datasheet 2021-10-29 | |
| Whole document | Rev 0.1 preliminary datasheet release |
| Rev 0.2 preliminary datasheet 2022-05-09 | |
| Whole document | Rev 0.2 preliminary datasheet release |

PRELIMINARY DATASHEET