Fast Charging Protocol Controller for USB Type-A

Hynetek Semiconductor Co., Ltd.

HUSB601

FEATURES

Qualcomm QC3+ certified: QC20210519235

Support multiple fast charging protocols

- BC1.2 DCP
- Apple 5 V, 2.4 A
- Samsung AFC
- QC2.0/3.0 (Class A & B), QC3+
- Huawei FCP and SCP

Configurable maximum charging voltage

Dynamically switching between fast charging and 5 V charging

Accurate adjustment of charging voltage

Automatic detection of powered devices

High voltage capability of DP, DM pins up to 25 V

Low quiescent current down to 50 μA

APPLICATIONS

Wall adapter

Car charger and Portable power bank

General USB Type-A output ports

GENERAL DESCRIPTION

The HUSB601 is a fast charging protocol controller dedicated for USB Type-A charging application. It supports multiple fast charging protocols including BC1.2 Dedicated, Charging Port (DCP), Qualcomm Quick Charge (QC) 2.0/3.0 Class A and Class B and QC3+, Samsung Adaptive Fast Charge (AFC), Huawei Fast Charger Protocol (FCP) and Smart Charge Protocol (SCP).

The HUSB601 detects the types of the powered devices automatically and selects the proper fast charging protocol. The maximum charging voltage during fast charging is configurable to limit the charging power. The HUSB601 supports charging power switching between fast charging and 5V charging dynamically, compatible with the power de-rating application in the charging system which has multiple charging ports.

The HUSB601 adjusts the charging voltage accurately by sourcing/sinking current through FB pin.

Low quiescent current of the HUSB601 ensures minimum power consumption and reduces the thermal stress of the charging system.

The HUSB601 is available in a SOT23-6 package.

TYPICAL APPLICATION CIRCUIT

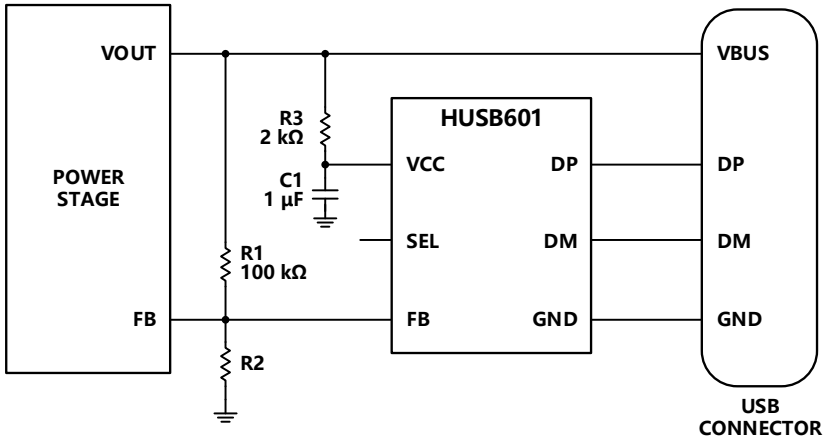

Figure 1. Typical Application Circuit

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REVISION HISTORY

Version	Date	Descriptions
Rev. 1.0	09/2022	Initial version
Rev. 1.1	04/2023	Update ordering guide (Adding HUSB601_ASA)
Rev. 1.2	07/2023	Add Package Top Marking

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

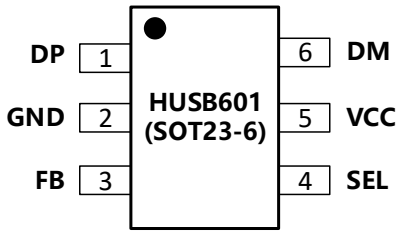


Figure 2. Pin Configuration (Top View)

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type[1]	Description
1	DP	DIO	USB D+ line. Connect this pin to D+ of the USB connector directly.
2	GND	P	Ground reference. Connect this pin to the ground of the system.
3	FB	AIO	Feedback control. Connect this pin to the feedback node of the power system.
4	SEL	DI	Maximum charging voltage selection.
5	VCC	PI	Supply power input. Connect this pin to GND pin through a 1 μF ceramic capacitor. Connect this pin to the output of the power system through a 2 kΩ resistor.
6	DM	DIO	USB D- line. Connect this pin to D- of the USB connector directly.

1 Legend:
A = Analog Pin
P = Power Pin
D = Digital Pin
I = Input Pin
O = Output Pin

SPECIFICATIONS

V_{CC} = 5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY		VCC pin				
Input Voltage Range	V_{CC}		2.9		5.5	V
Input Voltage UVLO Threshold						
VCC Rising	V_{CC_RISE}	VCC UVLO rising threshold		2.7		V
VCC Falling	V_{CC_FALL}	VCC UVLO falling threshold		2.5		V
Input Quiescent Current	I_{Q_VCC}	V_{CC} = 5V, no load		50	100	μA
VCC Shunt Regulator Voltage	V_{CC_SHUNT}	A 2 kΩ resistor is connected between VBUS and VCC	5.1	5.3	5.5	V
VCC Shunt Regulator Maximum Sink Current	I_{CLAMP_VCC}			15		mA
MAXIMUM CHARGE VOLTAGE SELECTION		SEL pin				
SEL Output Voltage	V_{SEL}	Typical output voltage when SEL is floating	1.4	1.5	1.6	V
SEL Input Low Threshold					0.3	V
SEL Input High Threshold			2.2		VCC	V
FEEDBACK CONTROL						
FB Sourcing Current LSB	I_{FB_SRC}			0.2		μA
FB Sinking Current LSB	I_{FB_SNK}			0.2		μA
DAC Resolution				10		bit
Voltage Change Slew Rate		With external 100 k resistor from Vout to FB		0.2		V/ms
FB Output Voltage Range	V_{FB}		0.4		2.5	V
BC1.2 DCP MODE						
DP and DM Shorting Resistance	R_{DPM_SHORT}	VDP = 0.6 V		20	40	Ω
DP Leakage Resistance	R_{DP_LKG}	VDP = 0.6 V		800		kΩ
DM Leakage Resistance	R_{DM_LKG}	VDP = 0.6 V		800		kΩ
DCP Mode Entry Threshold	V_{SEL_REF}		1.8	2	2.2	V
DCP Mode Entry Deglitch Time	t_{SEL_REF}			20		ms
APPLE DIVIDER3 MODE						
DP Output Voltage	V_{DP_APP}	V_{CC} = 5V	2.57	2.7	2.84	V
DM Output Voltage	V_{DM_APP}	V_{CC} = 5V	2.57	2.7	2.84	V
DP Output Impedance	R_{DP_PAD}	I_{DP} = -5μA		30		kΩ
DM Output Impedance	R_{DM_PAD}	I_{DM} = -5μA		30		kΩ
HVDCP MODE						
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
DP High Glitch Filter Time	$T_{GLITCH\_BC\_DONE}$		1	1.25	1.5	s
DM Low Glitch Filter Time	$T_{GLITCH\_DM\_LOW}$		1	2		ms
Output Voltage Glitch Filter Time	$T_{GLITCH\_V\_CHANGE}$		20	40	60	ms
DM Pull-Down Resistance	R_{DM_DWM}			15		kΩ
QC MODE						
Pulse Glitch Filter Time	$T_{GLITCH\_CONT\_CHANGE}$	For QC 3.0 in continues mode	100	150	200	μs
FB Sourcing Current LSB in QC3+	$I_{FB\_SRC\_QC3+}$			0.2		μA
FB Sinking Current LSB in QC3+	$I_{FB\_SNK\_QC3+}$			0.2		μA
FCP MODE						
DM FCP TX Valid Output High	V_{TX_VOH}		2.5		3.6	V
DM FCP TX Valid Output Low	V_{TX_VOL}				0.3	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DM FCP RX Valid Input High	V_{RX_VIH}		1.4		3.6	V
DM FCP RX Valid Input Low	V_{RX_VIL}				1	V
DM Output Pull-Low Resistance	R_{DMPL}		130	180	250	Ω
Unit Interval for FCP	UI	125 kHz clock	144	160	176	μs

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC	−0.3 V to +6.5 V
FB	−0.3 V to +6.5 V
SEL	−0.3 V to +6.5 V
DP, DM	−0.3 V to +25 V
Operating Temperature Range (Junction)	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Mode	4000V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-6	220	100	°C/W

ESD CAUTION

Electrostatic Discharge Sensitive Device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

The HUSB601 is a highly integrated, fast charging protocol controller for USB Type-A charging application. The HUSB601 supports multiple fast charging protocols and it detects the attached powered devices automatically. The proper charging protocol is selected for the powered device for the best charging.

INPUT SHUNT REGULATOR

A shunt regulator with 5 V output voltage is integrated in VCC pin of the HUSB601. The output voltage of the shunt regulator follows VBUS during power on until VBUS is higher than 5 V. When the voltage on VBUS rises above 5 V, the shunt regulator clamps its output voltage at 5 V.

Connect a 1 μF ceramic capacitor from VCC pin to GND pin of the HUSB601. Connect a 2 kΩ resistor between VCC pin and VBUS.

MAXIMUM FAST CHARGING VOLTAGE SELECTION

The HUSB601 allows the user to configure the maximum fast charging voltage by applying different status on the SEL pin as shown in Table 5 and Table 6. The HUSB601_LSA and HUSB601_ASA support QC3.0 Class A, and the HUSB601_HSA supports QC3.0 Class B.

Table 5. SEL Pin Configuration for HUSB601_LSA or HUSB601_ASA

SEL Pin Status	Maximum Charging Voltage (V)
High (pulled up to VCC)	12
Floating	9
Low	5

Table 6. SEL Pin Configuration for HUSB601_HSA

SEL Pin Status	Maximum Charging Voltage (V)
High (pulled up to VCC)	20
Floating	20
Low	12

SEL Pin should be pulled up to VCC via a pull-up resistor if SEL Pin status needs to set high.

Take HUSB601L for example, when SEL pin is driven high, the maximum charging voltage on VBUS is 12 V. The fast charging function is enabled. When leaving SEL pin floating, the maximum charging voltage is reduced to 9 V.

In the charging system where multiple charging ports are supported, for example 1A1C, it may require the USB-A port to reduce its charging power so that USB-C port runs at full power. In this case, SEL pin can be driven low and only 5 V charging protocol is allowed.

The SEL pin status can be changed dynamically when the HUSB601 is working.

DIRECT FEEDBACK VOLTAGE CONTROL

The HUSB601 uses a direct feedback voltage control method to adjust the VBUS, that is the output voltage of the front end power stage. The FB pin of the HUSB601 is connected to the feedback node of the front end power stage as shown in figure 3. The front end power stage can be a AC-DC or a DC-DC regulator.

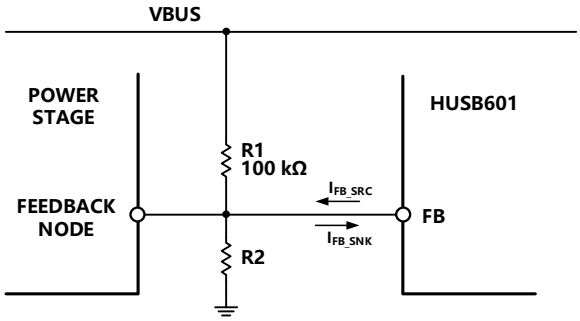


Figure 3. HUSB601 Direct Feedback Control

The HUSB601 sources or sinks a current to adjust the VBUS voltage depending on the request on the DP/DM lines by the powered device and the SEL pin status. The current output DAC on FB pin has a LSB of 0.2 μA. When the top resistor of the feedback network of the front end power stage is set to 100 kΩ, the VBUS voltage changes 20 mV per step.

In order to guarantee the valid VBUS range, the feedback resistor network of the front end power stage should be set to output 5 V on VBUS, where no source nor sink current is flowing on FB pin of the HUSB601 (I_{FB_SRC} = I_{FB_SNK} = 0 A).

Follow the equation below to choose the R2 value:

$$R2 = \frac{V_{FB} \times R1}{VBUS - V_{FB}}$$

where, V_{FB} is the feedback node voltage of the front end power stage.

For example, if V_{FB} = 0.8 V, R1 = 100 kΩ, VBUS = 5 V, then R2 is calculated as 19.04 kΩ. Choose the standard resistor value 19.1 kΩ, as R2 value. It is recommended to choose resistors with 1% accuracy for both R1 and R2 values.

When VBUS needs to be adjusted, follow the equations below to calculate the values of I_{FB_SRC} or I_{FB_SNK}.

Increasing VBUS higher than 5 V:

$$I_{FB\_SNK} = \frac{VBUS}{R1} - V_{FB} \times \left(\frac{1}{R1} + \frac{1}{R2} \right)$$

Decreasing VBUS lower than 5 V:

$$I_{FB\_SRC} = V_{FB} \times \left(\frac{1}{R1} + \frac{1}{R2} \right) - \frac{VBUS}{R1}$$

CHARGING PROTOCOLS AUTO SELECTION

The HUSB601 supports various fast charging protocols including BC1.2 DCP, Apple Divider 3, QC 2.0/3.0 Class A and Class B, QC3+, AFC, FCP, and SCP. According to the different status of DP and DM pins, the HUSB601 recognizes the attached powered devices and apply the fast charging protocol automatically.

LOW POWER CONSUMPTION MODE

In order to achieve low power consumption when there is no load attached, the HUSB601 turns off internal digital clock under DPDM_APP modes to achieve low quiescent current requirement. The internal digital clock turns on immediately when HUSB601 exits DPDM_APP mode.

This function is controlled by internal fuse and is enabled by default.

DP AND DM OVER VOLTAGE PROTECTION

In USB-A port design, the D+/D- lines are close to the VBUS line, which may have high voltage represent. Under abnormal use cases, the D+/D- lines may short to VBUS directly and be damaged. In order to protect D+/D- lines of the powered devices, as well as the DP/DM pins of the HUSB601 from being damaged under shorting to VBUS case, the HUSB601 adjusts the VBUS to default 5 V by turning off the source/sink current on FB pin and pulls FB pin high to let the front end power stage enter into over voltage protection mode when the DP/DM pin voltage is higher than 4.5V.

The pulling FB pin action when DP/DM over voltage happens can be enabled or disabled by internal fuse options.

TYPICAL APPLICATION CIRCUITS

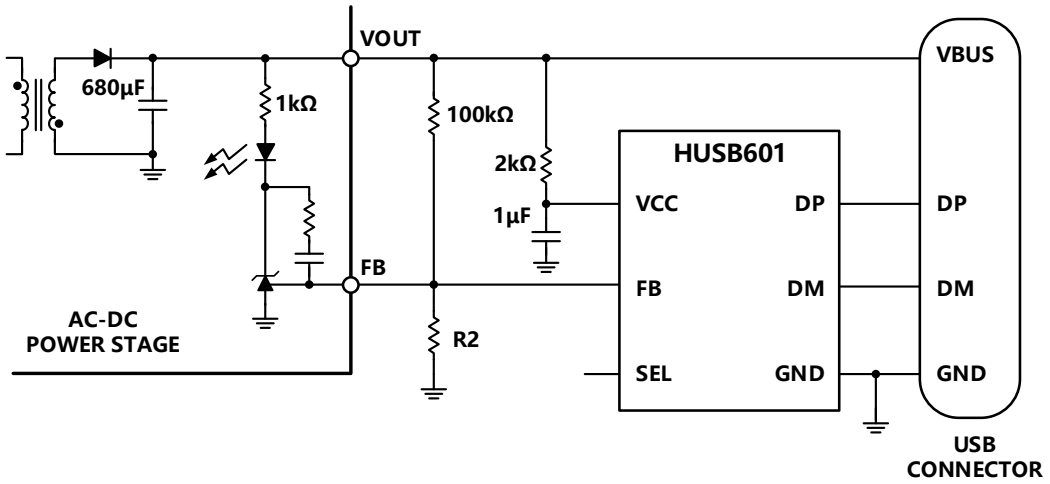


Figure 4. Typical Wall Adapter Application Circuit

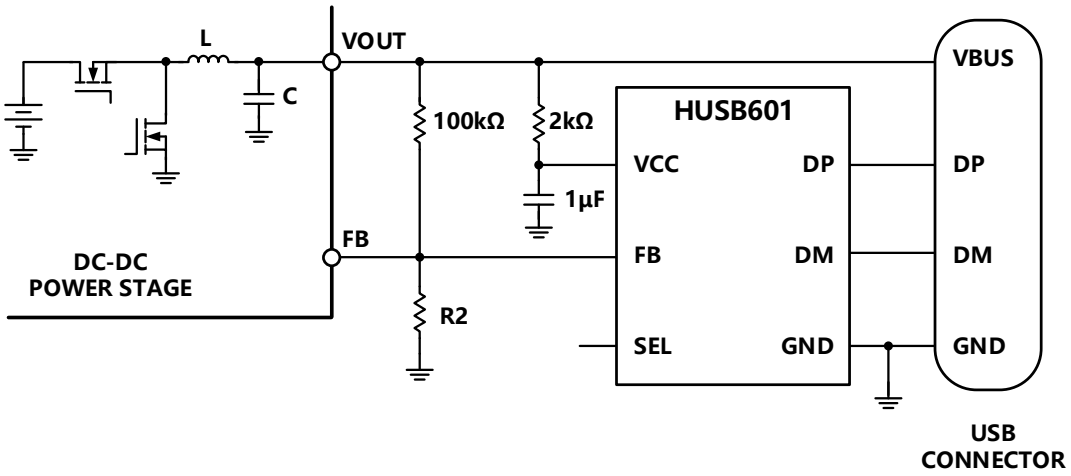
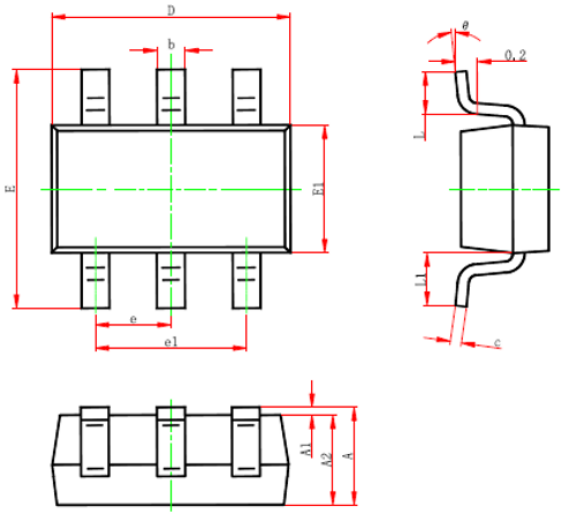


Figure 5. Typical Car Charger Application Circuit

PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

Figure 6. 6-Lead Small Outline Transistor Package [SOT23]
2.92 mm x 2.8 mm

PACKAGE TOP MARKING

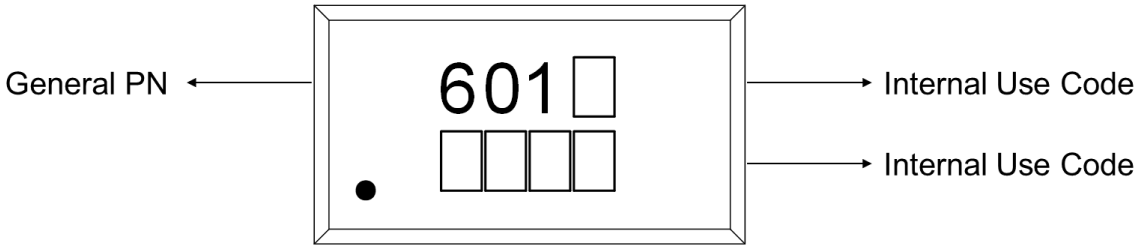


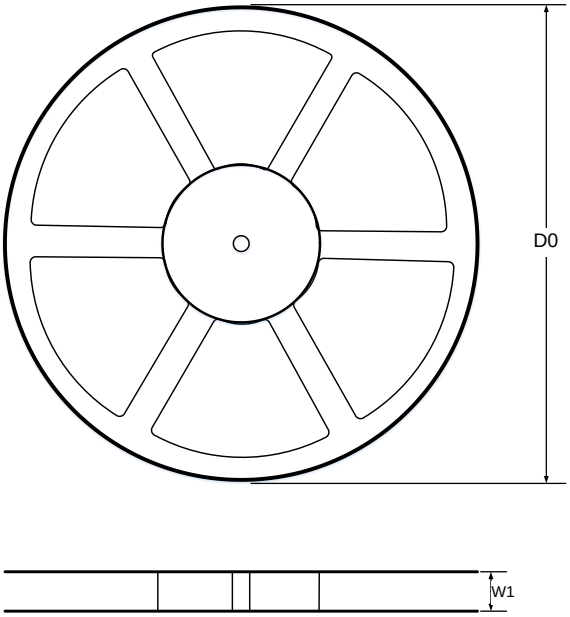
Figure 7. Package Top Marking

ORDERING GUIDE

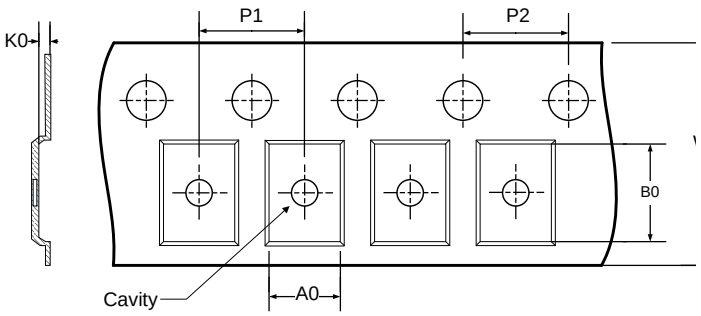
Model	Op Temp (℃)	Package	Max Charging Voltage (V)	SCP	Package Option	Package Qty
HUSB601_LSA	-40 to 125	SOT23-6L	12	5V/4.5A & 4.5V/5A	T&R	3000ea
HUSB601_HSA	-40 to 125	SOT23-6L	20	5V/4.5A & 4.5V/5A	T&R	3000ea
HUSB601_ASA	-40 to 125	SOT23-6L	12	10V/2.25A	T&R	3000ea

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W： Overall width of the carrier tape
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel Diameter
W1：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

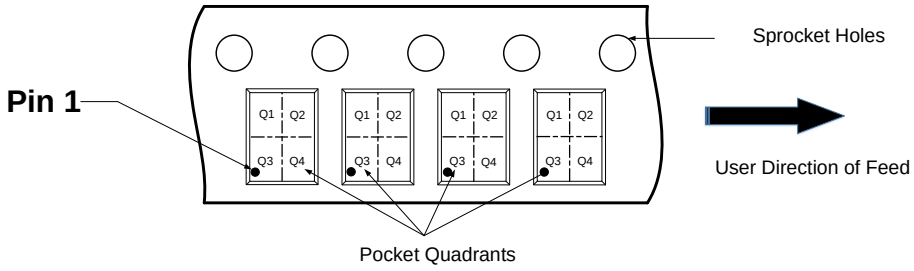


Figure 8. Tape and Reel Information

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