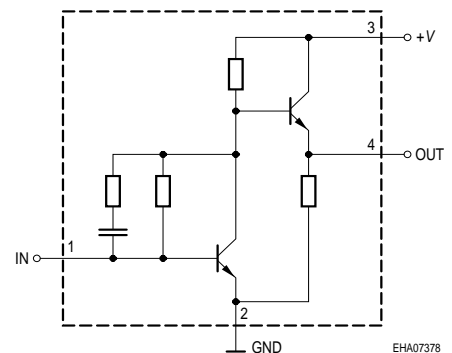
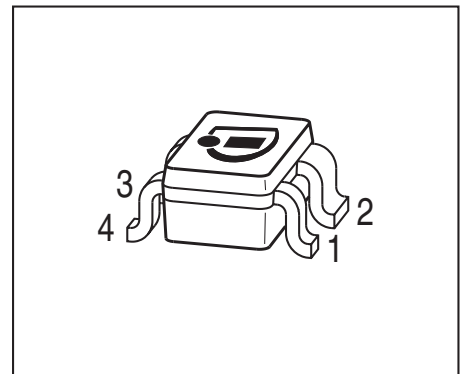


**Si-MMIC-Amplifier in SIEGET® 25-Technologie**

- Cascadable 50 Ω-gain block
- Unconditionally stable
- Gain  $|S_{21}|^2 = 18.5$  dB at 1.8 GHz (Appl.1)  
gain  $|S_{21}|^2 = 22$  dB at 1.8 GHz (Appl.2)  
 $IP_{3out} = +7$  dBm at 1.8 GHz ( $V_D=3V, I_D=9.4mA$ )
- Noise figure  $NF = 2.2$  dB at 1.8 GHz
- Typical device voltage  $V_D = 2$  V to 5 V
- Reverse isolation  $> 35$  dB (Appl.2)
- Pb-free (RoHS compliant) package


**Circuit Diagram**

**ESD (Electrostatic discharge) sensitive device, observe handling precaution!**

Type	Marking	Pin Configuration				Package
BGA427	BMs	1, IN	2, GND	3, +V	4, Out	SOT343

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Device current	$I_D$	25	mA
Device voltage	$V_{D,+V}$	6	V
Total power dissipation $T_S = 120$ °C	$P_{tot}$	150	mW
RF input power	$P_{RFIn}$	-10	dBm
Junction temperature	$T_j$	150	°C
Ambient temperature range	$T_A$	-65 ... 150	
Storage temperature range	$T_{stg}$	-65 ... 150	

**Thermal Resistance**

Junction - soldering point <sup>1)</sup>	$R_{thJS}$	$\leq 295$	K/W
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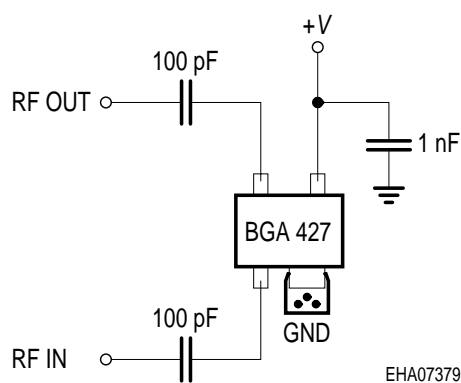
<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

**Electrical Characteristics** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

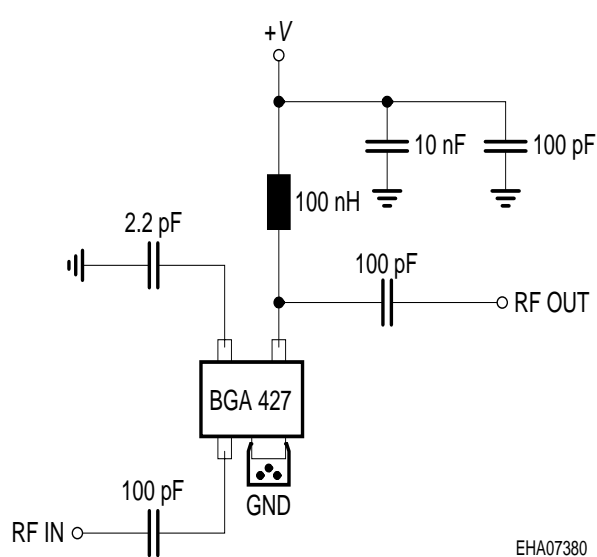
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>AC characteristics</b> $V_D = 3\text{ V}$ , $Z_0 = 50\Omega$ , Testfixture Appl.1					
Insertion power gain $f = 0.1\text{ GHz}$ $f = 1\text{ GHz}$ $f = 1.8\text{ GHz}$	$ S_{21} ^2$	-	27 22 18.5	-	dB
Reverse isolation $f = 1.8\text{ GHz}$	S12	-	22	-	
Noise figure $f = 0.1\text{ GHz}$ $f = 1\text{ GHz}$ $f = 1.8\text{ GHz}$	NF	-	1.9 2 2.2	-	
Intercept point at the output $f = 1.8\text{ GHz}$	$IP_{3out}$	-	+ 7	-	dBm
Return loss input $f = 1.8\text{ GHz}$	$RL_{in}$	-	>12	-	dB
Return loss output $f = 1.8\text{ GHz}$	$RL_{out}$	-	>9	-	

### Typical configuration

#### Appl.1



#### Appl.2



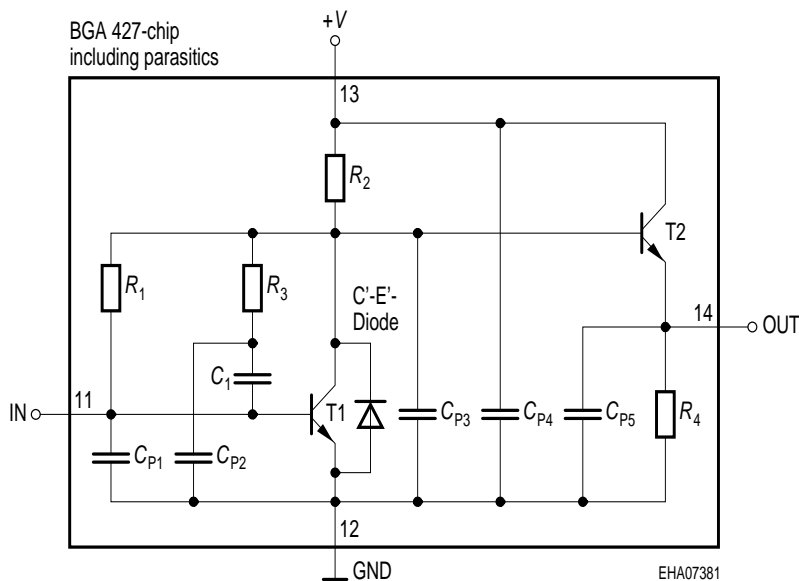
- Note: 1) Large-value capacitors should be connected from pin 3 to ground right at the device to provide a low impedance path (appl.1).  
 2) The use of plated through holes right at pin 2 is essential for pc-board-applications. Thin boards are recommended to minimize the parasitic inductance to ground.

**S-Parameters at  $T_A = 25\text{ }^\circ\text{C}$ , (Testfixture, Appl.1)**

$f$	$S_{11}$		$S_{21}$		$S_{12}$		$S_{22}$	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG

 $V_D = 3V, Z_0 = 50\Omega$ 

0.1	0.1382	-38.3	24.821	164.9	0.0022	50.7	0.6435	174.8
0.2	0.1179	-16	24.606	158.9	0.0046	71.8	0.6278	166.9
0.5	0.1697	-20.8	22.236	135.2	0.0104	83.8	0.54	147.3
0.8	0.1824	-56.9	18.258	115.4	0.0169	94.8	0.4453	140.2
0.9	0.1782	-69.1	17.152	109.4	0.0194	97.3	0.4326	139.4
1	0.176	-80.6	15.786	104	0.0225	98.3	0.4129	138.1
1.5	0.1827	-133.5	10.923	84.9	0.0385	99.7	0.3852	139.6
1.8	0.1969	-156.1	9.029	77	0.0479	99.3	0.3917	139.3
1.9	0.2021	-162.8	8.486	74.7	0.0517	98.9	0.3946	138.8
2	0.2116	-167.7	8.015	72.3	0.0549	98.8	0.3991	138.3
2.5	0.2437	172.8	6.259	63	0.0709	97.1	0.4202	134.6
3	0.258	153.3	5.103	55	0.0892	96.9	0.4477	131

**Spice-model BGA 427**


T1	T501
T2	T501
$R_1$	14.5k $\Omega$
$R_2$	280 $\Omega$
$R_3$	2.4k $\Omega$
$R_4$	170 $\Omega$
$C_1$	2.3pF
$C_{P1}$	0.2pF
$C_{P2}$	0.2pF
$C_{P3}$	0.6pF
$C_{P4}$	0.1pF
$C_{P5}$	0.1pF
C'-E'-diode	T1

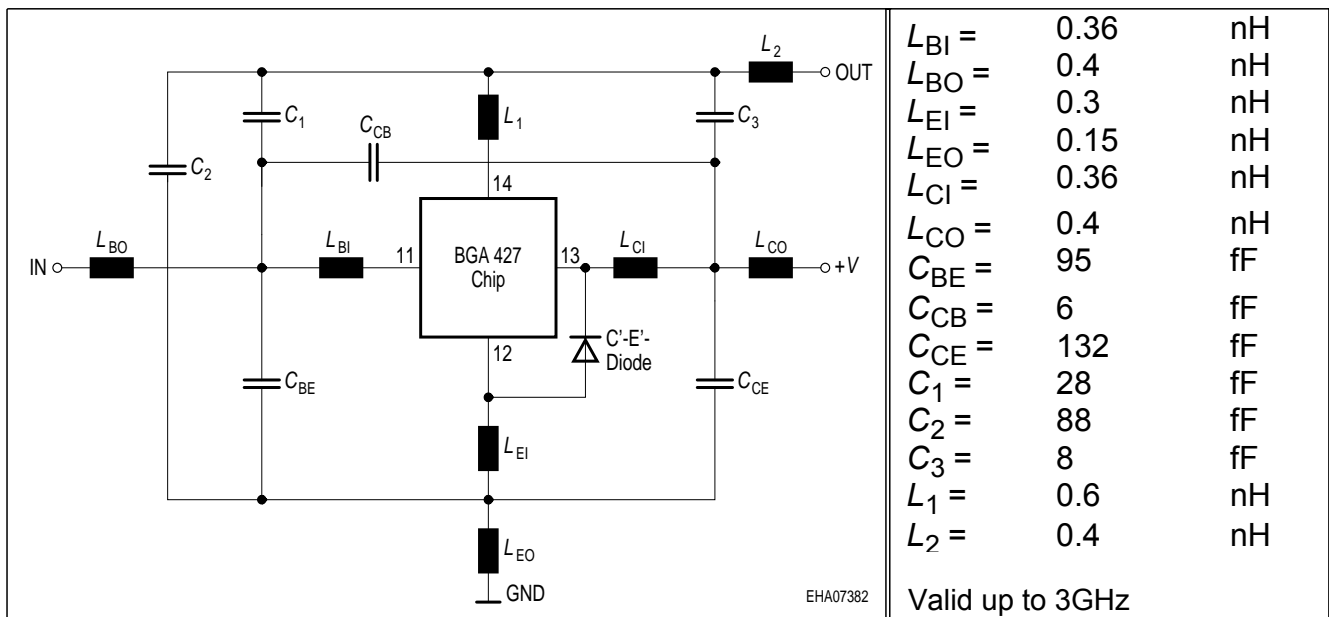
**Transistor Chip Data T1 (Berkley-SPICE 2G.6 Syntax) :**

IS =	0.21024	fA	BF =	83.23	-	NF =	1.0405	-
VAF =	39.251	V	IKF =	0.16493	A	ISE =	15.761	fA
NE =	1.7763	-	BR =	10.526	-	NR =	0.96647	-
VAR =	34.368	V	IKR =	0.25052	A	ISC =	0.037223	fA
NC =	1.3152	-	RB =	15	$\Omega$	IRB =	0.21215	A
RBM =	1.3491	$\Omega$	RE =	1.9289		RC =	0.12691	$\Omega$
CJE =	3.7265	fF	VJE =	0.70367	V	MJE =	0.37747	-
TF =	4.5899	ps	XTF =	0.3641	-	VTF =	0.19762	V
ITF =	1.3364	mA	PTF =	0	deg	CJC =	96.941	fF
VJC =	0.99532	V	MJC =	0.48652	-	XCJC =	0.08161	-
TR =	1.4935	ns	CJS =	0	fF	VJS =	0.75	V
MJS =	0	-	XTB =	0	-	EG =	1.11	eV
XTI =	3	-	FC =	0.99469	-	TNOM	300	K

**C'-E'-Diode Data (Berkley-SPICE 2G.6 Syntax) :**

IS =	2	fA	N =	1.02	-	RS =	20	$\Omega$
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All parameters are ready to use, no scaling is necessary

**Package Equivalent Circuit:**


Extracted on behalf of Infineon Technologies AG by:  
 Institut für Mobil-und Satellitentechnik (IMST)

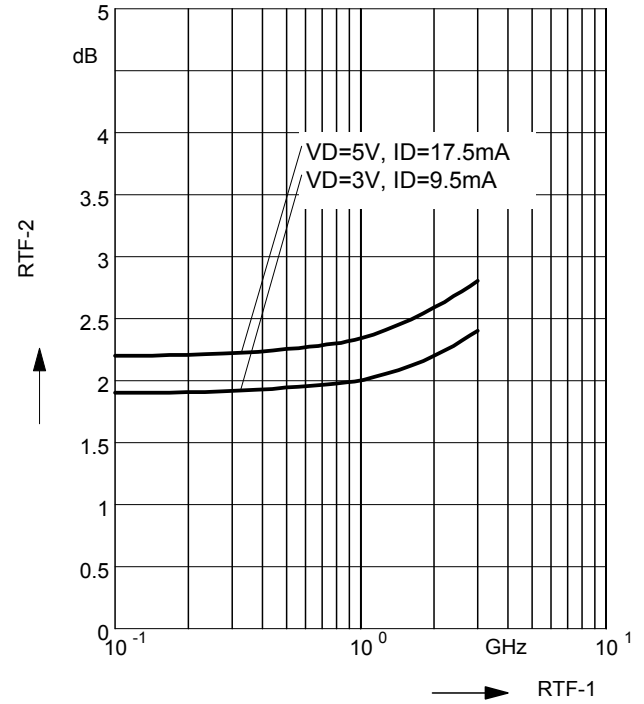
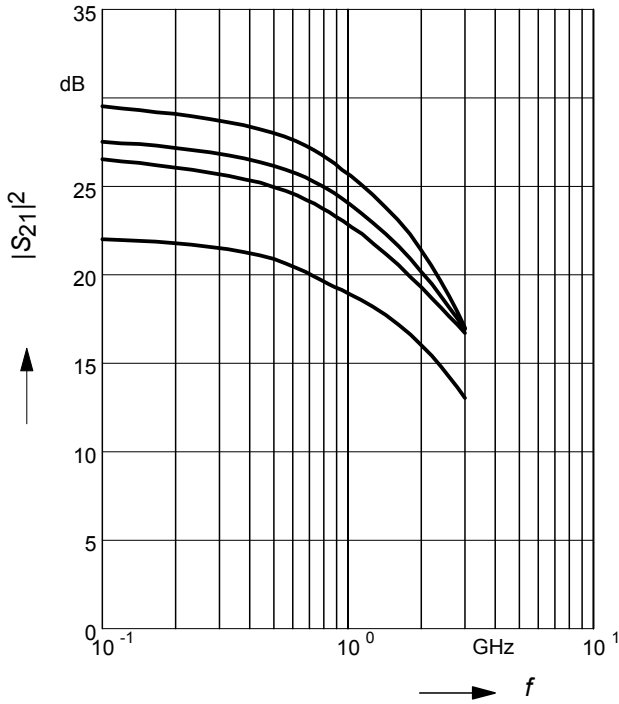
For examples and ready to use parameters please contact your local Infineon Technologies distributor or sales office to obtain a Infineon Technologies CD-ROM or see Internet:  
<http://www.infineon.com/silicondiscretres>

**Insertion power gain  $|S_{21}|^2 = f(f)$**

**Noise figure  $NF = f(f)$**

$V_D, I_D = \text{parameter}$

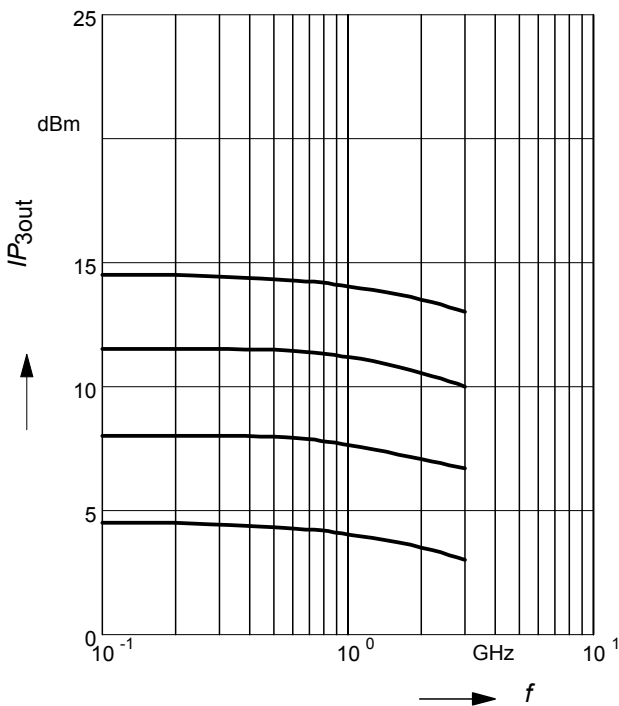
$V_D, I_D = \text{parameter}$



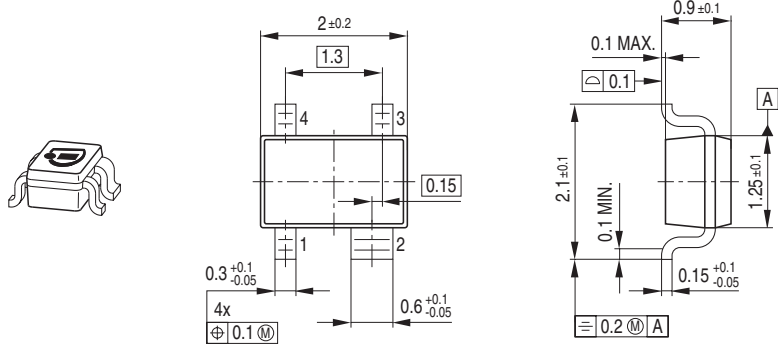
**Intercept point at the output**

$IP_{3out} = f(f)$

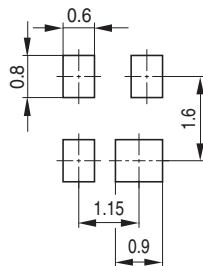
$V_D, I_D = \text{parameter}$



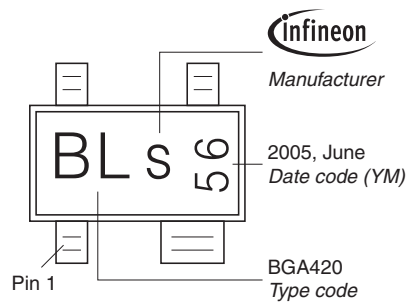
Package Outline



Foot Print

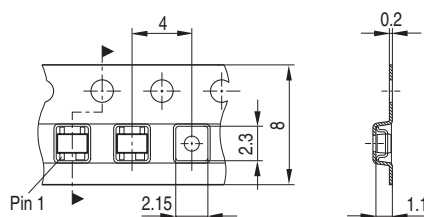


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel  
 Reel ø330 mm = 10.000 Pieces/Reel



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