100V, 1A, COT Mode Buck Converter

EA8961

Datasheet

General Description

The EA8961 is a 100V, 1A, COT mode buck converter. Built-in high/low side Power-MOSFETs has high efficiency at light load and heavy load. COT mode operation provides very fast transient response. The EA8961 output voltage accuracy is ±2% over the full temperature range. The EA8961 has complete protection functions, including peak current limit, OTP and UVLO protection.

The EA8961 operation mode can be set by using FPWM pin. The device can works in CCM mode over full output loading current range or works in DCM mode at light loading current. The EA8961 can be designed as a buck-boost architecture to generate a negative voltage output. At this time, the reference voltage of the device is not GND but the negative voltage output, so the input range is VIN+|VOUT|.

Features

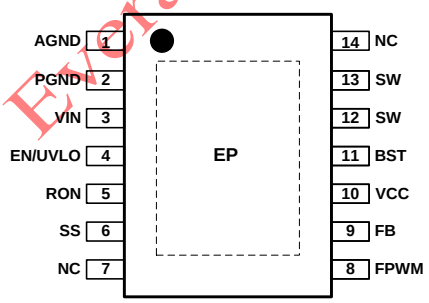
- 5V to 100V Input Voltage Range
- Built-in High/Low Side Power MOSFETs
- 1A Continuous Load Current
- ±2% Output Voltage Accuracy
- COT Mode Operation & Fast Transient Response
- Programmable Light Load operation (CCM or DCM)
- Nearly Constant Switching Frequency (Maximum 1MHz)
- Programmable Soft-Start Function
- Peak Current Limit
- Input UVLO Protection
- Auto Recovery OTP Protection

Applications

- IGBT Gate Driver Power Supply
- Industrial Programmable Logic Controller
- Telecom DC/DC Power Supply
- Power Line Communication

Pin Configurations

(TOP VIEW)



TSSOP14L-EP

Pin Description

Pin Name	Function Description	Pin No.
AGND	Analog ground.	1
PGND	Power ground.	2
VIN	Power input.	3
EN/UVLO	The device turns on/turns off control input and UVLO Comparator input.	4
RON	On time setting pin. Connect this pin to VIN pin via a resistor to set the on time.	5
SS	Soft-Start time setting pin.	6
NC	Not Connect.	7, 14
FPWM	Mode selecting pin. Connect this pin to AGND for DCM mode. Connect this pin to VCC for CCM mode.	8
FB	Feedback voltage input.	9
VCC	Internal circuit power supply.	10
BST	The power input of the internal high side N-MOSFET gate driver.	11
SW	Switching output.	12, 13
EP	Exposed Pad. Connect to AGND for dissipate heat.	

Function Block Diagram

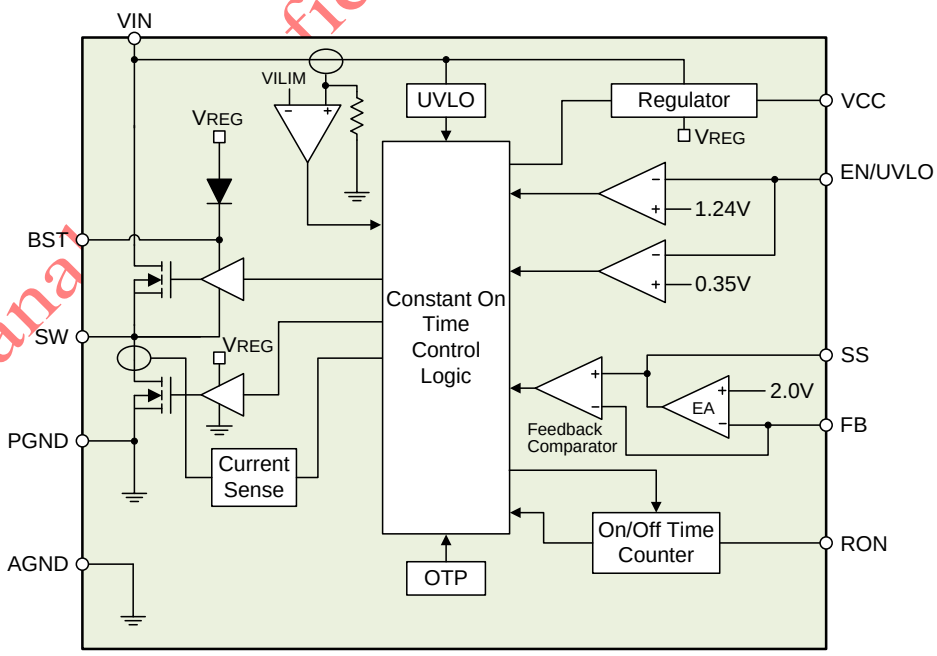


Figure 1. EA8961 internal function block diagram

Absolute Maximum Ratings

Parameter	Value
Input Voltage (V_{IN})	-0.3V to +100V
EN/UVLO Pin Input Voltage (V_{EN})	-0.3V to +100V
RON Pin Voltage (V_{RON})	-0.3V to +100V
BST Pin Voltage (V_{BST})	-0.3V to +107V
VCC Pin Voltage (V_{CC})	-0.3V to +7V
FPWM Pin Voltage (V_{FPWM})	-0.3V to +7V
SS Pin Voltage (V_{SS})	-0.3V to +7V
FB Pin Voltage (V_{FB})	-0.3V to +7V
SW Pin Voltage (V_{SW})	-1.5V to +100V
BST Pin to SW Pin Voltage	-0.3V to +7V
BST Pin to VCC Pin Voltage	100V
SW Pin to AGND Pin Voltage (20ns)	-3V
Ambient Temperature operating Range (T_A)	-40°C to +85°C
Maximum Junction Temperature (T_{Jmax})	+150°C
Lead Temperature (Soldering, 10 sec)	+260°C
Storage Temperature Range (T_S)	-65°C to +150°C

Note (1): Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability and lifetime.

Package Thermal Characteristics

Parameter	Value
TSSOP14L-EP Thermal Resistance (θ_{JC})	23.7°C/W
TSSOP14L-EP Thermal Resistance (θ_{JA})	39.5°C/W
TSSOP14L-EP Power Dissipation at T_A=25°C (P_{Dmax})	3.2W

Note (1): P_{Dmax} is calculated according to the formula: $P_{DMAX}=(T_{JMAX}-T_A)/\theta_{JA}$.

Electrical Characteristics

V_{IN}=48V, T_A=25°C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current						
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		35	60	uA
Quiescent Current	I_Q	V_{FB} = 3V, I_{LOAD} = 0A		1.3	2	mA
VCC Power Supply						
VCC Voltage	V_{CC}	I_{CC} = 20mA	4.5	5.0	5.5	V
VCC Current	I_{CC}				30	mA
UVLO Threshold	V_{UVLO}	V_{CC} Rising		3.85		V
UVLO Hysteresis	V_{UV-HYS}			200		mV
VIN-VCC Dropout Voltage		V_{IN} = 5V, I_{CC} = 20mA		600		mV
Power MOSFET						
High Side MOSFET On-Resistance	$R_{DS(ON)-HM}$	I_{SW} = 0.5A		300		mΩ
Low Side MOSFET On-Resistance	$R_{DS(ON)-LM}$	I_{SW} = 0.5A		150		mΩ
BST Pin UVLO Threshold				2.9		V
BST Pin UVLO Hysteresis				200		mV
Current Limit						
High Side MOSFET Current Limit	I_{LIM-HM}			1.61		A
Low Side MOSFET Souring Current Limit	$I_{SOURCE-LM}$		1.3	1.6	1.9	A
Low Side MOSFET Sinking Current Limit	$I_{SINK-LM}$			3		A
High Side MOSFET Current Limit Respose Time	t_{LIM-HM}	I_{LIM-HM} threshold detect to MOSFET turn off		100		ns
High Side MOSFET Current Limit Turn off Time	t_{OFF}	FB = 0V, V_{IN} = 72V		16.5		μs
	t_{OFF1}	FB = 0.1V, V_{IN} = 72V		13		μs
	t_{OFF2}	FB = 1V, V_{IN} = 72V		2.7		μs
FPWM Pin						
FPWM Pin Input High Voltage	V_{FPWM-H}		3			V

FPWM Pin Input Low Voltage	V_{FPWM-L}				1	V
Zero Current Detection	I_{ZX}	FPWM = 0V		22.5		mA
Feedback Pin						
FB Pin Voltage Accuracy	V_{REF}		1.96	2	2.04	V
FB Pin Input Current	I_{FB}				100	nA
SS Pin						
Soft-Start Current	I_{SS}	SS = 0.5V		10		μA
EN/UVLO Pin						
EN/UVLO Pin UVLO Voltage Threshold	V_{EN-TH}	EN/UVLO Rising	1.2	1.24	1.27	V
EN/UVLO Pin Shutdown Mode Voltage Threshold	V_{EN-SD}	EN/UVLO Falling	0.29	0.35		V
EN/UVLO Pin Shutdown Mode Voltage Hysteresis	$V_{EN-SD-TH}$			50		mV
EN/UVLO Pin Input Current	I_{EN}	EN/UVLO = 1.4V	15	20	25	μA
Thermal Shutdown						
Thermal Shutdown Threshold	T_{OTP}			175		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
(2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

Ordering Information

Part Number	Package Type	Packing Information
EA8961SCR	TSSOP14L-EP	Tape & Reel

Note (1):"SC": Package type code.
(2):"R": Tape & Reel.

Application Circuit Diagram

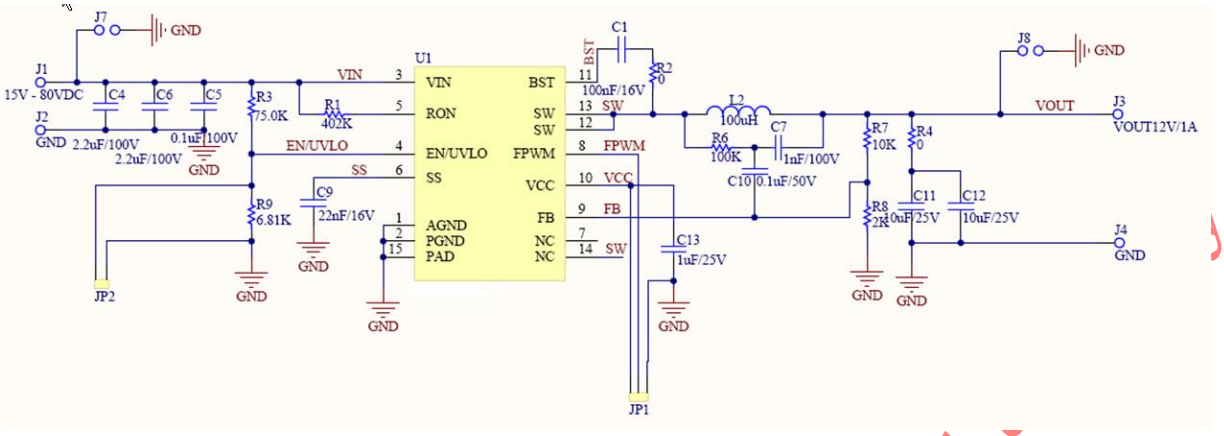


Figure 2. Typical buck converter application circuit

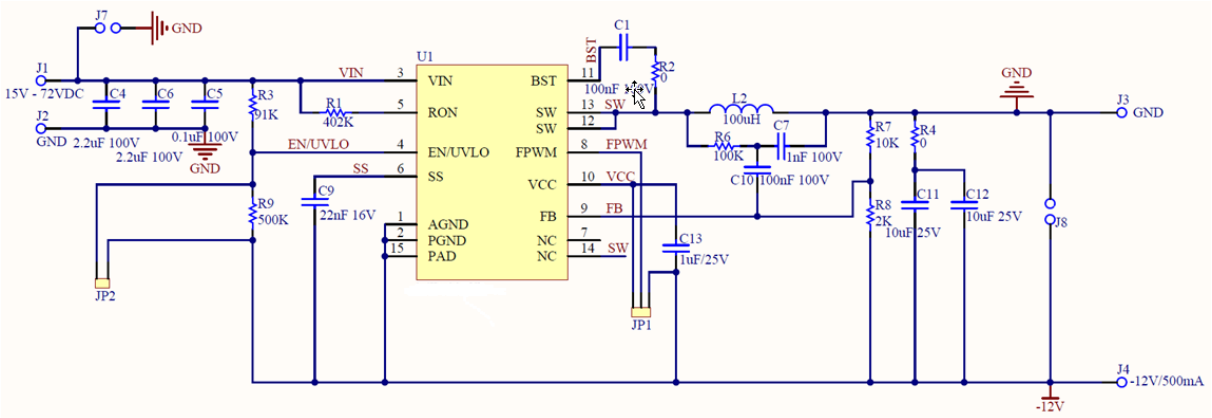


Figure 3. Negative output voltage application circuit

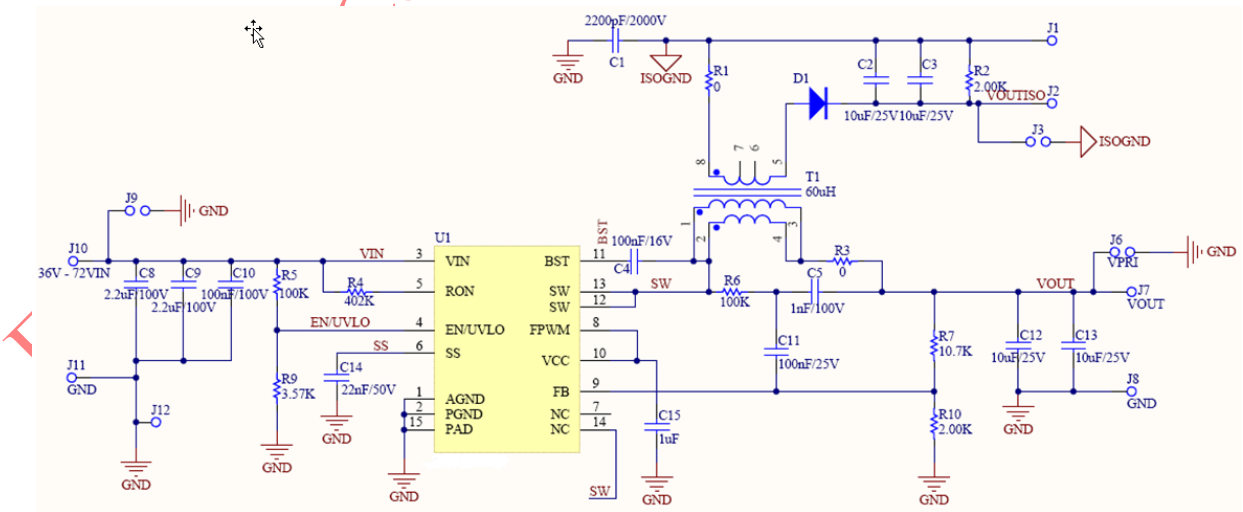
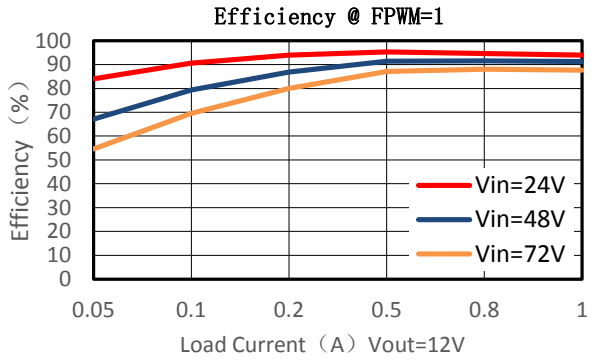
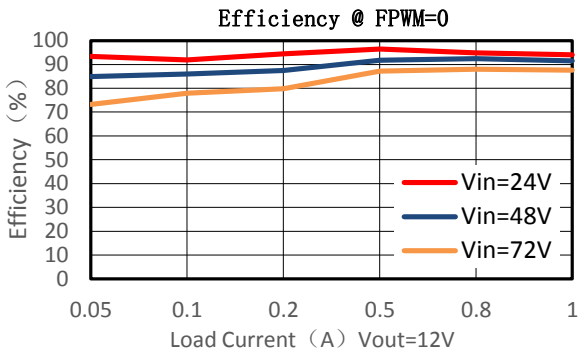


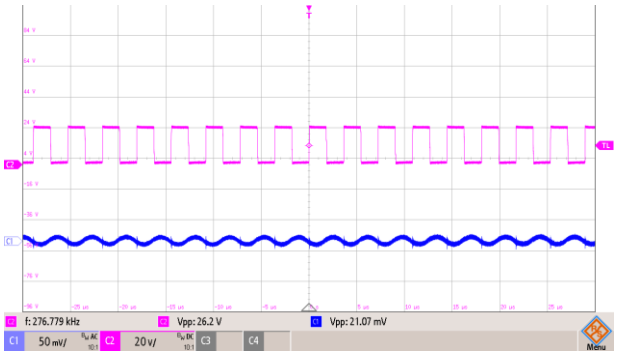
Figure 4. 12V,10W isolated DC/DC application circuit

Typical Operating Characteristics

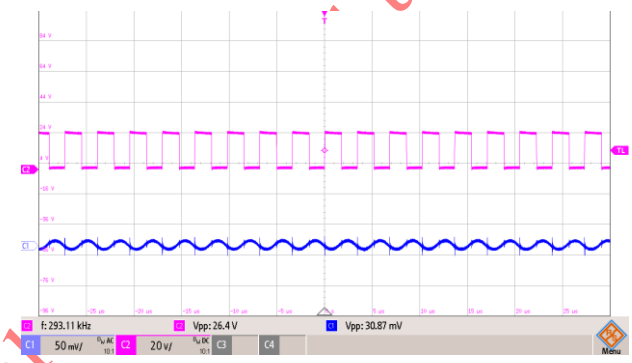
Buck Converter, T_A=25°C, unless otherwise noted



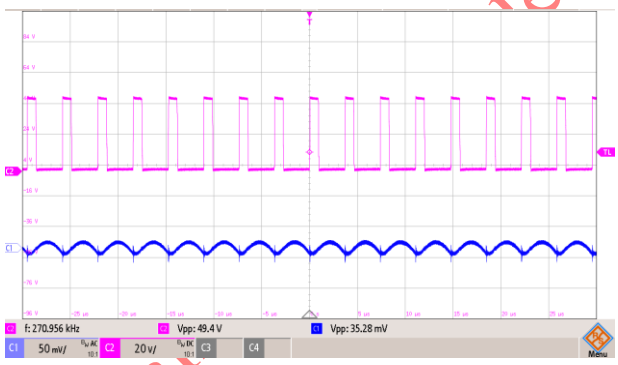




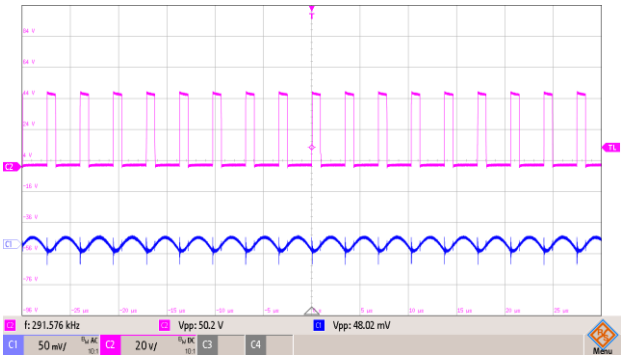
CH1:V_{OUT} CH2:SW
V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0.05A, FPWM=1



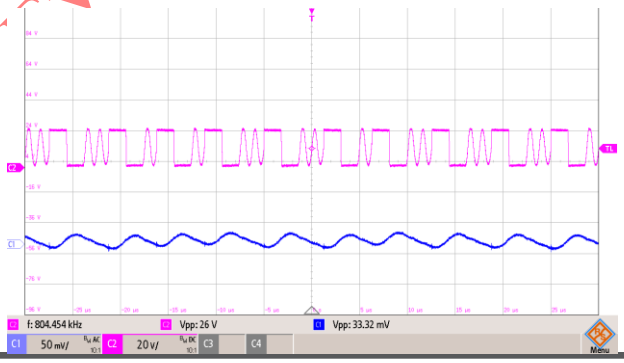
CH1:V_{OUT} CH2:SW
V_{IN}=24V, V_{OUT}=12V, I_{OUT}=1A, FPWM=1

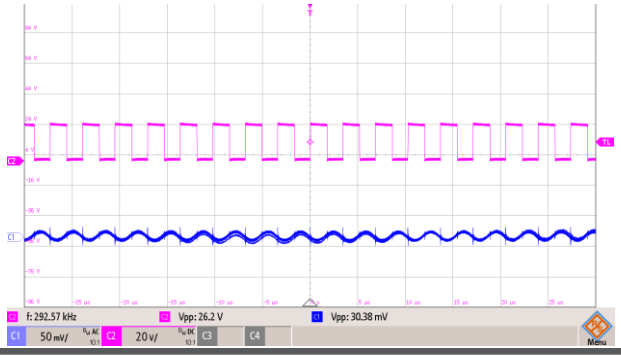


CH1:V_{OUT} CH2:SW
V_{IN}=48V, V_{OUT}=12V, I_{OUT}=0.05A, FPWM=1

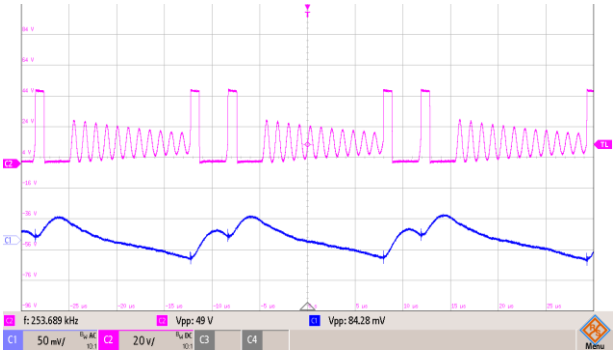


CH1: V_{OUT} CH2:SW
VIN=48V, V_{OUT}=12V, I_{OUT}=1A, FPWM=1

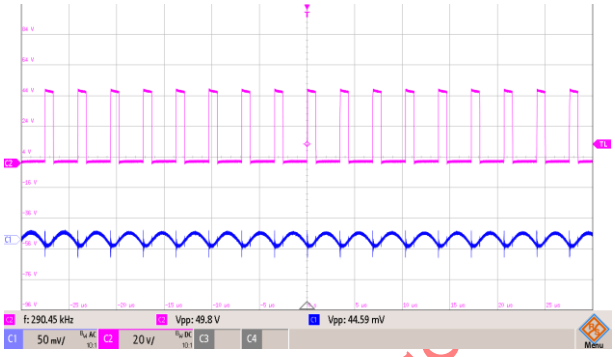




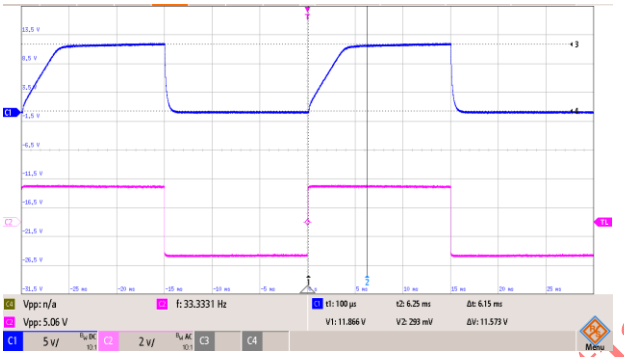
CH1: V_{OUT} CH2:SW
V_{IN}=24V, V_{OUT}=12V, I_{OUT}=0.05A, FPWM=0



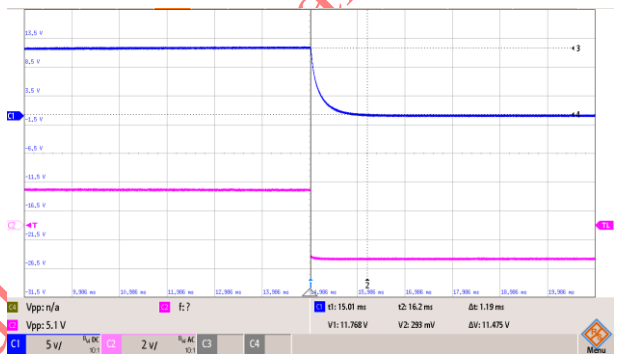
CH1: V_{OUT} CH2:SW
V_{IN}=24V, V_{OUT}=12V, I_{OUT}=1A, FPWM=0



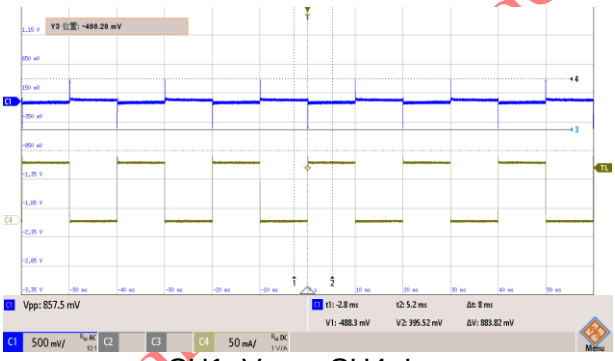
CH1: V_{OUT} H2:SW
V_{IN}=48V, V_{OUT}=12V, I_{OUT}=0.05A, FPWM=0



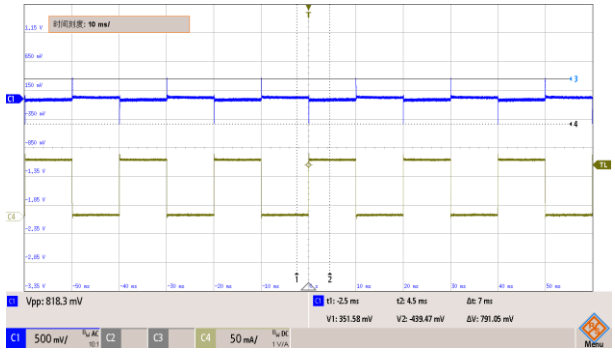
CH1: V_{OUT} CH2:SW
V_{IN}=48V, V_{OUT}=12V, I_{OUT}=1A, FPWM=0



CH1: V_{OUT} CH2:EN
EN Start-up, V_{IN}=48V, I_{OUT}= 1A



CH1: V_{OUT} CH2:EN
EN Shutdown, V_{IN}=48V, I_{OUT}=1A

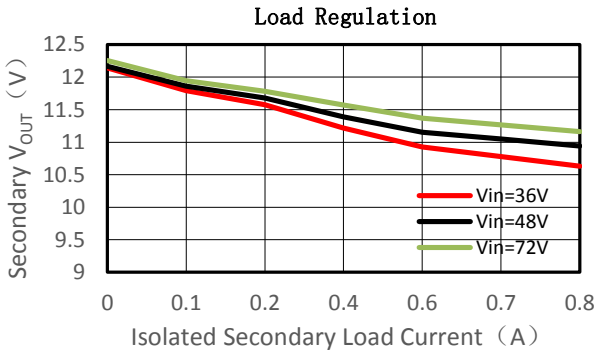


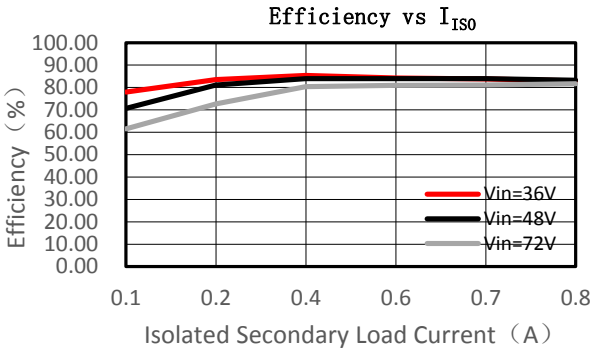
CH1: V_{OUT} CH4: I_{OUT}
Load Transient (0A-1A), V_{IN}=48V

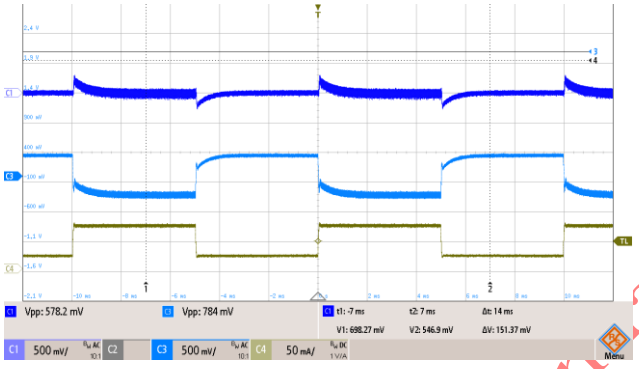
CH1: V_{OUT} CH4: I_{OUT}
Load Transient (0.05A-1A), V_{IN}=48V

Typical Operating Characteristics

Isolated DC/DC Converter, T_A=25°C, unless otherwise noted







CH1:V_{OUT}，CH3:V_{OUTISO}，CH4:I_{OUTISO}
Secondary LoadTransient (0.25A-0.75A),
V_{IN}=48V

CH1:V_{IN}，CH2: V_{OUT}，CH3:V_{OUTISO}
VIN Start-up, I_{ISO}=500mA

Functional Description

Control Logic

The control structure of EA8961 includes a comparator and a single pulse on-timer generating circuit, which compares the output voltage feedback (FB) with the voltage (VSS) of the soft-start (SS) pin, if the FB voltage is lower than VSS, the internal main switch is turned on, and the turn-on time is determined by the input voltage and the resistance RON. After the on-time, the main switch must remain in the off state, forced to close by the minimum off-time OFF-time, until the FB voltage is lower than VSS again, and the single-pulse on-timer circuit works. During fast start-up or when there is a sudden increase in load current, the regulator operates with a minimum off-time per cycle. When regulating the output in steady state, the off-time is automatically adjusted to produce the duty cycle required for output voltage regulation.

EA8961 works in continuous conduction CCM mode under heavy load. If the FPWM pin is grounded or floating, the system works in discontinuous conduction DCM mode under light load, and it works in continuous conduction mode under sufficient load. If the FPWM pin is connected to VCC, the system works in continuous conduction CCM mode under light load and heavy load. The continuous operating frequency (in Hz) is determined by the RON pin resistance, calculated according to formula as below, and RON is expressed in ohms.

$$F_{SW} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times R_{ON}} \text{Hz}$$

The output voltage is set by two external resistors (R_{FB1}, R_{FB2}). Calculate the output voltage according to formula as below, where V_{REF}=2V is the feedback reference voltage.

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} V$$

VCC Power Supply

The EA8961 contains an internal high voltage LDO regulator with a nominal output voltage of 5 V. VCC regulator internal current limit minimum 30mA. This regulator powers internal circuitry, including synchronous Low-side MOSFET gate driver and logic. At the same time, VCC charges the capacitance of the BST pin through an internal diode to provide power for the high-voltage side High-side MOSFET gate driver. The system starts up when the voltage on the VCC pin reaches the undervoltage lockout ($VCC_{\_UVLO}$) threshold of 3.85 V.

Soft-Start Circuit

The EA8961 reduces current surge through soft-start function. When the EN/UVLO pin is above the EN/UVLO standby threshold 1.24V, and VCC exceeds the undervoltage value 3.85V, an internal 10uA current source switches the external capacitor at the SS pin from 0 V is charged to 2V. Soft-start function ends when the SS capacitor charges to the 2V. A ramp voltage at the SS pin produces a controlled, monotonic output voltage start-up. In all applications, a minimum soft-start capacitor of 1nF must be used.

On-Time Generator Circuit

The turn-on time of the main switch High side MOSFET is determined by the resistance of RON, which is inversely proportional to the input voltage (VIN). The system has a nearly constant frequency. The conduction time can be calculated as below, and RON is expressed in ohms.

$$t_{ON} = \frac{1.008 \times 10^{-10} \times R_{ON}}{V_{IN}} s$$

To set the continuous conduction mode switching frequency (FSW in Hz), the RON resistance is determined by equation shown as below:

$$R_{ON} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}} \Omega$$

Select the minimum on-time of RON (when VIN is maximum) must be greater than 150ns to work properly. This minimum on-time requirement limits the maximum switching frequency for applications with higher VIN and lower VOUT.

Current Limit

The EA8961 provides a current limited off-timer with adjustable off time. If the current peak in the buck switch exceeds 1.6A, the on-timer is immediately terminated and a non-resettable off-timer is started. The length of the off time is determined by the FB voltage and the input voltage VIN. For example, when V_{FB}=0.1V and VIN=72V, the off time is set to 13us. This can occur if the output is shorted or during the initial stages of start-up. In output overload conditions where FB voltage is greater than 0V, the current limit trip time is shortened. The current limit turn-off time t_{OFF} is calculated by formula：

$$T_{OFF(CL)} = \frac{V_{IN}}{20V_{FB} + 4.35} \mu s$$

EN/UVLO Function

The EA8961 contains a dual-level undervoltage lockout (EN/UVLO) circuit. When the EN/UVLO pin voltage is below 0.35V, the regulator is in low current shutdown mode. When the EN/UVLO pin voltage is greater than 0.35V but less than 1.24V, the system is in standby mode. In standby mode, the VCC regulator operates, but the converter switch remains off. When the voltage at the VCC pin exceeds the VCC rising threshold 3.85V and the EN/UVLO pin voltage is greater than 1.24V, the system switch works. An external resistor divider from VIN to GND can be used to set the minimum operating voltage.

EN/UVLO Pin Voltage	VCC Regulator	Mode	Description
< 0.35V	Turn-off	Shutdown	VCC regulator turn off, MOSFET turn off
0.35V~1.24V	Turn-on	Standby	VCC regulator turn on, MOSFET turn off
> 1.24V	VCC < $VCC_{\_UVLO}$	Standby	VCC regulator turn on, MOSFET turn off
	VCC > $VCC_{\_UVLO}$	Operation	VCC regulator turn on, MOSFET turn on

If the EN/UVLO set point is not required, the EN/UVLO pin can be driven by a logic signal as an enable input, or connected directly to the VIN pin. If EN/UVLO is directly connected to the VIN pin, the regulator will start operating when VCC voltave over the $VCC_{\_UVLO}$ voltage.

FPWM Function

By setting the FPWM pin voltage, CCM or DCM operation mode can be selected at light load. When the FPWM pin is grounded or floating, the pulse-skipping PFM mode and the zero-current detection circuit are enabled. When the inductor current drops close to zero, the zero-crossing detector turns off the low-side MOSFET, allowing the EA8961 to operate in DCM mode at light loads. In the DCM state, the switching frequency decreases as the load decreases. At the same time, the internal ripple injection circuit works for a typical buck application circuit. This feature applies over the entire load and input voltage range. Eliminates the need for an external feedback ripple injection circuit.

If the FPWM pin is pulled high, the EA8961 will work in CCM mode under any load condition. CCM operation reduces efficiency at light loads, but improves the output's transient response to step load changes and provides a nearly constant switching frequency. Additionally, the isolation transformer output structure requires continuous conduction mode. The internal ripple injection circuit is disabled in CCM mode. To generate optimal ripple at the FB node, an external ripple injection circuit or an ESR resistor in series with the output capacitor is required.

FPWM Pin Connecting	Logic	Description
GND or Floating	0	DCM mode at light load. The internal ripple injection circuit is working and eliminates the need for an external feedback ripple injection circuit.
VCC	1	CCM mode at light load. The internal ripple injection circuit is disabled and an external feedback ripple injection circuit is required.

Application Information

Typical Buck Converter

A typical application is a synchronous buck converter, which operates from 15V to 80V and provides a stable 12V output voltage with a maximum output current capability of 1A.

Parameter	Design Value
Input Voltage	15V to 80V
Output Voltage	12V
Output Loading	1A
Typical Frequency	300kHz
Light Load Operating	CCM, FWPM=1

Output Voltage Setting

Set the output voltage by selecting R_{FB1} and R_{FB2}:

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} V$$

Switching Frequency Setting

The duty cycle required to maintain the output at the minimum input voltage limits the maximum switching frequency of the EA8961. The maximum value of the minimum forced off time t_{OFF_min} limits the duty cycle and therefore the switching frequency. The maximum frequency to avoid output attenuation at minimum input voltage can be calculated.

$$F_{SW.max(@V_{IN.min})} = \frac{V_{IN.min} - V_{OUT}}{V_{IN.min} \times t_{OFF\_min}(ns)}$$

For example, based on the maximum frequency limited by t_{OFF_min} minimum off time, i.e. 170ns calculated as FSW, max(@VIN,min)=1.2MHz. This value is higher than 1MHz, which is the maximum possible operating frequency of EA8961.

At maximum input voltage, the maximum switching frequency of the EA8961 is limited to a minimum time t_{ON_min}, thereby limiting the minimum duty cycle of the converter. The maximum frequency at maximum input voltage can be calculated using equation shown as below.

$$F_{SW.max(@V_{IN.min})} = \frac{V_{OUT}}{V_{IN.max} \times t_{ON\_min}(ns)}$$

Using above equation and T_{ON_min}(typ)=150ns, the maximum achievable switching frequency is FSW, max(@VIN, min)=1000 kHz. Taking this value as the maximum possible operating switching frequency over the input voltage range, the design chooses a nominal switching frequency of FSW=300kHz. The value RON of the resistor sets the nominal switching frequency according to below equation. For the application of FSW=300kHz, RON is calculated as 396kΩ (taken as 402 kΩ).

$$R_{ON} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}} \Omega$$

Selecting the inductor

Choose the inductor to limit the inductor ripple current to between 20% and 40% of the maximum load current. The minimum value of inductance required in this application can be calculated according to the equation:

$$L_{min} = \frac{V_O \times (V_{IN.max} - V_O)}{V_{IN.max} \times F_{SW} \times I_{O.max} \times 0.4}$$

According to above equation, at VIN=80V, the minimum value of the inductor is calculated to be 85µH, and the inductor current ripple will be 40% of the maximum load current. Considering the inductance variation and inductance saturation margin, this design chooses L=100µH.

In the design of the chip with a maximum output current of 1A, in addition to the maximum peak current, the saturation current of the inductor also needs to be considered. In an overload or short circuit condition, the peak value of the inductor current will be limited by the high-side FET current limit. According to the high-side MOSFET current limit specification in the electrical characteristics, an inductor with a saturation current rating greater than 1.9A (maximum) should be selected.

Selecting the Output Capacitor

The output capacitor is chosen to limit the capacitive ripple at the output of the buck converter. The required output capacitance for the ripple voltage ΔVO across the capacitor is calculated according to equation:

$$C_{OUT} = \frac{\Delta I_{L.max}}{8 \times F_{SW} \times \Delta V_{O.ripple}}$$

If the ΔVO, ripple=10mV, then the C_{OUT}=15µF. Select 2 standard 10µF ceramic capacitors in parallel and the C_{OUT} should use X7R type capacitors rated at 25V or higher to limit capacitance reduction due to DC bias.

Selecting the Serial Ripple Resistor R_{ESR} when FPWM = 1

If FPWM=1, i.e. when connected to VCC, the FPWM pin is pulled high, a resistor R_{ESR} in series with the output capacitor or an external ripple injection circuit must be selected to ensure sufficient ripple injection at the feedback pin FB (>25mV). The ripple generated by R_{ESR} is proportional to the inductor current ripple, therefore, R_{ESR} should be calculated from the minimum inductor current ripple occurring at the minimum input voltage. Calculate RESR according to formula shown as below.

$$R_{ESR} \geq \frac{25mV \times V_O}{V_{REF} \times \Delta I_{L.min}}$$

When VO=12V, V_{REF}=2V and ΔIL, min=81 mA (at VIN, min=15V), it requires R_{ESR} to be greater than or equal to 1.87Ω. When R_{ESR}=2Ω is selected, the maximum output voltage ripple is about 700 mV at the maximum VIN. However, due to the internal DC error correction loop, load and line regulation will be greatly improved despite adding a larger R_{ESR} in the circuit.

For applications requiring lower output voltage ripple, a Type 2 or Type 3 ripple injection circuit must

be used, as described in Ripple Configuration. In this design example, when FPWM=1, a 0Ω ESR resistor is selected and an external Type 3 ripple injection circuit is used.

Selecting the VCC and Bootstrap Capacitors

The VCC capacitor charges the bootstrap capacitor C_{BST} when the high-side switch is turned off, and supplies the internal logic circuits and the low-side MOSFET gate driver. The bootstrap capacitor powers the gate drive of the high-side MOSFET during its on-time. The optimal value of C_{VCC} is 1μF. The best value for C_{BST} is 10nF. Both capacitors must be high quality X7R ceramic capacitors.

Selecting the Intput Capacitor

The input capacitor must be large enough to limit the input voltage ripple to acceptable levels. The input capacitance C_{IN} required for the worst-case input ripple for ΔVIN ripple.

$$C_{IN} = \frac{I_{O.max} \times D \times (1 - D)}{\Delta V_{IN.ripple} \times F_{SW}}$$

According to above formula, the value of the input capacitor is calculated to be about 1.68μF when D=0.5. Considering that the capacitance decreases with the applied voltage, two 2.2μF standard value ceramic capacitors are selected. The input capacitors should be rated to withstand the maximum input voltage under all operating and transient conditions. This design selects 100V, X7R ceramic capacitors. A 0.1μF input ceramic capacitor is required as a bypass path for the high frequency components of the input switch current. This bypass capacitor must be placed directly across VIN and PGND (pins 3 and 2) close to the IC. C_{IN} value and location are critical to reducing switching noise and transients.

Selecting the C_{SS} Capacitor

A capacitor connected to the SS pin determines the soft-start time. The capacitance value is determined by equation:

$$C_{SS} = \frac{I_{SS} \times t_{Startup}}{V_{SS}}$$

C_{SS}=22nF and V_{SS} = 2V, I_{SS} = 10μA, the soft-start time is close to 4ms.

Selecting the EN/UVLO Pin Resistor

EN/UVLO resistors R3 (R_{UV2}) and R9 (R_{UV1})set the input undervoltage lockout threshold and hysteresis value according to equations shown as below:

$$V_{IN(HYS)} = I_{UVLO(HYS)} \times R_{UV2}$$

$$V_{IN,UVLO(rising)} = V_{UVLO(TH)} \times \left(1 + \frac{R_{UV2}}{R_{UV1}}\right)$$

Where I_{UVLO_HYS} = 20μA, V_{UVLO_TH} = 1.24V.

Isolated DC/DC Converter

Another typical application example is an isolated DC/DC converter operating from an input voltage range of 36V to 72V. It provides a stable 12V isolated output voltage with an output power capability of 10W. The EA8961 isolated DC/DC application is designed to operate on a nominal 48V DC supply (line variation ranges from 36V to 72V) and can provide a highly efficient 12V isolated output solution with a secondary load current capability of 0A to 0.8A. In applications, the primary coil can be left unloaded. The switching frequency is nominally 300kHz. This design achieves a peak efficiency of over 88%.

Parameter	Design Value
Input Voltage	36V to 72V
Output Voltage	12V (±10%)
Output Loading	0A to 0.8A
Typical Frequency	300kHz
Peak Efficiency	≥ 87%
Operating Mode	FWPM=1

V_{OUT} and The Transformer Turns Ratio

The primary output voltage of an isolated DC/DC converter should not exceed half the minimum input voltage. Therefore, with a minimum VIN of 36V, the primary output voltage (VOUT) should not be higher than 18 V. The isolated output voltage of VOUTISO in Figure 4 is scaled 1:1 by selecting the turns ratio (N1:N2). Using this turns ratio, the primary output voltage, V_{OUT}, is calculated as below:

$$V_{OUT} = \frac{V_{OUTISO} + V_{FD1}}{\frac{N_2}{N_1}} = \frac{V_{OUTISO} + 0.7V}{1} = 12.7V$$

The 0.7V(V_{FD1}) of VOUTISO represents the forward voltage drop of the secondary rectification diode. By choosing the correct feedback resistor, the primary output voltage V_{OUT} is set to 12.7V and the secondary voltage is regulated to 12V.

Selecting Secondary Rectifier Diode

The secondary rectifier diode must be able to block the voltage reflected from the maximum input voltage to the secondary switching node. The minimum diode reverse voltage V_{RD1} rating is given by:

$$V_{RD1} = V_{IN(max)} \times \frac{N_2}{N_1} + V_{OUTISO} = 72V \times 1 + 12V = 84V$$

In this application, a diode with a reverse voltage rating of 100V or higher must be selected considering the worst-case transient input voltage.

External Ripple Injection Circuit

The EA8961 FPWM pin must not be grounded or kept open in an isolated DC/DC converter. The ripple injection circuit chooses the third type. See Ripple Configuration for ripple injection design information.

Output Capacitor (C_{VISO})

The output capacitor of an isolated DC/DC converter conducts higher ripple current than the output capacitor of a buck converter. The ripple voltage across the isolated output capacitor is calculated from the time the rectifier diode is off. During this time, the entire output current is supplied by the output capacitor. The required capacitance for the worst-case ripple voltage can be calculated as below, where ΔVISO is the expected ripple voltage at the secondary output.

$$C_{VISO} = \frac{I_{ISO}}{\Delta V_{ISO}} \left(\frac{V_{PRI}}{V_{IN(MIN)}} \right) \times \frac{1}{f_{sw}}$$

The equation is an approximation that ignores the ripple components associated with the ESR and ESL of the output capacitor. For ΔV_{ISO}=100mV, it requires a minimum C_{VISO}=11.12μF. Here we choose two 10μF X7R ceramic capacitors.

Ripple Configuration

The EA8961 adopts a constant on-time (COT) control scheme. The turn-on time of the system switch is determined by the on-timer, and the turn-off time of the system switch is obtained by comparing the feedback voltage V_{FB} with the reference voltage. Therefore, for stable operation, the FB voltage must decrease monotonically and be in phase with the inductor current during the off-time. Additionally, the change in feedback voltage V_{FB} during the switch off time must be large enough to dominate any noise present at the feedback node.

Table 1 shows three different ways to generate the proper voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the converter output ripple to the feedback node FB. The output voltage ripple has two components: (1) The capacitor ripple generated by the inductor current ripple charging or discharging the output capacitor. (2) Resistor ripple caused by inductor current ripple through output capacitor ESR and R3. The capacitor ripple is not synchronous with the inductor current, and the capacitor ripple does not decrease monotonically during the off-time. The resistor ripple is in phase with the inductor current and decreases monotonically during the off time. Therefore, the resistor ripple must exceed the output capacitor ripple (VOUT) for stable operation. If this condition is not met, unstable switching behavior is observed in COT converters, with multiple on-time pulses in succession followed by long off-times.

Type 3 ripple injection is to utilize the ripple injection circuit with RA, CA and switch node (SW) voltages to generate a triangular ramp. This triangular ramp is then AC coupled to feedback node FB using capacitor CB. Since this circuit does not use the output voltage ripple, it is suitable for applications requiring low output voltage ripple.

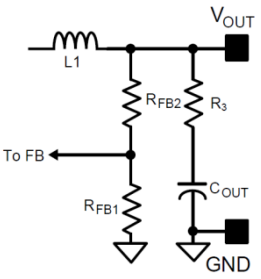
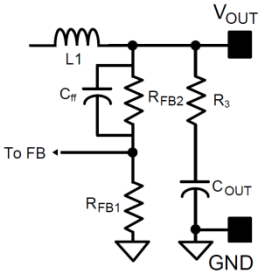
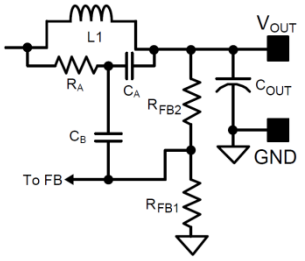
Type 1	Type 2	Type 3
		
$R_3 \geq \frac{25mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} // R_{FB1})}$ $R_3 \geq \frac{25mV}{\Delta I_{L1,min}}$	$R_A C_A \leq \frac{(V_{IN,min} - V_O) \times T_{ON(@V_{IN,min})}}{25mV}$

Table 1. Ripple Injection Structure

PCB Layout

Proper layout is critical to the performance of the circuit, and the following layout guidelines are recommended:

a. There is switching current in the loop composed of the input capacitor C_{IN}, VIN pin and PGND pin, therefore, The input capacitor must be close to the IC and directly connected to VIN and PGND pins to minimize the loop area.
b. The RON resistor and SS capacitor between the VIN and RON pins should be placed as close as possible to their respective pins.
c. VCC and bootstrap (BST) bypass capacitors provide switching current to the high-side and low-side gate drivers, these two capacitors should also be placed as close as possible to the IC, and the connecting wire length and loop area must be kept to a minimum.
d. Care must be taken in routing the feedback loop to avoid coupling any noise into this pin, in particular the feedback loop must be short and not near magnetics or in parallel with any other switching traces.
e. In FPWM=1 mode, if a ripple injection circuit is used at the FB pin to generate ripple, the feedback ripple is injected into the DC loop and the VOUT loop, and a differential layout is a better choice to help reduce scope for any noise injection at the FB pin.
f. The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise, the SW node area must be kept to a minimum.

Package Information

TSSOP14L-EP