Application Note: SY6982C

High Efficiency, 2A, Two-Cell Boost Li-Ion Battery Charger

General Description

SY6982C is a 3.0-5.5V_{IN}, 2A two-cell synchronous Boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit with selectable threshold for safety battery charge operation. SY6982C can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6982C along with small QFN3×3 footprint provides small PCB area application.

Ordering Information

SY6982 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6982CQDC	QFN3×3-16	

Features

- Low Profile QFN3×3 Package
- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Adaptive Input Current Limit with selectable threshold
- Maximum 2A Constant Charge Current
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Constant Voltage Selectable
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When Battery Removed

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

Typical Applications

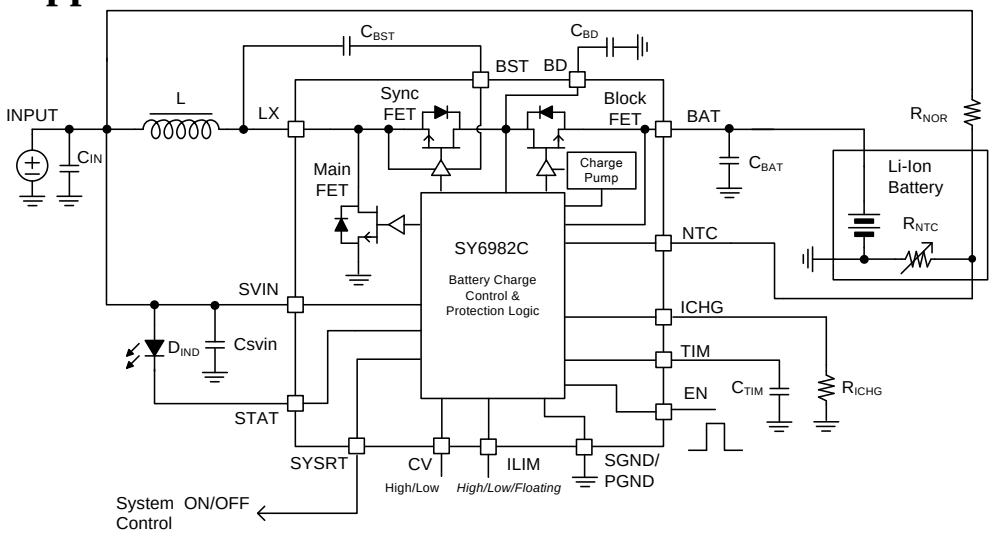
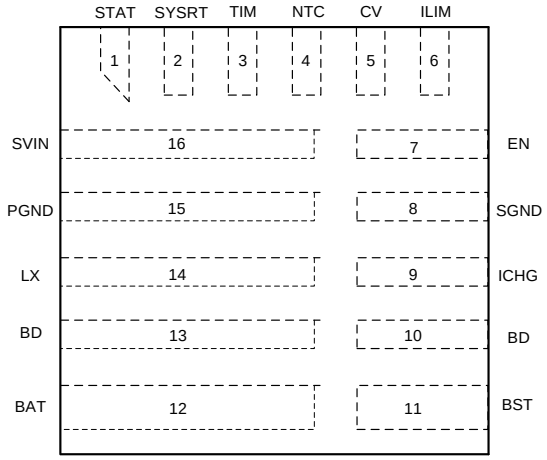


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-16)

Top Mark: **XX*xyz***, **(**Device code: XX, ***x=year code, y=week code, z= lot number code***)

Name	Pin Number	Description
STAT	1	Charge status indication pin. It is open drain output pin and pulled high to S_{VIN} thru a LED to indicate the charge in process. When the charge is done, LED is off.
SYSRT	2	System ON/OFF control pin. When V_{BAT} is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when V_{BAT} is high than 6V, SYSRT pin outputs high logic to turn on the system operation.
TIM	3	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/10 of CC charge time.
NTC	4	Thermal protection pin. UTP threshold is typical 76%V_{SVIN} and OTP threshold is typical 30.5%V_{SVIN}. Pulling up to SVIN can disable charge logic and make the IC operate as normal Boost regulator.
CV	5	Battery CV voltage selection pin. Program 4 different CV thresholds by setting different voltage on these two pins. The detailed information is shown in description section.
ILIM	6	Adaptive input current limit setting Pin. Select the permitted maximum input voltage drop to trigger the input current limit function. Pull high for 500mV voltage drop, pull low for 375mV, floating for 250mV.
EN	7	Enable control pin. High logic for enable on, and low logic for enable off.
SGND	8	Signal ground pin.
ICHG	9	Charge current program pin. Pull down to GND with a resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external RC network thru ICHG pin and compared to the internal reference 1V. So I_{CC} = (1V/ R_{ICHG}) ×10000, I_{TC}=(1V/ R_{ICHG})×1000.
BD	10, 13	Connect to the Drain of internal Blocking FET. Bypass at least a 4.7μF ceramic cap to GND.
BST	11	Boost-strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with a 0.1μF ceramic cap.
BAT	12	Battery positive pin.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.

Absolute Maximum Ratings

STAT, NTC, CV, ILIM, EN, ICHG, BD, BAT, LX, SVIN ---------- -0.5V to 18V
SYSRT, TIM, BST-LX ---------- -0.5V to 4V
LX Pin Current Continuous ---------- 5A
Power Dissipation, P_D @ T_A = 25℃, QFN3×3 ---------- 2.6W
Package Thermal Resistance
θ_{JA} ----------38℃/W
θ_{JC} ----------4℃/W
Junction Temperature Range ---------- -40℃ to 125℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 125℃

Recommended Operating Conditions

SVIN ---------- 3V to 5.5V
STAT, NTC, CV, ILIM, EN, ICHG, BD, BAT, LX, ---------- -0.3V to 16V
SYSRT, TIM ---------- -0.3V to 3.3V
LX Pin Current Continuous ---------- 5A
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(T_A=25℃, V_{IN}=5V, GND=0V, C_{IN}=4.7μF, L=0.68μH, R_{ICHG}=10kΩ, C_{TIM}=470nF, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
Supply Voltage	V_{SVIN}		3		16	V
V_{SVIN} Under Voltage Lockout Threshold	V_{UVLO}	V_{SVIN} rising and measured from V_{SVIN} to GND			2.9	V
V_{SVIN} Under Voltage Lockout Hysteresis	ΔV_{UVLO}	Measured from V_{SVIN} to GND		100		mV
Input Over Voltage Protection	V_{OVP}	V_{SVIN} rising and measured from V_{SVIN} to GND	5.8			V
Input Over Voltage Protection Hysteresis	ΔV_{OVP}	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
Battery Discharge Current	I_{BAT}	Shutdown IC, EN=NTC=0			25	μA
Input Quiescent Current	I_{IN}	Disable Charge, EN=1,NTC=0			1.5	mA
Oscillator and PWM						
Switching Frequency	f_{SW}			1000		kHz
Main N-FET Minimum Off Time	t_{OFF_MIN}	With 18V rating		100		ns
Main N-FET Maximum Off Time	t_{OFF_MAX}	With 18V rating		30		μs
Main N-FET Minimum On Time	t_{ON_MIN}	With 18V rating		100		ns
Power MOSFET						
$R_{DS(ON)}$ of Main N-FET	R_{NFET_M}			80		mΩ
$R_{DS(ON)}$ of Rectified N- FET	R_{NFET_R}			40		mΩ
$R_{DS(ON)}$ of Blocking N- FET	R_{NFET_B}			40		mΩ
Voltage Regulation						
Battery Charge Voltage	V_{BAT_REG}	V_{CV}<1V	8.32	8.40	8.48	V
		V_{CV}>2V	8.62	8.70	8.78	
High Level Logic for CV	V_{CV_H}		2			V
Low Level Logic for CV	V_{CV_L}				1	V
Recharge Threshold Refer to V_{BAT_REG}	ΔV_{RCH}		100	200	300	mV
Trickle Current Charge Mode Battery Voltage Threshold	V_{TRK}	Rising edge threshold	5.4	5.6	5.8	V
Battery Connect Detection						
NTC Voltage Threshold for Battery Detect	V_{DET}	NTC Falling Edge	85%		95%	V_{SVIN}
Detect Delay Time	t_{DET}		30	35	40	ms

Charge Current						
Internal Charge Current Accuracy for Constant Current Mode		I_{CC}=1000mA	-10		10	%
Internal Charge Current Accuracy for Trickle Current Mode		I_{TC}=100mA	-50		50	%
Termination Current	I_{TERM}	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
Output Voltage OVP Threshold	V_{OVP}		105%	110%	115%	V_{BAT_REG}
Input Current Limit						
V_{SVIN} Drop for Slow CC REF Discharge Voltage Threshold	V_{DISS}	Float ILIM		250		mV
		Pull low ILIM		375		
		Pull high ILIM		500		
Slow Discharge Voltage Hysteresis	ΔV_{DISS}	Positive edge		50		mV
V_{SVIN} Drop for Fast CC REF Discharge Voltage Threshold	V_{DISF}	Float ILIM		500		mV
		Pull low ILIM		750		
		Pull high ILIM		1000		
Fast Discharge Voltage Hysteresis	ΔV_{DISF}	Positive edge		50		mV
Timer						
Trickle Current Charge Timeout	t_{TC}	C_{TIM}=330nF	0.425	0.5	0.575	hour
Constant Current Charge Timeout	t_{CC}		3.825	4.5	5.175	hour
Charge Mode Change Delay Time	t_{MC}			30		ms
Termination Delay Time	T_{TERM}			30		ms
Recharge Time Delay	T_{RCHG}			30		ms
Short Circuit Protection						
Output Short Protection Threshold	V_{SHORT}		1.70	2.00	2.30	V
System ON/OFF Control						
High Logic of System ON/OFF Control	V_{SYSRT_H}		2.1			V
Low Logic of System ON/OFF Control	V_{SYSRT_L}				0.6	V
Hysteresis for Positive and Negative Edge	V_{SYSRT_HYS}			100		mV
Linear Charger Mode						
Battery Charger Current When the Blocking FET is in Linear Mode	I_{SC}	V_{BAT}<V_{SHORT}		5%		I_{CC}
Peak Linear Current When Battery is Absent	I_{L_PEAK}			1		A
BD Voltage Regulation	V_{BD}	V_{SHORT} <V_{BAT}< V_{TRK}	5.8	6	6.2	V
Blocking FET Fully Turn On Threshold V_{TRON}=V_{BAT}- V_{SVIN}	V_{TRON}	V_{BAT} > V_{TRK}		100		mV
Enable ON/OFF Control						
High Level Logic for Enable Control	V_{EN_H}		1.5			V
Low Level Logic for Enable Control	V_{EN_L}				0.4	V
Battery Thermal Protection NTC						
Under Temperature Protection	V_{NTC_UTP}		75%	76%	77%	V_{SVIN}
Under Temperature Protection Hysteresis	$V_{NTC\_UTP\_HYS}$	Falling edge		6%		
Over Temperature Protection	V_{NTC_OTP}		29.5%	30.5%	31.5%	

Over Temperature Protection Hysteresis	$V_{NTC\_OTP\_HYS}$	Rising edge		2%		
Thermal Fold-back and Thermal shutdown						
Thermal Fold-back Threshold	T_{Fold}	Rising edge		120		℃
Thermal Fold-back Threshold Hysteresis	T_{Fold_HYS}			20		℃
Thermal Fold-back Ratio				0.25		I_{CC}
Thermal Shutdown Temperature	T_{SD}	Rising edge		160		℃
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			30		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

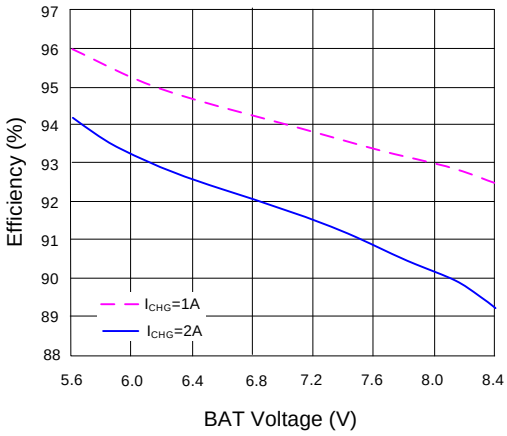
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

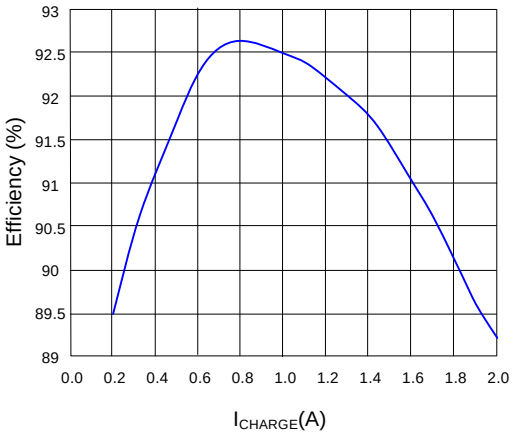
Typical Performance Characteristics

(T_A=25℃, V_{IN}=5V, L=0.68μH, R_{ICHG}=10kΩ, unless otherwise specified.)

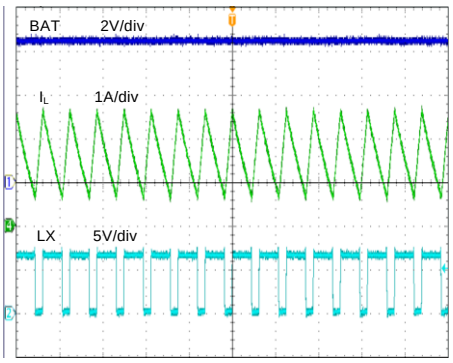
Efficiency vs. Bat Voltage (CC Mode)



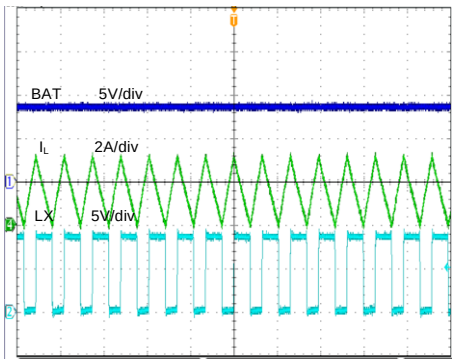
Efficiency vs. Charge Current (CV Mode)



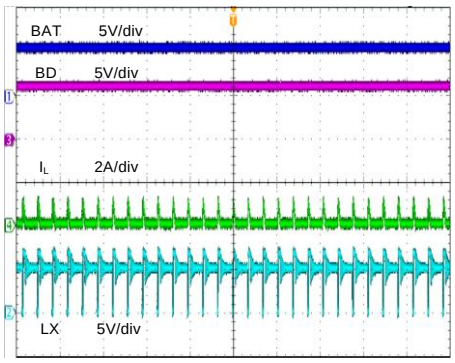
Steady Waveform (CC Mode)



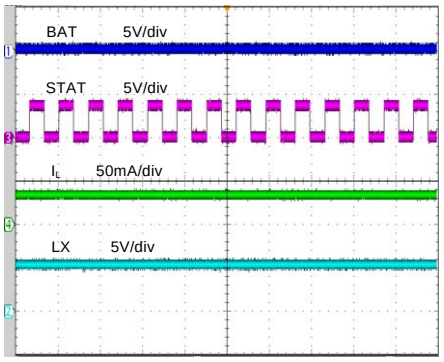
Steady Waveform (CV Mode)



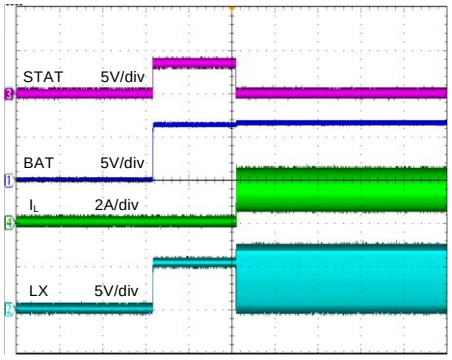
Steady Waveform (TC Mode)



Steady Waveform (Short Mode)

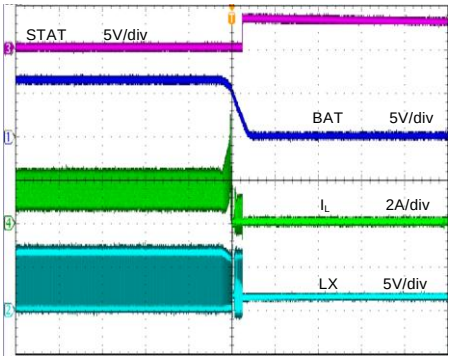


Power ON (CC Mode)



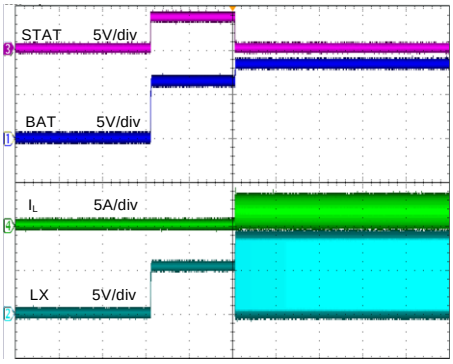
Time (400ms/div)

Power OFF (CC Mode)



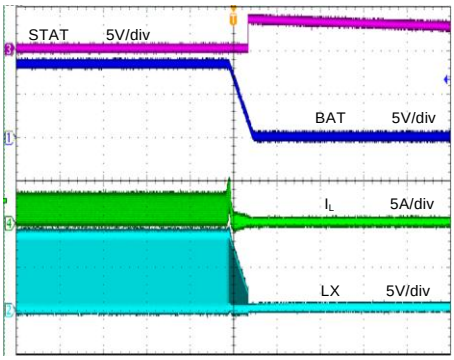
Time (2ms/div)

Power ON (CV Mode)



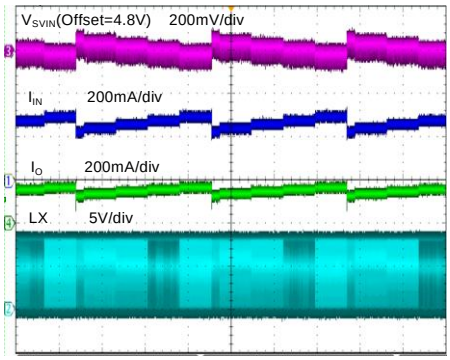
Time (400ms/div)

Power OFF (CV Mode)



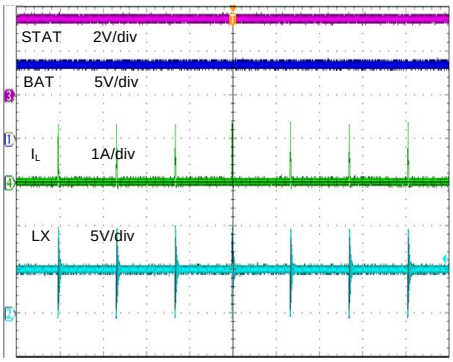
Time (4ms/div)

Adaptive Input Current Limit



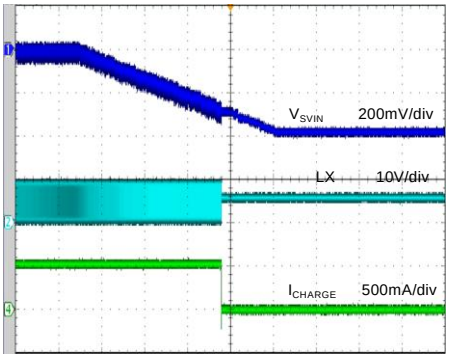
Time (4s/div)

Boost Mode (Null Load)



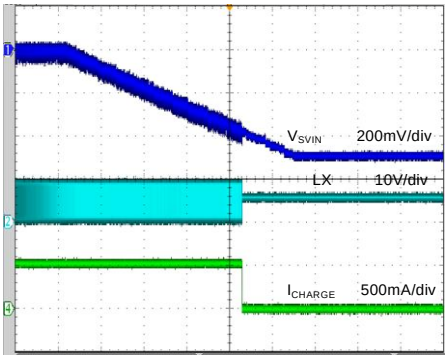
Time (20μs/div)

Different Input Current Limit Threshold
(Float ILIM)



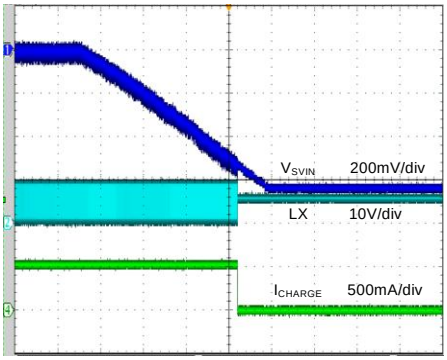
Time (4s/div)

Different Input Current Limit Threshold
(Pull low ILIM)



Time (4s/div)

Different Input Current Limit Threshold
(Pull High ILIM)



Time (4s/div)

General Function Description

SY6982C is a 3.0-5.5V_{IN}, 2A two-cell synchronous Boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit for safety battery charge operation. SY6982C can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-in-process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.3Hz frequency. Connect a LED from SVIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.
   Fault Mode includes Input OVP, BAT OVP, BAT Short Circuit, NTC(UTP/OTP), Thermal Shutdown and Charge Timeout.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

SY6982C is a switching mode Boost charger for the applications with USB power input. SY6982C utilizes quasi-fixed frequency constant OFF time control to simplify the internal close-loop compensation design. Slope compensation is not necessary for the stable operation. The quasi-fixed frequency settled at 1MHz is easy for the size minimization of peripheral circuit design. During the light load operation, when the output voltage of the internal error amplifier is lower than the minimum threshold, the OFF time is going to be stretched to achieve frequency fold back.

Operation Principle

SY6982C can normally work with or without Li-Ion battery both.

Battery Present

Before SY6982C start-up, C_{BD} is charged by the battery thru the body diode of blocking FET, and V_{BD} equals to V_{BAT}.

If the plug in input voltage V_{SVIN} is higher than V_{BD}=V_{BAT}, C_{BD} is charged by V_{SVIN} further thru the body diode of sync-FET. Under this condition, the Boost charger operates in light load mode and regulates the V_{BD} at 6V and the blocking FET works in linear charge mode. If the V_{BAT} is lower than the internal short circuit threshold V_{SHORT}, the linear charge current is 1/20 I_{CC}. When V_{BAT} is higher than V_{SHORT} but lower than the threshold of trickle charge, the linear charge current is 1/10 of I_{CC}. Note that, charging current would not be increased to I_{CC} when the block FET operates in linear mode. With the increasing of V_{BAT}, when V_{BAT} is higher than both V_{SVIN} and V_{TRK}, the blocking FET is fully turned on and the switching mode Boost charger takes over the battery charging. The current in the blocking FET is mirrored to be as the charging current I_{CHG}. If V_{SVIN} is lower than V_{BD}=V_{BAT} at the plug in time, the switching mode Boost charger starts work directly.

During the charging mode, constant (trickle) charging current loop is active firstly. When V_{BAT} equals to constant voltage threshold V_{CV}, constant voltage loop takes over and pulls down the charging current. When I_{CHG} is lower than the termination current threshold I_{TERM}, the main FET of Boost charger is turned off firstly. Sync-FET and blocking FETs are turned off together when the current is down to zero. Then, SY6982C is waiting for recharge mode.

Battery Absent

If there's no battery connection detected thru NTC pin, SY6982C operates as a normal switching mode Boost converter. When V_{SVIN} is higher than UVLO threshold, the blocking FET is softly turned on. After the blocking FET fully turn-on, switching mode Boost converter starts work. The internal current loop and voltage loop are active both.

Basic Protection Principle

SY6982C has fully battery charging protection. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the main FET of the Boost charger is turned off immediately. The sync-FET and the blocking FET are turned off later when the current is down to zero. When the V_{BAT} is lower than V_{SHORT}, the short circuit protection happens. The main FET is turned off firstly. The block FET enters linear mode with 1/20 I_{CC} charging current. When V_{BAT} recovers back to be higher than V_{SHORT}, the Boost charger restarts to work at light load and regulates V_{BD} at 6V. The linear charge current is

increased from 1/20 I_{CC} to 1/10 I_{CC}. When V_{BAT} recovers back to be higher than V_{TRK}, the Boost switching charger takes over.

Basic Adaptive Input Current Limit Principle

SY6982C has adaptive input current limit function. Before the IC starts charging work, the input voltage is detected and saved as reference V_{INREF}. Once IC starts to charge, the output charging current I_{CHG} is ramped up softly and the V_{SVIN} drop is monitored simultaneously. When the input voltage drop is larger than V_{DISS} the output charging current reference I_{CHGREF} starts to be discharged slowly and when the voltage drop is larger than V_{DISF} the I_{CHGREF} starts to be fast discharged. With the discharging of I_{CHGREF}, the charging current is deceased and the V_{SVIN} would recover. Once the V_{SVIN} goes back into the normal range, the I_{CHGREF} is kept on the current value. The I_{CHGREF} would be decreased along with the increasing of output voltage to keep the input power at the maximum value. The internal digital machine state is built up to achieve this function.

Constant Voltage Threshold Program Principle

SY6982C can program the constant voltage threshold thru the CV pin. When V_{CV} is higher than 2V, the constant voltage threshold is 8.7V; when V_{CV} is lower than 1V, the constant voltage threshold is 8.4V.

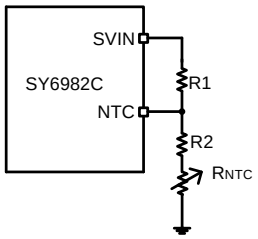
Applications Information

Because of the high integration of SY6982C, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R1, R2 and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC Resistor

SY6982C monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{SVIN}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =75~77%
2. Define K_{OT}, K_{OT} =29.5~31.5%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2,

$$R2=\frac{K_{OT}(1-K_{UT})R_{UT}-K_{UT}(1-K_{OT})R_{OT}}{K_{UT}-K_{OT}}$$

5. Calculate R1

$$R1=(1/K_{OT}-1)(R2+R_{OT})$$

If choose the typical values K_{UT} =76% and K_{OT}=30.5%, then

$$R2=0.16R_{UT}-1.16R_{OT}$$

$$R1=2.3(R2+R_{OT})$$

Timer Capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$C_{TIM}=2\times10^{-11}\ S\times T_{CC}$ Unit: F

T_{CC} is the target constant charge time，unit: s.

Input Capacitor C_{IN}

The ripple current through input capacitor is greater than

$$I_{C_{IN}-RMS}=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{2\sqrt{3}\times L\times F_{SW}\times V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 4.7μF capacitance are recommended to handle this ripple current.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or a better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{CC} \times (V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple. I_{CC} is the setting charge current.

For SY6982C, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with greater than 10μF capacitance is recommended.

Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

Where F_{SW} is the switching frequency and I_{CC} is the setting charge current.

The SY6982C is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

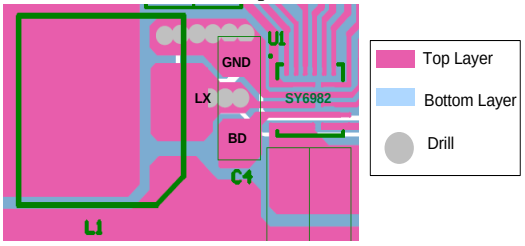
$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right) \times \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Layout Design

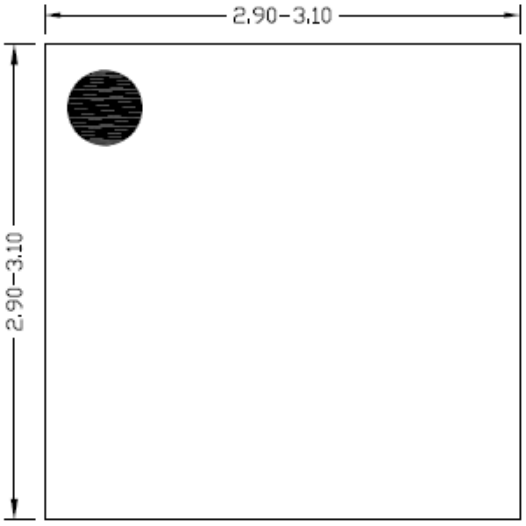
The layout design of SY6982C regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{SVIN}, L, C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible

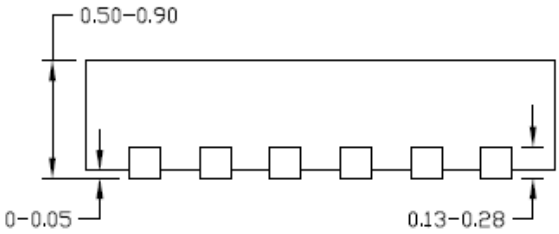


2) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance.
3) C_{SVIN} must be close to pin SVIN and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
5) The small signal component R_{ICHG} must be placed close to IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

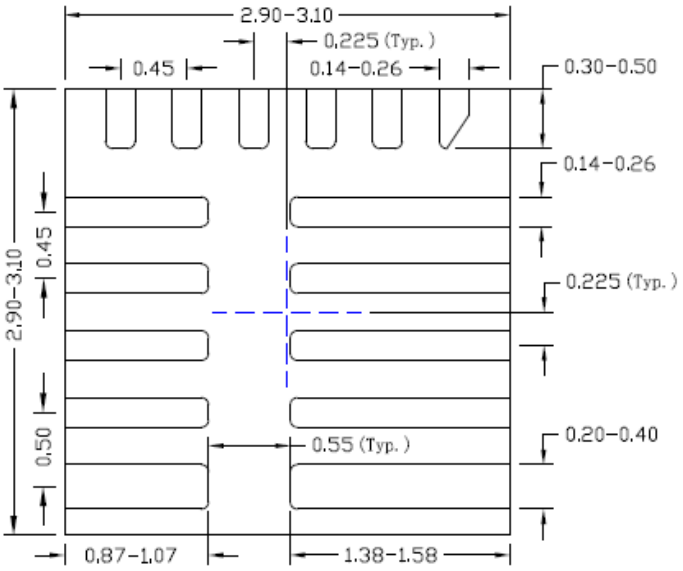
QFN3×3-16 Package Outline Drawing



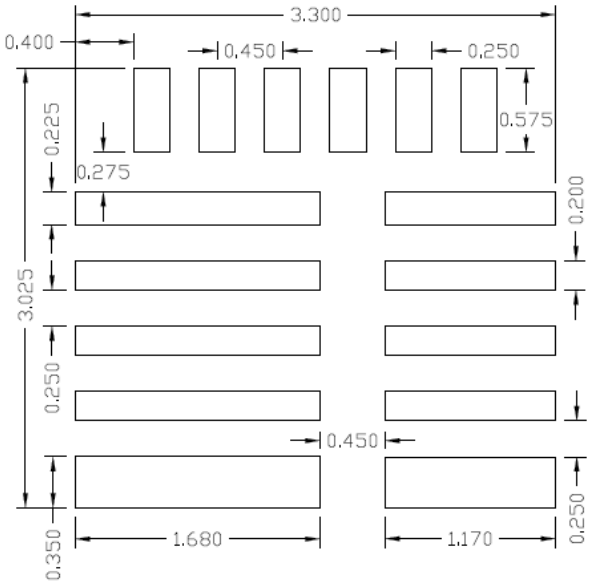
Top View



Side View



Bottom View



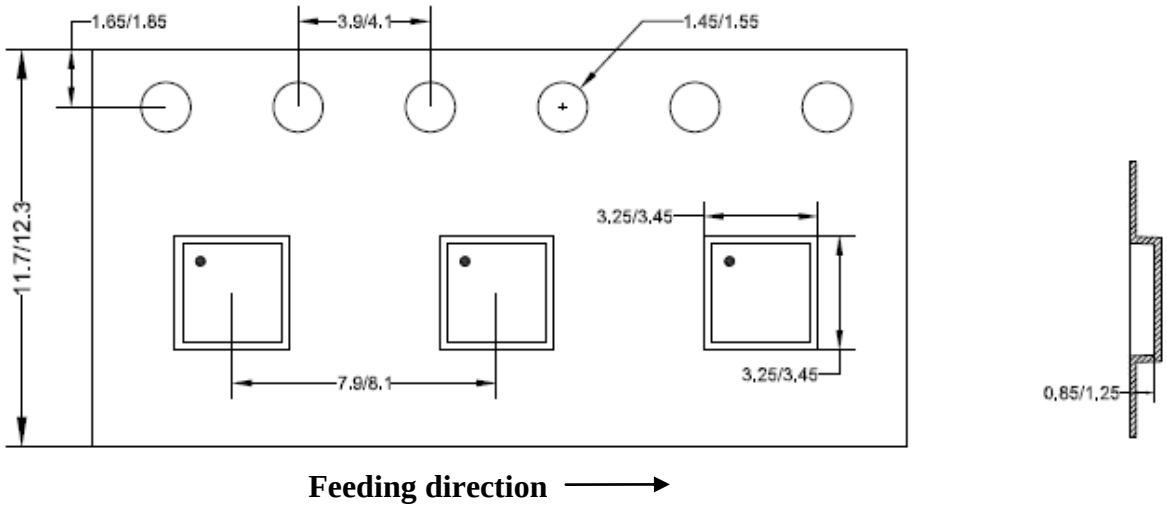
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

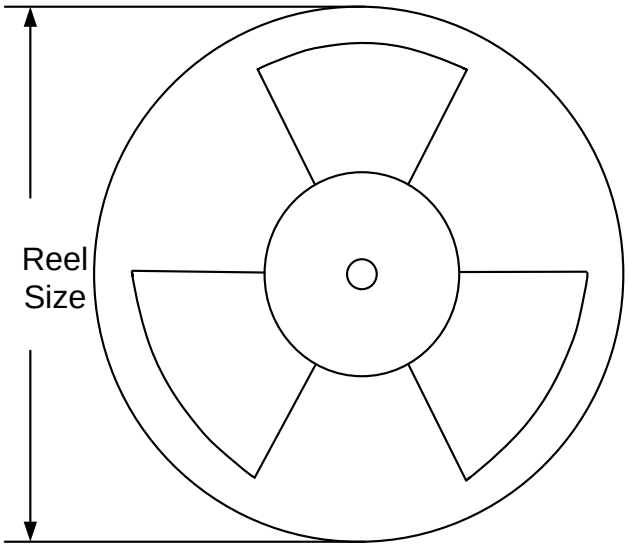
1. Taping orientation

QFN3×3



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com