

# P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>d</sup>	Q <sub>g</sub> (Typ.)			
- 30	0.011 at V <sub>GS</sub> = - 10 V	- 13.5	29.5 nC			
	$0.015$ at $V_{GS} = -4.5$ V	- 11.6	29.5110			

#### **FEATURES**

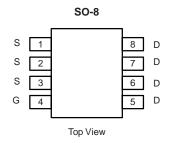
- Halogen-free
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

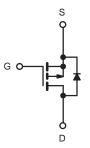


RoHS

#### **APPLICATIONS**

- Load Switch
- · Notebook Adaptor Switch





P-Channel MOSFET

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 30	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20	V	
	T <sub>C</sub> = 25 °C		- 13.5	
Continuous Drain Current (T <sub>.I</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 , [	- 11.9	
Continuous Diam Current (1) = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	- 10.9 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		- 8.6 <sup>a, b</sup>	
Pulsed Drain Current	<u>.</u>	I <sub>DM</sub>	- 50	Α
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		- 4.1	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	- I <sub>S</sub> -	- 2.2 <sup>a, b</sup>	
Avalanche Current	1 0411	I <sub>AS</sub>	- 20	
Single-Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	20	mJ
	T <sub>C</sub> = 25 °C		5.0	
Manianum Danian Disain ation	T <sub>C</sub> = 70 °C		3.2	w
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.7 <sup>a, b</sup>	VV
	T <sub>A</sub> = 70 °C	1	1.7 <sup>a, b</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c</sup>	t ≤ 10 s	R <sub>thJA</sub>	38	46	°C/W	
Maximum Junction-to-Foot	Steady State	R <sub>thJF</sub>	20	25	5/ * *	

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s
- c. Maximum under Steady State conditions is 85 °C/W.
- d. Based on  $T_C$  = 25 °C.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 30			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = - 250 μA		- 34		mV/ °C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.3		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	- 1.4		- 2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			± 100	nA
Zara Cata Valtaga Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	μA
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 30			Α
	_	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		0.011		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 8 A	0.015			Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 10 A		28		S
Dynamic <sup>b</sup>				<u> </u>		
Input Capacitance	C <sub>iss</sub>			2550		pF
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		455		
Reverse Transfer Capacitance	C <sub>rss</sub>			390		
T. 10 1 01	0	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 10 A		57	86	20
Total Gate Charge	Q <sub>g</sub> V <sub>DS</sub> = 13 v, v <sub>GS</sub> = 10 v, i <sub>D</sub> = 1			29.5	45	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10 \text{ A}$		8		nC
Gate-Drain Charge	$Q_{gd}$			22		
Gate Resistance	R <sub>g</sub>			2.2	4.4	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			13	25	
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 1.5 \Omega$		12	24	=
Turn-Off DelayTime	t <sub>d(off)</sub>	$I_D \cong$ - 10 A, $V_{GEN}$ = - 10 V, $R_g$ = 1 $\Omega$		40	70	
Fall Time	t <sub>f</sub>			9	18	
Turn-On Delay Time	t <sub>d(on)</sub>			48	80	ns
Rise Time	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_{L} = 1.5 \Omega$		92	160	
urn-Off DelayTime t <sub>d(of</sub>		$I_D \cong$ - 10 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 1 $\Omega$		34	60	1
Fall Time	t <sub>f</sub>	1		19	35	
Drain-Source Body Diode Characteris	tics	,				
Continous Source-Drain Diode Current I <sub>S</sub>		T <sub>C</sub> = 25 °C			- 4.1	_
Pulse Diode Forward Current	I <sub>SM</sub>	_			- 60	Α
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3 A, V <sub>GS</sub> = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	3 / 65		27	45	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1		16	27	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = -10 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 \text{ °C}$		12		
Reverse Recovery Rise Time	t <sub>b</sub>	1		15		ns

#### Notes:

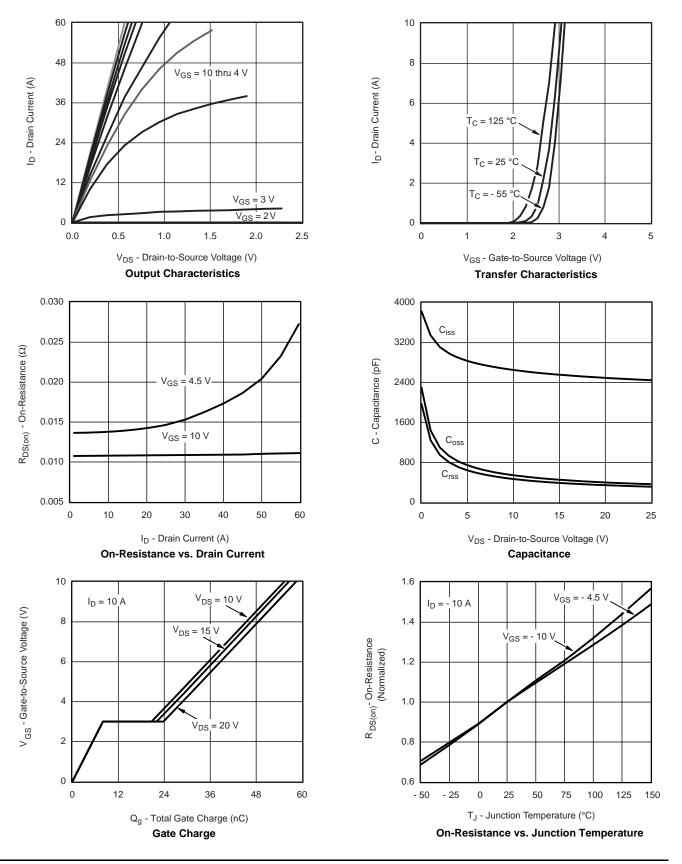
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.

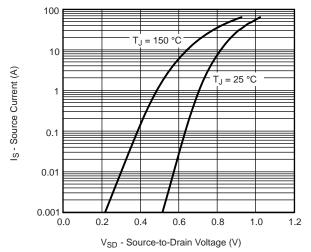


#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

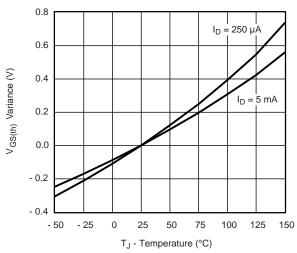




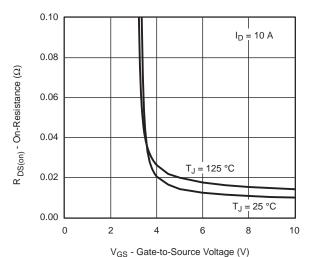
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



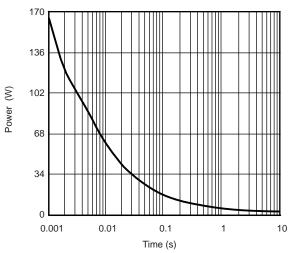
#### Source-Drain Diode Forward Voltage



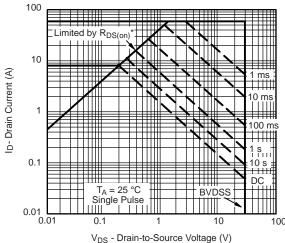
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

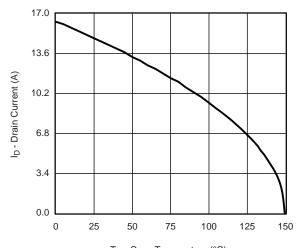


\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

Safe Operating Area

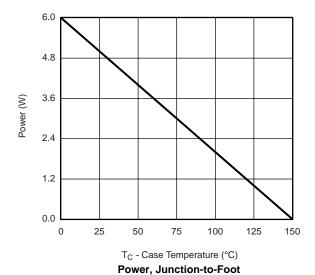


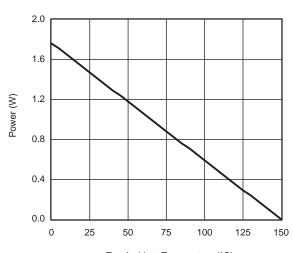
## MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$  - Case Temperature (°C)

#### **Current Derating\***



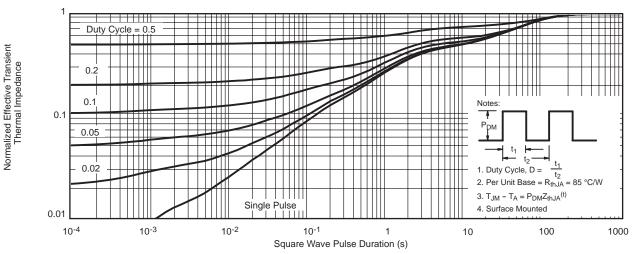


 $\label{eq:TA-Ambient Temperature (°C)}$  Power Derating, Junction-to-Ambient

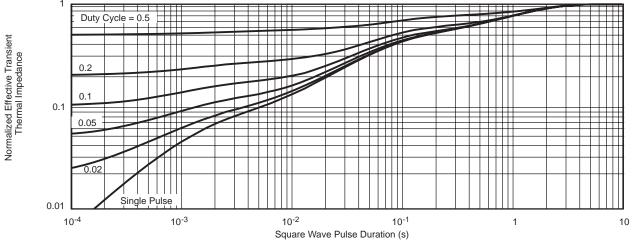
 $<sup>^*</sup>$  The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package



#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

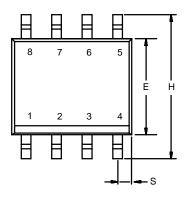


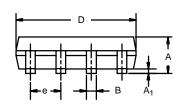
Normalized Thermal Transient Impedance, Junction-to-Foot

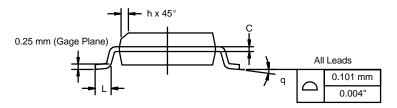
服务热线:400-655-8788 6



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







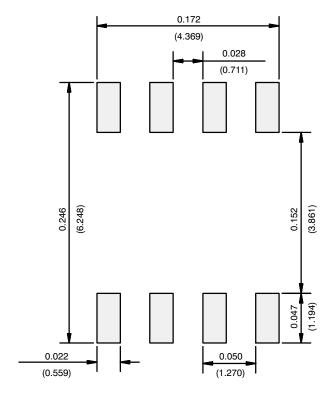
	MILLIM	IETERS	INC	HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev I 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)



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