Dual Channel High Speed Low Side Driver with Negative Input Capability (20V Supply, 5A peak source and sink)

1 FEATURES

- 5A Peak Source Current and 5A Peak Sink Current
- 4.5V - 20V Wide Supply Voltage Range
- Down to -5V Negative Input Voltage Capability
- Fast Propagation Delay: 13ns
- Fast Rising and Falling Time: 8.5ns and 6.5ns
- TTL Input-Logic Threshold
- Under Voltage Lock Out Protection
- Low Quiescent Current: 65uA
- Output Low When Input Floating
- Available in WSON-8 Package

2 APPLICATIONS

- Power MOSFET Gate Driver
- IGBT Gate Driver
- Switching Power Supply
- Motor Control, Solar Power

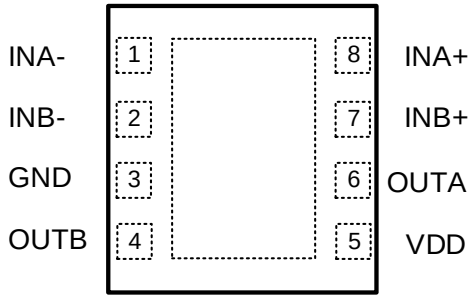
3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE
GBI7256NMCR	7256	WSON-8

4 DISCRIPTION

The GBI7256, dual channel high speed low side gate driver, provides 5A peak source and sink current along with rail-to-rail driving capability for MOSFET, IGBT, and GaN power device. The device features a minimum 13ns input to output propagation delay and 20V power supply rail makes it suitable for high frequency power converter application. The negative input is acceptable down to -5V for enhancing the input noise immunity. The wide input hysteresis is compatible for both TTL and CMOS low voltage logic. Each channel of the device adopts non-overlap driver design to avoid the shoot-through of output stage. It operates over a wide temperature range -40°C to 150°C. The GBI7256 is available in WSON-8 Package.

5 PIN CONFIGURATION



Top View (WSON-8)

Table 1. PIN CONFIGURATION

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
INA-	1	I	Channel A Inverting Input. When Channel A is used in Non-inverting configuration, connect INA- to GND to enable Channel A output. OUTA held low if INA- is floating or biased high.
INB-	2	I	Channel B Inverting Input. When Channel B is used in Non-inverting configuration, connect INB- to GND to enable Channel B output. OUTB held low if INB- is floating or biased high.
GND	3	-	Power Ground
OUTB	4	I	Channel B Output
VDD	5	O	System Power Supply.
OUTA	6	I	Channel A Output
INB+	7	O	Channel B Non-Inverting Input. When Channel B is used in Inverting configuration, connect INB+ to high to enable Channel B output. OUTB held low if INB+ is floating or biased low.
INA+	8	I	Channel A Non-Inverting Input. When Channel A is used in Inverting configuration, connect INA+ to high to enable Channel A output. OUTA held low if INA+ is floating or biased low.

6 SPECIFICATIONS

6.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Logic Input & Input Enable	INA+, INA-, INB+, INB-,	-5	22	V
Gate Driver Output	OUTA, OUTB	-0.3	22	V
Supply Voltage	VDD	-0.3	22	V
Operating junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

6.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

6.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	20	V
$V_{INA+, INA-, INB+, INB-}$	Input & Enable voltage range	-5	20	V
T_J	Operating junction temperature	-40	150	°C

6.4 THERMAL INFORMATION

PARAMETER	THERMAL METRIC	WSON-8	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	46.7	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	46.7	°C/W
ψ_{JT}	Junction to top characterization parameter	0.7	°C/W
ψ_{JB}	Junction to board characterization parameter	22.6	°C/W

6.5 ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{DD}	Operating supply voltage		4.5		20	V
V_{DD_UVLO}	Input UVLO	V_{DD} rising		4.2	4.5	V
	Hysteresis			300		mV
I_Q	Quiescent current	IN+=IN-=GND, V_{DD}=3.5V		65		uA
		IN+=IN-=GND, V_{DD}=12V		315		uA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUTS						
$V_{INA+, INB+\ H}$	Output high for non-inverting input pins			2.15		V
$V_{INA+, INB+\ L}$	Output low for non-inverting input pins			1.20		V
$V_{INA+, INB+\ Hys}$	Hysteresis			0.9		V
$V_{INA-, INB-\ H}$	Output low for inverting input pins			2.15		V
$V_{INA-, INB-\ L}$	Output high for inverting input pins			1.05		V
$V_{INA-, INB-\ Hys}$	Hysteresis			1.10		V
OUTPUT						
$I_{SINK/SRC}$	Output Sink/Source peak current	C_{Load}=10nF, F_{sw}=1kHz		5		A
R_{OH}	Output pull high resistance	I_{OUT}= - 10mA, V_{OUT} logic high		10		Ω
	Dynamic pull high resistance	V_{OUT}= 0V		0.5		Ω
R_{OL}	Output pull low resistance	I_{OUT}= 10mA		0.6		Ω
Timing						
T_R	Output rising time	C_{Load}=1nF		8.5		ns
T_F	Output falling time	C_{Load}=1nF		6.5		ns
T_{D_IN}	IN to output propagation delay, Rising edge			13		ns
	IN to output propagation delay, Falling edge			13		ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		15		ns

7 TYPICAL CHARACTERISTICS

V_{DD}=12V, C_{load}=1nF, T_A= 25°C.

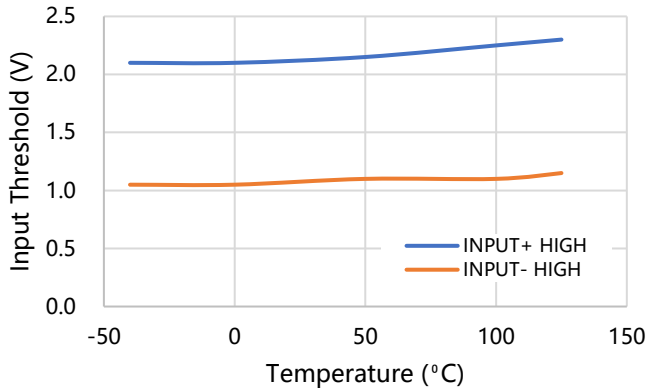


Figure 1. IN Threshold Vs Temperature

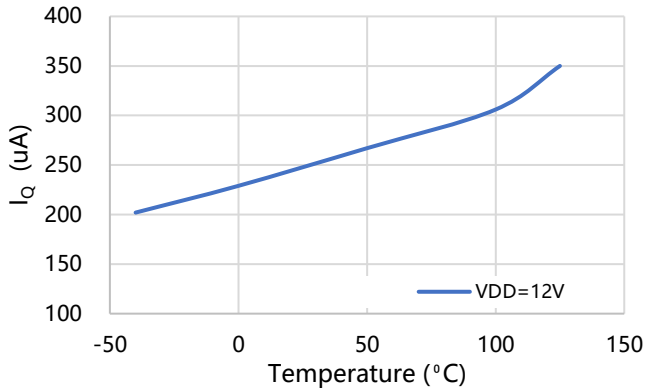


Figure 2. Quiescent Current Vs Temperature

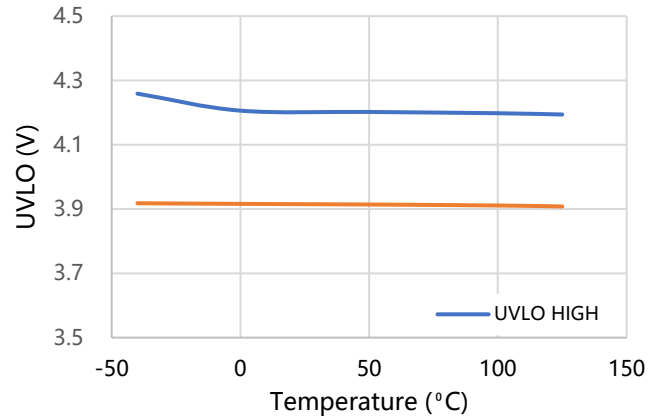


Figure 3. UVLO Vs Temperature

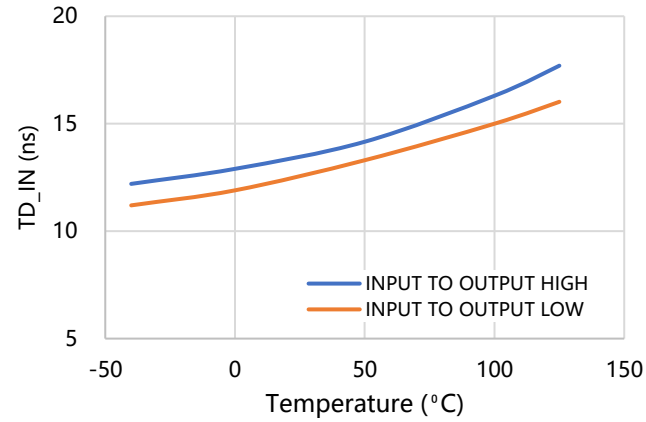


Figure 4. Propagation Delay vs Temperature

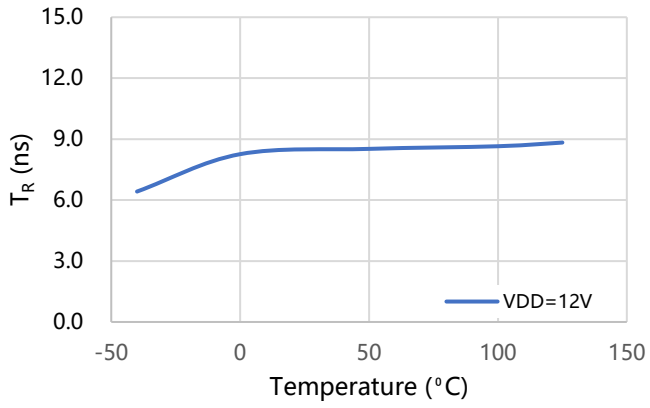


Figure 5. Output Rising Time Vs Temperature

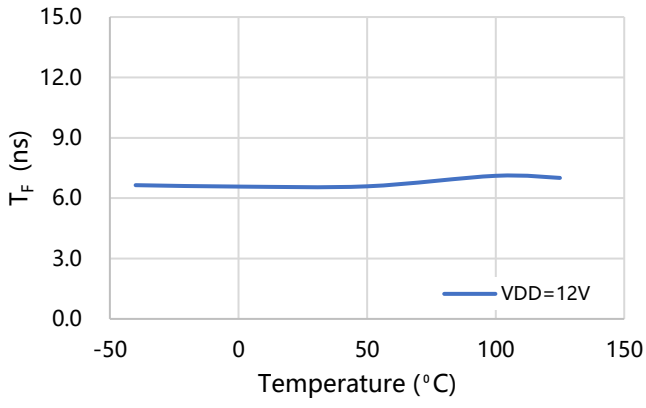


Figure 6. Output Falling Time Vs Temperature

8 FUNCTIONAL BLOCK DIAGRAM

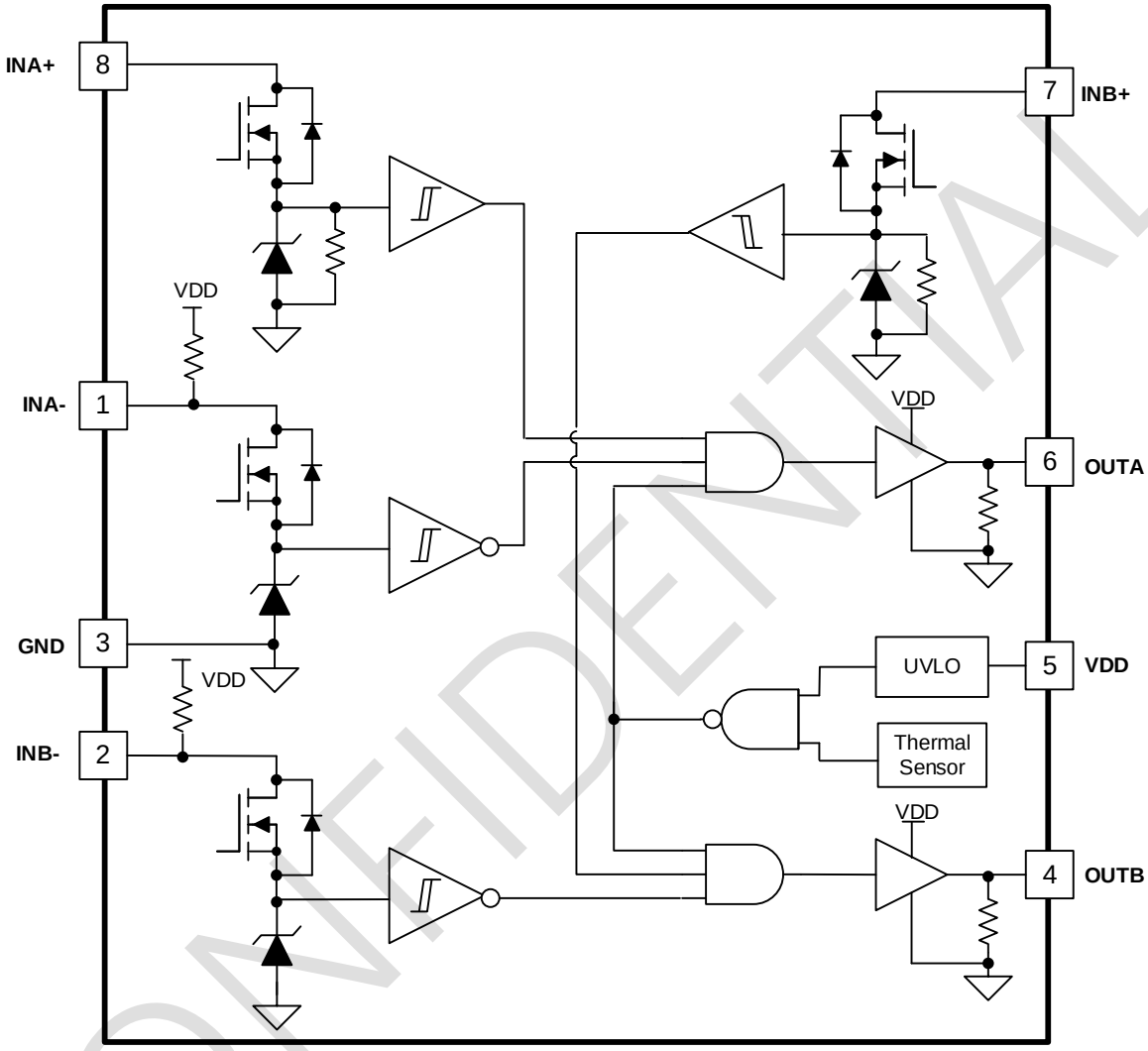


Figure 7. GBI7256 Block Diagram

9 DISCRIPTION

9.1 Overview

The GBI7256 is a dual channel, high speed, low side gate driver for power MOSFET, IGBT and GaN HMET with up to 20V wide supply and 5A source/sink peak current each channel along with the minimum input to output propagation delay of 13ns. The GBI7256 supports both invertible and non-invertible outputs depending on adopted inputs. The input is able to be down to -5V DC which enhances the driver input stage noise immunity.

The 20V rail-to-rail output improves the GBI7256 output stage robustness during the switching load fast transition.

Table 2. GBI7256 Device Logic

INA+	INA-	OUTA	INB+	INB-	OUTB
L	L	L	L	L	L
L	H	L	L	H	L
H	L	H	H	L	H
H	H	L	H	H	L
Floating	Any	L	Floating	Any	L
Any	Floating	L	Any	Floating	L

9.2 VDD Power Supply

The GBI7256 operates under a supply voltage range between 4.5V to 20V. It' s recommended to put two VDD bypass capacitor in parallel to prevent noise problems on supply VDD. It has to put a 0.1uF SMT ceramic capacitor as close as possible between the VDD pin to the GND pin. To avoid the unexpected VDD glitch, a large capacitor (ex. 1uF or 10uF) with relatively low ESR must be connected in parallel with that 0.1uF capacitor. This parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

9.3 VDD Under Voltage Lock Out (UVLO)

The GBI7256 implements the Under Voltage Lock Out (UVLO) with rising threshold of typically 4.2 V along

with 300mV typical hysteresis. The VDD voltage which is able to down to 4.5V is especially suitable for driving wide band gap power device, like GaN.

The UVLO holds the output low regardless of the input status when VDD is rising but the level is below the UVLO threshold. The hysteresis prevents output bouncing caused by the noise impact on the power supply. During power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD till VDD steady state reached.

The inverting operation in Figure 8 shows that the output remains low till the UVLO threshold reached, and then the output is in-phase with the input.

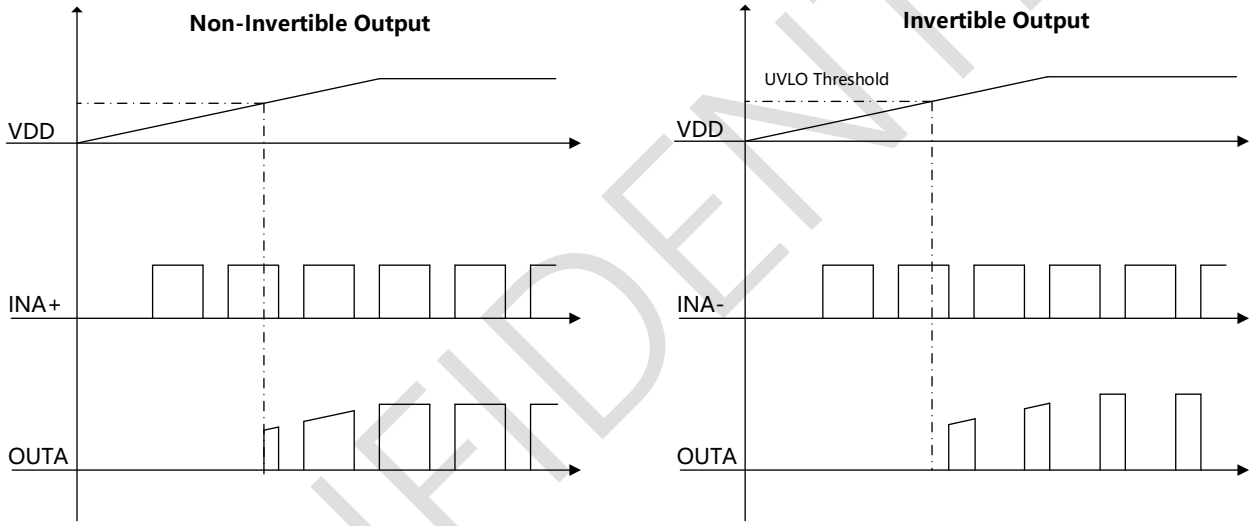


Figure 8. GBI7256 Invertible and Non-Invertible Output Vs VDD

9.4 Input Stage

The GB7256 input is compatible on TTL logic which is independent of the VDD supply voltage. The typical threshold is 2.1-V (high) and 1.0-V (low), which make the device easily driven by PWM control signals derived from 3.3-V and 5-V digital power-controller devices. The device features wider hysteresis compared to typical threshold of 0.5V which offers enhanced noise immunity. It also implements tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

9.5 Enable Function

The GBI7256 does not feature the enable pins, but it can easily implement an enable/disable function with unused input pins, where the unused positive input is the logic high based and the negative input is logic low based.

Table 3. GBI7256 Logic Configuration for EN/Disable Function

INA+	INA-	OUTA	INB+	INB-	OUTB
EN Low	L	L	EN Low	L	L
EN Low	H	L	EN Low	H	L
EN High	L	H	EN High	L	H
EN High	H	L	EN High	H	L
L	EN Low	L	L	EN Low	L
H	EN Low	H	H	EN Low	H
L	EN High	L	L	EN High	L
H	EN High	L	H	EN High	L
Floating	Any	L	Floating	Any	L
Any	Floating	L	Any	Floating	L

10 APPLICATION INFORMATION

Typical Application

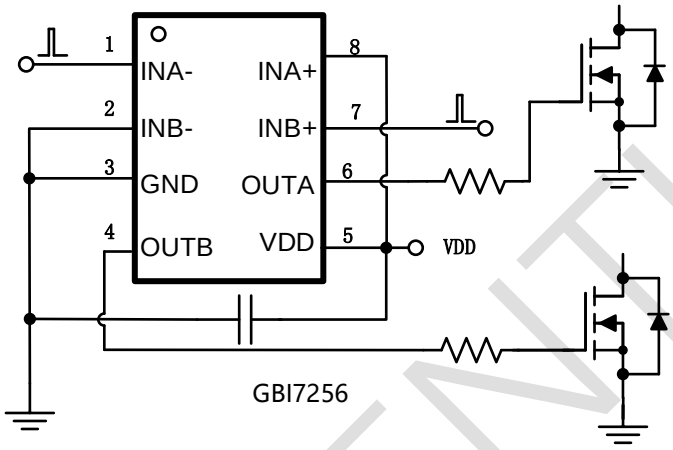


Figure 9.Channel A in Inverting and Channel B in Non-inverting Configuration

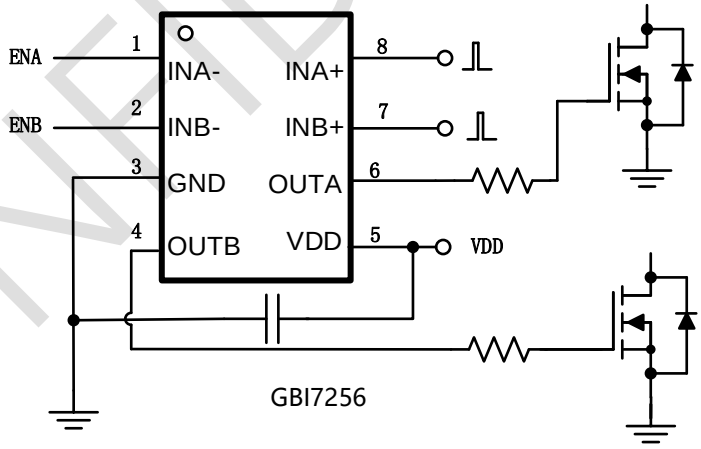


Figure 10. Channel A in Non-inverting and Channel B in Non-inverting Configuration with Enable Function Implemented

Driver Power Dissipation

Generally, the power dissipation depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The GBI7256 is designed with very low quiescent currents and internal logic to eliminate any output-stage shoot-through.

The power loss of GBI7256 caused by pure capacitive load is:

$$P_G = C_{Load} * V_{DD}^2 * f_{SW} \quad (1)$$

Where

- V_{DD} is supply voltage
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

This equation (1) is also able to be adopted to calculate the switching load of power MOSFET, where gate charge Qg determines the capacitor charges.

$$Q_g = C_{LOAD} \times V_{DD} \quad (2)$$

Normally power device manufacturers provide specifications with the typical and maximum Qg, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{DD} * f_{SW} \quad (3)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is the supply voltage

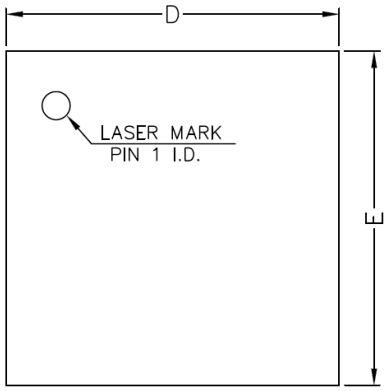
Sometimes, circuit designers put a resistor R_{GATE} between the driver output pin and the gate terminal of power device to slow down the power device transition. As a result, the ringing caused by the parasitic inductor is eliminated. The power dissipation of the driver shows as below:

$$P_G = \frac{1}{2} * Q_g * V_{DD} * f_{SW} * \left(\frac{R_L}{R_L + R_{GATE}} + \frac{R_H}{R_H + R_{GATE}}\right) \quad (4)$$

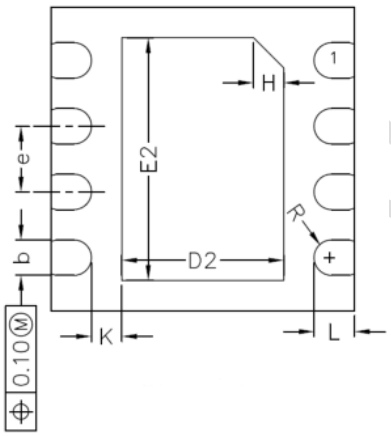
Where

- R_H is the equivalent pull up resistance of GBI7256
- R_L is the pull-down resistance of GBI7256
- R_{GATE} is the gate resistance between driver output and gate of power device.

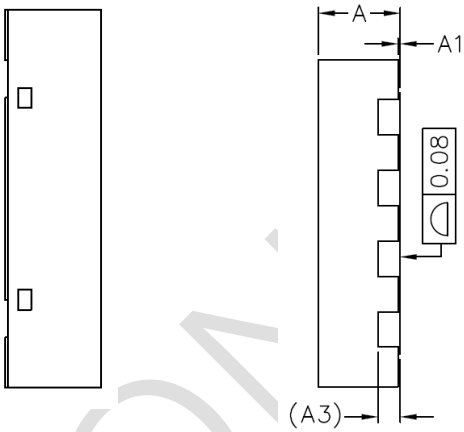
PACKAGE INFORMATION-DFN3x3-8L



Top View



Bottom View



Side View

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.30	0.35	0.40
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.50	1.60	1.70
E2	2.30	2.40	2.50
e	0.55	0.65	0.75
H		0.30REF	
K	0.20	0.30	0.40
L	0.30	0.40	0.50
R	0.16	—	—

- Units of measurement is millimeter