# 40V, 5A Non-Synchronous Step-Down DCDC Converter With High Efficiency Sleep Mode

## 1 FEATURES

- Wide Input Range: 4.0V-40V
- Up to 5A Continuous Output Current
- 0.8V ± 1% Feedback Reference Voltage
- Integrated 80mΩ High-Side Power MOSFET
- Adjustable Frequency 200KHz to 2.5MHz
- Pulse Skipping Mode (PSM) at Light Load
- 100uA Quiescent Current in Sleep Mode
- Programmable Soft-Start Time
- Integrated Loop Compensation
- Available in an eSOP-8L Package

## 2 APPLICATIONS

- 12-V, 24-V, Industry Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

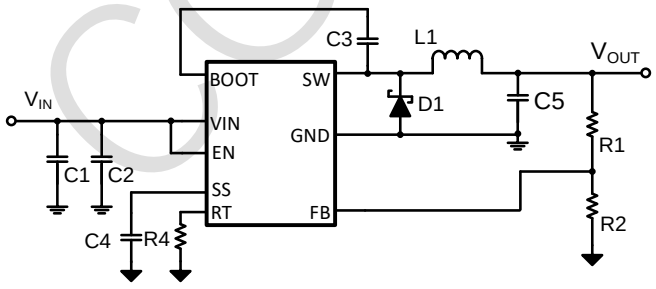
## 3 ORDERING INFORMATION

| TYPE | MARKING | PACKAGE |
|---|---|---|
| GBI1450SMAR | 1450 | eSOP-8 |

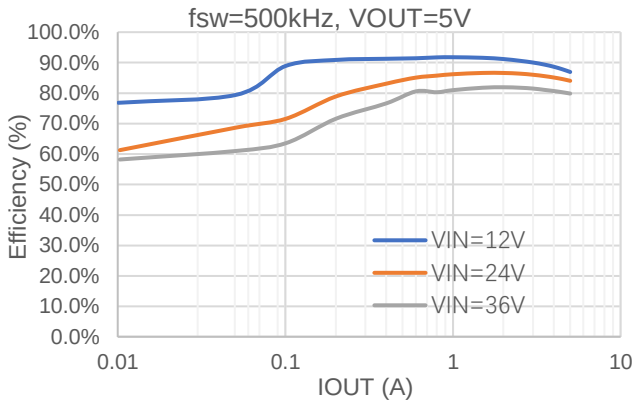
## 4 DISCRIPTION

The GBI1450 is 40V, 5A buck converter with an integrated 80 mΩ high-side MOSFET. The GBI1450 has wide input range from 4.0V to 40V, the GBI1450 is suitable for variable applications which is from unregulated sources, like industrial or automotive applications. The device adopts peak current mode and supports a wide adjustable switching frequency range, setting by external resistor. The quiescent current of this device is 100uA in sleep mode and the shutdown current is 1uA, making it suitable for battery-powered system. The device integrates protections, like cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. It’ s available in an 8-pin eSOP-8L package.

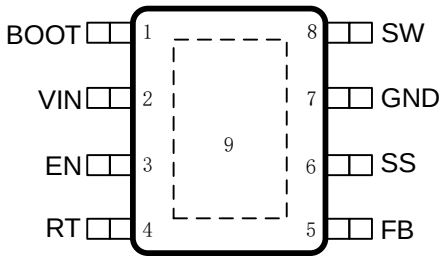
## 5 TYPICAL APPLICATIONS




Simplified Schematic



## 6 PIN CONFIGURATION AND FUNCTIONS




Top View: GBI1450 eSOP-8L

| PIN OUT | | I/O | PIN FUNCTION |
|---|---|---|---|
| NAME | NO. | | |
| BOOT | 1 | I | Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BOOT pin and SW pin. |
| VIN | 2 | I | Power supply input. Must be locally bypassed. |
| EN | 3 | I | Enable logic input. Floating the pin enables the device. This pin supports high voltage up to VIN supply. The device has precision enable thresholds 1.21V rising / 1.05V falling for programmable UVLO threshold. The hysteresis is programmable by external resistor network. |
| RT | 4 | I | Resistor Timing. |
| FB | 5 | I | Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT node to FB pin and from FB pin to GND to set up output voltage. The device regulates FB to the internal reference of 0.8V typically. |
| SS | 6 | I | Connect to a capacitor to set soft-start time. |
| GND | 7 | G | Ground. |
| SW | 8 | O | Switching node of the buck converter. |
| Thermal Pad | 9 | G | Must be grounded in PCB layout. |

# 7 SPECIFICATIONS

## 7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

| DESCRIPTION | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Voltage | VIN, EN to GND | -0.3 | 42 | V |
| | FB to GND | -0.3 | 6.5 | V |
| | SS to GND | -0.3 | 6.5 | V |
| | RT to GND | -0.3 | 6.5 | V |
| Output Voltage | SW to GND | -3 | 42 | V |
| | BOOT to SW | | 6.5 | V |
| Junction temperature | $T_J$ | -40 | 150 | °C |
| Storage temperature | $T_{STG}$ | -65 | 150 | °C |

## 7.2 ESD RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1) | | ±2000 | V |
| | Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1) | | ±500 | V |

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

## 7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Supply voltage range | 4.0 | 40 | V |
| BOOT to SW | | 0 | 6 | V |
| FB, PG | | 0 | 6 | V |
| EN | | 0 | 40 | V |
| $f_{SW}$ | Switching frequency range at RT mode | 200 | 2500 | kHz |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

## 7.4 THERMAL INFORMATION

| PARAMETER | THERMAL METRIC | eSOP-8L | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance | 42.5 | °C/W |
| $R_{\theta JC\_top}$ | Junction to case (top) thermal resistance | 56.1 | °C/W |
| $R_{\theta JC\_bot}$ | Junction to case (bottom) thermal resistance | 3.8 | °C/W |
| $\psi_{JB}$ | Junction to board characterization parameter | 25.4 | °C/W |

## 7.5 ELECTRICAL CHARACTERISTICS

$V_{IN}$=EN=4.0V~40V, $T_J$=-40°C~125°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 4.0 | | 40 | V |
| $V_{IN\_UVLO}$ | Input UVLO<br>Hysteresis | $V_{IN}$ rising | | 3.6<br>350 | 3.8 | V<br>mV |
| $I_{SHDN}$ | Shutdown current | EN=0, No load, 4.0V≤$V_{IN}$≤40V | | 1 | 4 | uA |
| $I_Q$ | Quiescent current | EN=floating, No load, No switch, 4.0V≤$V_{IN}$≤40V, BOOT-SW=5V | | 100 | | uA |
| **Enable and Feedback** | | | | | | |
| $V_{EN\_H}$ | Enable high threshold | | | 1.21 | | V |
| $V_{EN\_L}$ | Enable low threshold | | | 1.05 | | V |
| $V_{FB}$ | Feedback Voltage | | | 0.8 | | V |
| **Power MOSFET** | | | | | | |
| $R_{DSON\_H}$ | High side FET on-resistance | | | 80 | | mΩ |
| **Switching Characteristics** | | | | | | |
| $f_{SW}$ | Switching frequency | $R_T$=200k | | 500 | | KHz |
| | Maximum switching frequency | | | 2.5 | | MHz |
| $t_{ON\_MIN}$ | Minimum on-time | | | 100 | | ns |
| $D_{MAX}$ | Maximum duty cycle | $f_{SW}$=500kHz | | 95 | | % |
| **Soft Start Time and Protection** | | | | | | |
| $I_{SS}$ | Soft start current | GBI1450 | | 4 | | uA |
| $I_{LIM\_HSD}$ | HSD peak current limit | $V_{IN}$=24V | | 8 | | A |

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{SD}$ | Thermal shutdown threshold | | | 170 | | °C |
| | Hysteresis | | | 30 | | |
| **Output Voltage Protection** | | | | | | |
| $V_{OVP\_H}$ | Output over voltage protection rising | | | 109 | | % |
| $V_{OVP\_L}$ | Output over voltage protection falling | | | 105 | | % |
| $V_{UVP\_L}$ | Output under voltage protection falling | | | 90 | | % |
| $V_{UVP\_H}$ | Output under voltage protection rising | | | 95 | | % |

## 7.6 TYPICAL CHARACTERISTICS

$V_{IN}$=24V, $f_{SW}$=500kHz, L=5.6uH, $C_{OUT}$=88uF, $T_A$= 25°C.

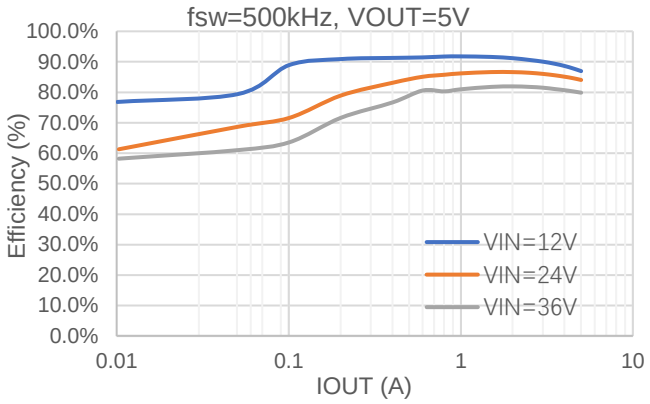



Figure 1 Power Efficiency

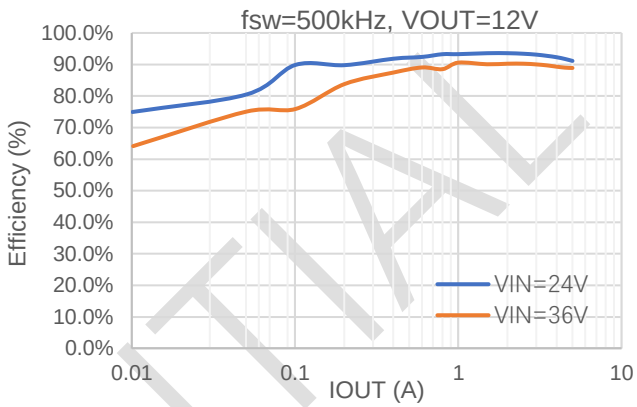



Figure 2 Power Efficiency

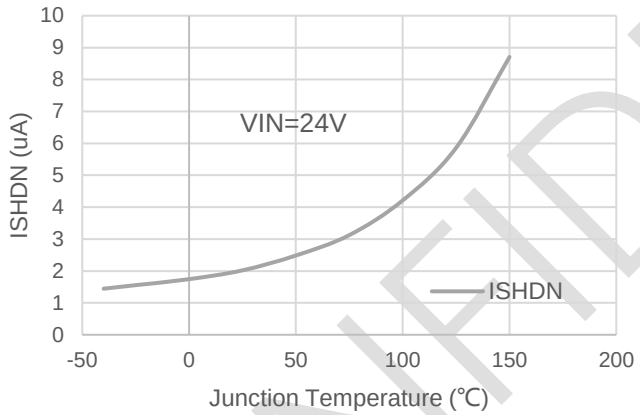



Figure 3 Shutdown Current

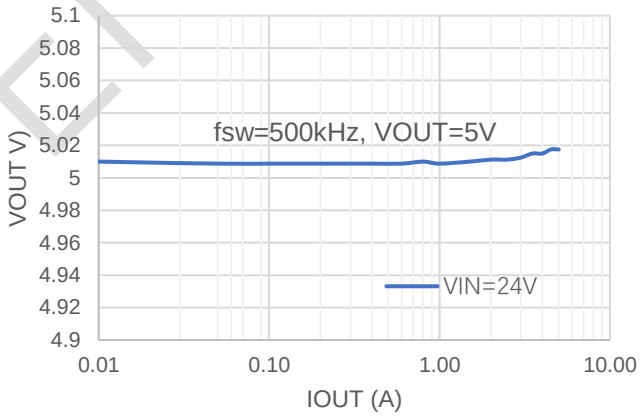



Figure 4 $V_{OUT}$ Vs. Load Regulation

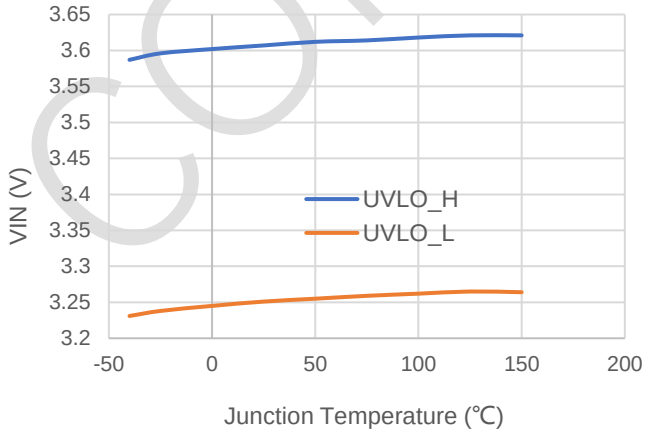



Figure 5 VIN UVLO Threshold

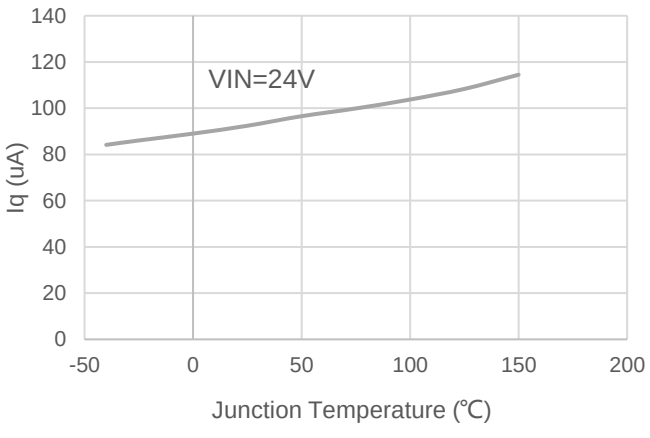



Figure 6 Quiescent Current

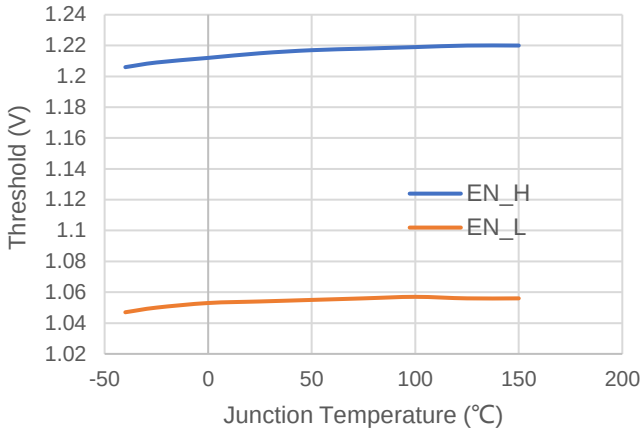



Figure 7 Enable Threshold

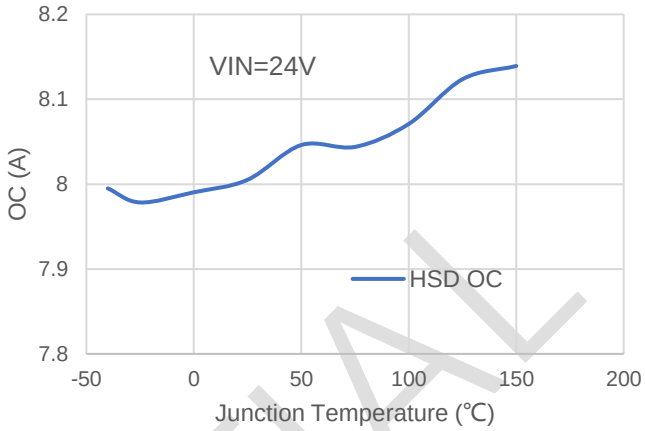



Figure 8 Over Current

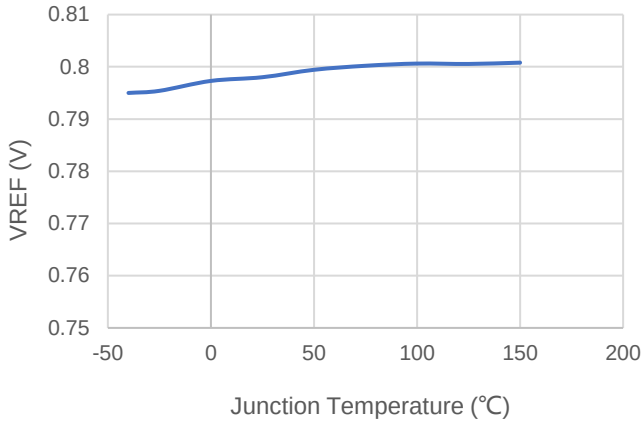



Figure 9 VREF Vs. Temperature

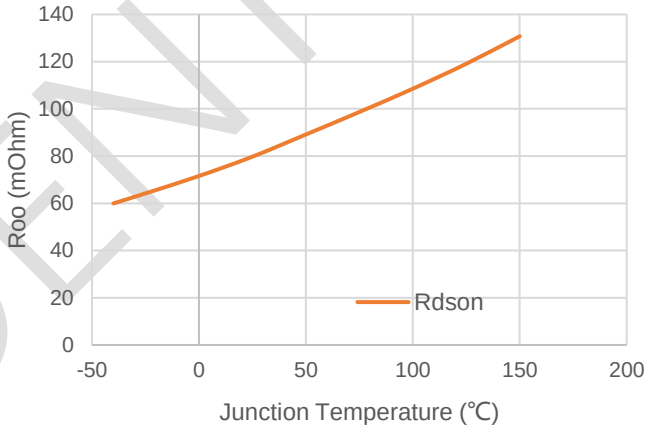



Figure 10 High Side MOSFET Rdson

# 8 FUNCTION BLOCK DIAGRAM

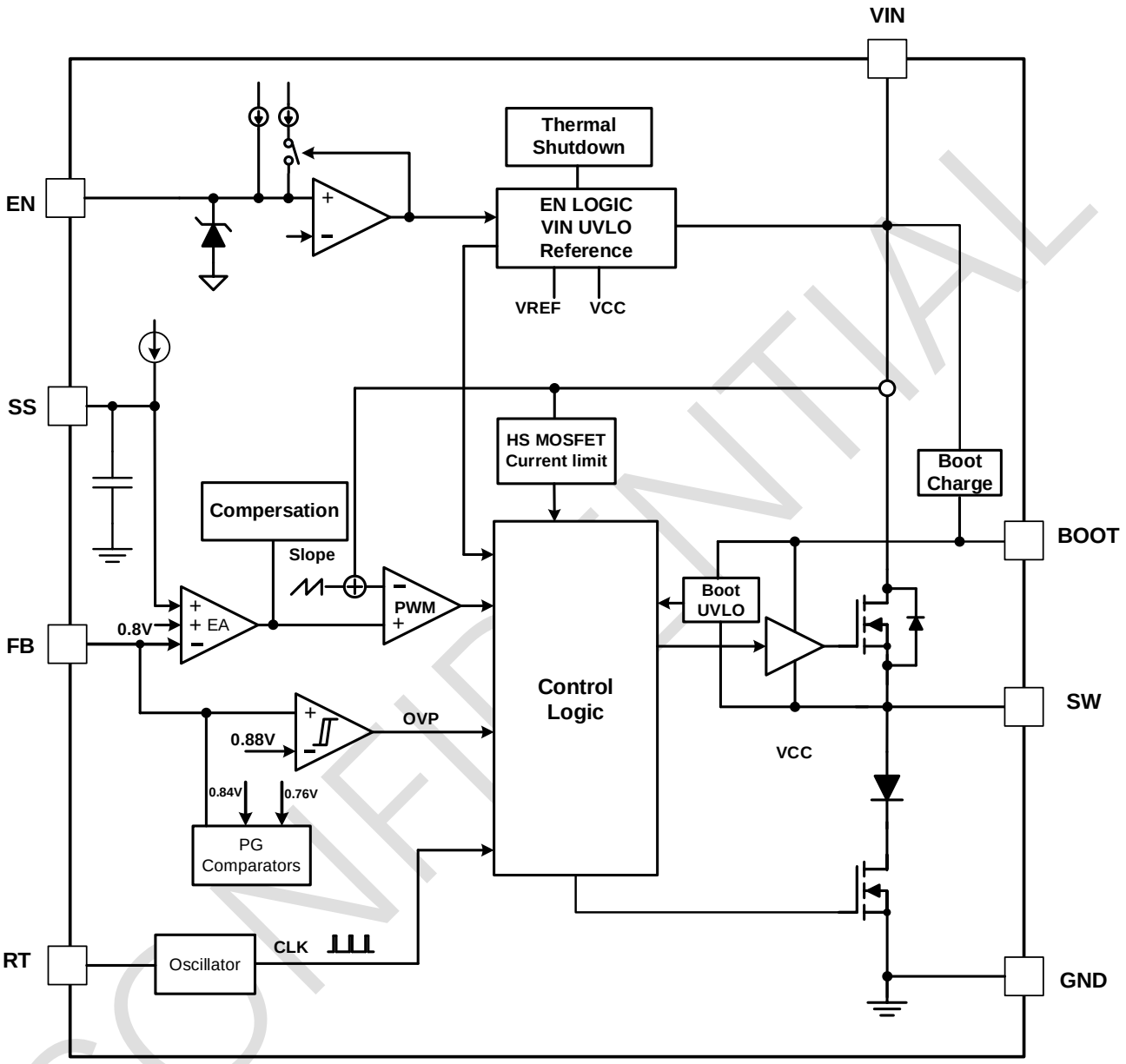



**Figure 11 Block Diagram of GBI1450**

# 9 DISCRIPTION

## 9.1 Overview

The GBI1450 is a 40V, 5A buck converter with an integrated 80 mΩ high-side MOSFET. With a wide input range from 4.0V to 40V, the device adopts peak current mode and supports a wide adjustable switching frequency range from 200kHz to 2.5MHz setting by external resistor.

The quiescent current of this device is 100uA in sleep mode and the shutdown current is 1uA. The GBI1450 adopts adjustable soft-start time by connecting an external capacitor from SS pin to GND.

The device has a default input start-up voltage of 3.6V with 350mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device. Connecting EN pin to VIN directly starts up the device automatically.

The device integrates protections, like cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device also supports monolithic startup with pre-biased output condition.

It's available in an 8-pin eSOP-8L package.

## 9.2 Peak Current Mode Control

The GBI1450 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the internal compensation voltage of the internal error amplifier, the high-side MOSFET turns off. When the high-side MOSFET turns off, the inductor current discharges through the external diode till the next clock cycle begins.

The integrated error amplifier and the internal compensation builds up the feedback loop to regulates the output voltage to the reference. The error amplifier comparing the voltage of the FB pin with an internal reference voltage of 0.8V. The load current increasement reduces the feedback voltage which is relative to a voltage raise of the error amplifier output till the average inductor current matches the increased load current.

The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

## 9.3 Pulse Skipping Mode (PSM)

The GBI1450 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. A



decrease of the load current leads an increasement in the feedback voltage which yields down the compensation voltage. When the compensation voltage drops to a low clamp threshold, the PSM is triggered. During the skipping period, the discharge of output capacitor leads the output voltage drop which makes the FB voltage decay. Once the FB voltage drops lower than the reference voltage and the compensation voltage rises above the low clamp threshold, the integrated high-side MOSFET turns on in next clock pulse. After several switching cycles with typical 0.35A peak inductor current, the internal compensation voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This PSM helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. Regarding to improve efficiency further, the quiescent current is 100uA during skipping period with no switching.

## 9.4 VIN Power

The GBI1450 is designed to operate from an input voltage supply range between 4.0V to 40V, at least 0.1uF and 47uF decoupling ceramic cap are recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional 47uF electrolytic bulk capacitor may be required in addition to the local ceramic bypass capacitors.

## 9.5 Under Voltage Lockout Threshold and Enable

The EN pin of GBI1450 is a high voltage pin which can be connected to VIN directly to start-up the device. The GBI1450 is enabled when the EN pin voltage higher than the enable threshold of 1.21V and disabled when the EN pin voltage lower than 1.05V. Grace to the internal 1.0uA pull-up current, the device is default enabled when the EN pin floats.

The Under Voltage Lock Out (UVLO) default startup threshold is typical 3.6V with VIN rising and shutdown threshold is 3.25V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin. Connect an external resistor divider (RL and RH) shown in Figure 7 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.



$$\mathrm{RH} = \frac{V_{rise} - V_{fall}}{3.0uA} \quad (1)$$

$$\mathrm{RL} = \frac{1.21\mathrm{V}}{\frac{V_{rise} - 1.21V}{R_H} + 1.0uA} \quad (2)$$

where

- $V_{rise}$ is rising threshold of Vin UVLO
- $V_{fall}$ is falling threshold of Vin UVLO

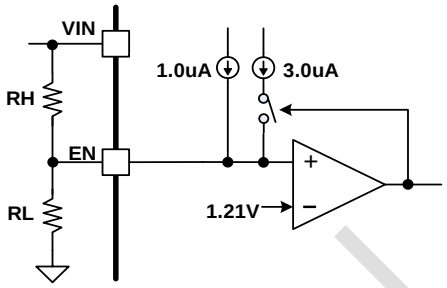



Figure 12 System UVLO by EN divider

## 9.6 Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off.

The floating supply (BOOT to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs.

## 9.7 Output Voltage

The GBI1450 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range.

The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the value is higher, the regulator will be more noise sensitive. RFB_BOT in the range of 10kΩ to 100kΩ is recommended for most application.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{0.8V} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- $R_{FB\_TOP}$ is the resistor connecting the output to the FB pin.
- $R_{FB\_BOT}$ is the resistor connecting the FB pin to the ground.

## 9.8 Switching Frequency

The switching frequency of the GBI1450 is set by placing a resistor between RT pin and the GND. The RT pin is not allowed to be left floating or shorted to the GND.

In resistor setting frequency mode, use Equation 4. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (4)$$

where, fsw is switching clock frequency.

## 9.9 Programmable Soft-Start (GBI1450)

GBI1450 features programmable soft-start time to avoid inrush current during start-up stage by placing a soft-start capacitor from SS pin to ground. The soft-start time is easily calculated following equation 5.

$$C_{soft-start} = t_{ss} * \frac{4\text{uA}}{0.8V} \quad (5)$$

Where:

- $C_{soft\text{-}start}$ is the soft-start capacitor connected from SS pin to the ground
- $t_{ss}$ is the soft-start time

## 9.10 Overcurrent and Short Circuit Protection

The GBI1450 adopts the peak current mode control. In the overcurrent momentum, the output voltage is yield down by heavy load and the error amplifier drives the compensation voltage high to increase the switching current. As the error amplifier output increases, it will be clamped internally, and the high-side current is clamped by a maximum peak current threshold. The peak current threshold is constant over the full duty cycle range.

When the output overcurrent or short circuit occurs, the device will trigger a frequency foldback by dividing the oscillator frequency with a pre-set frequency foldback factor to protect itself by increasing the switching frequency and the off time of high-side MOSFET. This will lead more time for the inductor current to ramp down. Otherwise, a lower switching frequency contributes on lower switching loss and avoiding overheating and other potential damages.

The frequency foldback factor is relative with the FB pin voltage.



**Table 1 Frequency Foldback Factor vs $V_{FB}$**

| FB pin voltage | Frequency Foldback Factor |
|---|---|
| 75% $V_{REF}$ | 2 |
| 50% $V_{REF}$ | 4 |
| 25% $V_{REF}$ | 8 |

## 9.11 Overvoltage Protection

The GBI1450 implements the overvoltage protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. When the FB pin voltage reaches the rising OVP threshold which is typically 109% of $V_{REF}$, the high-side MOSFET will be turned off immediately which make the device under OVP. When the FB pin voltage drops below the falling OVP threshold, the high-side MOSFET is turned on and resumed normal operation. The falling OVP threshold is typically 105% of $V_{REF}$.

## 9.12 Thermal Shutdown

The GBI1450 features an internal thermal shutdown circuit to protect the device from the damage during excessive heat and power dissipation conditions. The thermal shutdown circuit will be asserted when the junction temperature exceeds typically 170°C. When the junction temperature falls below 150C, the device restarts with internal soft start phase.

# 10 APPLICATION INFORMATION

### Typical Application

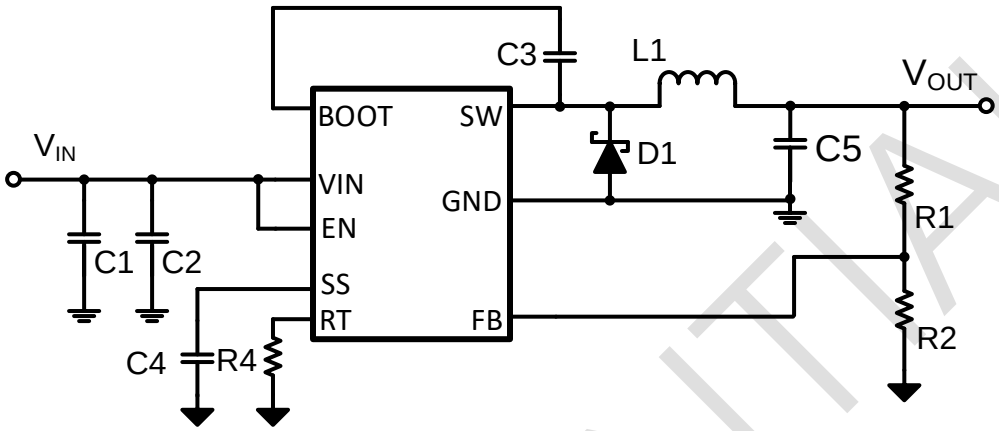



Figure 13 24V INPUT, 5V 5A OUTPUT

**Table 2. Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 24V typical, 7~40V |
| Output Voltage | 5V |
| Output Current | 5A |
| Output voltage ripple (peak to peak) | <50mV |
| Overshoot/Undershoot range (0.75~2.25A) | 5% |
| Input Voltage ripple (peak to peak) | <400mV |
| Switching Frequency | 500kHz |

## 10.1 Set Output Voltage

The GBI1450 output voltage can be easily set up using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 9. Use Equation (6) to calculate the resistor divider values.

$$R1 = \frac{(V_{OUT} - 0.8) \times R2}{0.8} \quad (6)$$

In this design example the Vout is 5V. Set the resistor R2 value to be approximately 10k.

$$R1 = \frac{(V_{OUT} - 0.8) \times R2}{0.8} = \frac{(5 - 0.8) \times 10k\Omega}{0.8} = 52.5\ k\Omega$$

Slightly increasing or decreasing R1 to a closest available resistance, the 52.3 kΩ is selected.

## 10.2 Set Switching Frequency

The GBI1450 switching frequency is able to be set-up by placing a local resistor from RT/SYNC pin to GND. Use following equation to calculate the resistor value.

$$R4(K\Omega) = \frac{100000}{fsw(KHz)} = \frac{100000}{500} = 200\ k\Omega \quad (7)$$

For 500kHz switching frequency, the R4 is 200 kΩ.

## 10.3 Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A X7R ceramic capacitor 4.7uF to 22μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin. These capacitors must be rated for at least 50V.

For this design, two 4.7uF X7R capacitors and one 0.1uF capacitor rated 50V is recommended.

The input voltage ripple can be calculated by using Equation (8) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{5A}{2 \times 4.7uF \times 500k} \times \frac{5V}{24V} \times \left(1 - \frac{5V}{24V}\right) = 180\ mV \quad (8)$$

Where:

- $C_{IN}$ is the input capacitor value
- $f_{sw}$ is the converter switching frequency
- $I_{OUT}$ is the maximum load current

## 10.4 Inductor Selection

The performance of inductor affects the power supply' s steady state operation, transient behavior, loop stability, and buck converter efficiency. The critical parameters of inductor is the inductance, the DC resistance (DCR), the saturation current and the RMS current.

Use following equation to the minimum inductance:

$$L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (9)$$

Where

- $V_{OUT}$ is output voltage
- $K_{IND}$ is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here

- $V_{INMAX}$ is the maximum input voltage
- $f_{SW}$ is the converter switching frequency
- $I_{OUT}$ is the output current

In this design example:

$$L > L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} = \frac{5V \times (40V - 5V)}{40V \times 0.4 \times 5A \times 500KHz} = 4.375\ uH$$

Generally, the Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation. The peak switching current of inductor is calculated in equation 11:

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} = 5A + 0.4 \times \frac{5A}{2} = 6\ A$$

A minimum inductance of 4.7uH and the peak saturation current of 8.5A is recommended.

## 10.5 Output Capacitor

The output capacitor must be chosen carefully with the reason that this capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Generally, choose a low-ESR output capacitor like a ceramic capacitor from X5R or X7R family to get small output voltage ripple.

From the required output voltage ripple (<50mV), use the Equation 10 to calculate the minimum required effective capacitance, $C_{OUT}$.

$$C_{OUT} > \frac{\Delta I_{LPP}}{8 \times V_{OUT\_Ripple} \times f_{SW}} = \frac{K_{IND} \times I_{OUT}}{8 \times V_{OUT\_Ripple} \times f_{SW}} \quad (10)$$

The allowed maximum ESR of the output capacitor is calculated by the equation 11.

$$R_{ESR} < \frac{V_{OUT\_Ripple}}{k_{IND} \times I_{OUT}} \quad (11)$$

Where

- $V_{OUT\_Ripple}$ is output voltage ripple caused by charging and discharging of the output capacitor.
- $k_{IND}$ is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.4 is recommended here
- $I_{OUT}$ is the maximum output current
- $f_{SW}$ is the converter switching frequency.

In this design, $V_{OUT\_Ripple}$ is smaller than 50mV, $f_{SW}$ is 500kHz, $I_{OUT}$ is 5A and $K_{IND}$ is 0.4:



$$C_{OUT} > \frac{0.4 \times 5A}{8 \times 50mV \times 500k} = 10\ uF$$

$$R_{ESR} < \frac{50mV}{0.4 \times 5A} = 25\ m\Omega$$

In buck converter, higher capacitor values can be used to improve the load transient response. Normally the converter control loop needs to take some switching clock cycles to respond to the output voltage changes. The output capacitors must be relatively large enough to charge or discharge current to maintain the output voltage within the specified range in 3 clock cycles. The following two Equations are used to calculate the minimum capacitance to keep the undershoot and overshoot voltages within a specified range.

$$C_{OUT} > \frac{3 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} \quad (12)$$

$$C_{OUT} > \frac{I_{TOH}^2 - I_{TOL}^2}{(V_{OUT} + V_{OOS})^2 - V_{OUT}^2} \times L \quad (13)$$

Where

- $I_{TOH}$ is the high level of output current during load transient
- $I_{TOL}$ is the low level of output current during load transient
- $V_{OUS}$ is the undershoot voltage
- $V_{OOS}$ is the overshoot voltage
- L is the inductance of inductor in design
- $f_{SW}$ is the converter switching frequency.

For this design example:

$$C_{OUT} > \frac{3 \times (I_{TOH} - I_{TOL})}{f_{SW} \times V_{OUS}} = \frac{3 \times (3.75A - 1.25A)}{500kHz \times 250mV} = 60\ uF$$

$$C_{OUT} > \frac{3.75A^2 - 1.25A^2}{(5V + 250mV)^2 - 5^2} \times 8.2uH = 24.6\ uF$$

Therefore, X7R capacitor of 88uF with 16V DC rating and 15mΩ ESR is selected

## 10.6 Catch Diode

The GBI1450 requires an external catch diode between the SW pin and GND. The critical parameters of this catch diode are the reverse voltage, the peak current, the forward voltage and the junction capacitance. Generally, the reverse voltage rating equal to or greater than the maximum input voltage. The peak current

must be greater than the maximum inductor current. Lower forward voltage and smaller junction capacitance yields higher efficiency and lower power dissipation. The Schottky diodes are typically good choose as the catch diode.

In this design example, the B540C-13-F is selected with 40V reverse voltage, 5A maximum current, 0.55V forwards voltage and 300pF junction capacitance.

The power dissipation is calculated as in following equation

$$P_{DMAX} = \frac{(V_{INMAX} - V_{OUT}) \times I_{OUT} \times V_{fd}}{V_{INMAX}} + \frac{C_j \times f_{SW} \times (V_{INMAX} + V_{fd})^2}{2} \quad (14)$$

Where

- $V_{INMAX}$ is the maximum input voltage
- $I_{OUT}$ is the output current
- $V_{OUT}$ is the output voltage
- $f_{SW}$ is the switching frequency
- $V_{fd}$ is the forward voltage

In this design example:

$$P_{DMAX} = \frac{(40V - 5V) \times 5A \times 0.55V}{40V} + \frac{300pF \times 500kHz \times (40V + 0.55V)^2}{2} = 2.52\ W$$

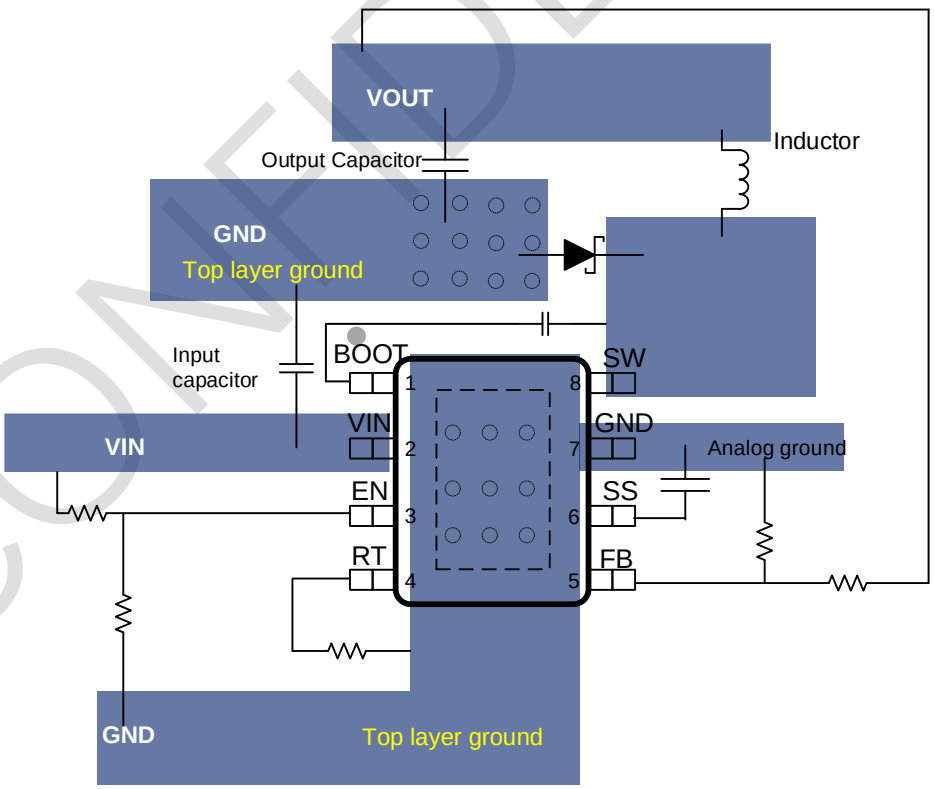
## 10.7 Bootstrap Capacitor

For proper operation of the device, a 0.1uF ceramic capacitor of X5R or X7R must be placed between the SW pin to the BOOT pin. The DC rating of this capacitor is must be 10V or higher voltage level.

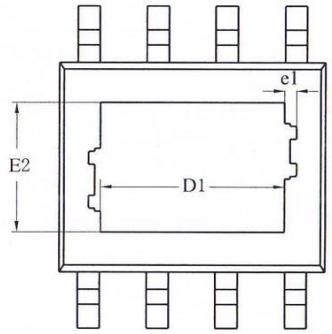
## 11 Layout Guideline

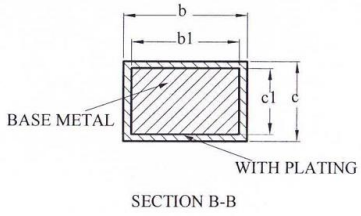
Layout is critical for proper operation. Please follow the layout guidelines.

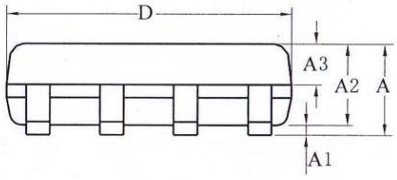
1. The power ground is very critical. The power trace should take lowest impedance as possible and the ground area should be sufficient and event to optimize thermal.
2. The GND Pin should be connected directly to the thermal pad under the IC, 8mil Max thermal via recommended.
3. Place the bypass input capacitor with low ESR as close as possible to the VIN pin and GND. The bypassing loop from VIN terminal to the GND should be as short as possible.
4. The RT is sensitive to noise. The RT resistor should be placed as close as possible to the RT pin with minimum trace length to the GND.
5. The inductor should be located as close as possible to the SW pin for reducing magnetic and electrostatic noise
6. The feedback resistor divider should be placed close to the FB pin.
7. The ground connected to the diode, input capacitors and output capacitors should be tied to the system ground plane in only one spot to minimize conducted noise to the system ground plane
8. Four-layer layout is strongly recommended for better thermal performance.

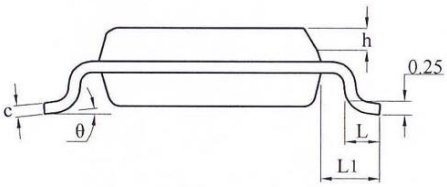


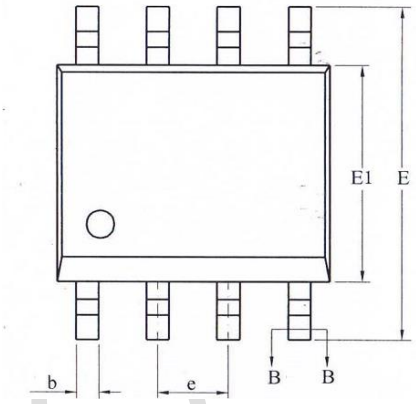
## PACKAGE INFORMATION (eSOP-8L Package)




| LF Size | D1 | E2 | e1 |
|---|---|---|---|
| 95*130 | 3.1 | 2.21 | 0.16 |

| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nor | Max |
| A | - | - | 1.65 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.3 | 1.4 | 1.5 |
| A3 | 0.6 | 0.65 | 0.7 |
| b | 0.39 | - | 0.7 |
| b1 | 0.38 | 0.41 | 0.44 |
| c | 0.2 | - | 0.24 |
| c1 | 0.19 | 0.2 | 0.21 |
| D | 4.8 | 4.9 | 5.0 |
| E | 5.8 | 6.0 | 6.2 |
| E1 | 3.8 | 3.9 | 4.0 |
| e | 1.27BSC | | |
| h | 0.25 | - | 0.5 |
| L | 0.5 | 0.6 | 0.8 |
| L1 | 1.05REF | | |
| θ | 0 | - | 8° |