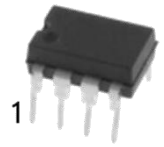
Serial Timekeeper Chip

Features

- Operating voltage: 2.0V~5.5V
- Maximum input serial clock: 500kHz at V_{DD}=2V, 2MHz at V_{DD}=5V
- Operating current: less than 1μA at 2V,less than 1.2μA at 5V
- TTL compatible
  - V_{IH}:2.0V~V_{DD}+0.3V at V_{DD}=5V
  - V_{IL}:0.3V~+0.8V at V_{DD}=5V
- Two data transmission modes: single-byte,or burst mode
- Serial I/O transmission
- All registers store BCD format
- HT1380: 8-pin DIP package
  HT1381: 8-pin SOP package



DIP-8

SOP-8

Applications

- Microcomputer serial clock
- Clock and Calendar

Ordering Information

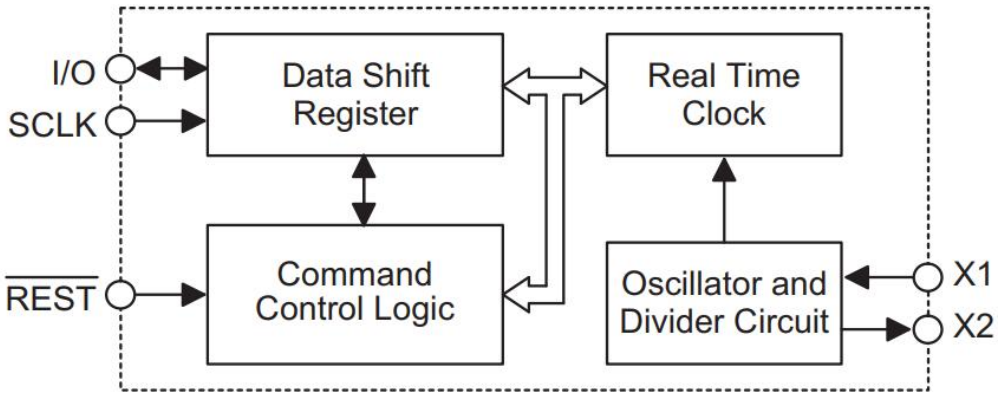
DEVICE	Package Type	MARKING	Packing	Packing Qty
HT1380N	DIP-8	HT1380	TUBE	2000pcs/box
HT1381M/TR	SOP-8	HT1381	REEL	2500pcs/reel

General Description

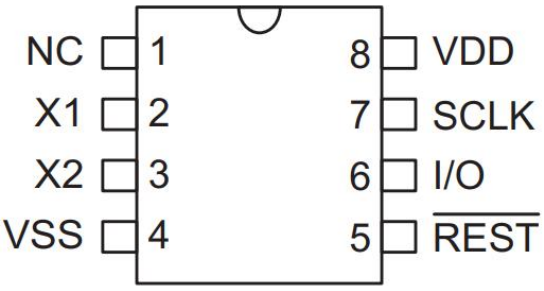
The HT1380/HT1381 is a serial timekeeper IC which provides seconds, minutes, hours, day, date, month and year information. The number of days in each month and leap years are automatically adjusted. The HT1380/HT1381 is designed for low power consump- tion and can operate in two modes: one is the 12-hour mode with an AM/PM indicator, the other is the 24-hour mode.

The HT1380/HT1381 has several registers to store the corresponding information with 8-bit data format. A 32768Hz crystal is required to provide the correct tim- ing. In order to minimize the pin number, the HT1380/HT1381 use a serial I/O transmission method to interface with a microprocessor. Only three wires are required: (1) $\overline{\text{REST}}$ (2) SCLK and (3) I/O. Data can be delivered 1 byte at a time or in a burst of up to 8 bytes.

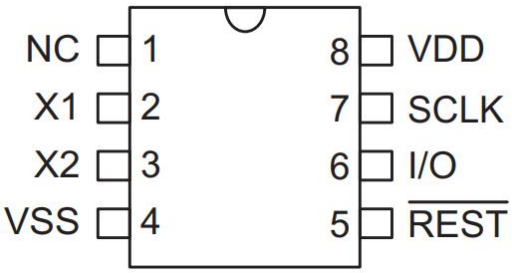
Block Diagram



Pin Assignment



DIP-8（HT1380）



SOP-8（HT1381）

PIN Description

PIN No.	PIN Name	I/O	Internal Connection	Description
1	NC			No internal commection
2	X1	I	CMOS	32768Hz crystal input pad
3	X2	O	CMOS	Oscillator output pad
4	VSS		CMOS	Negative power supply, ground
5	$\overline{\text{REST}}$	I	CMOS	Reset pin with serial transmission
6	I/O	I/O	CMOS	Data input/output pin with serial transmission
7	SCLK	I	CMOS	Serial clock pulse pin with serial transmission
8	VDD		CMOS	Positive power supply

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	0.3	5.5	V
Input Voltage	V_{SS}-0.3V	V_{DD}+0.3V	V
Operating Temperature	0	70	°C

Note: These are stress ratings only. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

（Ta=25℃）

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage			2		5.5	V
I_{STB}	Standby Current	2V				100	nA
		5V				100	nA
I_{DD}	Operating Current	2V	No load		0.7	1.0	μA
		5V			0.7	1.2	μA
I_{OH}	Source Current	2V	V_{OH}=1.8V	0.2	0.4		mA
		5V	V_{OH}=4.5V	0.5	1.0		mA
I_{OL}	Sink Current	2V	V_{OL}=0.2V	0.7	1.5		mA
		5V	V_{OL}=0.5V	2.0	4.0		mA
V_{IH}	“H” Input Voltage	5V		2			V
V_{IL}	“L” Input Voltage	5V				0.8	V

Note: ISTB is specified with SCLK, I/O, $\overline{\text{REST}}$ open. The clock halt bit must be set to logic 1 (oscillator disabled).

A.C.Characteristics

（Ta=25℃）

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{DC}	Data to Clock Setup	2V		200			ns
		5V		50			
t_{CDH}	Clock to Data Hold	2V		280			ns
		5V		70			
t_{CDD}	Clock to Data Delay	2V				800	ns
		5V				200	
t_{CL}	Clock Low Time	2V		1000			ns
		5V		250			
t_{CH}	Clock High Time	2V		1000			ns
		5V		250			
f_{SCLK}	Clock Frequency	2V				0.5	MHz
		5V				2.0	
t_r	Clock Rise and Fall Time	2V				2000	ns
t_f		5V				500	
t_{CC}	Reset to Clock Setup	2V		4			us
		5V		1			
t_{CCH}	Clock to Reset Hold	2V		240			ns
		5V		60			
t_{CWH}	Reset Inactive Time	2V		4			us
		5V		1			
t_{CDZ}	Reset to I/O High Im- pedance	2V				280	ns
		5V				70	

Functional Description

The HT1380/HT1381 mainly contains the following in- ternal elements: a data shift register array to store the clock/calendar data, command control logic, oscillator circuit and read timer clock. The clock is contained in eight read/write registers as shown below. Data con- tained in the clock register is in binary coded decimal format.

Two modes are available for transferring the data be- tween the microprocessor and the HT1380/HT1381. One is in single-byte mode and the other is in multi- ple-byte mode.

The HT1380/HT1381 also contains two additional bits, the clock halt bit (CH) and the write protect bit (WP).

These bits control the operation of the oscillator and so data can be written to the register array. These two bits should first be specified in order to read from and write to the register array properly.

Command Byte

For each data transfer, a Command Byte is initiated to specify which register is accessed. This is to determine whether a read, write, or test cycle is operated and whether a single byte or burst mode transfer is to occur. Refer to the table shown below and follow the steps to write the data to the chip. First give a Command Byte of HT1380/HT1381, and then write a data in the register.

This table illustrates the correlation between Command Byte and their bits:

Function Description	Command Byte							
	C7	C6	C5	C4	C3	C2	C1	C0
Select Read or Write Cycle								R/W
Specify the Register to be Accessed					A2	A1	A0	
Clock Halt Flag	C							
For IC Test Only	1	0	0	1	x	x	x	1
Select Single Byte or Burst Mode	1	0	1	1	1	1	1	x

Note: “X” stands for don’t care

The following table shows the register address and its data format:

Register Name	Range Data	Register Definition D7	D6	D5	D4	D3	D2	D1	D0	Address A2~A0	Bit R/W	Command Byte
Seconds	00~59	CH	10 SEC			SEC				000	W R	10000000 10000001
Minutes	00~59	0	10 MIN			MIN				001	W R	10000010 10000011
Hours	01~12 00~23	12\ 24	0 0	AP 10	HR HR	HOUR				010	W R	10000100 10000101
Date	01~31	0	0	10 DATE		DATE				011	W R	10000110 10000111
Month	01~12	0	0	0	10M	MONTH				100	W R	10001000 10001001
Day	01~07	0	0	0	0	DAY				101	W R	10001010 10001011
Year	00~99	10 YEAR				YEAR				110	W R	10001100 10001101
Write Protect	00~80	WP	ALWAYS ZERO							111	W R	10001110 10001111

CH：Clock Halt bit
CH=0 oscillator enabled
CH=1 oscillator disabled
WP：Write protect bit
WP=0 register data can be written in
WP=1 register data can not be written in
Bit 7 of Reg2：12/24 mode flag
bit 7=1, 12-hour mode
bit 7=0, 24-hour mode
Bit 5 of Reg2：AM/PM mode defined
AP=1 PM mode
AP=0 AM mode

R/W Signal

The LSB of the Command Byte determines whether thedata in the register be read or be written to.

When it is set as “0”means that a write cycle is to take place otherwise this chip will be set into the read mode.

A0~A2

A0 to A2 of the Command Byte is used to specify which registers are to be accessed. There are eight registers used to control the month data, etc., and each of these registers have to be set as a write cycle in the initial time.

Burst Mode

When the Command Byte is 10111110 (or 10111111), the HT1380/HT1381 is configured in burst mode. In this mode the eight clock/calendar registers can be written (or read) in series, starting with bit 0 of register address 0 (see the timing on the next page).

Test Mode

When the Command Byte is set as 1001xxx1, HT1380/HT1381 is configured in test mode. The test mode is used by Holtek only for testing purposes. If used generally, unpredictable conditions may occur.

Write Protect Register

This register is used to prevent a write operation to any other register. Data can be written into the designated register only if the Write Protect signal (WP) is set to logic 0. The Write Protect Register should be set first be- fore restarting the system or before writing the new data to the system, and it should set as logic 1 in the read cy- cle. The Write Protect bit cannot be written to in the burst mode.

Clock HALT Bit

D7 of the Seconds Register is defined as the Clock Halt Flag (CH).

When this bit is set to logic 1, the clock oscillator is stopped and the chip goes into a low-power standby mode. When this bit is written to logic 0, the clock will start.

12-hour/24-hour Mode

The D7 of the hour register is defined as the 12-hour or 24-hour mode select bit.

When this bit is in high level, the 12-hour mode is se- lected otherwise it s the 24-hour mode.

AM-PM Mode

These are two functions for the D5 of the hour register determined by the value D7 of the same register.

One is used in AM/PM selection on the 12-hour mode. When D5 is logic 1, it is PM, otherwise it s AM. The other is used to set the second 10-hour bit (20~23 hours) on the 24-hour mode.

Reset and Serial Clock Control

The $\overline{\text{REST}}$ pin is used to allow ccess data to the shift register like a toggle switch. When the $\overline{\text{REST}}$ pin is takenhigh, the built-in control logic is turned on and the address/command sequence can access the correspond- ing shift register. The $\overline{\text{REST}}$ pin is also used to terminate either single-byte or burst mode data format.

The input signal of SCLK is a sequence of a falling edge followed by a rising edge and it is used to synchronize the register data whether read or write. For data input, the data must be read after the rising edge of SCLK. The data on the I/O pin becomes output mode after the fall- ing edge of the SCLK. All data transfer terminates if the $\overline{\text{REST}}$ pin is low and the I/O pin goes to a high imped-ance state. The data transfer is illustrated on the next page.

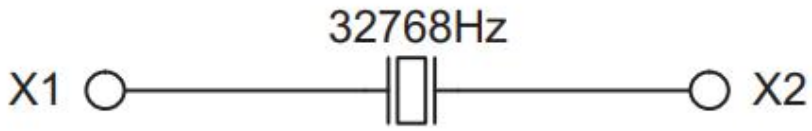
Data Input and Data Out

In writing a data byte with HT1380/HT1381, the read/write should first set as R/W=0 in the Command Byte and follow with the corresponding data register on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data inputs are entered start- ing with bit 0.

In reading a data on the register of HT1380/HT1381, R/W=1 should first be entered as input. The data bit out- puts on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted on the first falling edge after the last bit of the read command byte is written. Additional SCLK cycles re-transmits the data bytes as long as $\overline{\text{REST}}$ remains at high level. Data out- puts are read starting with bit 0.

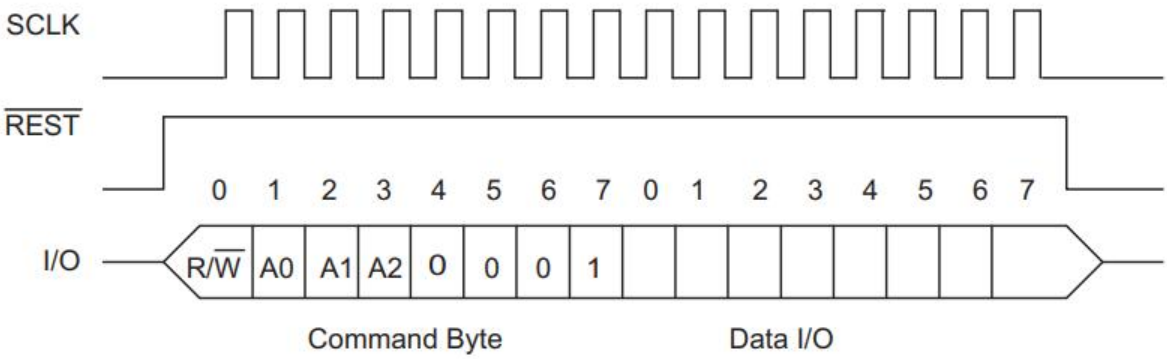
Crystal Selection

A 32768Hz crystal can be directly connected to the HT1380/HT1381 on pins 2 and 3 which are the crystal X1 and X2 pins. In order to ensure that the desired fre- quency is achieved, it is recommended to use a crystal with a capacitance of 9.0pF. It is not recommended that additional load capacitors are connected to the X1 and X2 pins. Refer to the following page for the crystal speci- fications.

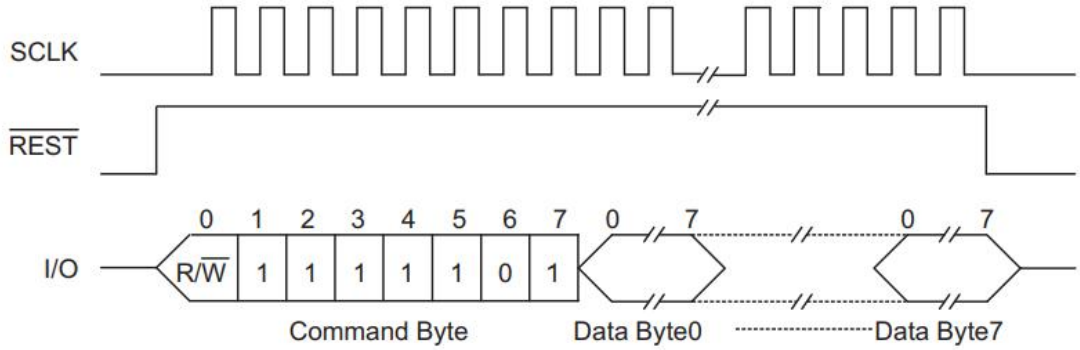


The following diagram shows the single and burst mode transfer:

Single Byte Transfer



Burst Mode Transfer



Crystal Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_O	Nominal Frequency		32.768		kHz
ESR	Series Resistance			50	kΩ
C_L	Load Capacitance		9.0		pF

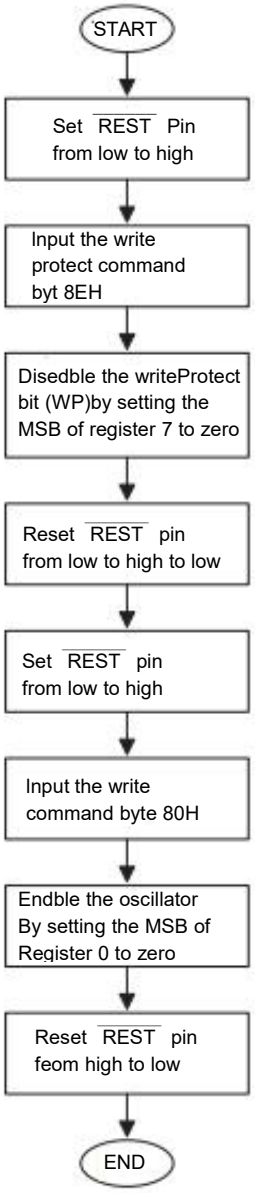
Note: 1. It is strongly recommended to use a crystal with a load capacitance of 9.0 pF. Never use a crystal with a load capacitance of 12.5 pF.
2. The oscillator selection can be optimized using a high quality resonator with a small ESR value. Refer to the crystal manufacturer for more details: www.microcrystal.com.

Operating Flowchart

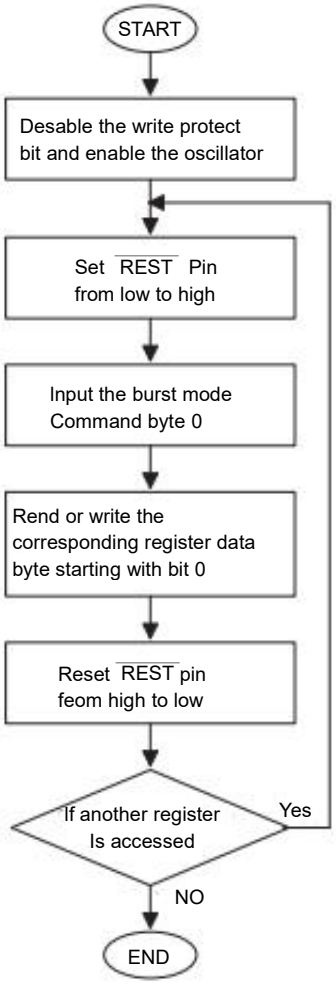
To initiate any transfer of data, $\overline{\text{REST}}$ is taken high and an 8-bit command byte is first loaded into the control logic to pro- vide the register address and command information. Following the command word, the clock/calendar data is serially transferred to or from the corresponding register. The $\overline{\text{REST}}$ pin must be taken low again after the transfer operation is completed. All data enter on the rising edge of SCLK and outputs on the falling edge of SCLK. In total, 16 clock pulses are needed for a single byte mode and 72 for burst mode. Both input and output data starts with bit 0.

In using the HT1380/HT1381, set first the WP and CH to 0 and wait for about 3 seconds, the oscillator will generate the clocks for internal use. Then, choose either single mode or burst mode to input the data. The read or write operating flowcharts are shown on the next page.

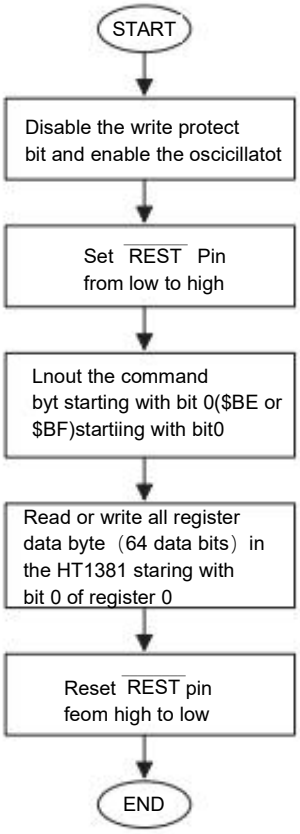
- To disable the write protect (WP=0) bit and enable the oscillator (CH=0)



- Single byte data transfer



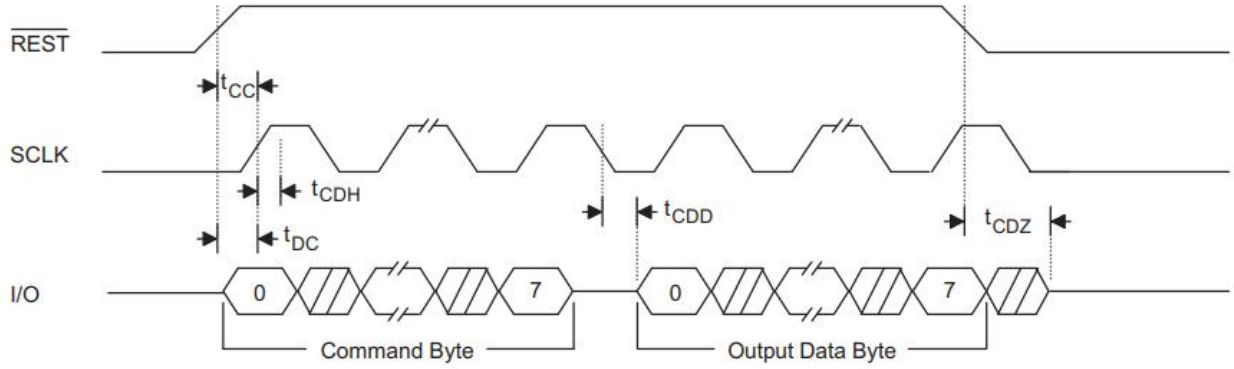
- Burst mode data transfer



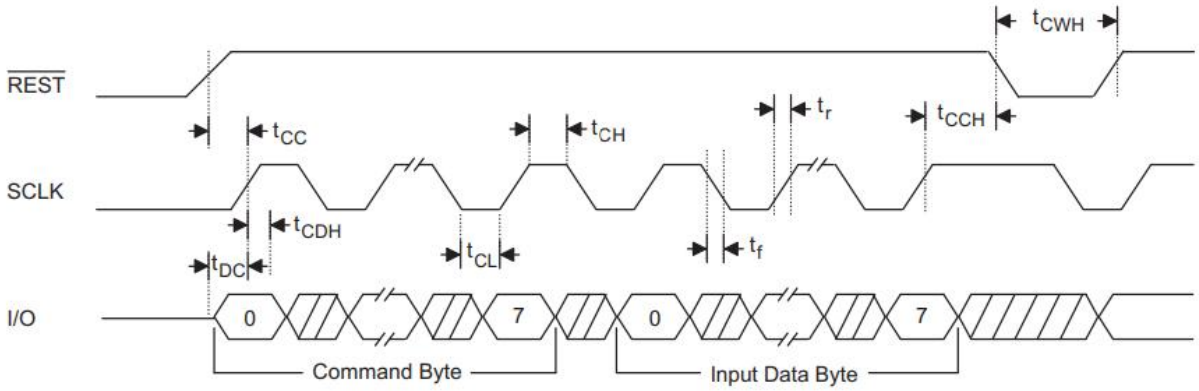
Note:*In reading data byte from HT1380/HT1381 register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

Timing Diagrams

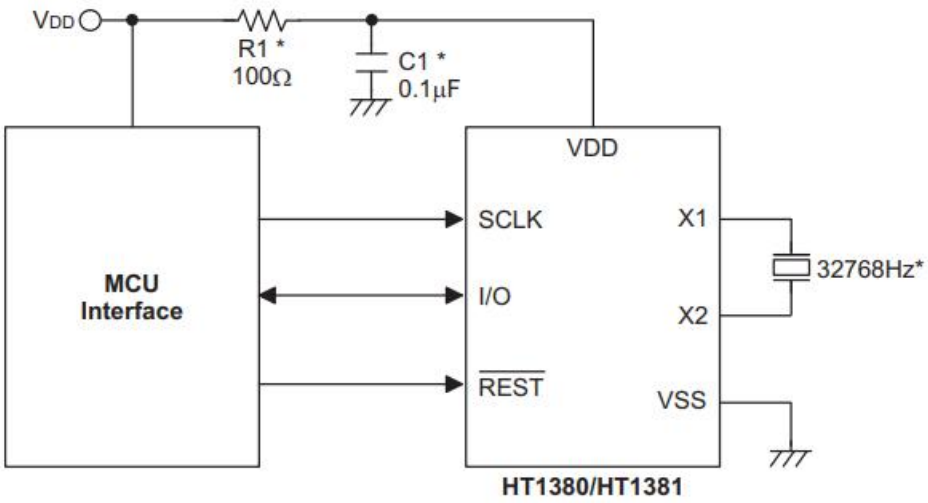
Read Data Transfer



Write Data Transfer



Application Circuits



Note: *

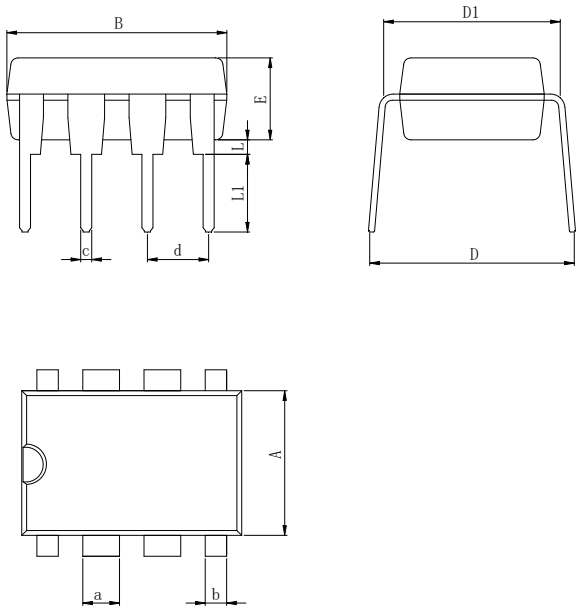
In order to obtain the correct frequency, it is recommended to use a crystal with a load capacitance of 9.0pF.

It is not recommended to connect load capacitors to the X1 and X2 pins.

If the power line is noisy, it is recommended to add R1 and C1 for filtering out noise.

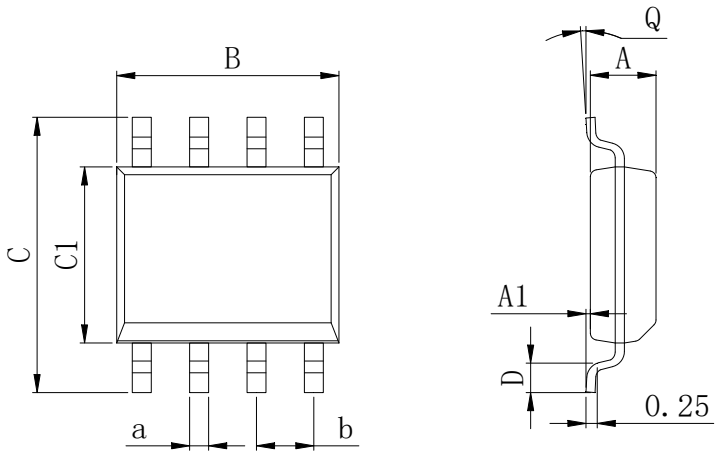
Physical Dimensions

DIP8



Dimensions In Millimeters(DIP8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.40	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP8 (150mil)



Dimensions In Millimeters(SOP8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Revision History

DATE	REVISION	PAGE
2014-6-5	New	1-16

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.