3A, Ultra-Low Dropout Voltage Regulator

General Description

The DS8570 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a VIN as low as 1V and VDD voltage 3V with programmable output voltage as low as 0.8V. The DS8570 features ultra low dropout, ideal for applications where VOUT is very close to VIN. Additionally, it has an enable pin to further reduce power dissipation while shutdown. The DS8570 provides excellent regulation over variations in line, load and temperature. The DS8570 provides a power good signal to indicate if the voltage level of VO reaches 90% of its rating value.

Features

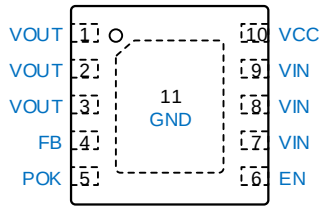
- Output Current up to 3A
- High Accuracy ADJ Voltage 1.5%
- Dropout Voltage 350mV @ 3A Typically
- VOUT Power Good Signal
- VOUT Pull Low Resistance when Disable
- Current Limiting Protection
- Thermal Shutdown Protection
- DFN3x3-10L & ESOP-8 Package Available

Applications

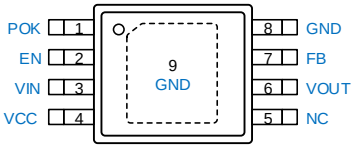
- Notebook PC Applications
- Motherboard Applications
- Graphics Cards Applications

Pin Configurations

DFN3x3-10L



ESOP-8



Ordering Information

DS8570XX

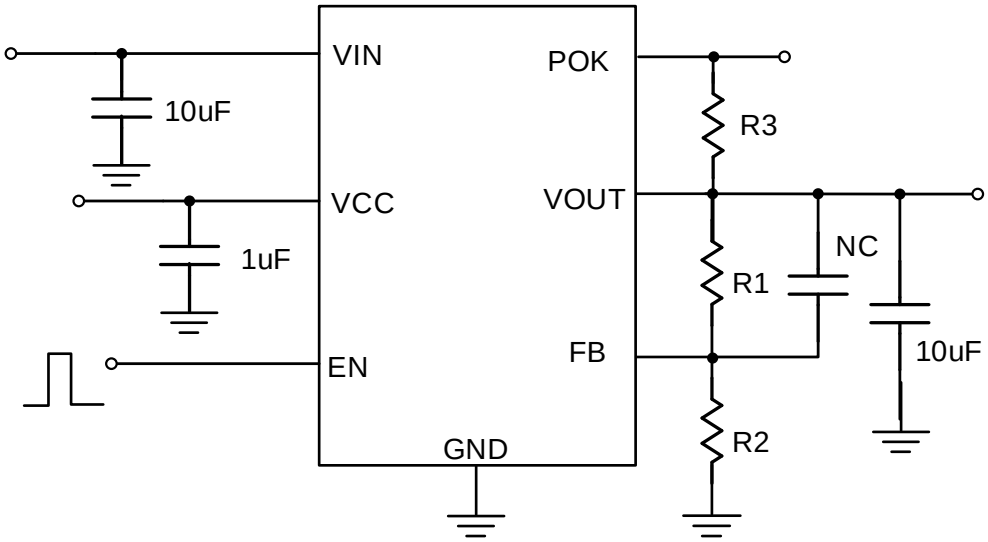
Designator	Description	Symbol	Description
X X	Package type	D10	DFN3x3-10L
		F8	ESOP-8

Example: DFN3x3-10L. Part no = DS8570D10

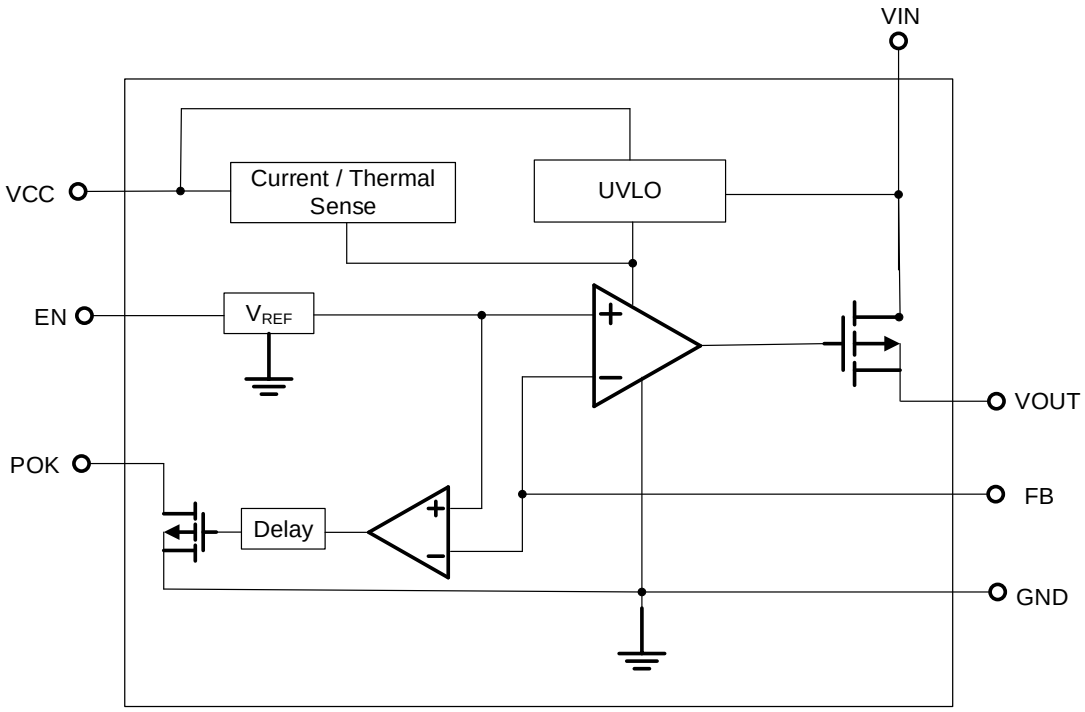
Description of Functional Pins

Pin No		Pin Name	Pin Function
DFN3x3-10L	ESOP-8		
1 , 2 , 3	6	VOUT	Output Voltage.
4	7	FB	Output voltage setting. VOUT = VREF x (R1+R2)/R2.
5	1	POK	Power good open drain output.
6	2	EN	Enable control input.
7 , 8 , 9	3	VIN	Input of Supply Voltage .
10	4	VCC	Supply Voltage of control circuit.
	5	NC	No Internal Connection.
	8	GND	Ground .
11 Exposed Pad	9 Exposed Pad	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuits



Function Block Diagram



Absolute Maximum Ratings (Note 1)

VIN & VCC to GND ---------- -0.3V to 6V

VOUT to GND ---------- -0.3V to 6V

Other to GND ---------- -0.3V to 6V

Package Thermal Resistance (Note 2)

ESOP-8 , θ_{JA} ---------- 75 °C /W

DFN3x3-10L , θ_{JA} ---------- 70 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -60 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

Recommended Operating Conditions

Input Voltage VIN ---------- 1V to 5.5V

Control Voltage, VCC (VCC > VOUT + 1.5V) ---------- 3V to 5.5V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Electrical Characteristics

(VCC = 5V, C_{IN} = C_{OUT} = 10uF, C_{VCC} = 1uF, T_A = 25℃, unless otherwise specified)

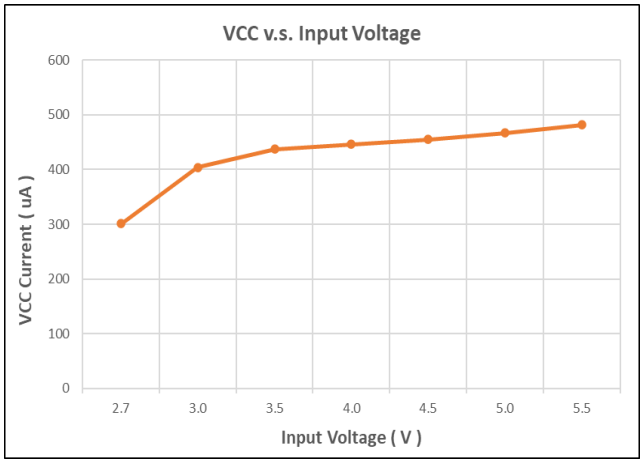
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Operation Range	V_{DD}		3	--	5.5	V
VCC POR Threshold	V_{POR_VCC}	V_{CC} Rising	2.4	2.7	3	V
VCC POR Falling Hysteresis	V_{POR_VCC}	V_{CC} Falling	0.15	0.2	--	V
Quiescent Current	IQ	EN on, no load	--	0.6	1.2	mA
Input Voltage Range	V_{IN}		1	--	5.5	V
VIN POR Threshold	V_{POR_VIN}	V_{IN} Rising	0.7	0. 8	0.9	V
VIN POR Falling Hysteresis	V_{POR_VIN}	V_{IN} Falling	0.15	0. 2	0.25	V
Reference Voltage	VREF		0.788	0.8	0.812	V
VOUT Load Regulation	VLOAD	IOUT = 1mA to 3A, VIN = VOUT + 1V	--	0.5	1	%
OUT Line Regulation	VLINE	V_{CC} = 3.6V to 5.5V, V_{IN} = V_{OUT} + 1V to 5V, I_{OUT} = 1mA	--	0.2	0.6	%
Dropout Voltage	VDROP	I_{OUT} = 2A	--	250	350	mV
		I_{OUT} = 3A	--	350	450	
Current Limit	ILIM	V_{IN} = 3.6V	3.1	3.6	4.2	A
Short Circuit Current	ISC	V_{OUT} < 0.2V	1	1.4	1.8	A
VOUT Pull Low Resistance	RPULL	VEN = 0V	--	150	--	Ω
Thermal Shutdown Temperature	TSD		--	160	--	ºC
Thermal Shutdown Recovery Temperature	TSDR		--	30	--	ºC
POK Rising Threshold	V_{TH_POK}	V_{OUT} Rising	--	90	--	%
POK Hysteresis	V_{TH_POK}	V_{OUT} Falling	--	10	--	%
POK Delay Time			--	1	1.5	mS
POK Sink Capability	V_{POK}	I_{SINK} = 10mA	--	0.2	0.4	V
EN Input Voltage	Logic-High	VIH	1.2	--	--	V
	Logic-Low	VIL	--	--	0.4	
EN Delay Time			0.3	0.85	1.4	mS
EN Pin Bias Current	IEN	VEN = 5V	--	12	--	uA

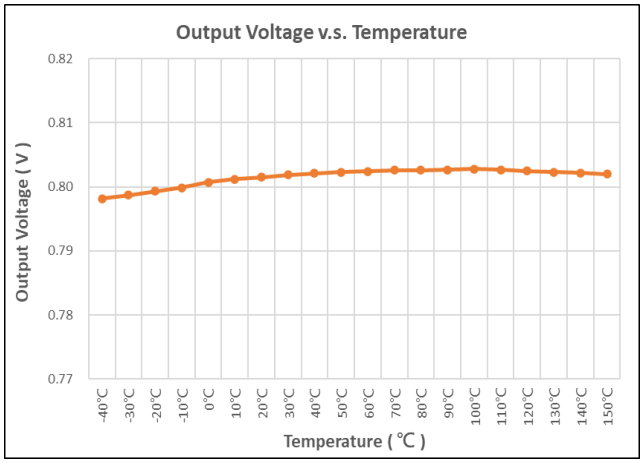
VDD Pin Shutdown Current	ISHDN_VDD	VEN = 0V	--	--	1	uA
VIN Pin Shutdown Current	ISHDN_VIN	VEN = 0V, VIN = 5V	--	--	1	uA
Inrush Current	I_{INRUSH}	VOUT = 1.8V, COUT = 10uF, ILOAD = 1A	--	0.5	--	A
Soft-Start Time	T_{SS}		1.9	2.8	3.75	mS

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

Typical Characteristics





Application Guideline

Adjustable Mode Operation

The output voltage of the DS8570 is adjustable from 0.8V to VIN by external voltage divider resisters as shown in Typical Application Circuit. The value of resisters R1 and R2 should be more than 10kΩ to reduce the power loss. The output voltage can be calculated by the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where VREF is the reference voltage (0.8V typical).

Enable

The DS8570 goes into shutdown mode when the EN pin is in the logic low condition. During this condition, the pass transistor, error amplifier, and band gap are turned off, reducing the supply current to 1uA typical. The DS8570 goes into operation mode when the EN pin is in the logic high condition. If the EN pin is floating, please notice the DS8570 internal initial logic level. For the DS8570, the EN pin function pulls low level internally. So the regulator will be turned off when EN pin is floating.

Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10uF input capacitor or greater located as close as possible to the IC is recommended.

Power Good

The power good function is an open-drain output. Connect 100KΩ pull up resistor to VOUT to obtain an output voltage.

The POK pin will output high immediately after the output voltage arrives 90% of normal output voltage.

Output Capacitor

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The DS8570 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor which value is at least 10μF on the DS8570 output ensures stability. The DS8570 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the DS8570 and returned to a clean analog ground.

Current Limit

The DS8570 contains an independent current limit and the short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimum limiting the output current to 3.1A typical. When the output voltage is less than 0.2V, the short circuit current protection starts the current fold back function and maintains the loading current at maximum 1.8A. The output can be shorted to ground indefinitely without damaging the part.

Thermal Shutdown Protection

Thermal protection limits power dissipation to prevent IC over temperature in the DS8570. When the operation junction temperature exceeds 160°C, the over temperature protection circuit starts the thermal shutdown function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, DSTECH PCB,
The max PD(Max) = (125°C − 25°C) / (70°C/W) = 1.43W for DFN3x3-10L packages.

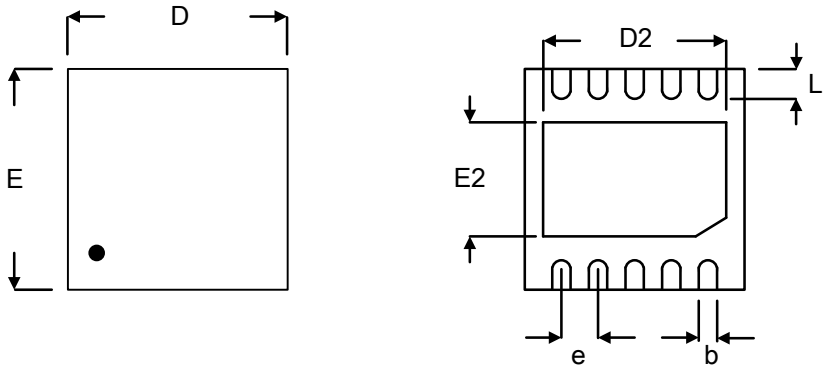
The max PD(Max) = (125°C − 25°C) / (75°C/W) = 1.33W for ESOP-8 packages.

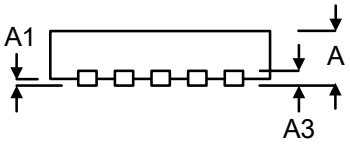
Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:
PD = (VIN – VOUT) × IOUT

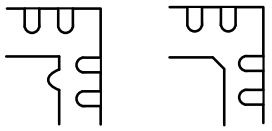
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the Charger, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the DS8570 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information:







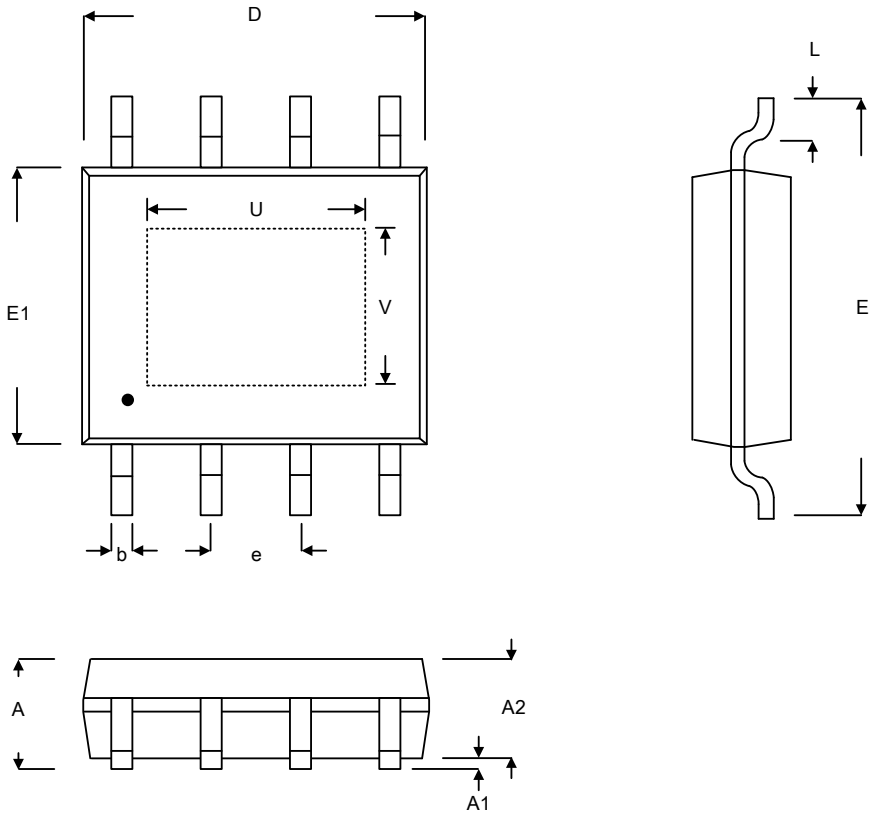
DETAILA

PIN #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.300	0.006	0.012
D	2.900	3.100	0.114	0.122
D2	2.390	2.600	0.094	0.102
E	2.900	3.100	0.114	0.122
E2	1.450	1.800	0.057	0.071
e	0.500		0.020	
L	0.300	0.500	0.012	0.020

DFN3x3-10L



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.800	0.051	0.071
A1	0.000	0.152	0.000	0.006
A2	1.300	1.500	0.051	0.059
b	0.330	0.510	0.013	0.020
D	4.800	5.000	0.189	0.197
e	1.270		0.050	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.200	0.016	0.047
U	3.100		0.122	
V	2.210		0.087	

ESOP-8