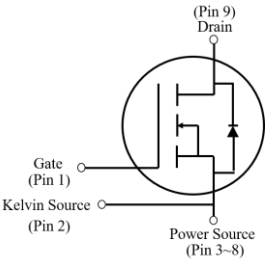
IV1Q06040L1 – 650V 40mΩ SiC MOSFET

Features

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin source pin easing driver circuit design

Outline:



TOLL

Applications

- UPS
- Motor drivers
- EV/HEV drivers
- High voltage DC/DC converters
- Switch mode power supplies

Marking Diagram:

1Q06040L1
YYWWZ
XXXX

1Q06040L1 = Specific Device Code
YY = Year
WW = Work Week
Z = Assembly Location
XXXX = Lot Traceability

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	650	V	V_{GS}=0V, I_D=100μA	
V_{GSmax} (DC)	Maximum DC voltage	-5 to 22	V	Static (DC)	
V_{GSmax} (Spike)	Maximum spike voltage	-10 to 25	V	<1% duty cycle, and pulse width<200ns	
V_{GSon}	Recommended turn-on voltage	20±0.5	V		
V_{GSoff}	Recommended turn-off voltage	-3.5 to -2	V		
I_D	Drain current (continuous)	63.5	A	V_{GS}=20V, T_C=25°C	Fig. 21
		46.4	A	V_{GS}=20V, T_C=100°C	
I_{DM}	Drain current (pulsed)	158.7	A	Pulse width limited by SOA	Fig. 24
P_{TOT}	Total power dissipation	247.9	W	T_C=25°C	Fig. 22
T_{stg}	Storage temperature range	-55 to 175	°C		
T_J	Operating junction temperature	-55 to 175	°C		
T_L	Solder Temperature	260	°C	wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{θ(J-C)}$	Thermal Resistance from Junction to Case	0.605	°C/W	Fig. 23

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		3	100	μA	V_{DS}=650V, V_{GS}=0V	
I_{GSS}	Gate leakage current			±100	nA	V_{DS}=0V, V_{GS}=-5~20V	
V_{TH}	Gate threshold voltage	1.8	3.2	5	V	V_{GS}=V_{DS}, I_D=6.1mA	Fig. 8, 9
			2.2			V_{GS}=V_{DS}, I_D=6.1mA @ T_C=175°C	
R_{ON}	Static drain-source on-resistance		40	55	mΩ	V_{GS}=20V, I_D=20A @T_J=25°C	Fig. 4, 5, 6, 7
			53		mΩ	V_{GS}=20V, I_D=20A @T_J=175°C	
C_{iss}	Input capacitance		2692		pF	V_{DS}=600V, V_{GS}=0V, f=1MHz, V_{AC}=25mV	Fig. 16
C_{oss}	Output capacitance		179		pF		
C_{rss}	Reverse transfer capacitance		10.8		pF		
E_{oss}	C_{oss} stored energy		35.6		μJ		Fig. 17
Q_g	Total gate charge		110.8		nC	V_{DS}=400V, I_D=20A, V_{GS}=-5 to 20V	Fig. 18
Q_{gs}	Gate-source charge		26.8		nC		
Q_{gd}	Gate-drain charge		35.7		nC		
R_g	Gate input resistance		2		Ω	f=1MHz	
E_{ON}	Turn-on switching energy		215.9		μJ	V_{DS}=400V, I_D=30A, V_{GS}=-3.5 to 20V, $R_{G(ext)}$=4.7Ω, L=250μH	Fig. 19, 20
E_{OFF}	Turn-off switching energy		73.27		μJ		
$t_{d(on)}$	Turn-on delay time		6.7		ns		
t_r	Rise time		20.5				
$t_{d(off)}$	Turn-off delay time		31.2				
t_f	Fall time		13.8				

Reverse Diode Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		4.0		V	I_{SD}=20A, V_{GS}=0V	Fig. 10, 11, 12
			3.6		V	I_{SD}=20A, V_{GS}=0V, T_J=175°C	
t_{rr}	Reverse recovery time		34.4		ns	V_{GS}=-3.5V/+20V, I_{SD}=30A, V_R=400V, $R_{G(ext)}$=15Ω, di/dt=3000A/μs, L=250μH	
Q_{rr}	Reverse recovery charge		289.8		nC		
I_{RRM}	Peak reverse recovery current		20		A		
E_{rr}	Reverse recovery energy		37.3		nJ		

Typical Performance (curves)

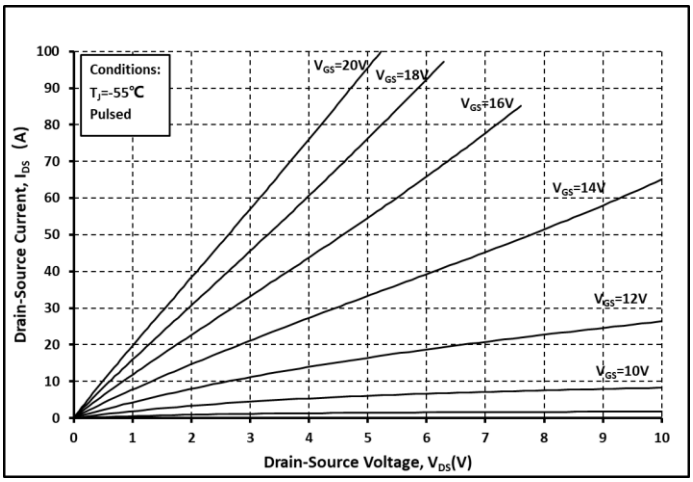


Fig. 1 Output Curve @ T_J=-55°C

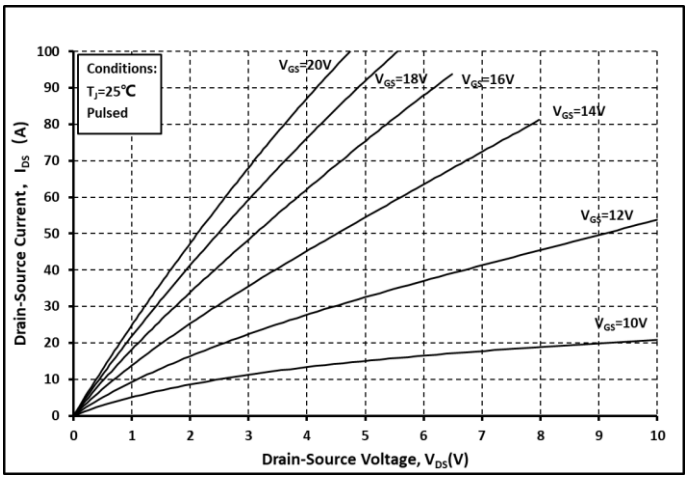


Fig. 2 Output Curve @ T_J=25°C

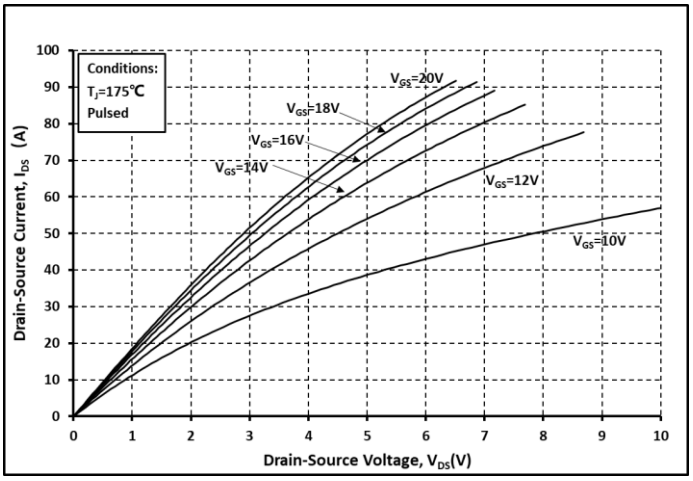


Fig. 3 Output Curve @ T_J=175°C

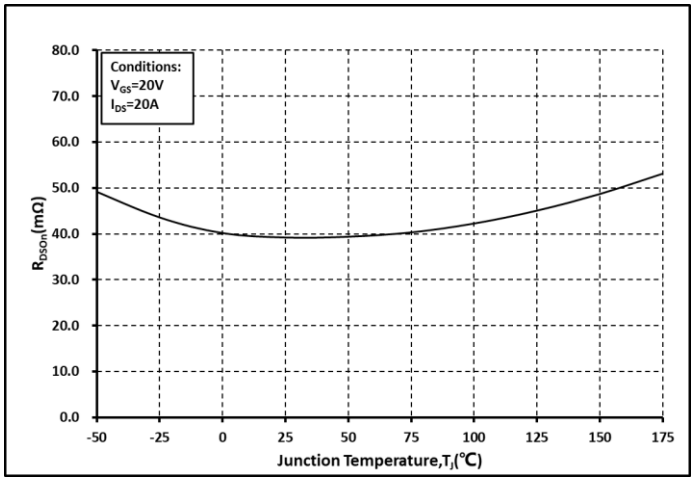


Fig. 4 Ron vs. Temperature

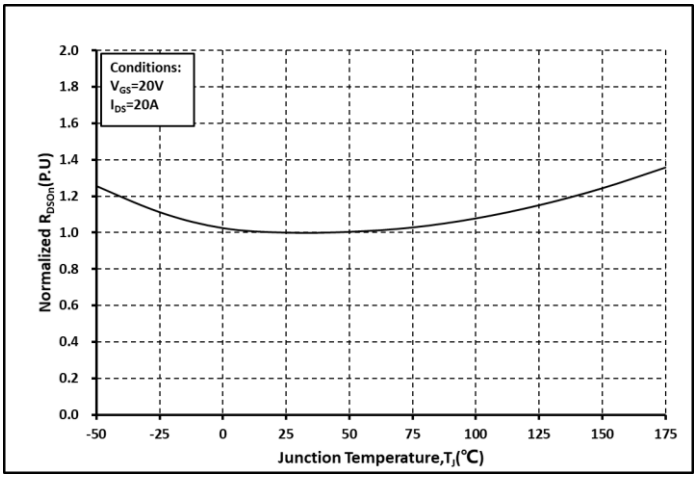


Fig. 5 Normalized Ron vs. Temperature

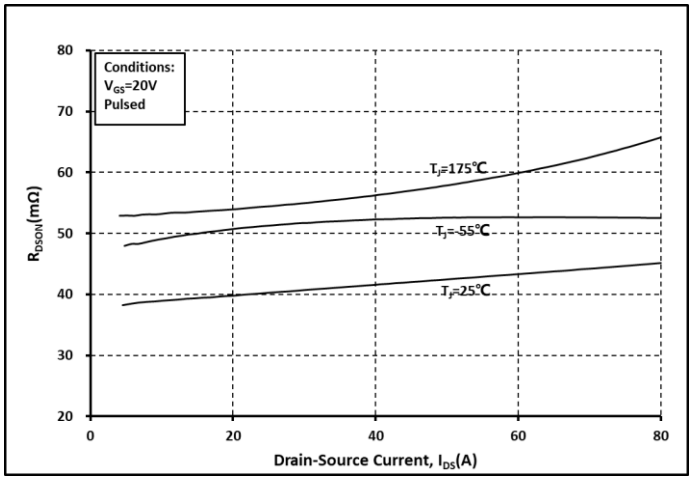


Fig. 6 Ron vs. I_{DS} @ Various Temperature

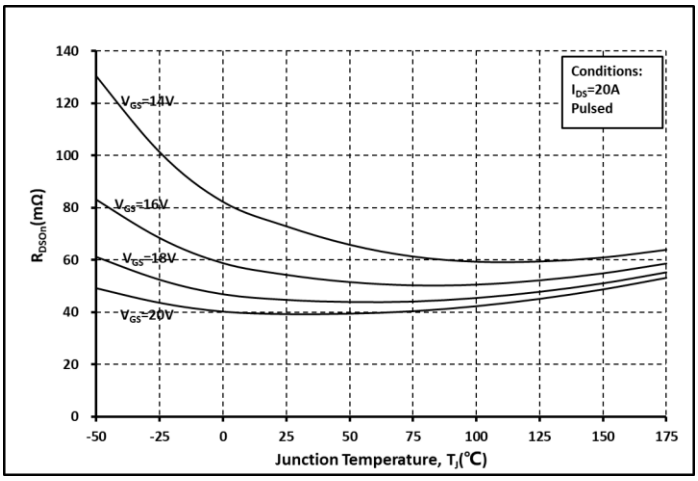


Fig. 7 Ron vs. Temperature @ Various V_{GS}

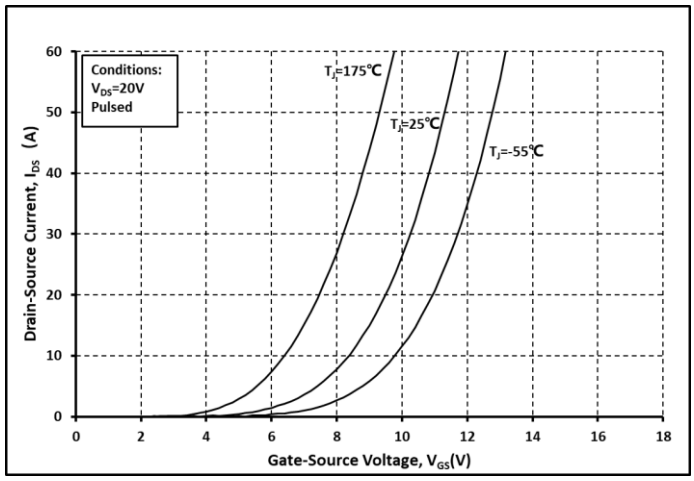


Fig. 8 Transfer Curves @ Various Temperature

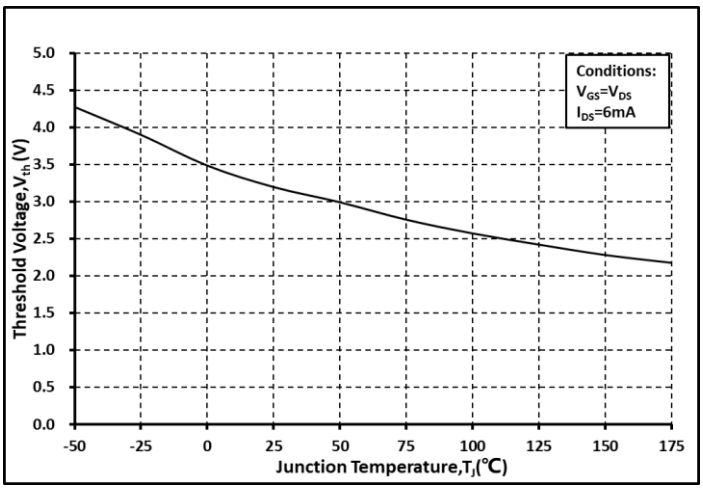


Fig. 9 Threshold Voltage vs. Temperature

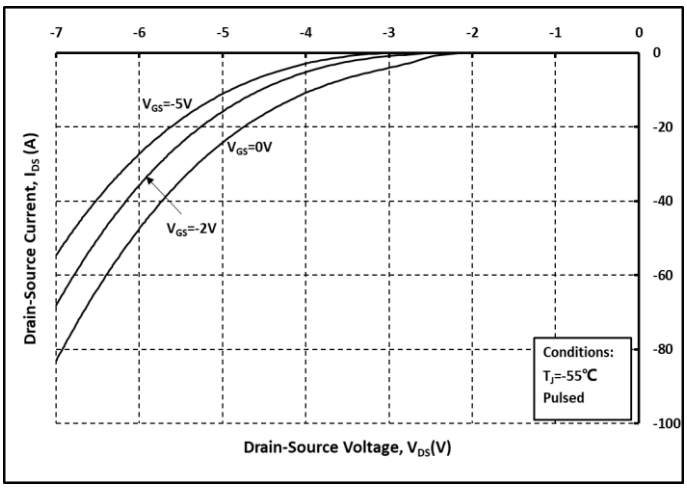


Fig. 10 Body Diode Curves @ T_J=-55°C

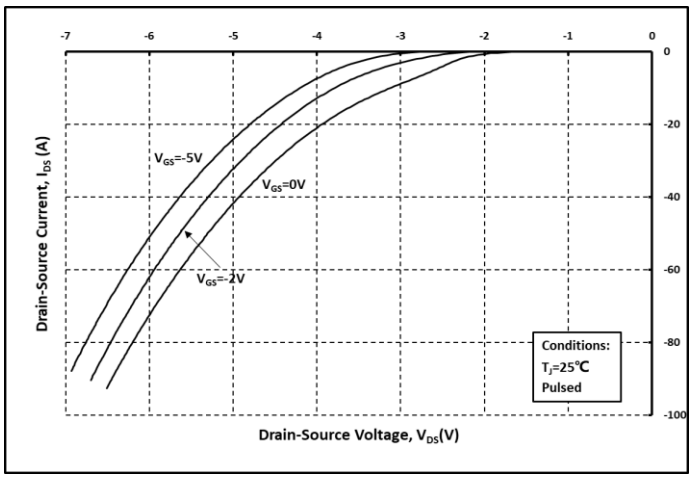


Fig. 11 Body Diode Curves @ T_J=25°C

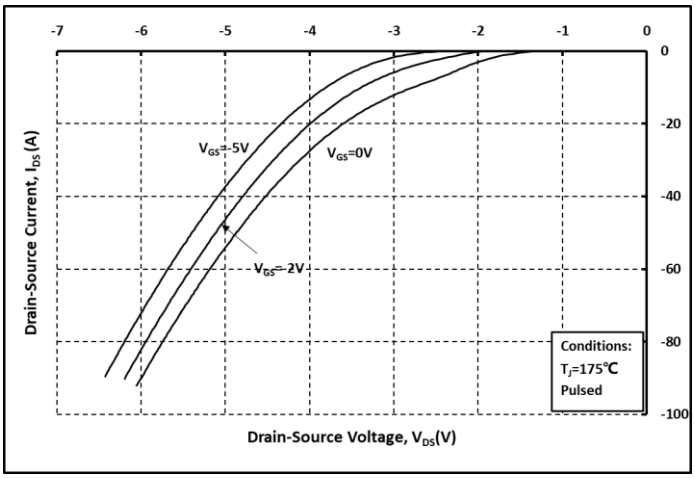


Fig. 12 Body Diode Curves @ T_J=175°C

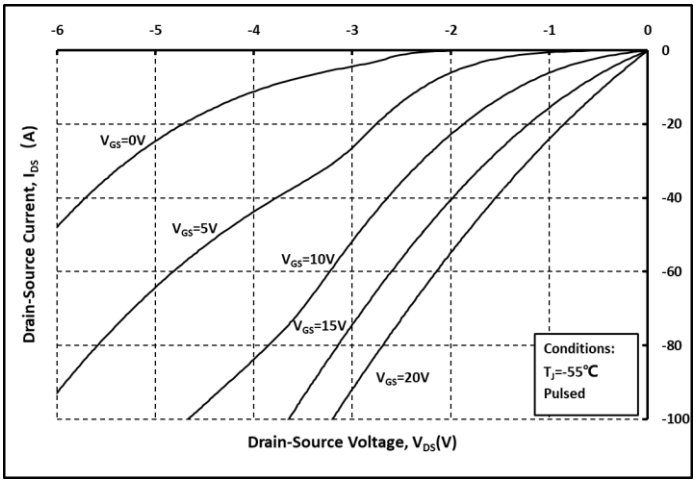


Fig. 13 3rd Quadrant Curves @ T_J=-55℃

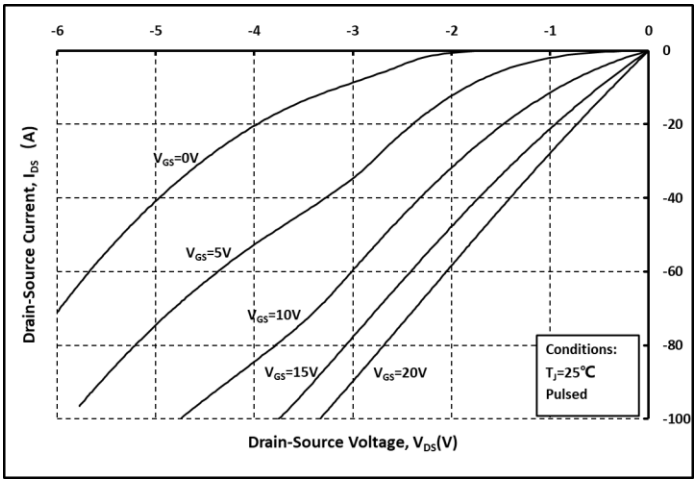


Fig. 14 3rd Quadrant Curves @ T_J=25℃

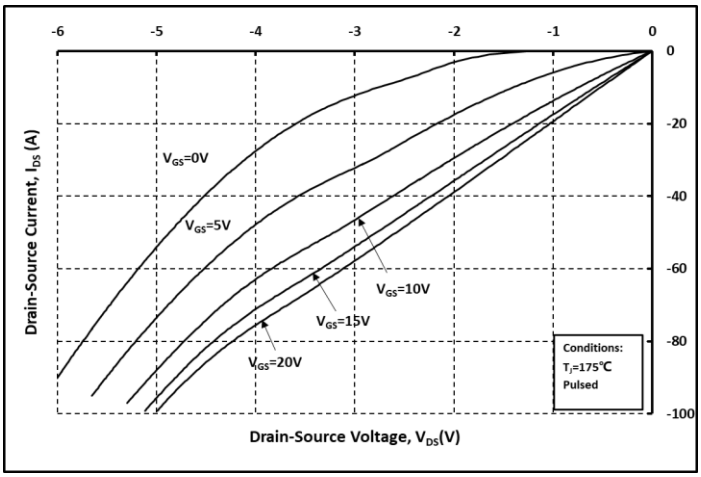


Fig. 15 3rd Quadrant Curves @ T_J=175℃

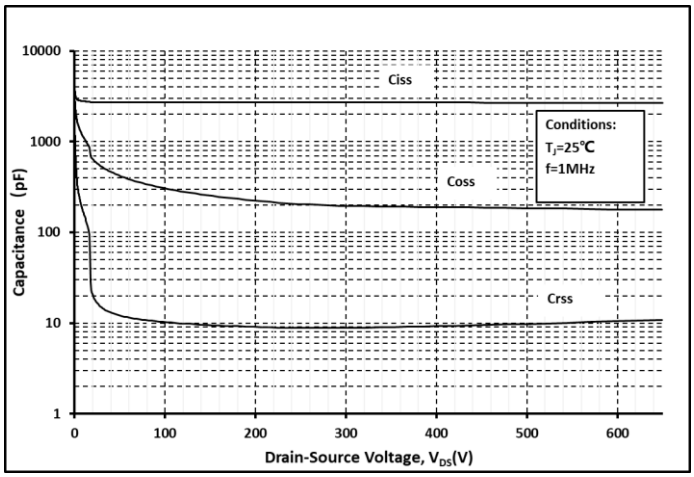


Fig. 16 Capacitance vs. V_{DS}

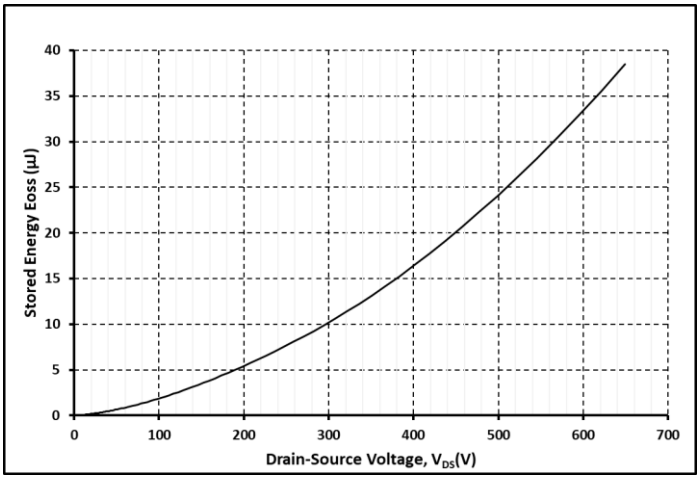


Fig. 17 Output Capacitor Stored Energy

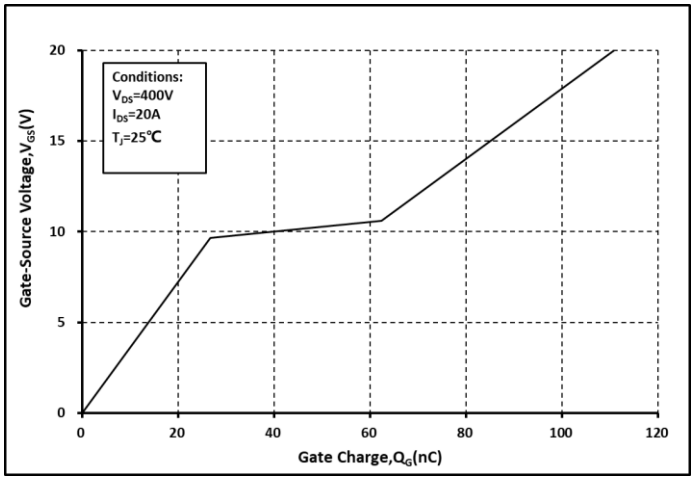


Fig. 18 Gate Charge Characteristics

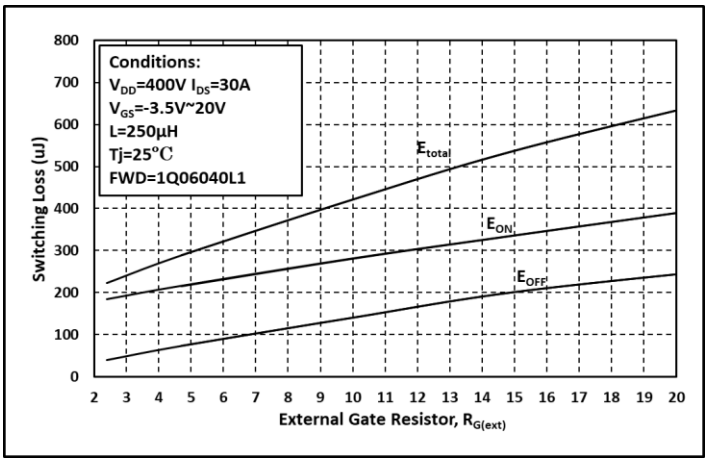


Fig. 19 Switching Energy vs. $R_{G(ext)}$

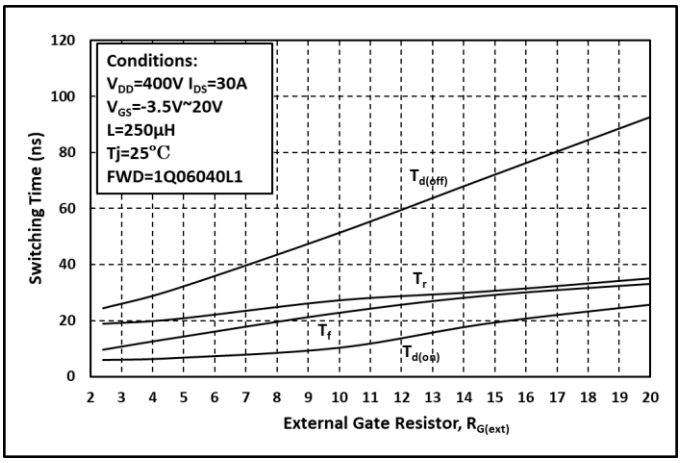


Fig. 20 Switching Times vs. $R_{G(ext)}$

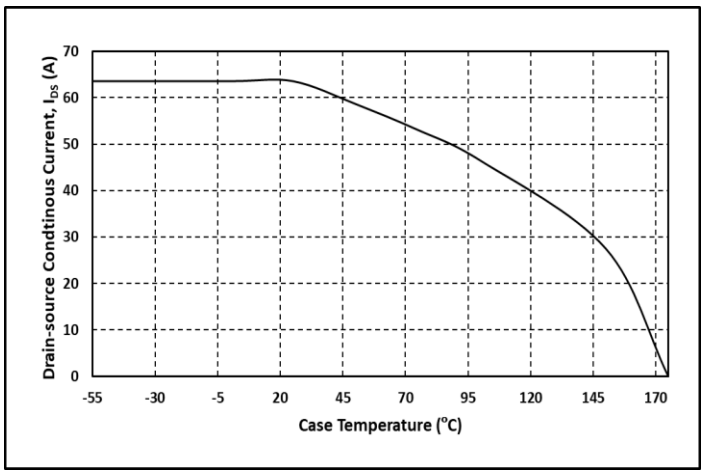


Fig. 21 Continuous Drain Current vs. Case Temperature

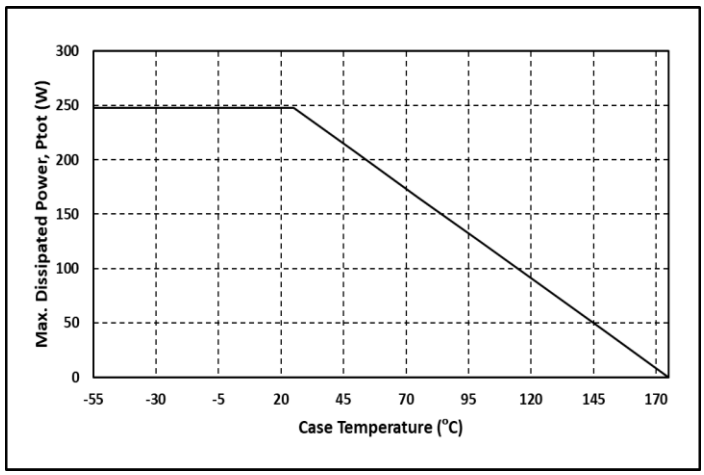


Fig. 22 Max. Power Dissipation Derating vs. Case Temperature

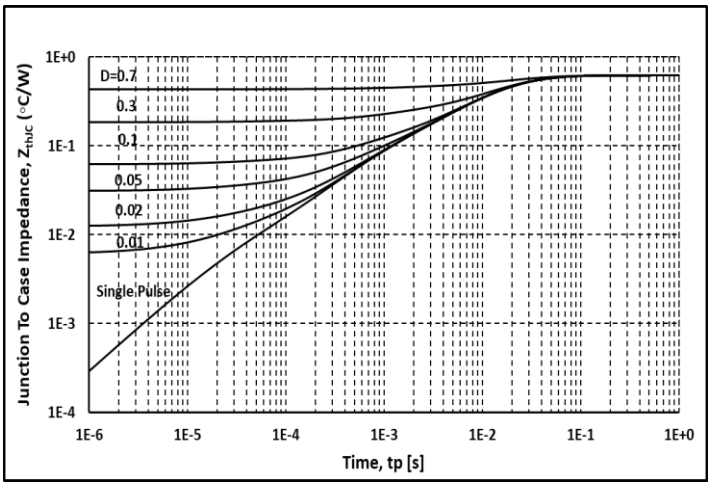


Fig. 23 Thermal Impedance

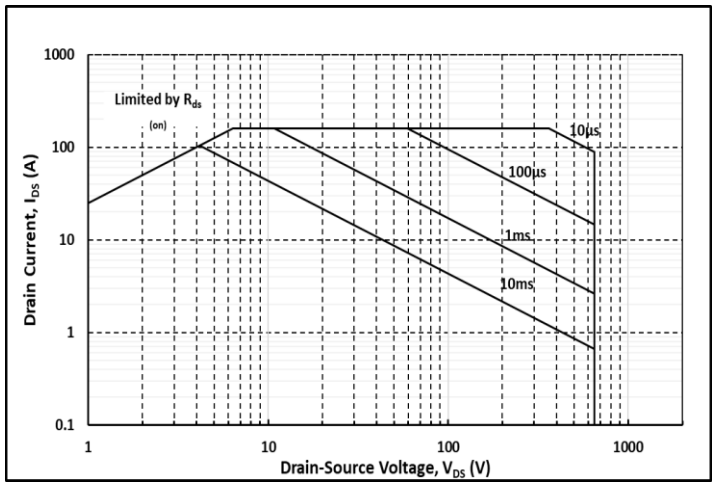
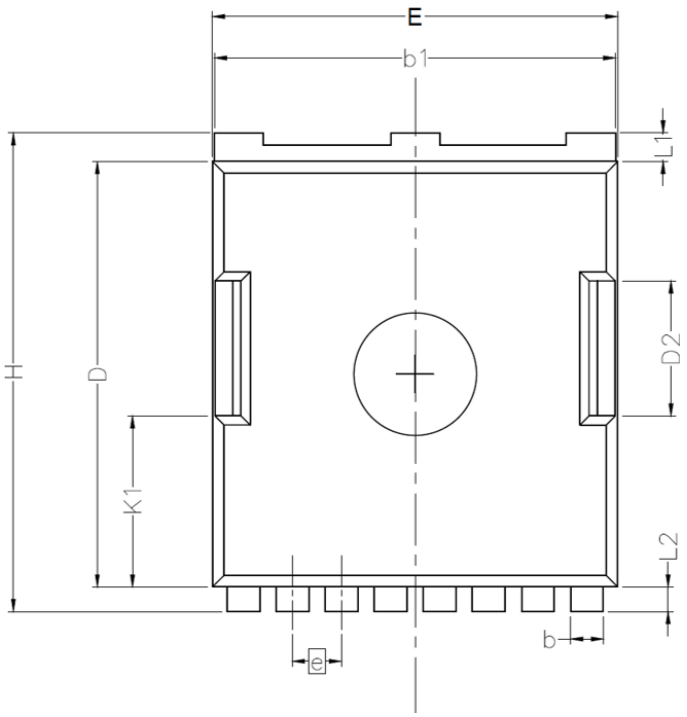
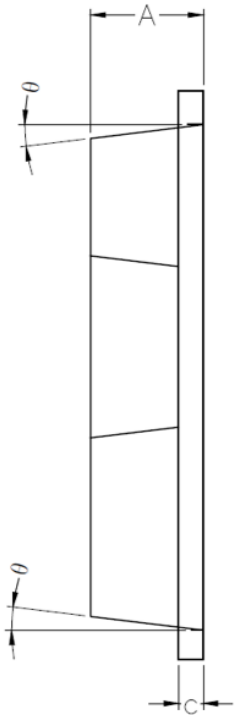


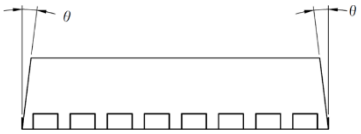
Fig. 24 Safe Operating Area

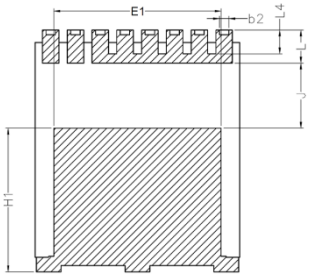
Package Dimensions



Dimensions In Millimeters		
SYMBOL	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.7	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°







Note:

1. Package Reference: JEDEC TOLL, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash
5. Subject to Change Without Notice

Notes

For further information please contact IVCT's office.

The Information in this document is subject to change without notice.

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