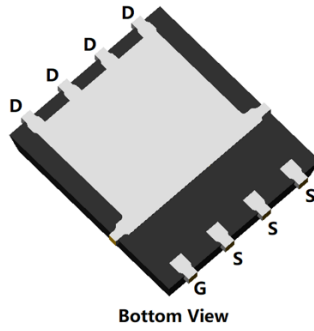
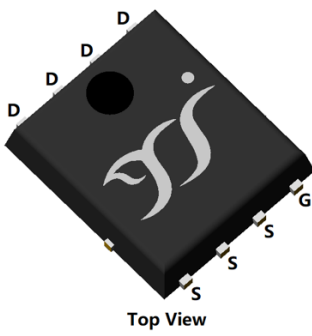
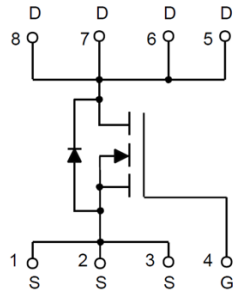


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



Product Summary

- V_{DS} 60V
- I_D 95A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <math>< 2.9\text{ mohm}</math>
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current (Silicon limited)	I_D	155	A
Drain Current ^A	I_D	$T_A=25^\circ\text{C}$	20
		$T_A=100^\circ\text{C}$	12
		$T_C=25^\circ\text{C}$	95
		$T_C=100^\circ\text{C}$	60
Pulsed Drain Current ^B	I_{DM}	390	A
Avalanche energy ^C	E_{AS}	800	mJ
Total Power Dissipation ^D	P_D	120	W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.04	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient ^E	$R_{\theta JA}$	20	
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG95G06BX	F1	YJG95G06BX	5000	10000	100000	13" reel



YJG95G06BX

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2.0	2.8	4.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		2.25	2.9	mΩ
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				95	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=100KHZ		5950		pF
Output Capacitance	C _{oss}			1250		
Reverse Transfer Capacitance	C _{rss}			85		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A		93		nC
Gate-Source Charge	Q _{gs}			17		
Gate-Drain Charge	Q _{gd}			14		
Reverse Recovery Charge	Q _{rr}	I _F =25A, di/dt=100A/us		73		
Reverse Recovery Time	t _{rr}			68		
Turn-on Delay Time	t _{d(on)}	V _{GS} =10V, V _{DD} =30V, I _D =25A R _{GEN} =2Ω		22.5		ns
Turn-on Rise Time	t _r			6.7		
Turn-off Delay Time	t _{d(off)}			80.3		
Turn-off fall Time	t _f			26.9		

Note:

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- T_J=25°C, V_{DD}=55V, V_G=10V, R_G=25Ω, L=4mH, I_{AS}=20A.
- P_D is based on max. junction temperature, using junction-case thermal resistance.
- The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 °C.



■ Typical Performance Characteristics

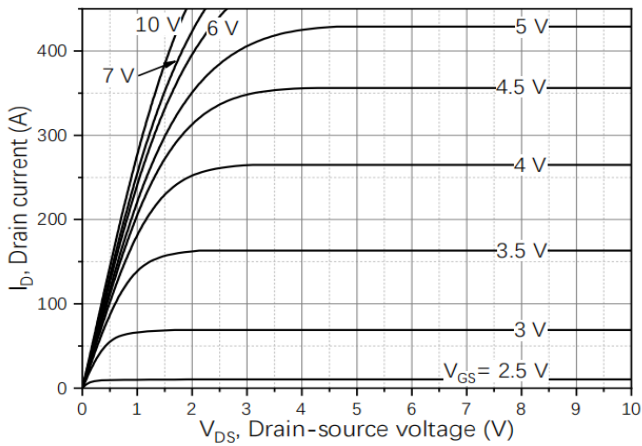


Figure1. Output Characteristics

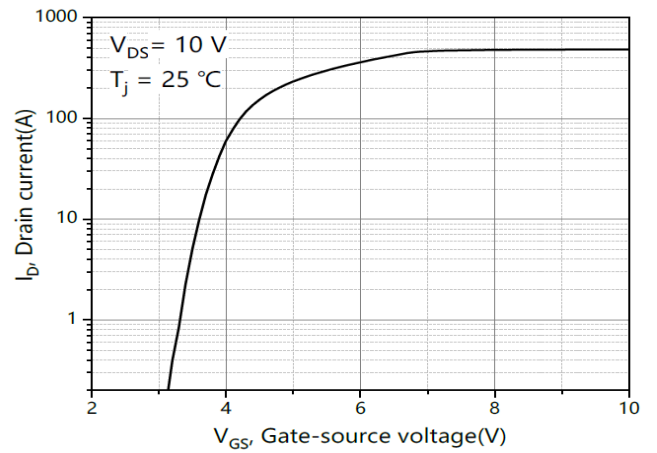


Figure2. Transfer Characteristics

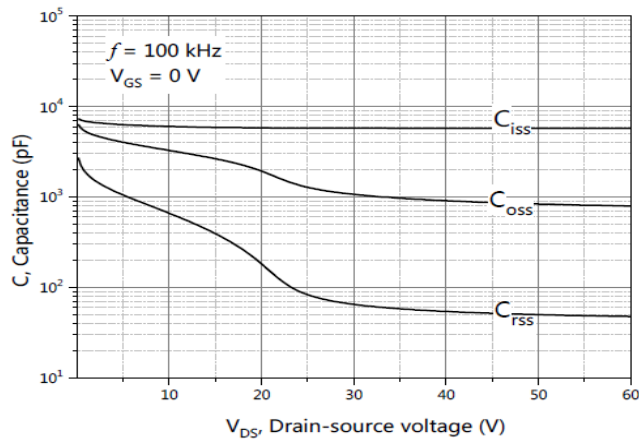


Figure3. Capacitance Characteristics

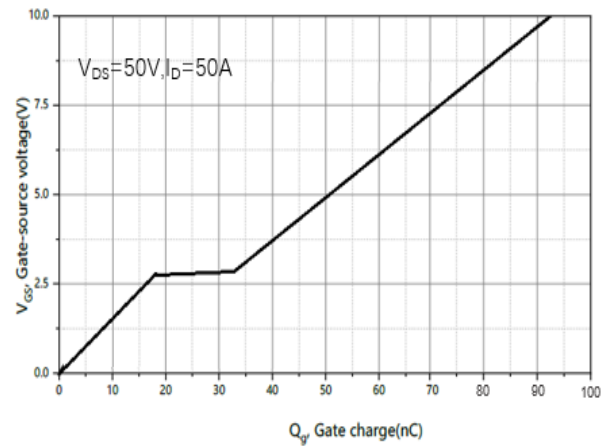


Figure4. Gate Charge

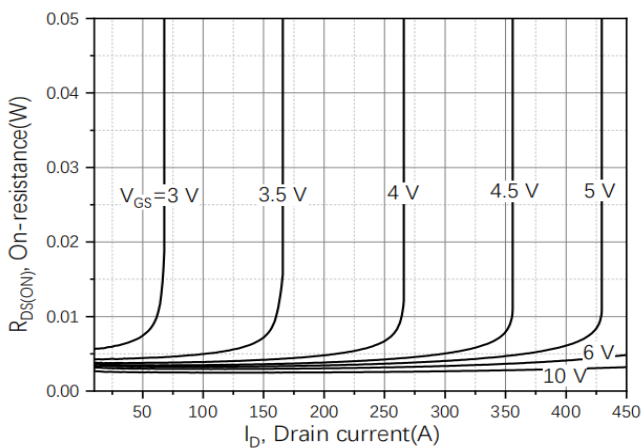


Figure5. Drain-Source on Resistance

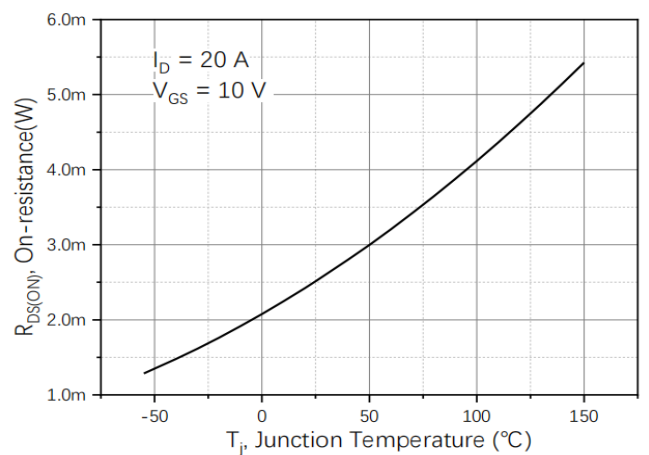


Figure6. Drain-Source on Resistance



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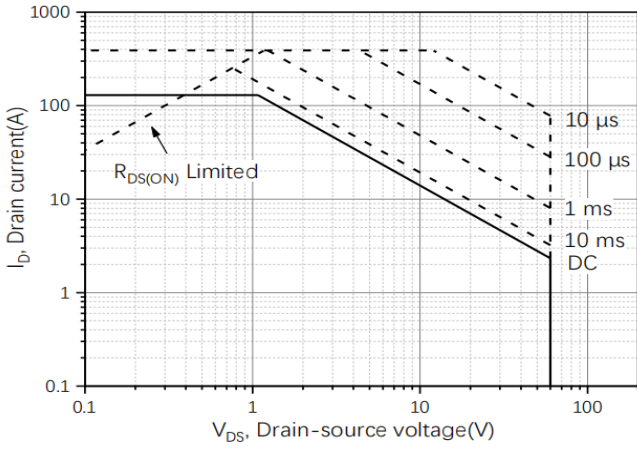


Figure 7. Safe Operation Area

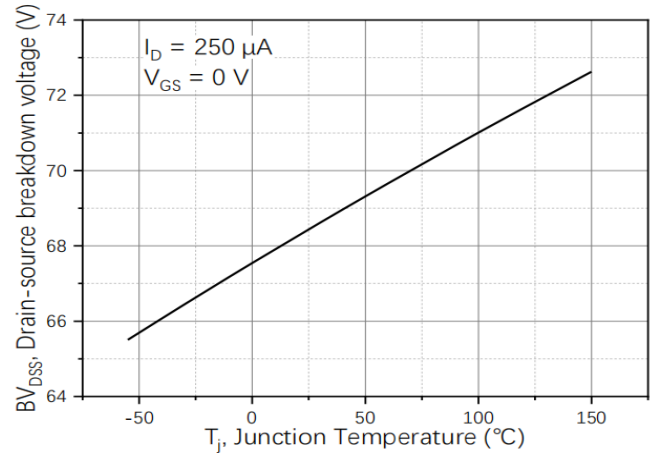


Figure 8. Drain-source breakdown voltage

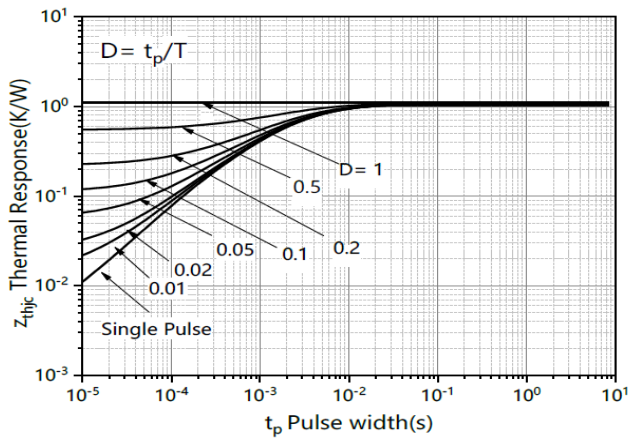


Figure 9. Transient thermal impedance

■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

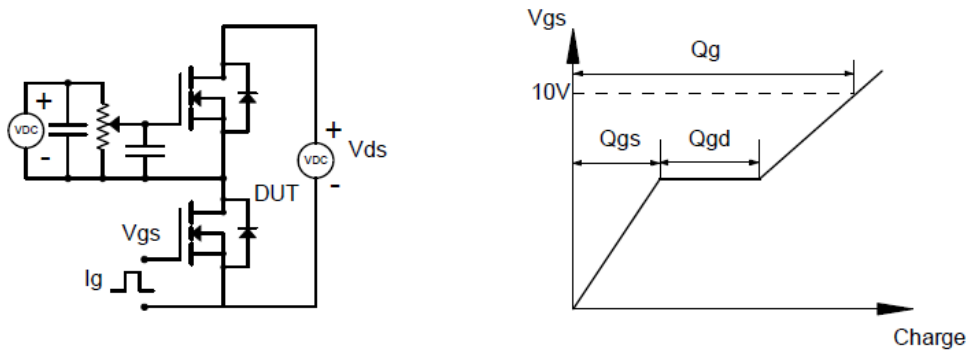


Figure B: Resistive Switching Test Circuit & Waveforms

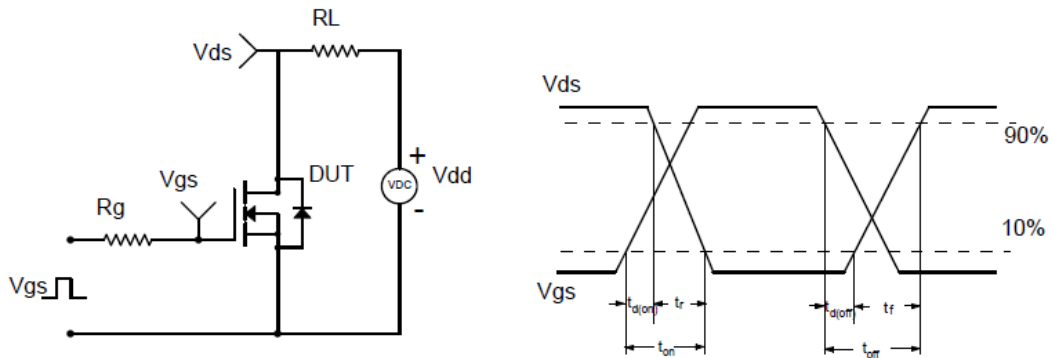


Figure C: Unclamped Inductive Switching (UIS) Test

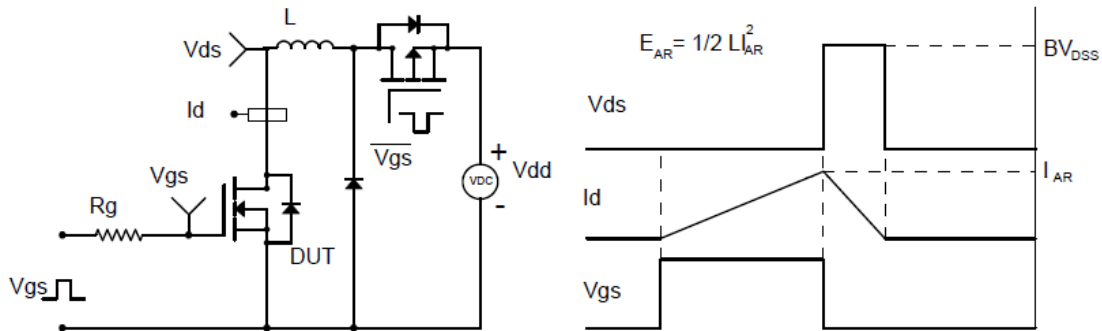
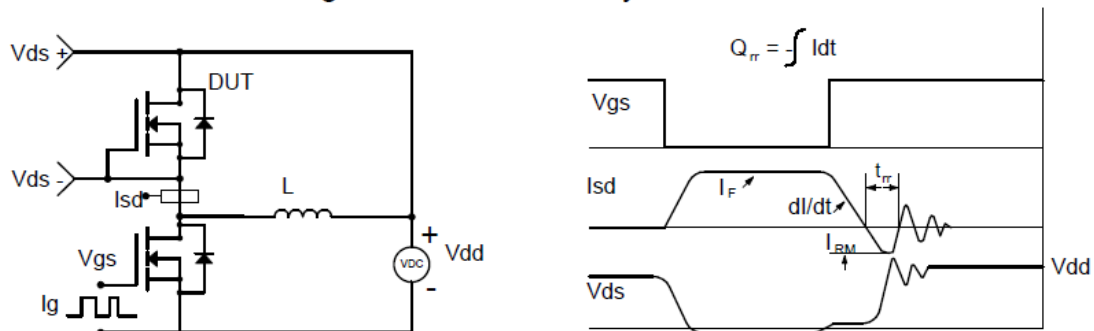


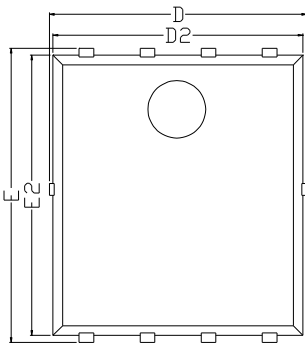
Figure D: Diode Recovery Test Circuit & Waveforms



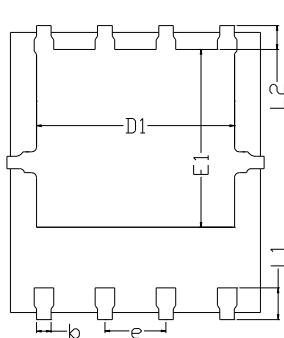


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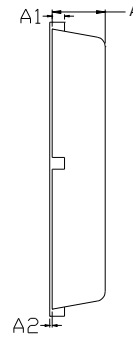
■ PDFN5060-8L-E-1.0MM Package Information



Top View
正面视图

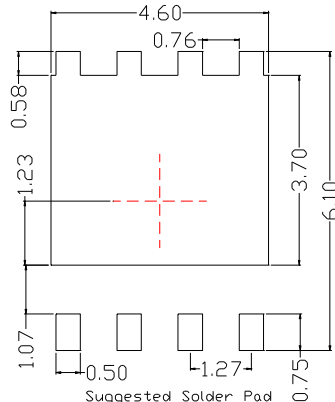


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.85	5.05	5.25
E	5.80	6.00	6.20
A	0.90	1.00	1.10
A1	0.254 BSC		
A2			0.10
D1	4.00	4.20	4.40
E1	3.35	3.55	3.75
D2	4.70	4.90	5.10
E2	5.55	5.75	5.95
L1	0.55	0.65	0.75
L2	0.575 BSC		
b	0.20	0.30	0.40
e	1.27 BSC		



Suggested Solder Pad
Layout
Top View

Note:

1. Controlling dimension in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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