TinyLogic HST 2-Input AND Gate

Description

The NC7ST08M5X is a single 2−Input high performance CMOS AND Gate, with TTL−compatible inputs. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. High gain circuitry offers high noise immunity and reduced sensitivity to input edge rate. The TTL−compatible inputs facilitate TTL to NMOS / CMOS interfacing. Device performance is similar to MM74HCT but with 1/2 the output current drive of HC / HCT.

Features

- Ultra Small MicroPak™ Leadless Package
- High Speed: t_{PD} = 6 ns (Typ), V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C
- Low Quiescent Power: I_{CC} < 1 μA Typ, V_{CC} = 5.5 V
- Balanced Output Drive: 2 mA I_{OL}, −2 mA I_{OH}
- TTL−compatible Inputs

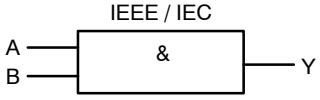
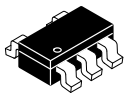
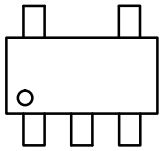
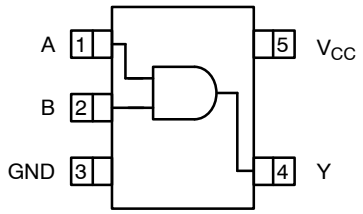


Figure 1. Logic Symbol





Pin Configurations



PIN DESCRIPTION

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−20	mA
		V_{IN} > V_{CC}	−	+20	
V_{IN}	DC Input Voltage		−0.5	V_{CC} + 0.5	V
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−20	mA
		V_{OUT} > V_{CC}	−	+20	
V_{OUT}	Output Voltage		−0.5	V_{CC} + 0.5	V
I_{OUT}	DC Output Source or Sink Current		−	±12.5	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin		−	±25	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature		−	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		−	+260	°C
P_D	Power Dissipation in Still Air		−	390	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IN}	Input Voltage		0	V_{CC}	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		–40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 5.0 V	0	10	ns/V
θ_{JA}	Thermal Resistance		–	320	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

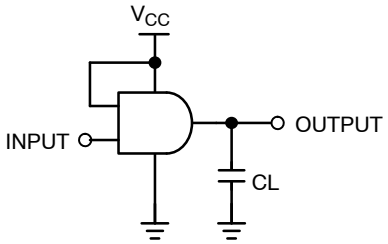
Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	4.5 – 5.5		2.0	–	–	2.0	–	V
V_{IL}	LOW Level Input Voltage	4.5 – 5.5		–	–	0.8	–	0.8	V
V_{OH}	HIGH Level Output Voltage	4.5 4.5	I_{OH} = –20 μA I_{OH} = –2 mA V_{IN} = V_{IH}	4.4 4.18	4.5 4.35	–	4.4 4.13	–	V
V_{OL}	LOW Level Output Voltage	4.5 4.5	I_{OL} = 20 μA I_{OL} = 2 mA V_{IN} = V_{IL}	–	0 0.10	0.1 0.26	–	0.1 0.33	V
I_{IN}	Input Leakage Current	5.5	0 ≤ V_{IN} ≤ 5.5 V	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND	–	–	1.0	–	10.0	μA
I_{CCT}	I_{CC} per Input	5.5	One Input V_{IN} = 0.5 V or 2.4 V, Other Input V_{CC} or GND	–	–	2.0	–	2.9	mA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 4, 6)	5.0	C_L = 15 pF	–	4	12	–	–	ns
				–	6	17	–	–	
		4.5	C_L = 50 pF	–	6	16	–	20	
				–	12	27	–	31	
		5.5		–	5	14	–	18	
				–	11	26	–	30	
t_{TLH}, t_{THL}	Output Transition Time (Figure 4, 6)	5.0	C_L = 15 pF	–	4	10	–	–	ns
		4.5	C_L = 50 pF	–	11	25	–	31	
		5.5		–	10	21	–	26	
C_{IN}	Input Capacitance	Open		–	–	10	–	–	pF
C_{PD}	Power Dissipation Capacitance (Figure 5)	5.0	(Note 2)	–	6	–	–	–	pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current. Current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 5) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = (C_{PD}) (V_{CC}) (f_{IN}) + (I_{CC}static).

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_W = 500 ns

Figure . AC Test Circuit

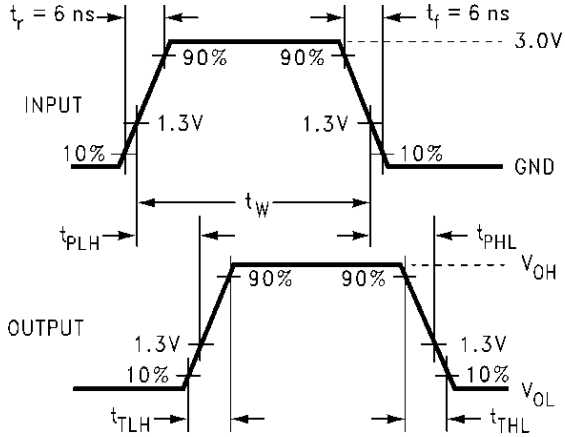
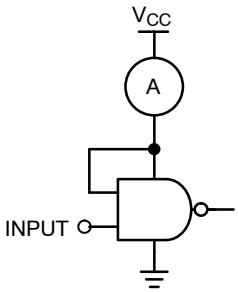
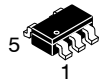


Figure . AC Waveforms

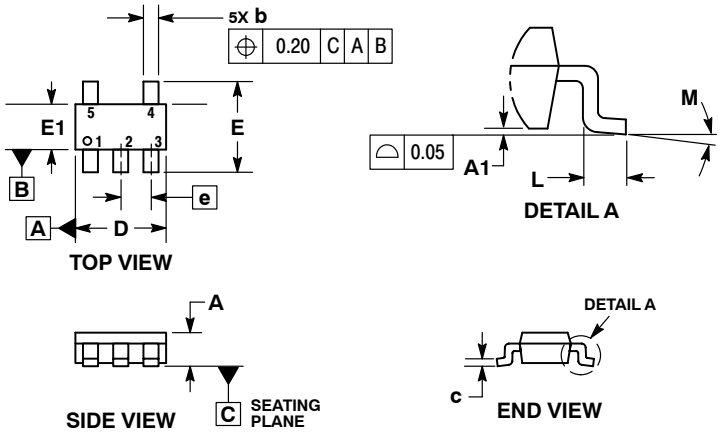


Input = AC Waveform;
PRR = Variable; Duty Cycle = 50%.

Figure . I_{CCD} Test Circuit



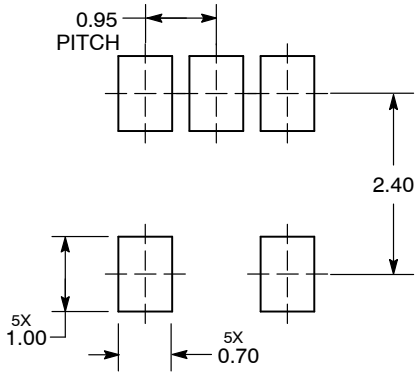
SCALE :



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS