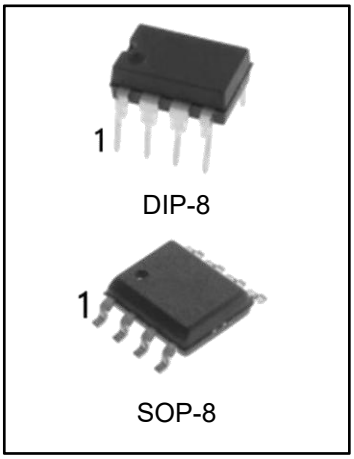
Current Mode PWM Controller for Forward and Flyback Application

Features

- Peak Current Mode Control
- Adj Switching Frequency up to 500 kHz
- Jittering Frequency
- Latched Primary OCP with 10 ms Delay
- Over load Protection(OLP) with 55ms Delay
- Delayed Operation Upon Start−up via an Internal Fixed Timer
- Adj Soft−start Timer
- VDD Range from 10V to 26V with Auto−recovery UVLO
- Auto−recovery Brown−Out Detection
- Internal 160 ns Leading Edge Blanking
- Adjustable Internal Ramp Compensation
- +500 mA / –800 mA Source / Sink Capability
- Ready for Updated No Load Regulation Specifications
- Maximum 50% Duty Cycle: A Version
- SOP−8 and DIP−8 Packages



Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
NCP1252N	DIP-8	NCP1252	TUBE	2000pcs/Box
NCP1252M/TR	SOP-8	NCP1252	REEL	2500pcs/Reel

Description

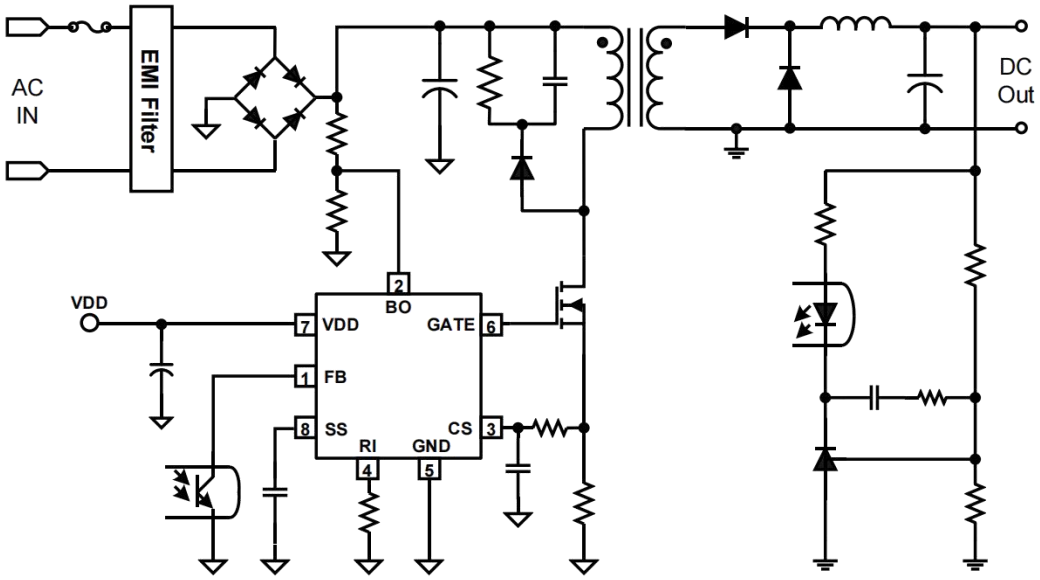
The NCP1252 controller offers everything needed to build cost−effective and reliable AC/DC switching supplies dedicated to ATX power supplies. Thanks to the use of an internally fixed timer, NCP1252 detects an output overload without relying on the auxiliary VDD. A Brown−Out input offers protection against low input voltages and improves the converter safety. Finally a SOP8 package saves PCB space and represents a solution of choice in cost sensitive project.

NCP1252 is offered in SOP-8/DIP-8 package.

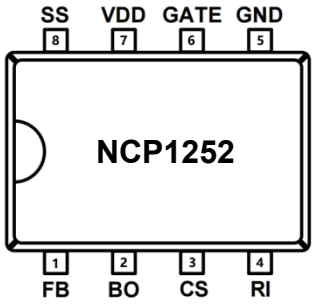
Applications

- Power Supplies for PC Silver Boxes, gameAdapter
- Flyback and Forward Converter

Block Diagram



Pin Configuration

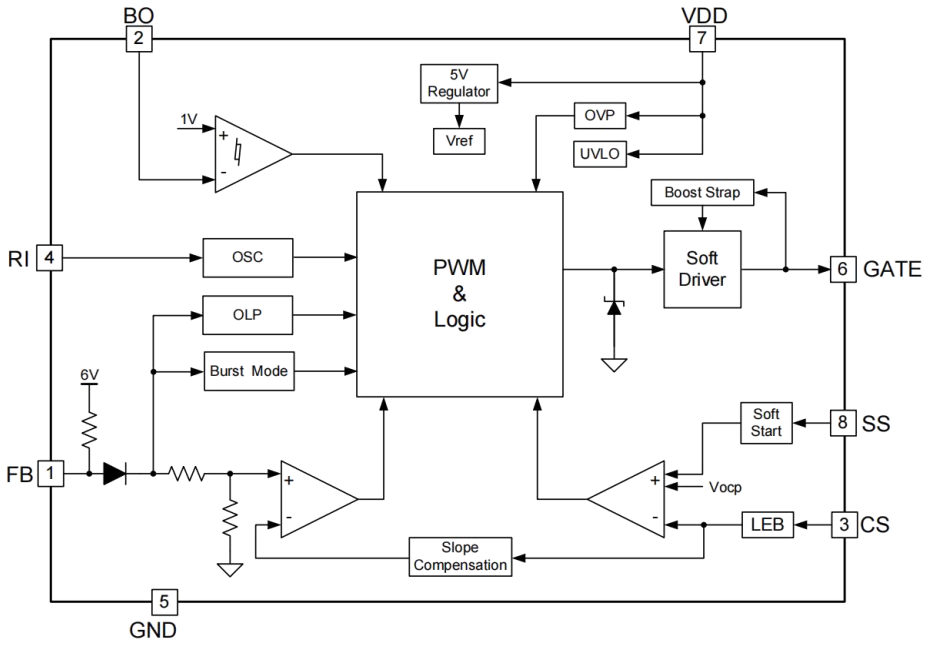


DIP-8/SOP-8

Pin Descriptions

Name	Pin	Description
FB	1	Feedback input pin
BO	2	This pin monitors the input voltage image to offer a Brown−out protection.
CS	3	Current sense input, connected through a resistor to GND to set the primary side peak current
RI	4	This pin is to program the switching frequency. By connecting a resistor to ground to set the switching frequency
GND	5	Ground
GATE	6	Totem-pole gate driver output for power MOSFET
VDD	7	IC DC power supply input
SS	8	Soft start pin,A capacitor connected to ground selects the soft−start duration. The soft start is grounded during the delay timer

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		30	V
I_{DD}	VDD DC Clamp Current		10	mA
V_{FB}	FB Input Voltage	-0.3V	5	V
V_{BO}	BO Input Voltage	-0.3V	5	V
V_{CS}	CS Input Voltage	-0.3V	5	V
V_{RI}	RI Input Voltage	-0.3V	5	V
V_{SS}	SS Input Voltage	-0.3V	5	V
R_{JA}	SOP-8 Thermal Resistance (Junction-to-Air)		150	℃/W
	DIP-8 Thermal Resistance (Junction-to-Air)		75	℃/W
T_J	Operating Junction Temperature	-20	150	℃
T_{STG}	Storage Temperature Range	-55	160	℃
T_L	Lead Temperature (Wave Soldering or IR,10Seconds)		260	℃
ESD	Human Body Model,JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These arestress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periodmay affect device’s reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	10	26	V
T_A	Operating Ambient Temperature	-25	125	℃

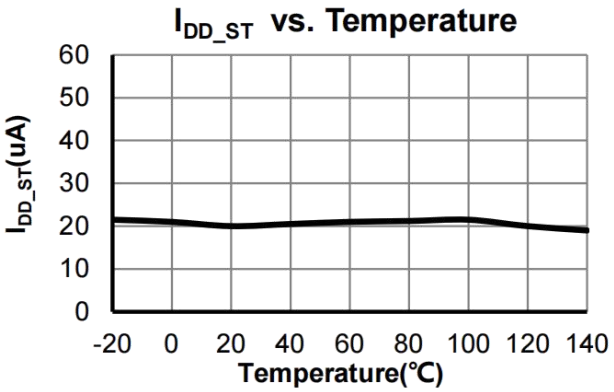
Electrical Characteristics(T_A = 25℃, V_{DD}=15V, RI=43KΩ, unless otherwise noted)

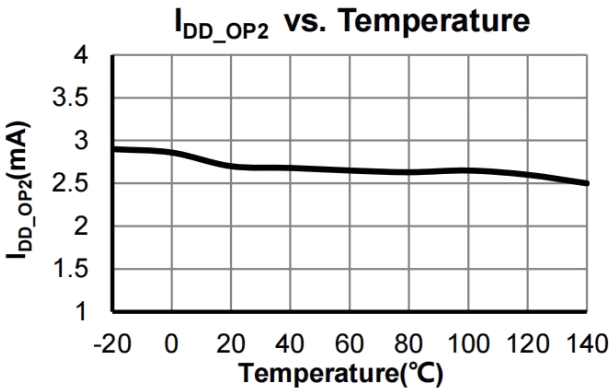
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)						
I_{DD_ST}	Startup Current	VDD=V_{DD_ON}-0.01V		20	100	uA
I_{DD_OP1}	Operation Current 1	F_{OSC}=100KHz	0.5	1.4	2.2	mA
I_{DD_OP2}	Operation Current 2	F_{OSC}=100KHz,C_L=1nF	2.0	2.7	3.5	mA
V_{DD_ON}	Threshold Voltage to Startup	VDD Rising	11.2	11.7	12.2	V
V_{DD_OFF}	Threshold Voltage to Stop Switching in Normal Mode	VDD Falling	8.3	9.0	9.7	V
V_{DD_OVP}	Over voltage protection voltage		26.5	27.5	28.5	V
T_{D_OVP}	OVP Debounce Time			6		cycle
V_{DD_Clamp}		IDD=10mA		30.0		V
Feedback Input Section(FB Pin)						
V_{FB_Open}	FB Open Loop Voltage			6.0		V
A_V	Internal ΔVFB/ ΔVCS			3		V/V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND	1.5			mA
$V_{Ref\_Burst\_L}$	The threshold enter Burst mode			0.3		V
$V_{Ref\_Burst\_H}$	The threshold exit Burst mode			0.33		V
V_{TH_PL}	Power limiting FB Threshold Voltage			4.6		V
T_{D_PL}	Power limiting Debounce Time			55		ms
$R_{pull-up}$	Internal pull-up resistor			3.5		KΩ
V_f	Internal Diode forward voltage			0.75		V
Z_{FB_IN}	Input Impedance			40		KΩ
Current Sense Input(CS Pin)						
V_{TH_OC}	Current Limiting Threshold Voltage		0.92	1	1.08	V
T_{LEB}	Leading edge blanking time			160		ns
T_{D_OC}	Over Current Detection and Control Delay			70	150	ns
I_{Bias}	Input Bias Current			0.02		uA
V_{Ramp}	Internal Ramp Compensation Voltage level		3.15	3.5	3.85	V
R_{Ramp}	Internal Ramp Compensation resistance to CS pin			26.5		KΩ

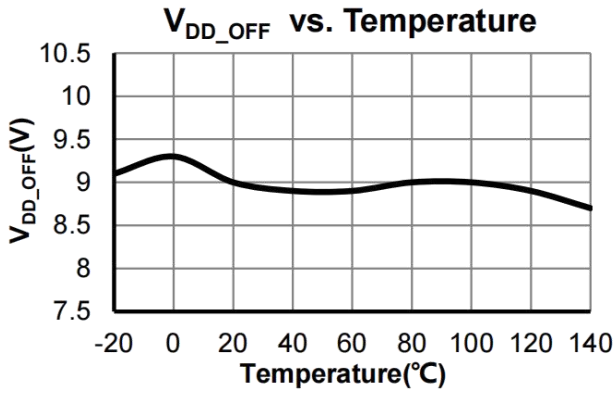
Electrical Characteristics(T_A = 25℃, V_{DD}=15V, RI=43KΩ, unless otherwise noted)

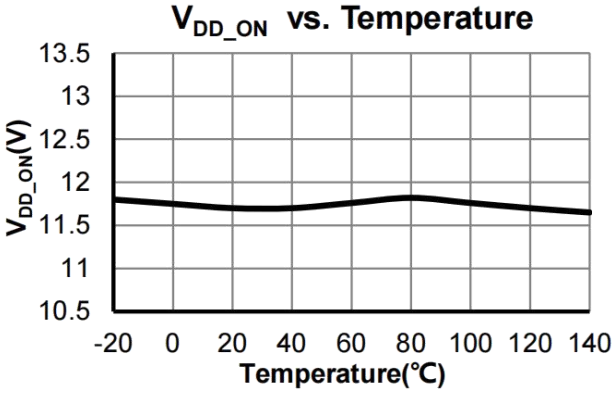
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator						
F_{OSC}	Normal Oscillation Frequency		92	100	108	KHz
F_{OSC}	Normal Oscillation Frequency	RI=8.5KΩ	425	500	550	KHz
F_{JR}	Frequency jitter range			+/-5		%
F_{Jitter}	jitter frequency			300		Hz
F_{MAX}	Max Oscillation Frequency		500			KHz
D_{MAX}	A version Max Duty cycle		45.6	48	49.6	%
	B version Max Duty cycle		76	80	84	%
	C version Max Duty cycle		61	65	69	%
GATE Driver						
R_{SRC}	Gate Source resistance			20	30	Ω
R_{SINK}	Gate Sink resistance			10	19	Ω
V_{Gate_Clamp}	Gate clamp voltage	V_{DD}=25V, C_L=1000pF		15	18	V
T_R	Gate rising time	C_L=1000pF		45		nS
T_F	Gate falling time	C_L=1000pF		30		nS
V_{H_Drop}	High-state voltage drop	V_{DD}=V_{DD_OFF}+0.1V C_L=1000pF		50	500	mV
Soft Start(SS Pin)						
I_{SS}	Soft start charge current	Short SS pin to GND	8.8	10	11	uA
V_{SS}	Soft start completion voltage threshold		3.5	4.0	4.5	V
T_{SS_Delay}	Internal delay before starting the Soft start when V_{DD_ON} is reached		100	120	155	ms
Protection						
V_{CS_Fault}	Current sense fault voltage level triggering the timer		0.9	1.0	1.1	V
T_{Fault}	Timer delay before latching a fault (overload or short circuit)	CS Pin>V_{CS_Fault}	10	15	20	mS
V_{BO}	Brown out voltage		0.97	1.00	1.03	V
I_{BO}	Internal current source Generating the Brown out hysteresis		8.6	10	11.2	uA

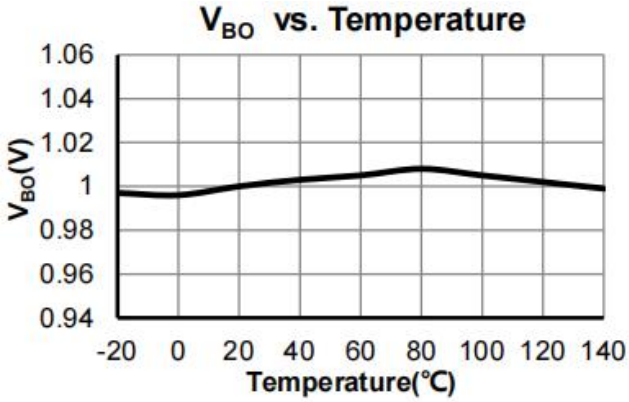
Performance Characteristics (T_A = 25℃, V_{DD}=15V, RI=43KΩ, unless otherwise noted)

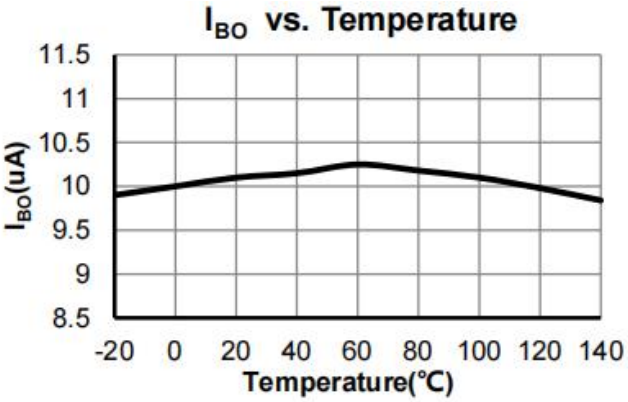


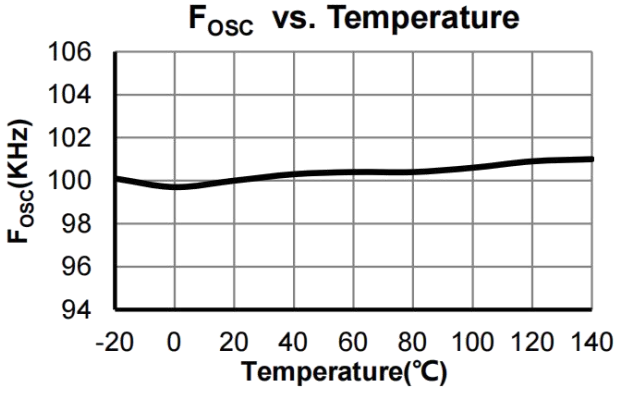


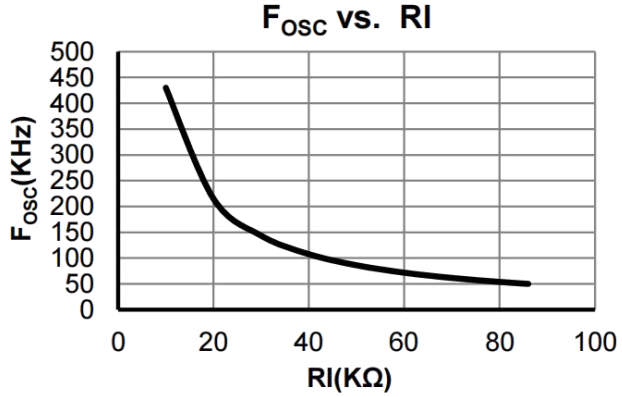












Functional Description

The NCP1252 hosts a high−performance current−mode controller specifically developed todrive power supplies designed for the ATX and the adapter market.

Current Mode Operation

Implementing peak current mode control topology,the circuit offers UC384X−like features to build rugged power supplies.

Adjustable Switching Frequency

A resistor to ground precisely sets the switching frequency between 50 kHz and a maximum of 500 kHz. The relationship between RI and switching frequency follows the below equation within the RI allowed range.

$$F_{OSC} = \frac{4300}{RI(K\Omega)}(KHz)$$

For example, a 43kΩ resistor RI could generate100kHz switching frequency.

Frequency Jitter for EMI Improvement

Frequency jittering of NCP1252 softens the EMIsignature by spreading out peak energy within aband ±5% from the center frequency, andtherefore eases the system design.

Low Startup Current

NCP1252 reaches a low no−load standby power represents a difficult exercise when the controller requires an external, lossy resistor connected to the bulk capacitor. The start−up current is guaranteed to be less than 100uA maximum, helping the designer to reach a low standby power level.

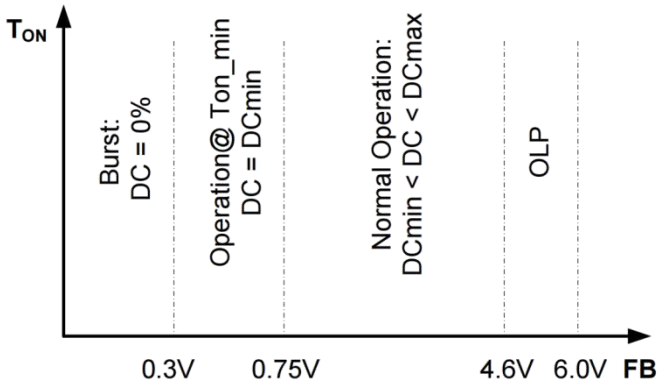
Adjustable Soft Start

The soft start is activated upon a start−up sequence (VDD going up and crossing V_{DD_ON}) after a minimum internal time delay of 120 ms (T_{SS_Delay}). But also when the BO pin is reset without in that case timer delay. This internal time delay gives extra time to the PFC to be sure that the output PFC voltage is in regulation. The SS pin is grounded until the internal delay is ended.

Burst Mode Feature

When the power supply loads are decreasing to alow level, the duty cycle also decreases to the minimum value the controller can offer. If the output loads disappear, the converter runs at the minimum duty cycle fixed by the propagation delay and driving blocks. It often delivers too much energy to the secondary side and it trips thevoltage supervisor. To avoid this problem, the FBis allowed to impose the min t_{ON} down to ~ Vf and it further decreases

down to $V_{Ref\_Burst\_L}$, zero duty cycle is imposed. This mode helps to ensure no load outputs conditions as requested by recently updated ATX specifications. Please note that the converter first goes to min t_{ON} before going to zero duty cycle: normal operation is thus not disturbed. The following figure illustrates the different mode of operation versus the FB pin level.



Short Circuit or Over Load Protection

A short circuit or an overload situation is detected when the CS pin level reaching its maximum level at 1V. In that case the fault status is stored in the latch and allows the digital timer count. If the digital timer ends then the fault is latched and the controller permanently stops the pulses on the driver pin.

If the fault is gone before ending the digital timer, the timer is reset only after 3 switching controller periods without fault detection (or when the CS pin <1V during at least 3 switching periods).

If the fault is latched the controller can be reset if a BO reset is sensed or if VDD is cycled down to V_{DD_OFF}.

Brown Out Protection

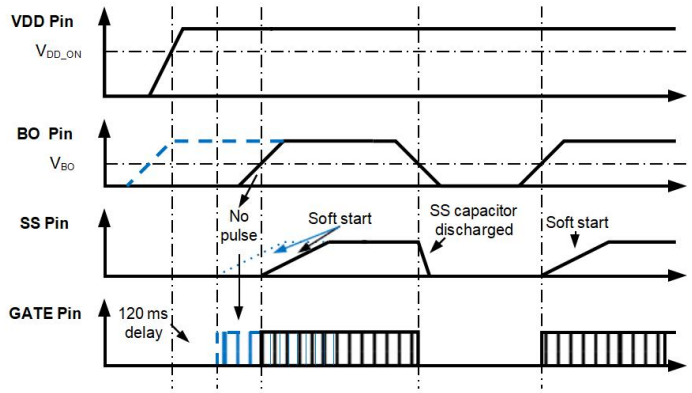
BO pin permanently monitors a fraction of the input voltage. When this image is below the V_{BO} threshold, the circuit stays off and does not switch. As soon the voltage image comes back within safe limits, the pulses are restarted via a startup sequence including soft start. The hysteresis is implemented via a current source connected to the BO pin; this current source sinks a current (I_{BO}) from the pin to the ground. As the current source status depends on the brown out comparator, it can easily be used for hysteresis purposes. A transistor pulling down the BO pin to ground will shut off the controller. Upon release, a new soft start sequence takes place.

Startup Sequence

The startup sequence is activated when VDD pin reaches V_{DD_ON} level. Once the startup sequence has been activated the internal delay timer (T_{SS_Delay}) runs. Only when the internal delay elapses the soft start can be allowed if the BO pin level is above VBO level. If the BO pin threshold is reached or

as soon as this level will be reached the soft start is allowed. When the soft start is allowed the SS pin is released from the ground and the current source connected to this pin sources its current to the external capacitor connected on SS pin. The voltage variation of the SS pin divided by 4 gives the same peak current variation on the CS pin.

The following figures illustrate the different startup cases.



When the VDD pin reaches the V_{DD_ON} level, the internal timer starts. As the BO pin level is above the VBO threshold at the end of the internal delay, a soft start sequence is started.at the end of the internal delay, the BO pin level is below the V_{BO} threshold thus the soft start sequence can not start. A new soft start sequence will start only when the BO pin reaches the V_{BO} threshold.

When the BO pin is grounded, the controller is shut down and the SS pin is internally grounded in order to discharge the soft start capacitor connected to this pin. If the BO pin is released, when its level reaches the V_{BO} level a new soft start sequence happens.

Ramp Compensation

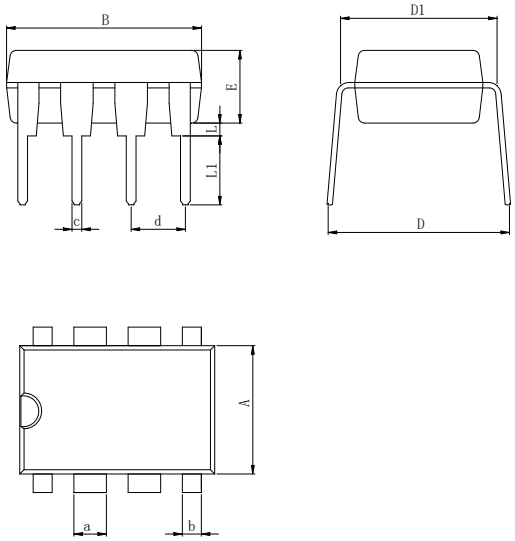
Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half of the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty-cycle close to and above 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. A simple resistor connected from the CS pin to the sense resistor allows the designer to inject ramp compensation inside his design.

Gate drive clamping

A lot of power MOSFETs do not allow their driving voltage to exceed 25V. The controller includes a low loss clamping voltage which prevents the gate from going beyond 18 V typical.

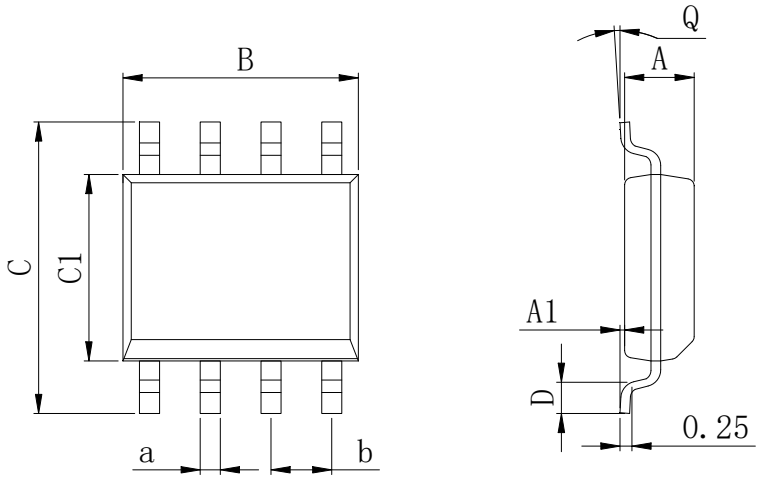
Physical Dimensions

DIP8



Dimensions In Millimeters(DIP8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.40	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	9.00	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP8 (150mil)



Dimensions In Millimeters(SOP8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

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