General Description:

JX-K04 is a high performance 4.0MP CMOS image sensor designed and fabricated with SOI's 2.2um pixel technology. It can deliver images at 60fps in full size mode and 30fps in HDR mode.

The JX-K04 consists of a 2696 x 1528 active pixel sensor (APS) array with on-chip 10-bit ADC, programmable gain control (PGA), and correlated double sampling (CDS) to significantly reduce fixed pattern noise (FPN). The sensor also has many standard programmable and automatic functions. It has the industry compliant MIPI CSI2 four-data lane serial interfaces. The external host controller can access this device through a standard serial interface.

It is available in wafer-level packaged CSP.

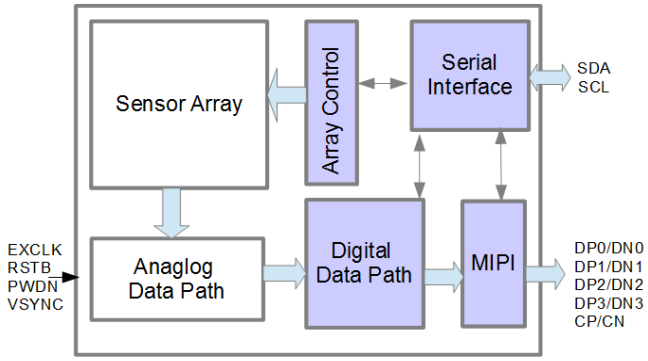
Features :

- Automatic functions:
  - ABLC – Automatic Black Level Calibration
- Programmable controls:
  - Gain, exposure, frame rate and size
  - Image mirror and flip
  - Window panning and cropping
  - I2C slave ID
- Output formats:
  - MIPI CSI2 (4-lane)
- Data formats:
  - 10-bit RAW RGB
- Others
  - 50/60Hz flick noise cancellation
  - Frame sync
  - Register group write capability
  - Black sunspot cancellation

Key Specifications:

Optical format		1/2.7"
Active Pixels		2696x1528
Pixel size		2.2 x 2.2 µm
Color filter array		RGB Bayer pattern
Chief Ray Angle		12◦degrees non-linear
Shutter type		Electronic rolling shutter
Maximum Frame Rate		Full: 2688x1520 @60fps HDR: HDR: 2688x1520@30fps (MIPI), 2 frames staggered output
Supply voltage	**Analog**	2.6 – 3.0V (2.8V nominal)
	I/O	1.7 – 3.45V (1.8V nominal)
Power consumption	**Active**	Typ.: 212 mW @Full 30fps
	Standby	Typ.: 300 uA
Output Formats		10-bit RGB Raw Data
Sensitivity		2390 mV/lux-sec
Max SNR		39.4 db
Dynamic range		78.3 db
Dark Current		6.5 mV/sec @ 45 °C
Operating junction temperature		-30 °C to 85 °C
Stable image junction temperature		60 °C

Functional Block:



Component Order Information:

Part Number	Description
JX-K04-C1-M3	CSP, MIPI interface @30fps
JX-K04-C1-M6	CSP, MIPI interface @60fps

Contents

Pin Diagram

JX-K04's pin diagram is shown in Figure 1 and each pin's description is shown in Table 1:

Figure 1: JX-K04 CSP top view

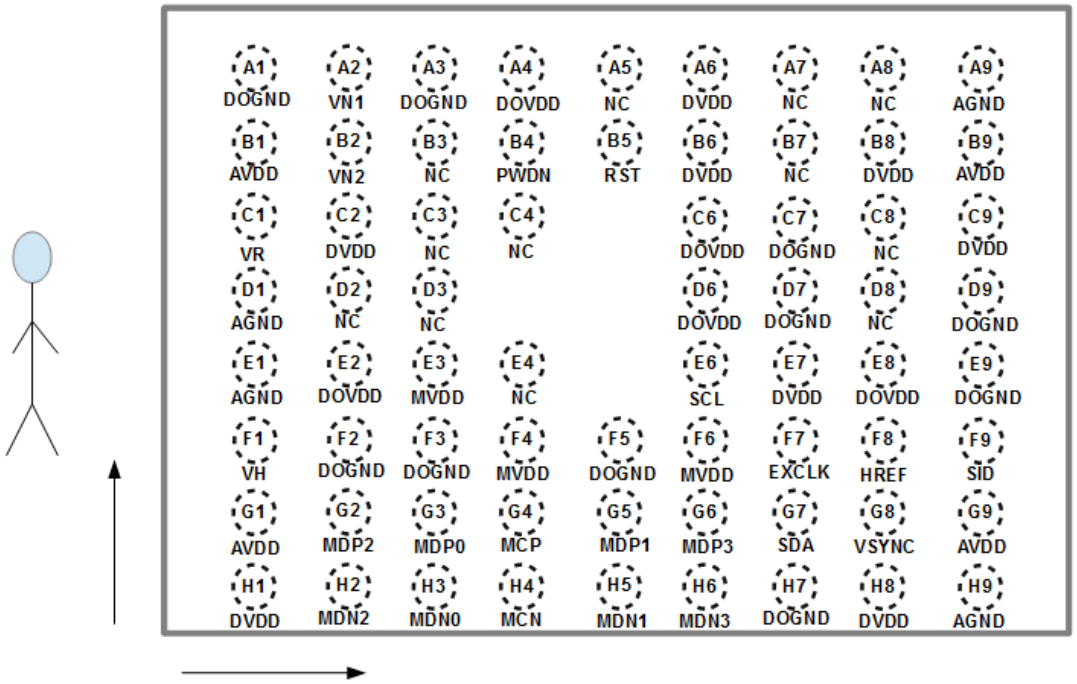
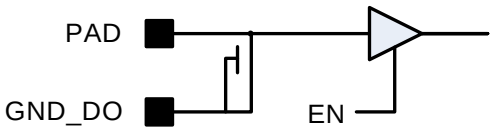
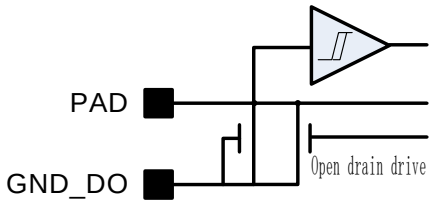
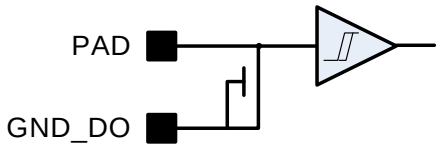
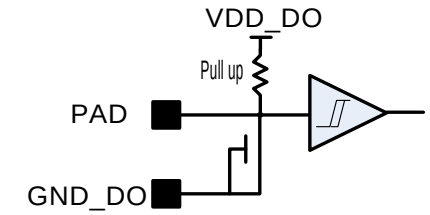
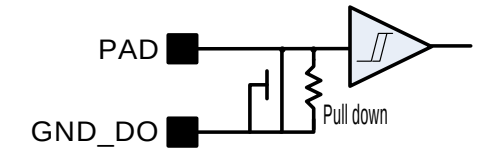
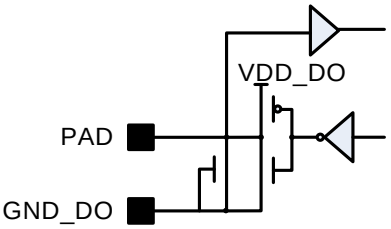
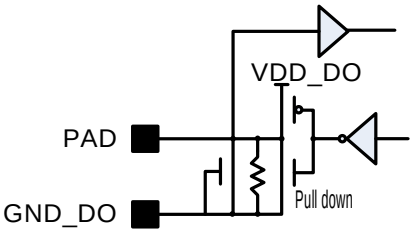
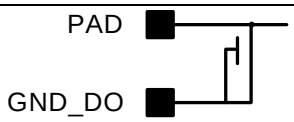
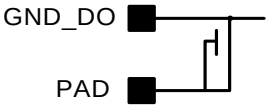


Table 1: Pin Description

Pin number	Pin name	Pin type	Description
A1	DOGND	Supply	Digital I/O ground
A2	VN1	Reference	Internal analog reference.
A3	DOGND	Supply	Digital I/O ground
A4	DOVDD	Supply	Digital I/O supply voltage.
A5	NC		No Connection
A6	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
A7	NC		No Connection
A8	NC		No Connection
A9	AGND	Supply	Analog ground
B1	AVDD	Supply	Analog supply voltage.
B2	VN2	Reference	Internal analog reference.
B3	NC		No Connection
B4	PWDN	Input	System power down control. High active.
B5	RSTB	Input	System synchronize reset when driven low, it resumes normal operation with all configuration register set to factory default
B6	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
B7	NC		No Connection
B8	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
B9	AVDD	Supply	Analog supply voltage.
C1	VR	Reference	Internal analog reference.
C2	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
C3	NC		No Connection
C4	NC		No Connection
			.
C6	DOVDD	Supply	Digital I/O supply voltage.
C7	DOGND	Supply	Digital I/O ground
C8	NC		No Connection
C9	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
D1	AGND	Supply	Analog ground
D2	NC		No Connection
D3	NC		No Connection
D6	DOVDD	Supply	Digital I/O supply voltage.
D7	DOGND	Supply	Digital I/O ground
D8	NC		No Connection
D9	DOGND	Supply	Digital I/O ground
E1	AGND	Supply	Analog ground
E2	DOVDD	Supply	Digital I/O supply voltage.
E3	MVDD	Supply	PLL block supply voltage. Connect to DVDD
E4	NC		No Connection
E6	SCL	Input	Serial interface clock input.
E7	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
E8	DOVDD	Supply	Digital I/O supply voltage.
E9	DOGND	Supply	Digital I/O ground
F1	VH	Reference	Internal analog reference.
F2	DOGND	Supply	Digital I/O ground
F3	DOGND	Supply	Digital I/O ground
F4	MVDD	Supply	PLL block supply voltage. Connect to DVDD.
F5	DOGND	Supply	Digital I/O ground
F6	MVDD	Supply	PLL block supply voltage. Connect to DVDD.
F7	EXCLK	Input	System clock input.
F8	HREF	I/O	Line data valid signal output.
F9	SID	I/O	I2C Slave ID programming bit, default pull down internally. I2C slave ID can be programmed as "80/81", "88/89" for write and read.

G1	AVDD	Supply	Analog supply voltage
G2	MDP2	I/O	MIPI data lane 2 positive output.
G3	MDP0	I/O	MIPI data lane 0 positive output.
G4	MCP	I/O	MIPI clock lane positive output.
G5	MDP1	I/O	MIPI data lane 1 positive output.
G6	MDP3	I/O	MIPI data lane 3 positive output.
G7	SDA	I/O	Serial data, pull to DOVDD with a 4.7k Ω resistor
G8	VSYNC	I/O	Vertical synchronize signal, drive high when last frame end and drive low before next frame start. Also, can be programmed as frame synchronize input
G9	AVDD	Supply	Analog supply voltage.
H1	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
H2	MDN2	I/O	MIPI data lane 2 negative output.
H3	MDN0	I/O	MIPI data lane 0 negative output.
H4	MCN	I/O	MIPI clock lane negative output.
H5	MDN1	I/O	MIPI data lane 1 negative output.
H6	MDN3	I/O	MIPI data lane 3 negative output.
H7	DOGND	Supply	Digital I/O ground
H8	DVDD	Supply	Digital core supply voltage. With embedded 1.5V regulator
H9	AGND	Supply	Analog ground

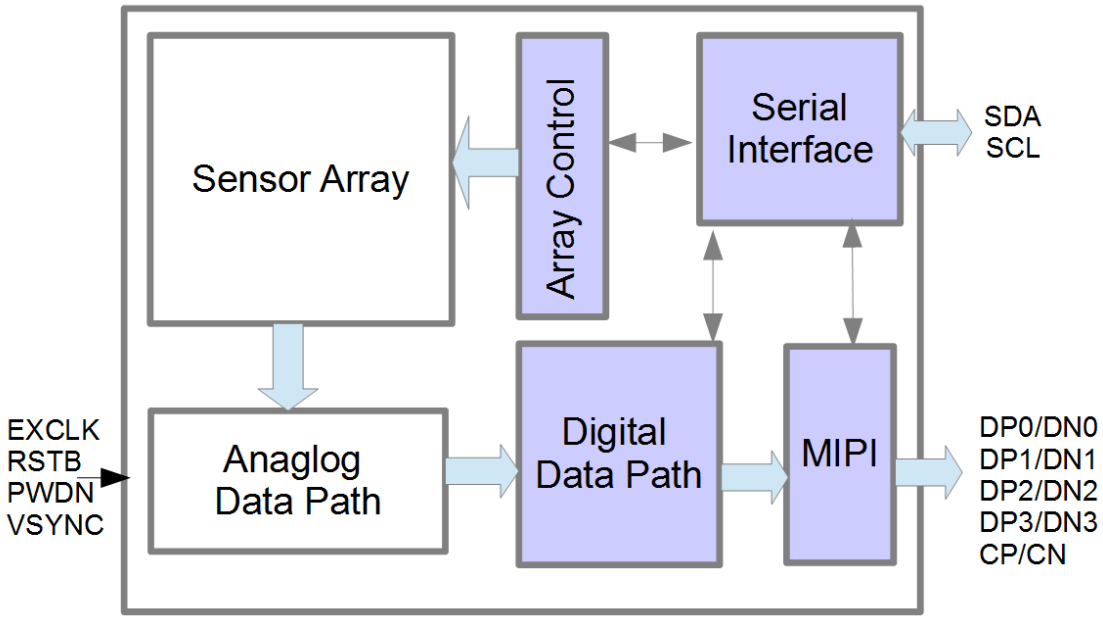
Table2: I/O Equivalent Circuit Diagram

Symbol	Equivalent Circuit
EXCLK	
SDA	
SCL	
RSTB	
PWDN	
HREF,VS, PCLK	
SID	
MDP3,MDN3,MDP2,MDN2, MDP1,MDN1, MDP0,MDN0,MCP, MCN,VH,VR	
VN1,VN2	

Functional Overview:

The JX-K04 is a progressive-scan CMOS image sensor. It has an on-chip, phase-locked loop (PLL) to generate internal clocks from a single master input clock running between 6 and 27MHz. Figure 2 illustrates the sensor's block diagram.

Figure 2. Functional Block Diagram



User can access and program JX-K04 sensor internal registers through the two-wire serial bus. The core of the sensor is a 2704x1560 pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting and reading that row, the pixels in the row integrate the incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal path to apply gain and analog signal to digital signal converter (ADC). The ADC output pas ses through a digital processing path for black level calibration. Then the data will output though a DVP port or MIPI CSI-2 standard interface.

Pixel Array Format:

The JX-K04 pixel array consists of a 2704-column by 1560-row matrix of pixels addressed by column and row. The address (column 0, row 0) represents the upper-right corner of the entire array (please refer to Figure 3 for JX-K04's Pixel array structure). The first 32 rows are optical black row for black level calibration. Outside of the 2688x1520 active pixels, there are several boundary pixels: 4 rows on top, 4 rows at the bottom, 4 columns on the right, and 4 columns on the left. Please note that only performance of the active image area is defined in the outgoing specifications, performance of dummy columns and rows are not guaranteed as same as the active image. The detailed pixel array arrangement and default read out direction is noted in the following two figures:

Figure 3: Pixel array structure

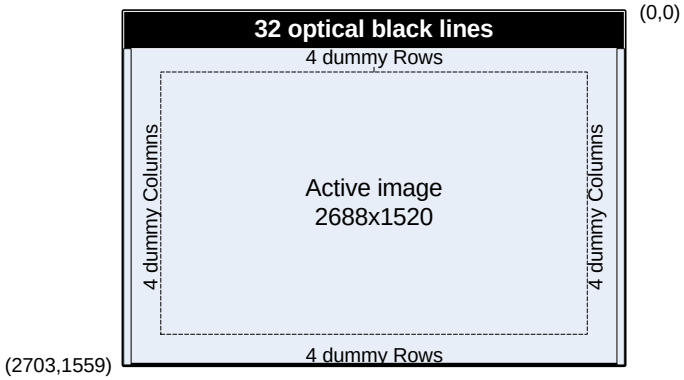
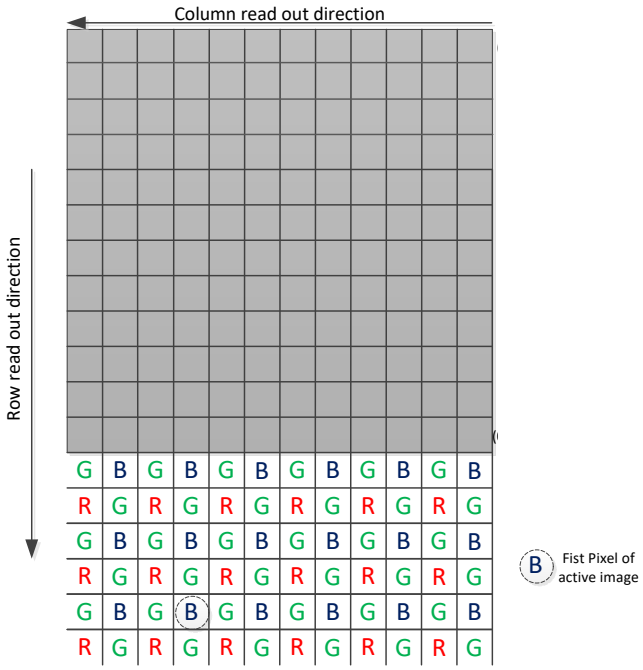


Figure 4: Pixel array detail with default read out direction.



Data Output Format:

The output images are divided into frames, which are further divided into lines. By default, the sensor produces 1556 lines (rows) of 2696 columns each. The VSYNC and HREF signals indicate the boundaries between frames and lines, respectively. PCLK can be used as a clock to latch the data. For each PCLK cycle, one 10-bit pixel data outputs on the D[9:0] pins (Figure 5). The pixel data is valid when HREF signal is asserted. The VSYNC signal indicates frame end and new frame start. JX-K04 default frame timing is illustrated as figure 6.

Figure 5: Row data output timing

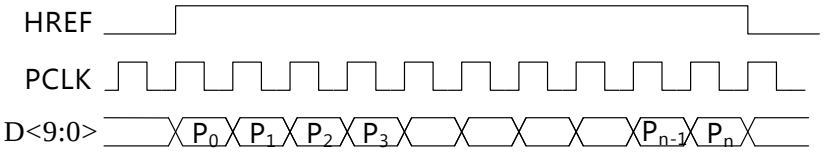
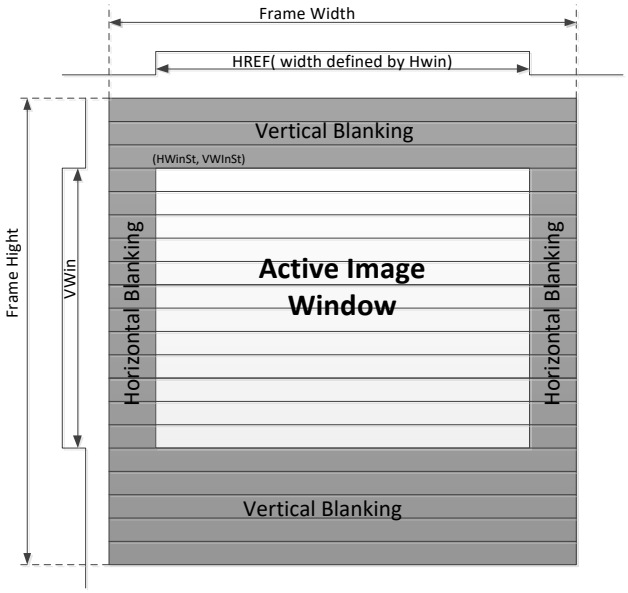


Figure 6: Default frame timing

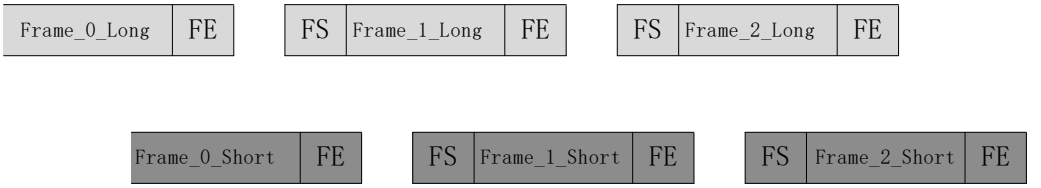


As shown above in Figure 6, a line (row) period can be calculated as Trow = Frame_width * Thclk, and frame rate can be calcul ated as fps=1/(Frame_hight * Trow).
As default configuration, VSYNC, PCLK and Data are all valid at PCLK rising edge. For user convenience, JX-K04 provides register bits to control HREF, VSYNC and PCLK polarity. In addition, PCLK also have adjustable delay control.
For pixel Bayer pattern data output, several settings can have effect on pixel output seque nces. These registers include HWIn_St, VWin_St, Haddr_St, Mirror, V_Flip. Please consult your SOI AE for further information.

HDR mode

JX-K04 support HDR mode, user can set 2 different exposure time and output 2 frame data (long and short exposure) in s taggered output mode. Figure 8,9 are diagrams to illustrate frame output timing under this mode.

Figure 8: HDR frame timing with VC in MIPI output



Notes: 1) Long_exposure + short_exposure <= Frame_high

Figure 9: HDR frame timing without VC in MIPI output

Test Pattern Output:

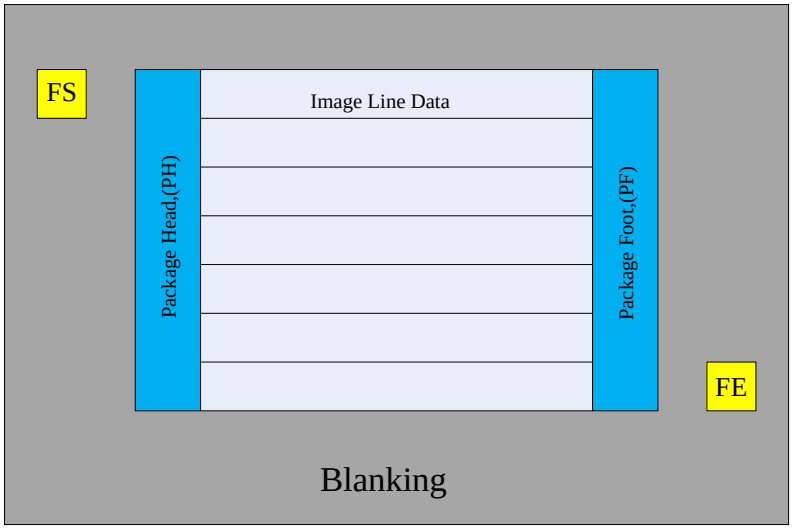
JX-K04 can output following test patterns as described below:

- Walking "1" test pattern: for most sensor module connectivity test, JX-K04 provides walking "1" test pattern.

MIPI interface:

JX-K04 supports MIPI CSI-2 compliant interface. It has four pairs of differential data lane. JX-K04 can output raw8 or raw10 mode through the MIPI interface. In raw8 mode, only 8 MSBs of 10-bit data will output and user needs to set MIPI clock speed at 8x parallel port pixel clock. In raw10 mode, user needs to set MIPI PHY clock as 10x parallel port pixel clock.

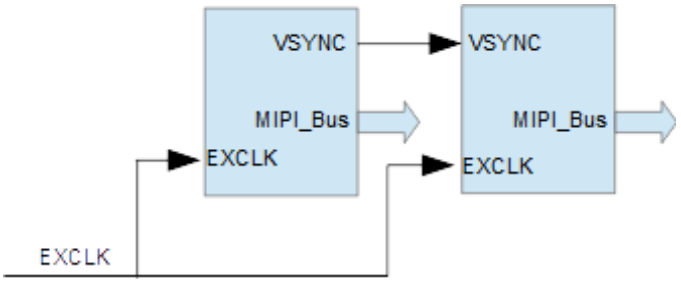
Figure 10: MIPI interface frame timing



Frame Synchronization:

JX-K04 provides the capability of frame synchronization. By setting VSYNC pin as input and enable frame-sync option, JX-K04 will work as slave device and synchronized with an external VSYNC. If all master devices and slave devices use same timing setting, all devices frame timing mismatch will be less than few pixel clocks. Figure 11 shows the way to realize frame synchronization.

Figure 11: Frame Synchronization illustration



Serial Interface:

The serial interface is a two-wire bi-directional bus. Both wires (Serial Clock –SCL and Serial Data – SDA) are connected to DOVDD via a pull-up resistor, and when the bus is free both lines are high. The two-wire serial interface defines several different transmission stages as follows:

- A start bit
- The slave device 7-bit address
- An (No) acknowledge bit coming from slave
- An 8-bit or 16-bit message (address and/or data)
- A stop bit (or another 8bit or 16bit message in multiple Read/Write access)

Figure 12: I2C Timing chart

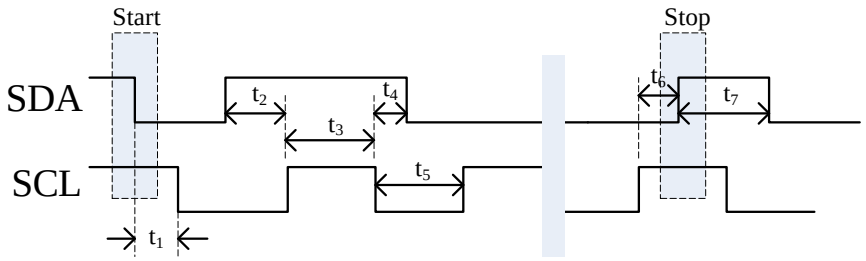
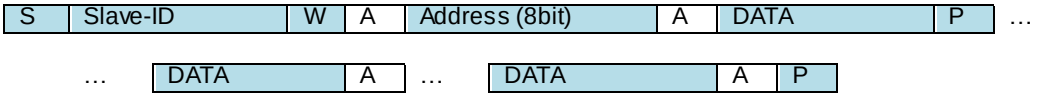


Table 3: I2C timing characteristic

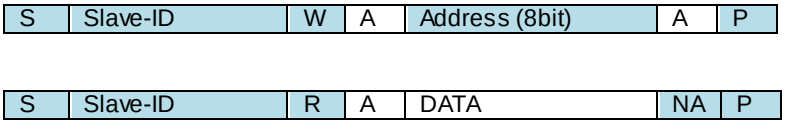
Symbol	Description	Min	Max	Units
	SCL clock frequency	0	400k	Hz
t1	Hold time for START condition	0.6	-	µs
t2	Data setup time	160	-	ns
t3	High period of the SCL clock	0.6	-	µs
t4	Data hold time	0.2	0.9	µs
t5	Low period of the SCL clock	1.3	-	µs
t6	Setup time for STOP condition	0.6	-	µs
t7	Bus free time between STOP and START condition	1.3	-	µs
	Rise time for both SDA and SCL signals		300	ns
	Fall time for both SDA and SCL signals		300	ns
Cb	Capacitive load for each bus line		400	pF

Single Write Mode operation

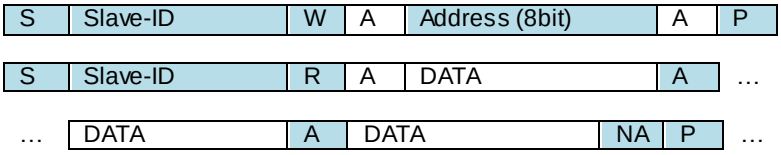
Multiple Write Mode (Register address is increased automatically) operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically) operation



S: start conditions, A: acknowledge bit, NA: no acknowledge, DATA: 8 bit data, P: stop condition.
JX-K04 slave ID is programmable, default is 0x80/81 for write and read. User can program SID data bit for other configuration. The slave ID program table is list below:

SID	Read/Write
X	81/80
Pull high	89/88

Register Group Write Function:

JX-K04 provides register group write function, user can pre-load address and data from register 0xC0 to 0xFF, then trigger this function by setting Reg0x1F[7], normally JX-K04 will auto write back group register content at next vertical blanking period and reset Reg0x1F[7] JX-K04 can update up to 32bytes of registers.

User can always monitor Reg0x1F[7] to make sure group write procedure is finished or not.

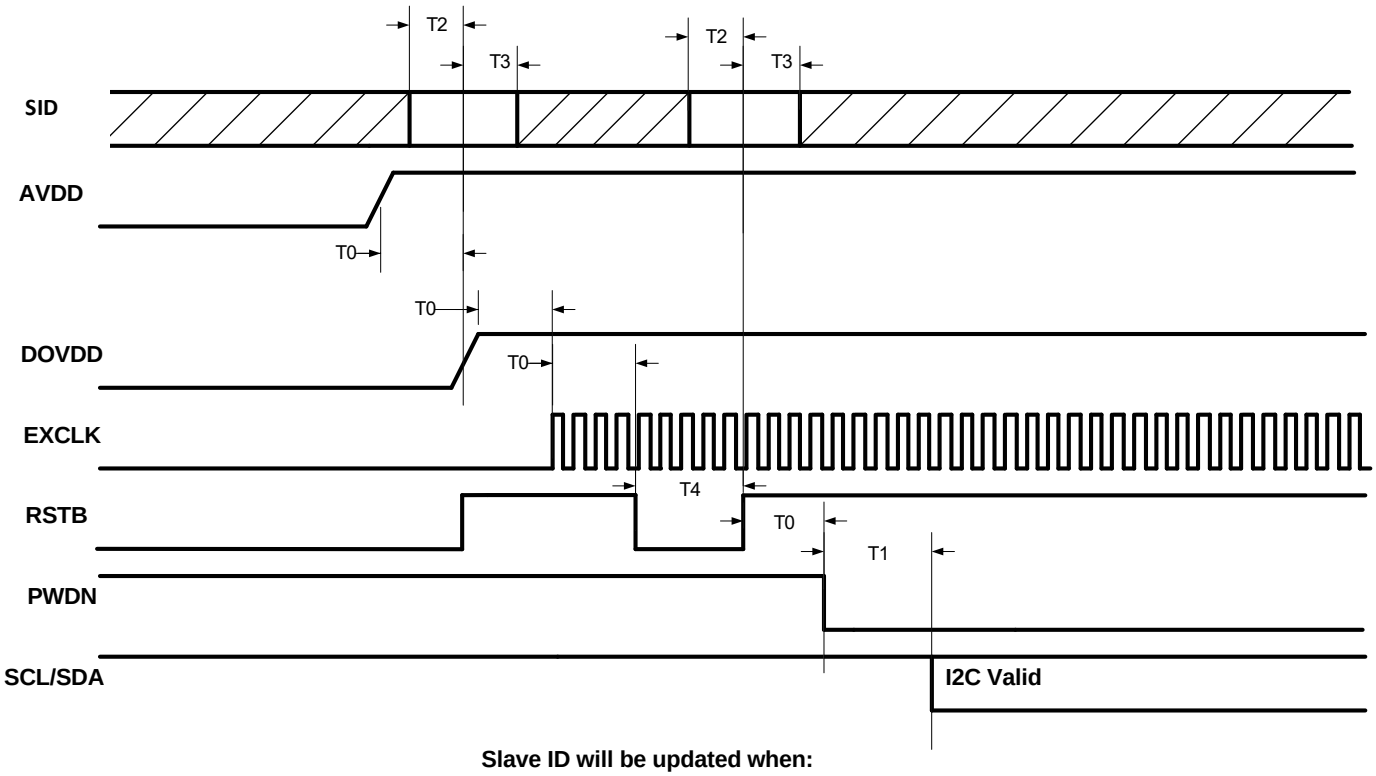
Register Page:

JX-K04 provides two pages of register, Page0 addressed to register 0x00~0xFF, Page1 addressed to register 0x100~0x1FF.
When switch from Page0 to Page1, it is necessary to set register BF[0].
Vice versa, when switch to Page1 from Page0, it is necessary to clear register BF[0].
Please refer to register description about register 0xBF.

Power on/off sequence:

Figure 13 shows a reference power up sequence of JX-K04.

Figure 13. Power up sequence for JX-K04



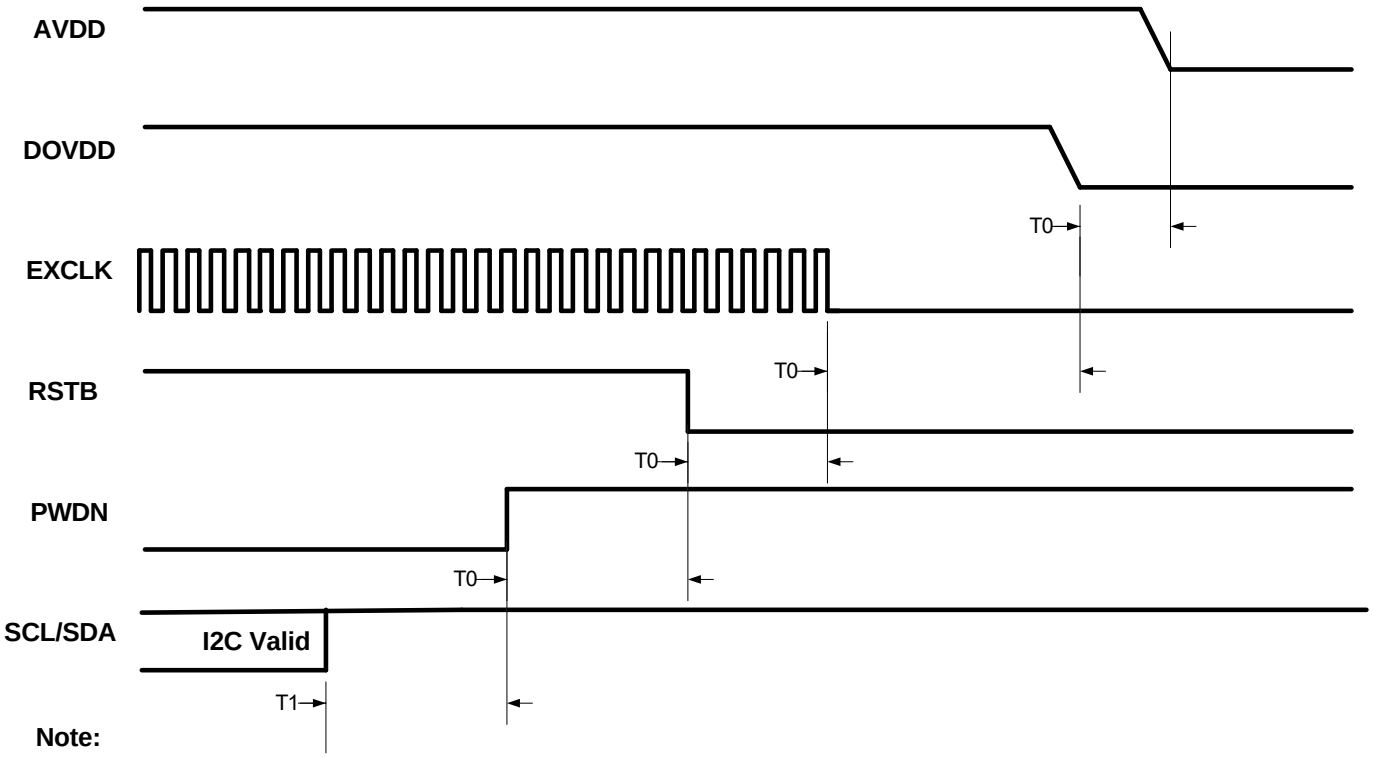
Note:
1. T0 >= 0 us
2. T1 >= 8192 EXCLK cycles
3. T2>= 1ms
4. T3>= 1ms
5. T4>= 10ms

Slave ID will be updated when:
1. Power up (DVDD/DOVDD)
2. Hardware reset pin: Low -> High
3. Software reset : Reg0x12[7]=" 1"

Please stable SID when issue above commands.

Figure 14 shows a reference power down sequence of JX-K04.

Figure 14. Power down sequence for JX-K04



Note:
1. T0 >= 0 ns
2. T1 >= 512 EXCLK cycle

Electrical Characteristics:

Table 4. Absolute maximum ratings

Symbol	Descriptions	Absolute maximum rating	Units
VDD-IO	I/O Digital Power	4.5	V
VDD-A	Analog Power	4.5	V
VDD-D	Core Digital Power	4.5	V
V_I	Input voltages	-0.3v to V_{DD-IO} + 1V	V
T_{AS}	Ambient Storage Temperature	-40 ~ 125	ºC

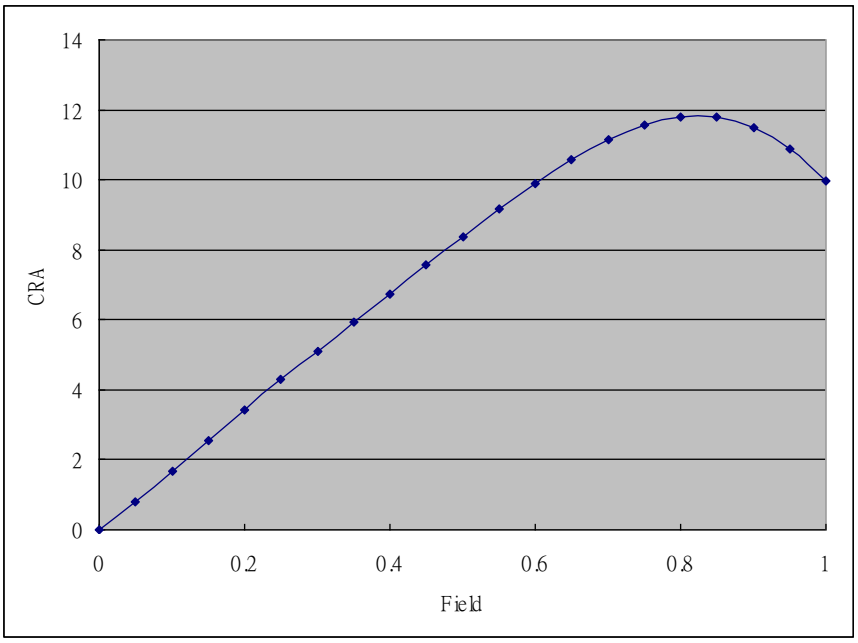
Table 5. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)

Symbol	Descriptions	Max	Typ	Min	Units
supply					
V_{DD-IO}	Supply voltage (DOVDD)	3.45	1.8	1.7	V
V_{DD-A}	Supply voltage (AVDD)	3.0	2.8	2.6	V
V_{DD-D}	Supply voltage (DVDD) With embed regulator	1.65	1.5	1.35	V
Digital Inputs					
V_{IL}	Input voltage LOW	0.2* V_{DD-IO}	-	-	V
V_{IH}	Input voltage HIGH			0.7*V_{DD-IO}	V
C_{IN}	Input capacitor	10			pF
Digital Outputs (loading 20pF)					
V_{OH}	Output voltage HIGH			V_{DD-IO} – 0.2	V
V_{OL}	Output voltage LOW	0.2			V
Power consumption (Internal DVDD, MVDD short to DVDD; MIPI output mode; AVDD=2.8V, DOVDD=1.8V)					
I_{DD-IO}	Supply current (V_{DD-IO}=1.8V@30fps MIPI4L full size)		40		mA
I_{DD-A}	Supply current (V_{DD-A}=2.8V@30fps MIPI4L full size)		50		mA
Ipwrdn	HW PWDN Pin active		300		uA

CRA Specifications:

JX-K04 is designed with a non-linear chief ray angle curve as shown in Figure 15. The shifting of the color filter and micro lenses on the sensor is critical to accommodate the ever-shorter height of the camera module as well as minimizing shading at the corner of the image.

Figure 15. CRA Curve for JX-K04



Field	CRA
0.00	0.00
0.05	0.80
0.10	1.66
0.15	2.54
0.20	3.42
0.25	4.28
0.30	5.11
0.35	5.94
0.40	6.75
0.45	7.57
0.50	8.37
0.55	9.16
0.60	9.90
0.65	10.58
0.70	11.15
0.75	11.57
0.80	11.80
0.85	11.78
0.90	11.48
0.95	10.88
1.00	9.96

Mechanical Specifications:

JX-K04 is available in CSP packaged component. Figure 16 shows top view and bottom view of the CSP component. Table 6 shows the nominal dimensions for the packaged chip.

Figure 16. CSP Top, Bottom, Side View

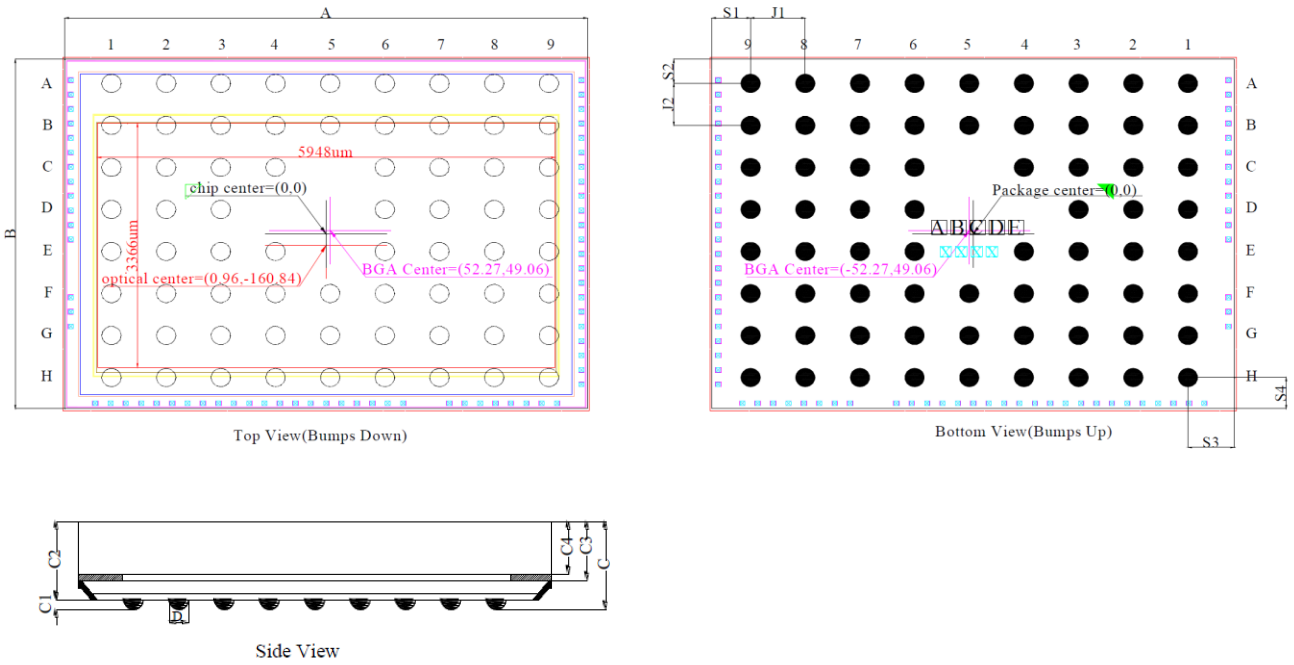
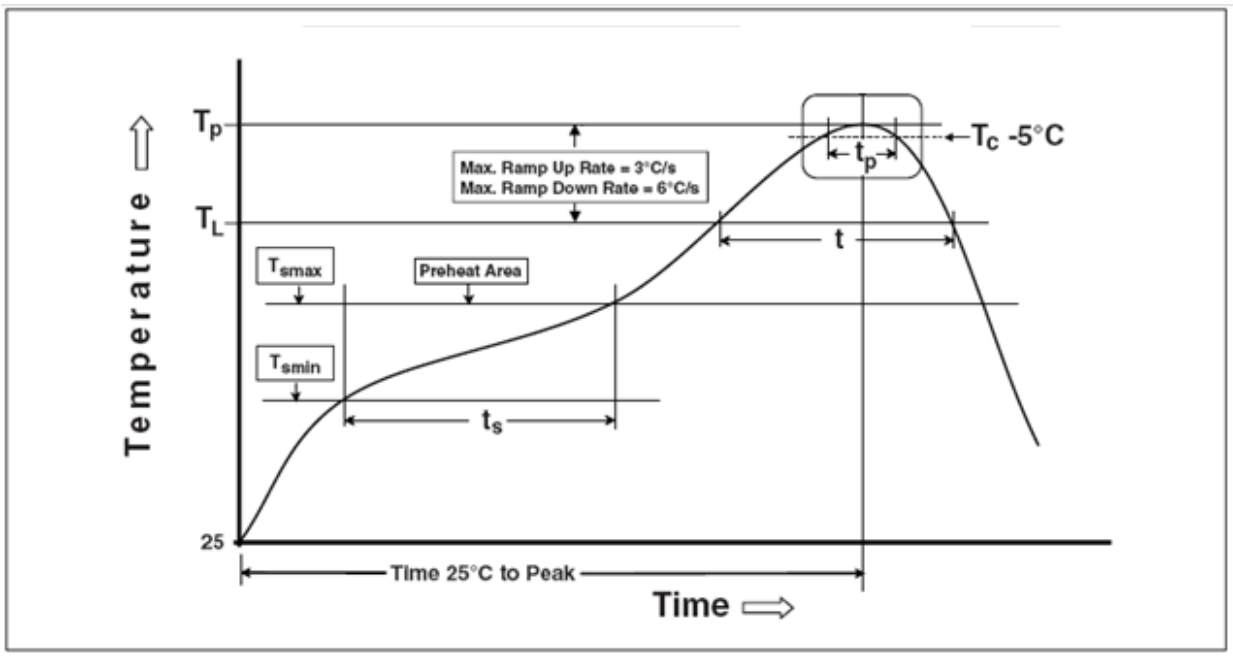


Table 6. Dimensions for JX-K04 CSP package (in mm)

	Symbol	Nominal	Min	Max	Nominal	Min	Max
		Millimeters			Inches		
Package Body Dimension X	A	6.784	6.759	6.809	0.26709	0.26610	0.26807
Package Body Dimension Y	B	4.824	4.799	4.849	0.18992	0.18894	0.19091
Package Height	C	0.770	0.710	0.830	0.03031	0.02795	0.03268
Ball Height	C1	0.130	0.100	0.160	0.00512	0.00394	0.00630
Package Body Thickness	C2	0.640	0.605	0.675	0.02520	0.02382	0.02657
Thickness from top glass surface to wafer	C3	0.445	0.425	0.465	0.01752	0.01673	0.01831
Glass Thickness	C4	0.400	0.385	0.415	0.01575	0.01516	0.01634
Ball Diameter	D	0.250	0.220	0.280	0.00984	0.00866	0.01102
Total Ball Count	N	68					
Pins pitch X axis	J1	0.710					
Pins pitch Y axis	J2	0.580					
Edge to Pin Center Distance along X1	S1	0.49973	0.469730	0.529730	0.01967	0.01849	0.02086
Edge to Pin Center Distance along Y1	S2	0.33294	0.302940	0.362940	0.01311	0.01193	0.01429
Edge to Pin Center Distance along X2	S3	0.60427	0.574270	0.634270	0.02379	0.02261	0.02497
Edge to Pin Center Distance along Y2	S4	0.43106	0.401060	0.461060	0.01697	0.01579	0.01815

IR Reflow:

Recommended IR-reflow profile and condition.



Profile Feature	Green Assembly
Preheat & Soak Temperature min (T_{Smin}) Temperature min (T_{Smax}) Time (T_{Smin} to T_{Smax}) (t_S)	 150℃ 200℃ 90-150 seconds (Optimal 100)
Average ramp-up rate(T_{Smax} to T_P)	3℃/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	217℃ 60-150 seconds (Optimal 120)
Peak package body temperature (T_P)*	240 +/-5℃
Time (t_P) within 5℃ of the specified classification temperature (T_C)	10~30 seconds
Average ramp-down rate (T_P to Tsmax)	6℃/second max.
Time 25℃ to Peak temperature	8 minutes max.

Note:

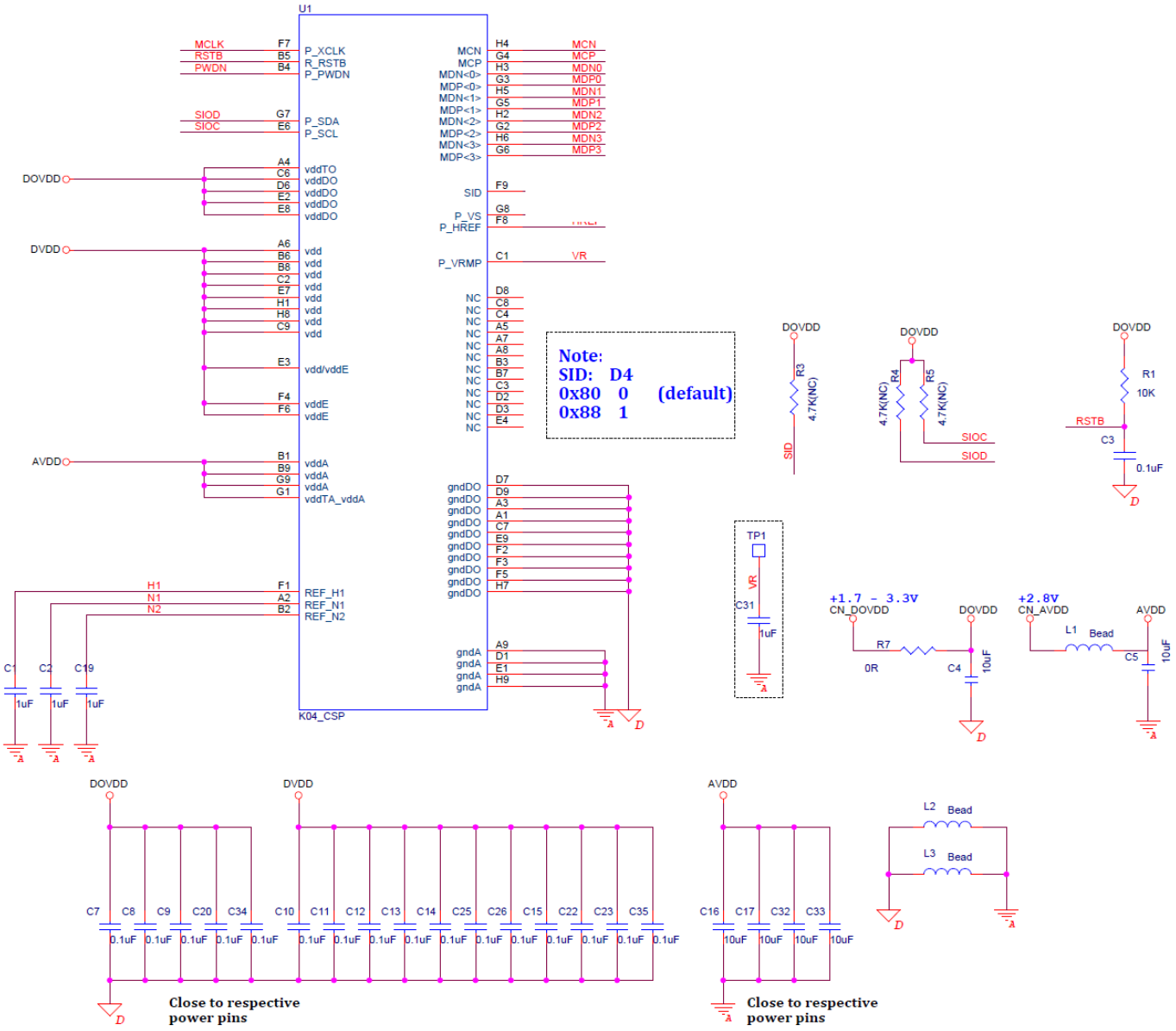
1, Maximum number of reflow cycles=3.

2, N2 gas reflow or control O2 gas ppm<500 as recommendation.

CSP Module Schematic (Reference):

Figure 17 shows reference schematics for CSP module.

Figure 17. Reference schematic for CSP module



Register Descriptions:

Write Slave ID:0x80/88 Read Slave ID:0x81/89

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	PGA	00	RW	Programmable gain, valid 00 to 3F, Total gain = 2^PGA[6:4]*(1+PGA[3:0]/16)
01	EXP	1F	RW	Exposure line LSBs, EXP [7:0]
02	EXP	00	RW	Exposure line MSBs, EXP[15:8].; AEC[15:8] Exposure time is defined by EXP[15:0] at line period base. T_{EXP}=EXP[15:0]*T_{Line}
03-04				RSVD
05	SAEC0	1F	RW	Short exposure lines.
06	SFramSt	1F	RW	SAEC[7:0] Short exposure frame start position in HDR mode
07	GainLmt	00	RW	GainLmt[7:4]: Max gain limitation in AEC/AGC auto mode. "00": 4x; "01":8x; "10":16x; "11":32x; GainLmt[3]: RSVD. GainLmt[2]: HDR mode option. 0: Fix short sample position. 1: Short sample delay long line as short exposure. GainLmt[1]: HDR mode short pre-pre-chg enable. GainLmt[0]: HDR mode short pre-chg enable.
08	SAEC1	00		[7:1] : RSVD. [0] : SAEC[8] with Reg06.
09				RSVD
0A	PIDH	04	R	PIDH[7:0]:Product ID MSBs. "0x04"
0B	PIDL	04	R	PIDL[7:0]: Product ID LSBs. "0x04"
0C	DVP1	40	RW	DVP control 1. DVP1[7]: RSVD DVP1[6]: Sensor sun spot elimination control, "1": disable sun spot elimination, "0": enable sun spot elimination. DVP1[5:4]: SRAM read out clock delay control. (after SRAM) DVP1[3:2]: RSVD DVP1[1:0]: DVP test mode output option. "00": DVP output normal image data. "01": DVP[9:0] = Output 10-bit walk "1" test pattern.; others:RSVD
0D	DVP2	50	RW	DVP control 2. DVP2[7:4]: P-Pump and N-Pump clock selection. DVP2[3:2]: PAD drive capability. "00": min, "11": max. DVP2[1:0]: RSVD
0E	PLL1	11	RW	PLL control 1. PLL1[7]: PLL bypass selection. "1": PLLclk = Input clock/PLL_Pre_Ratio. "0": see PLL2[1:0]. PLL1[6:4]: reserved PLL1[3]: Sys_Clk select, "0":sys normal divider clock before Sys_Clk divider, "1": select Mipi_HS_Clk before Sys_Clk divider PLL1[2]: external clock input pad circuit option, "0": internal no Schmitt trigger; "1": internal has Schmitt trigger. PLL1[1:0]: PLL pre-divider ratio. PLL_Pre_Ratio = 1 + PLL[1:0]

0F	PLL2	14	RW	PLL control 2. PLL2[7:4]: RSVD; PLL2[3]: "1" : MIPI high speed clock = VCO/2; "0": MIPI high speed clock = VCO; PLL2[2]: "1": work with MIPI 10bit mode, "0": work with MIPI 8bit mode PLL2[1:0]: PLL clock divider. PLLclk = VCO/(1+PLL2[1:0])
10	PLL3	22	RW	PLL control 3. PLL VCO multiplier. VCO = Input clock*PLL3[7:0]/PLL_Pre_Ratio
11	CLK	80	RW	Digital system clock control CLK[7]: System clock option. "1": system clock use PLLclk directly. "0": see system clock equation below. CLK[6]: system clock digital doubler on/off selection. "1": on, "0": off CLK[5:0]: system clock divide ratio. Equation: When CLK[5:0] > 0: System clock = PLLclk *(1+CLK[6])/(2*CLK[5:0]) When CLK[5:0] = 0: System clock = PLLclk*(1+CLK[6])/2
12	SYS	00	RW	System status set up SYS[7]: Soft reset initialize, "1": initial system reset, it will reset whole sensor to factory default status, and this bit will clear after reset. Default : "0": normal mode SYS[6]: Sleep mode on/off selection, "1": sensor into sleep mode. No data output and all internal operation stops. External controller can stop sensor clock, while I2C interface still can work. Default : "0" : normal mode SYS[5]: mirror image on/off, "1": mirrored image output, "0": normal image output SYS[4]: flip image on/off, "1": flipped image output, "0": normal image output. SYS[3]: HDR mode on/off selection. "0": normal mode, "1": HDR mode. SYS[2]: RSVD. SYS[1]: vertical skip or full mode selection. "0" : full mode,"1":vertical skip mode SYS[0]: Horizontal down sample mode enable.
13	LCCtrl1	81	RW	Luminance control register 1. LCCtrl1[7:1]:RSVD. LCCtrl1[0]: automatic luminance control on/off selection, "0": auto, "1": manual
14 – 18	LCCtrl2		RW	RSVD
19	LCCtrl17	20	RW	Luminance control register 7 LCCtrl7[7:6]: PCLK delay option. LCCtrl7[5]: AGC delay 1 frame valid option. "0": manual gain will apply at next VSYNC;"1": manual gain will delay 1 frame to apply. LCCtrl7[4]: RSVD LCCtrl[3]: Enable AE change every frame. LCCtrl[2:0]: RSVD
1A	LCCtrl8	80	RW	Luminance control register 8 LCCtrl8[7:0]: RSVD
1B	LCCtrl9	49	RW	Luminance control register 9 LCCtrl9[7:3]: RSVD LCCtrl9[2:1]: pre-precharge line selection, "00": 1 line, "01:2lines, "10": 3 lines, "11": 4 lines. LCCtrl9[0]: pre-precharge option on/off selection, "0": off, "1": on.
1C	LCCtrl10	00	R	Luminance control register 10 LCCtrl10[7:0]: image luminance average value.
1D	DVP3	00	RW	DVP control 3 DVP3[7:0]: GPIO direction control for data output port D[7:0]. "1": enable output. "0": tri-state output.
1E	DVP4	1C	RW	DVP control 4

				DVP4[7]: PCLK polarity control. "0": data output at rising edge of PCLK, "1":data output at falling edge of PCLK DVP4[6]: HREF polarity control. "0": positive, "1": negative DVP4[5]: VSYNC polarity control. . "0": positive, "1": negative DVP4[4:0]: GPIO direction control for output port: PCLK, HREF, VSYNC and D[9:8] . "1": enable output. "0": tri-state output.
1F	GLat	00	RW	Group latch control Glat[7]: Group write trigger. "1": system will write reg0xC0 to 0xFF content to proper register. This bit will clear after group write. "0": inactive group write function. Glat[6]: Group latch trigger time option, "0": trigger at vertical blanking period. "1": group latch trigger immediately. Glat[5:0]: reserved
20	FrameW	C0	RW	Sensor frame time width LSBs; FrameW[7:0]
21	FrameW	03	RW	Sensor frame time width MSBs; FrameW[15:8] FrameW[15:0]: sensor frame width
22	FrameH	20	RW	Sensor frame time high LSBs ;FrameH[7:0]
23	FrameH	06	RW	Sensor frame time high MSBs. FrameH[15:8] FrameH[15:0]: sensor frame high. Sensor frame rate is defined as Fpclk / (FrameW*FrameH). Fpclk: frequency of pixel clock.
24	Hwin	A0	RW	Image horizontal output window width LSBs: Hwin[7:0]
25	Vwin	F0	RW	Image vertical output window high LSBs: Vwin[7:0]
26	HVWin	52	RW	Image output window horizontal and vertical MSBs. { Vwin[11:8],Hwin[11:8]}
27	HwinSt	E0	RW	Image horizontal output window start position LSBs. HwinSt[7:0]
28	VwinSt	15	RW	Image vertical output window start position LSBs. VwinSt[7:0]
29	HVWinSt	01	RW	Image output window horizontal and vertical start position MSBs. {VwinSt[11:8],HwinSt[11:8]}
2A	Cshift1	DC	RW	Column shift control 1 Cshift1[7:0]: Column SRAM data shift start position LSBs. Cshift[7:0]
2B	Cshift2	11	RW	Column shift control 2 Cshift2[7:6]: SRAM read out start address MSBs. SenHASt[9:8] Cshift2[5:4]: RSVD Cshift2[3:0]: Column SRAM data shift timing start position MSBs , Cshift[9:8]
2C	SenHASt	00	RW	SRAM read out start address LSBs, SenHASt[7:0]; each bit represent 2 pixels
2D	SenVSt	00	RW	Sensor physical vertical start address, LSBs. SenVSt[7:0]; each bit represent 4 lines
2E	SenVEnd	84	RW	Sensor physical vertical end address, LSBs. SenVEnd[7:0] ;each bit represent 4 lines
2F	SenVadd	44	RW	Sensor vertical address settings. SenVadd[7:4]: RSVD SenVadd[3:2]: SenVEnd[9:8] SenVadd[1:0]: SenVSt[9:8]
30 -40			RW	RSVD
41	SenT12	A2	RW	Sensor timing control 12 SenT12[7:0]: Array SRAM shift out pixel number LSBs, in 4 pixels step.

42	SenT13	02	RW	Sensor timing control 13 SenT13[7:2]: RSVD SenT13[1:0]: Array SRAM shift out pixel number MSBs.
43	VS_POS 1	00	RW	VSYNC position LSBs: VS_POS[7:0];
44	VS_POS 2	40	RW	VS_POS2[7:4]: VSYNC width selection. VS_POS2[3:0]: VSYNC position MSBs VS_POS[11:8];
45-47			RW	RSVD
48	BLCOpt1	0F	RW	BLC control option 1 BLCopt1[7:4]: RSVD BLCopt1 [3:2]: "00": HCLK = SYS_CLK / 8 "01": HCLK = SYS_CLK / 4 "10": HCLK = SYS_CLK / 2 "11": HCLK = SYS_CLK. BLCopt1[1:0]: "00": SRAM_CLK = SYS_CLK /8 "01": SRAM_CLK = SYS_CLK /4 "10": SRAM_CLK = SYS_CLK /2 "11": SRAM_CLK = SYS_CLK
49	BLC_TG T	10	RW	Black level calibration target level. BLC_TGT[7]: sign bit."0" positive; "1" negative BLC_TGT[6:0]: target level.
4A	BLCCtrl	05	RW	BLC control BLCCtrl[7]: BLC_B bit 10 BLCCtrl[6]: BLC_Gb bit 10 BLCCtrl[5]: BLC_Gr bit 10 BLCCtrl[4]: BLC_R bit 10 BLCCtrl[3:2]: reserved BLCCtrl[1]: BLC action option. "0": Sensor do BLC only when triggered. "1": always do BLC. BLCCtrl[0]: auto BLC function on/off selection. "0": sensor stop calculate black value. "1": sensor calculates black value automatically.
4B	BLC_B	00	RW	B channel black value LSBs. BLC_B[7:0]
4C	BLC_Gb	00	RW	Gb channel black value LSBs. BLC_Gb[7:0]
4D	BLC_Gr	00	RW	Gr channel black value LSBs. BLC_Gr[7:0]
4E	BLC_R	00	RW	R channel black value LSBs. BLC_R[7:0]
4F	BLC_H	00	RW	Black value MSBs. {BLC_R[9:8],BLC_Gr[9:8],BLC_Gb[9:8],BLC_B[9:8]}
50-5E			RW	RSVD
5F	DAC_Pll 0	01	RW	DAC PLL control 0 DACPLL0[7]: DAC PLL bypass on/off selection; 1: Bypass on, 0: By pass off DACPLL0[6:4]: RSVD DACPLL0[3:2]: DAC PLL post divider bypass on/off selection; 1: Bypass on, 0: By pass off DACPLL0[1:0]: DAC PLL pre- divider DAC_CLK=input clock/(DAC PLL pre-divider + 1) * DAC PLL VCO multiplier / (DAC PLL post divider + 1)
60	DAC_Pll 1	20	RW	DAC PLL control 1 DACPLL1[7:6]: RSVD DACPLL1[5:0]:DAC PLL VCO multiplier

61 – 64			RW	RSVD
65	RAMP3	37	RW	RAMP3 [7:4]: reserved. RAMP3 [3:0]: Second stage black sun reference control. Strength: (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
66	PWC0	16	RW	PWC5[7:6]: RSVD PWC5[5:4]: D-phy Lp high voltage reference voltage control; 00- min, 11- max. PWC5[3:0]: RSVD;
67-68	RSVD		RW	RSVD
69	PWC3	BB	RW	PWC3[7:4]: RSVD; PWC3[3]: Second stage black sun switch on/off enable, "0": always off. "1": Black sun will switch to second stage when analog gain greater than Threshold RegA0[6:4]. PWC3[2:0]: RSVD;
6A	PWC4	1B	RW	Power control 4 PWC4[7:4]: reserved PWC4[3:0]: first stage black sun control. Strength: (Strong) 1,0,F,E,D,C,B,A,9,8,7,6,5,4,3,2. (Weak)
6B	DPHY1	00	RW	Mipi PHY control 1 DPHY1[7:6]: MPCKSkew[1:0] DPHY1[5:4]:HSCKSkew[1:0] DPHY1[3:2]CKSkew[1:0] Clock Lane Skew Control : 00:Min, .. 11:max. DPHY1[1:0]:D0Skew[1:0]
6C	DPHY2	40	RW	DPHY2[7]: Mipi interface power down. "0": enable;"1" normal mode DPHY2[6:5]:RSVD DPHY2[4]: Second data lane disable on/off selection "0": enable "; 1": disable; DPHY2[3:2]Pg_Vcm[1:0] D-phy Hs Tx output voltage control 01:min, 00,11,10 : max DPHY2[1:0]:D1Skew[1:0]
6D	DPHY3	02	RW	DPHY3[7:0]:RSVD
6E	DPHY4	0C	RW	DPHY3[7]: Mipi data lane 3 disable on/off selection; 1": disable; "0": enable DPHY3[6]: Mipi data lane 2 disable on/off selection; 1": disable; "0": enable DPHY3[5]: Mipi data lane 1 disable on/off selection; 1": disable; "0": enable DPHY3[4]: Mipi data lane 0 disable on/off selection; 1": disable; "0": enable DPHY3[1:0]: RSVD
6F	DPHY5	00	RW	RSVD
70	Mipi1	C9	RW	Mipi timing control 1 Mipi1[7:5]: Tlpx Mipi1[4:2]: Tck-pre Mipi1[1]: Mipi 8/10 bit mode switch, "0": 10-bit, "1": 8-bit mode Mipi1[0]: reserved
71	Mipi2	8A	RW	Mipi timing control 2 Mipi2[7:5]: Ths-zero Mipi2[4:0]: Tck-zero
72	Mipi3	C8	RW	Mipi timing control 3 Mipi3[7:5]: Ths-prepare Mipi3[4:0]: Tck-post
73	Mipi4	63	RW	Mipi timing control 4 Mipi4[7]: RSVD Mipi4[6:4]: Ths-trail Mipi4[3:0]: Tck-trail

74	Mipi5	63	RW	Mipi timing control 5 Mipi5[7:6]: Long Exp frame Virtual Channel. Mipi5[5:4]: Short Exp frame Virtual Channel. Mipi5[3]: RSVD. Mipi5[2]: Mipi byte clock revise Mipi5[1]: Mipi continues mode or strobe mode selection "1" free run; "0" Normal; Mipi5[0]: Mipi interface sleep on/off Mipi should wait a complete frame than enter sleep mode. "1" Sleep mode enable; "0" Normal;
75	Mipi6	2B	RW	Mipi data type ID;
76	Mipi7	60	RW	Mipi DataType.
77	Mipi8	09	RW	RSVD.
78	Mipi9	15	RW	Mipi timing control 9 [7:6]: MotionDetHwin option, "00":hwin, "01":hwin/2, "10/11":hwin/4 [5:3]: RSVD [2]: To MipiCtrl DVP_PCLK reverse, "1": reverse, "0": normal [1:0]: DataPath to Mipi Image Data bitwidth:"00": raw10, "01":raw8, "10/11":raw12
79-7F				RSVD
80	DigData	03	RW	DigData[7]: frame sync function enable DigData[6]: DVP data output sequence adjust DigData[5:0]: RSVD
81-85				RSVD
86	DPHY5	00	RW	DPHY5[7:6]: Mipi high speed clock input skew adjust DPHY5[5:4]: Mipi data lane 1 clock delay adjust DPHY5[3:2]: Mipi data lane 0 clock delay adjust DPHY5[1:0]: Mipi clock lane clock delay adjust
87-88				RSVD
89	Mipi10	00		Mipi timing control 10 Mipi10[7]: CK-pre-timing option 0: Auto; 1 Manual Mipi10[6:0]: Mipi TX start point adjust related to DVP HREF and internal FIFO
8A		00	RW	[7]: RSVD. [6:5] HBin: 00: No HBin; 01/10/11: 2xHBin [4:2]: RSVD. [1]: Precharge off/on, "0": normal, "1": no precharge [0]: RSVD
8B-95				RSVD
96	Gain_Ctrl	00	RW	Gain_Ctrl[7]: AutoDGain. 1: Auto Digital Gain distribution in 0x00 0: Manual set Digital Gain: 0x96[6:4] Gain_Ctrl[6:4]: DigitalGain. Gain_Ctrl[3:0]: Maximum Analog Gain.
97	FastAE0	FA	RW	FastAE_Ctrl0. [7]:RSVD [6]:weight enable. "1": enable, "0":disable. [5]:normal yavg calculate in FAE way. "1":On, "0":OFF. [4:3]: FastAE mode, "00": stop by FAE frame num; "01": stop by convg flag; "10": never stop; "11": stop @ convg or frame num. [2]:subsample control, "1": 1/16 FH, "0": 1/8 FH [1]:FastAE output control. "1": not output. "0":output.

				[0]:FastAE enable. "1":enable, "0":disable
98	FastAE1	44	RW	FastAE_Ctrl1. [7]:RSVD [6:4]:Gain limit extension value. [3:0]:FastAE Gain limit.
99	FastAE2	41	RW	FastAE_Ctrl2. [7:4]: Stable range. 0~15 [3:0]: FastAE VwinStart margin.
9A	FastAE3	40	RW	FastAE_Ctrl3. [7:4]:AGC threshold. Overflow part activates DGain. [3]:Convergence flag timing Option. "1": delay 1 frame. "0": not delay. [2]:RSVD [1:0]:FastAE stuck delay frame num, 0~3
9B ~ A3	PWC			RSVD
A4	FastAE4	60	RW	[7:0]: FastAE yavg target.
A5	FastAE5	00	RW	RSVD
A6	PHY6	00		Mipi PHY control 6 DPHY6[7:6]: D3Skew[1:0] DPHY6[5:4]: D2Skew[1:0] DPHY6[3:2]: Mipi data lane 3 clock delay adjust DPHY6[1:0]: Mipi data lane 2 clock delay adjust
A7 ~ AF				RSVD.
B0	MDT_Ctrl0	00	RW	MDT_Ctrl0. MDT_Ctrl0[7:5]: MDT Horizontal offset. MDT_Ctrl0[4:2]: MDT Vertical offset. MDT_Ctrl0[1]: MDT clock reverse, "1":rev, "0":normal MDT_Ctrl0[0]: MDT_En.
B1	MDT_Ctrl1	00	RW	MDT_Ctrl1. MDT_Ctrl1[7:0]: Motion Detect monitor threshold.
B2	MDT0	00	RO	MDT0[7:0]: Zone7~0 motion detect monitor.
B3	MDT1	00	RO	MDT1[7:0]: Zone15~8 motion detect monitor.
B4	MDT2	00	RO	MDT2[7:0]: Zone23~16 motion detect monitor.
B5	MDT3	00	RO	MDT3[7:0]: Zone31~24 motion detect monitor.
B6	MDT4	00	RO	MDT4[7:0]: Zone39~32 motion detect monitor.
B7	MDT5	00	RO	MDT5[7:0]: Zone47~40 motion detect monitor.
B8	MDT6	00	RO	MDT6[7:0]: Zone55~48 motion detect monitor.
B9	MDT7	00	RO	MDT7[7:0]: Zone63~56 motion detect monitor.
BA		00		RSVD.
BB	AZ2BLSW	19	RW	[7:4]:AZ2 to BLSW gap [3:0]:AZ1 to BLSW gap
BC		0F	RW	RSVD
BD	Mipi10	80	RW	Mipi word count LSBs

BE	Mipi11	0A	RW	Mipi word count MSBs
BF	SYSTEM	00	RW	SYSTEM[7:1]: RSVD. SYSTEM [0]: Control register Page Select.
C0	Group0	0A	RW	Group write 1st data address
C1	Group1	0A	RW	Group write 1st data value.
C2	Group2	0A	RW	Group write 2nd data address
C3	Group3	0A	RW	Group write 2nd data value.
…	…	…	…	…
FE	Group62	0A	RW	Group write 32nd data address
FF	Group63	0A	RW	Group write 32nd data value.
100	MDT_AVG0	00	RW	Zone0 average.
101	MDT_AVG1	00	RW	Zone1 average.
...	...	...	...	...
13F	MDT_AVG63	00	RW	Zone63 average.
140~1FF			RW	RSVD

Document Revision Control

Version Number #	Date Released	Comments
R0.1	May 20,2020	Initial release of JX-K04 datasheet
R1.0	Aug 01,2020	Update Key spec info, power consumption.
R1.1	Sep 28,2020	Update file format; Register default value. Order info update. JX-K04-C1-M6
R1.2	Sep 09,2021	Update description info
R1.3	Jun 06,2022	Update Key Spec info, power consumption info, Combine order info