TF Semiconductor Solutions

TF2005M

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 200V**
- **Drives two N-channel MOSFETs or IGBTs in high-side/ low-side configuration**
- **Outputs tolerant to negative transients**
- **Wide low-side gate driver and logic supply: 10V to 20V**
- **Logic inputs CMOS and TTL compatible (down to 3.3V)**
- **Schmitt triggered logic inputs with internal pull down**
- **Delay matching of 30ns maximum**
- **Source/sink pulsed current of 290mA/600mA typical**
- **Undervoltage lockout for high-side and low-side drivers**
- **Space-saving SOIC-8 package available**
- **Extended temperature range:-40°C to +125°C**

Description

The TF2005M is a mid voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/ low-side configuration. TF Semiconductor's high voltage process enables the TF2005M's high-side to switch to 200V in a bootstrap operation. The 30ns (max) propagation delay matching between the high and the low side drivers allows high frequency switching.

The TF2005M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. The low-side gate driver and logic share a common ground

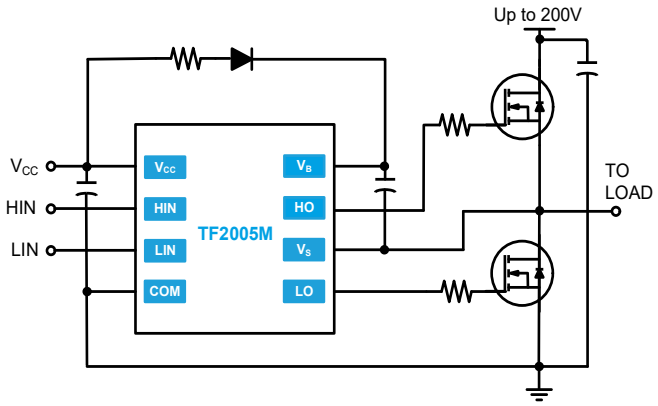
The TF2005M is available in a space-saving 8-pin SOIC package and the operating temperature extends from -40°C to +125°C .

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

SOIC-8(N)

Typical Application

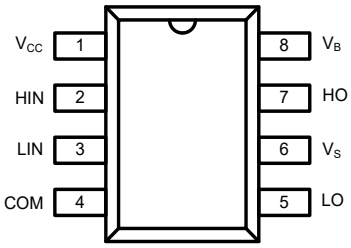


Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2005M-TAU	SOIC-8(N)	Tube / 100	YYWW TF2005M Lot ID
TF2005M-TAH	SOIC-8(N)	T & R/ 2500	YYWW TF2005M Lot ID

Pin Diagrams



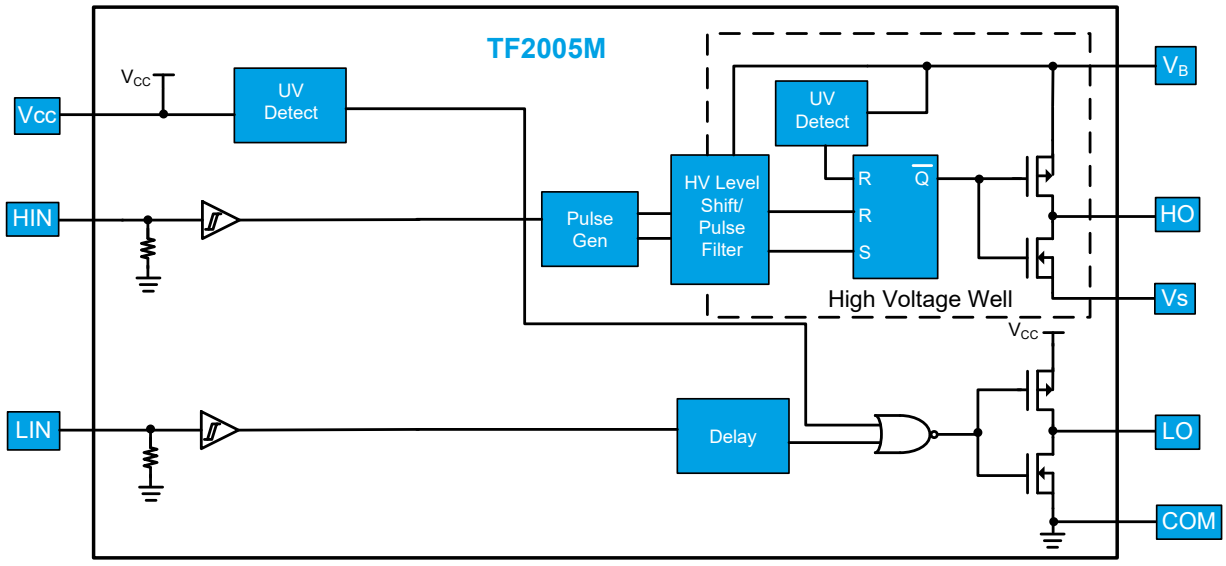
Top View: SOIC-8

TF2005M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return
NC	"No connect" pin

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +224V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10		V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***		200	V
V_{HO}	High side floating output voltage	V_S		V_B	V
V_{CC}	Low side and logic fixed supply voltage	10		20	V
V_{LO}	Low side output voltage	0		V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	0		5	V
T_A	Ambient temperature	-40		125	°C

NOTE3 *Logic operational for V_S = -5 to +200V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage		2.5			V
V_{IL}	Logic "0" input voltage				0.6	V
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	V
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	V
I_{LK}	Offset supply leakage current	VB = VS = 200V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	75	130	µA
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	60	120	180	µA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		5	20	µA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			2	µA
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.0	8.4	9.8	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		6.4	7.8	9	V
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.0	8.4	9.8	V
V_{BSUV-}	V_{CC} supply under-voltage negative going threshold		6.4	7.8	9	V
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10 µs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10 µs	270	600		mA

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C, and C_L = 1000pF, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		220	300	ns
t_{OFF}	Turn-off propagation delay	V_S = 0V or 200V		200	280	ns
t_r	Turn-on rise time			100	220	ns
t_f	Turn-off fall time	V_S = 0V		35	80	ns
t_{DM}	Delay matching				30	ns

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 440ns minimum.*

Timing Waveforms

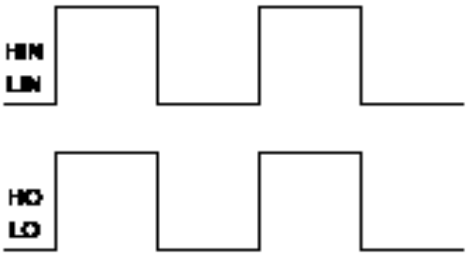


Figure 1. Input / Output Timing Diagram

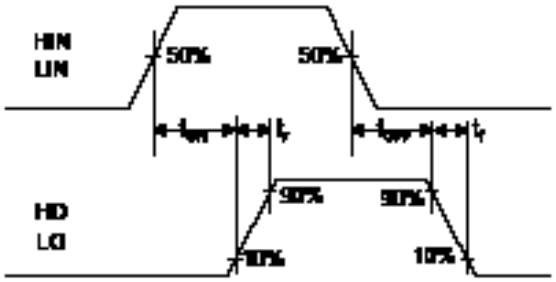


Figure 2. Switching Time Waveform Definitions

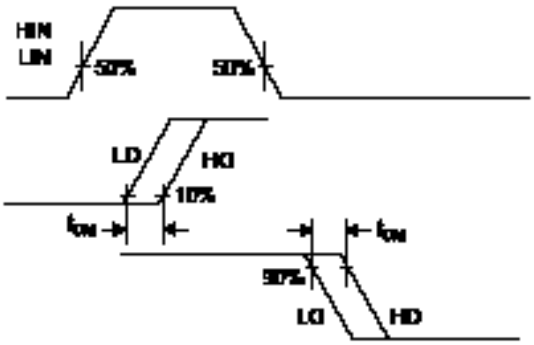


Figure 3. Delay Matching Waveform Definitions

Application Information

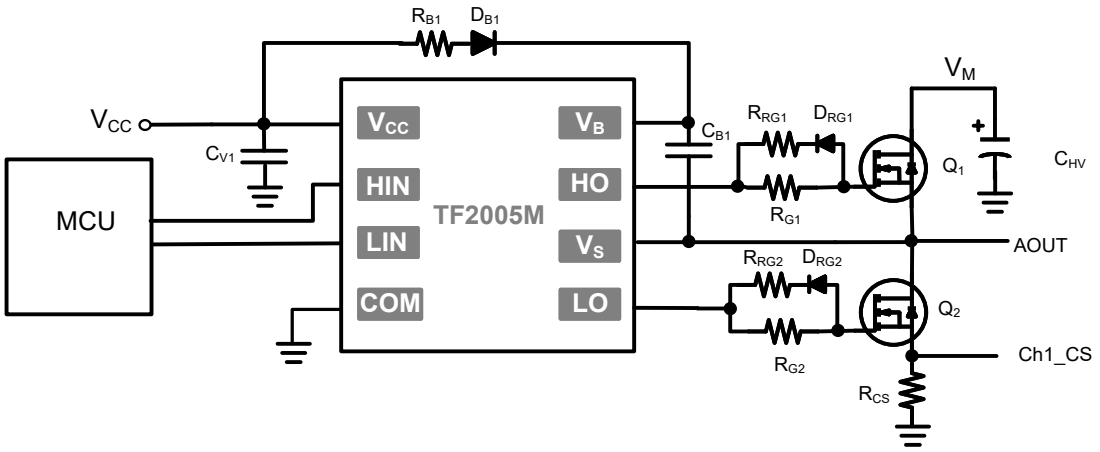


Figure 4. Single phase (of four) for Stepper motor driver application using the TF2005M

- RRG1 and RRG2 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- RG1 and RG2 values are typically between 10Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

- It is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for VDD=15V) with a minimum pulse width of 440ns.

Revision History

Rev.	Change	Owner	Date
1.0	First release, AI datasheet	Keith Spaulding	4/23/2021
1.1	Add Application Information	Keith Spaulding	8/25/2022

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