南京扬贺扬
HeYangTek

HYN1G08UKxCA1
HYN2G08UKxCC1

■ **Density**
- ❒ 1 Gb/ 2 Gb

■ **Architecture**
- ❒ Input / Output Bus Width: 8 bits
- ❒ Page Size
  - 1 Gb: (2048 + 64) bytes; 64-byte spare area
  - 2 Gb: (2048 + 128) bytes; 128-byte spare area
- ❒ Block Size: 64 Pages
  - 1 Gb: 128 KB + 4 KB
  - 2 Gb: 128 KB + 8 KB
- ❒ Plane Size
  - 1 Gb: 1024 blocks per plane or (128 MB + 4 MB)
  - 2 Gb: 1024 blocks per plane or (128 MB + 8 MB)
- ❒ Device Size
  - 1 Gb: 1 plane per device or 128 Mbyte
  - 2 Gb: 2 plane per device or 256 Mbyte

■ **NAND Flash Interface**
- ❒ Open NAND Flash Interface (ONFI) 1.0 compliant
- ❒ Address, Data, and Commands multiplexed

■ **NAND Flash Interface**
- ❒ Open NAND Flash Interface (ONFI) 1.0 compliant
- ❒ Address, Data, and Commands multiplexed

■ **Supply voltage**
- ❒ 3.3V device: V_{CC} = 2.7 V ~ 3.6 V

■ **Security**
- ❒ One Time Programmable (OTP) area
- ❒ Serial number (unique ID)
- ❒ Hardware program/erase disabled during power transition
- ❒ Volatile and Permanent Block Protection

■ **Electronic Signature**
- ❒ Manufacturer ID: 01h
- ❒ Device ID: follow industry standard for single and stacked die implementation

■ **Operating Temperature**
- ❒ Industrial: –40°C to 85°C

■ **Additional Features**
- ❒ Copy Back Program (HYN2Gb)
- ❒ Reset (FFh) command is required after power-on as a first command

Performance

■ **Page Read / Program**
- ❒ Read Page Time (t_R):
  - 45 µs (Typ) / Single Plane
  - 55 µs (Typ) / Multi Plane
- ❒ Program time / Multiplane Program time: 350 µs (Typ)

■ **Block Erase / Multiplane Erase**
- ❒ Block Erase time: 4 ms (Typ)

■ **Reliability**
- ❒ 80,000 Program/Erase cycles (Typ)
- ❒ 10 Year Data retention (Typ)
- ❒ Blocks 0-7 are good at the time of shipment

■ **Package Options**
- ❒ Pb-free and low halogen
- ❒ 48-Pin TSOP 12 × 20 × 1.2 mm
- ❒ 63-BALL BGA 9 × 11 × 0.8 mm

1. General Description

The HYN1G08UKTCA1 and HYN2G08UKTCC1 are offered with a 3.3V VCC power supply, and a x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. The page size for x8 is (2048 + spare) bytes.

To protect the system bus from transmission errors, the implementation of a 1 bit ECC is recommended.
The on-die ECC is designed to make HYN1G08UKTCA1/ HYN2G08UKTCC1 backward compatible with existing nodes and will work with application processors with existing 1 bit, 4 bit or 8 bit ECC engine.

The chip supports CE# don't care function. This function allows the direct download of the code from the NAND flash memory device by a micro controller, because the CE# transitions do not stop the read operation.

Like all other 2-KB page NAND flash devices, a program operation typically writes 2 KB in 350 µs and an erase operation can typically be performed in 4.0 ms on a 128-KB block.

In the Read operations, data in the page can be read out at 20ns cycle time per byte. The I/O pins serve as the ports for command and address input as well as data input/output. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of the footprint.

Commands, Data, and Addresses are asynchronously introduced using CE#, WE#, ALE, and CLE control pins.

The on-chip Program/Erase Controller automates all read, program, and erase functions including pulse repetition, where required, and internal verification and margining of data. A WP# pin is available to provide hardware protection against program and erase operations.

The output pin R/B# (open drain buffer) signals the status of the device during each operation. It identifies if the program/erase/read controller is currently active. The use of an open-drain output allows the Ready/Busy pins from several memories to connect to a single pull-up resistor. In a system with multiple memories the
R/B# pins can be connected all together to provide a global status signal.

The Reprogram function allows the optimization of defective block management — when a Page Program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The VPE input pin (Volatile Protection Enable) provides block granularity hardware protection against undesired data modification (program/erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.

The devices provide an innovative feature: Page Reprogram. The Page Reprogram re-programs one page. Normally, this operation is performed after a failed Page Program operation.

The device is available in the TSOP48 (12 x 20 mm) &63ball BGA(9 x 11 mm) packages and come with the following security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely identified.
- Volatile and Permanent Block Protection

Table 1. Product List

Device	Density (bits)		Number of Planes	Number of Blocks per Plane	Package
	Main	Spare			
HYN1G08UKTCA1	128M x 8	4M x 8	1	1024	TSOP48
HYN1G08UKFCA1					BGA63
HYN2G08UKTCC1	128M x 8	8M x 8	2	1024	TSOP48
HYN2G08UKFCC1					BGA63

1.1 Logic Diagram

Figure 1. Logic Diagram

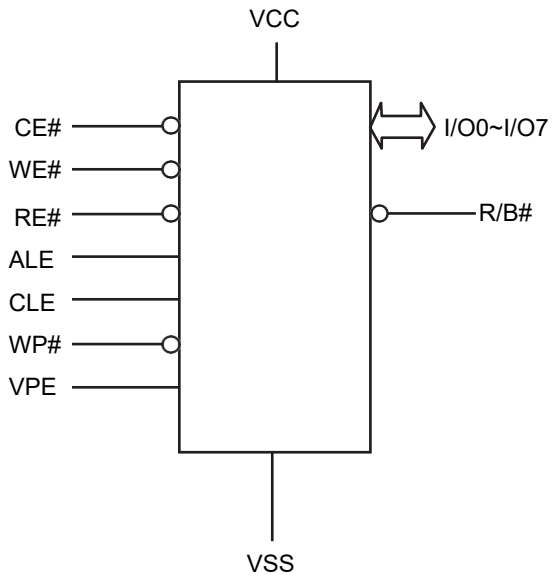
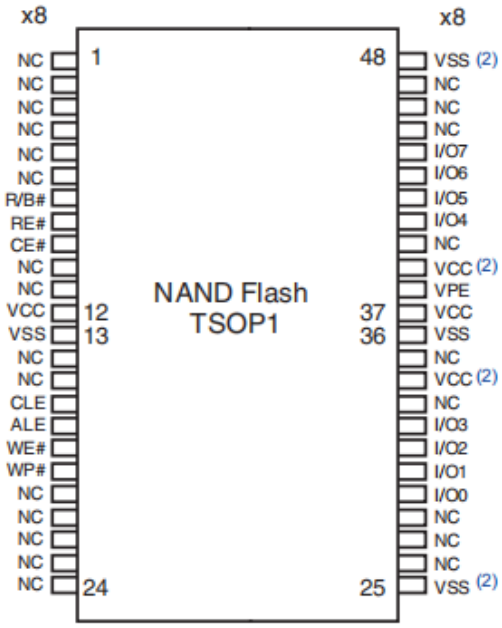


Table 2. Signal Names

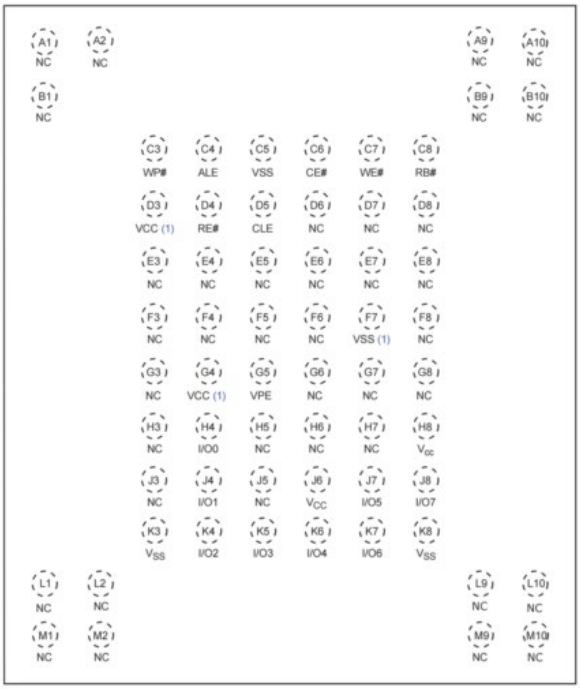
I/O7 - I/O0 (×8)	Data Input / Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
R/B#	Read/Busy
VPE	Volatile Protection Enable
VCC	Power Supply
VSS	Ground
NC	Not Connected

1.2 Connection Diagram

Figure 2. 48-Pin TSOP1 Contact ×8



63-ball BGA Contact ×8



Notes
1. These pins should be connected to power supply or ground (as designated) following the ONFI specification, however they might not be bonded internally.
2. These pins should be connected to power supply or ground (as designated) following the ONFI specification, however they might not be bonded internally.

1.3 Pin Description

Table 3. Pin Descrip Pin Nametion[3, 4] Description

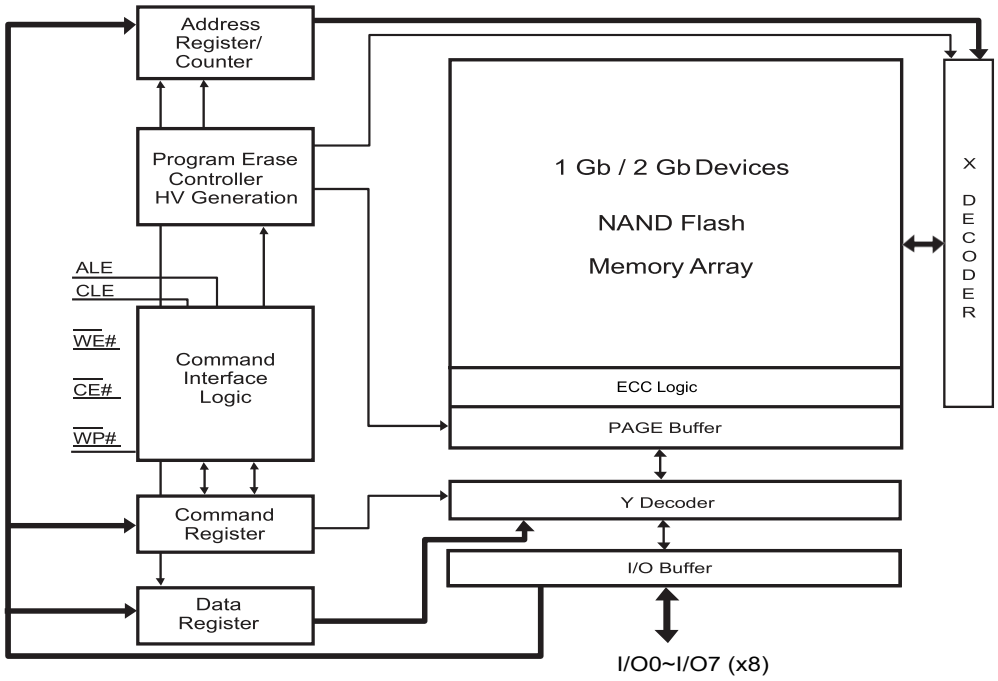
Pin Name	Description
I/O0 - I/O7 **(×8)**	**Inputs/Outputs**. The I/O pins are used for command input, address input, data input, and data output. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**Command Latch Enable.** This input activates the latching of the I/O inputs inside the Command Register on the rising edge of Write Enable (WE#).
ALE	**Address Latch Enable.** This input activates the latching of the I/O inputs inside the Address Register on the rising edge of Write Enable (WE#).
CE#	**Chip Enable.** This input controls the selection of the device. When the device is not busy CE# low selects the memory.
WE#	**Write Enable.** This input latches Command, Address and Data. The I/O inputs are latched on the rising edge of WE#.
RE#	**Read Enable.** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WP#	**Write Protect.** The WP# pin, when low, provides hardware protection against undesired data modification (program / erase).
R/B#	**Ready Busy**. The Ready/Busy output is an Open Drain pin that signals the state of the memory.
VPE	**Volatile Protection Enable.** The Volatile Protection Enable input, when high during power-on, provides block granularity hardware protection against undesired data modification (program/erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.
VCC	**Supply Voltage**. The V_{CC} supplies the power for all the operations (Read, Program, Erase). An internal lock circuit prevents the insertion of Commands when V_{CC} is less than V_{LKO}.
VSS	**Ground.**
NC	**Not Connected.**

Notes

3. A 0.1 µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.
4. An internal voltage detector disables all functions whenever V_{CC} is below 1.8 V to protect the device from any involuntary program/erase during power transitions.

1.4 Block Diagram

Figure 3. Functional Block Diagram



1.5 Array Organization

Figure 4. Array Organization — HYN1Gb(Default)

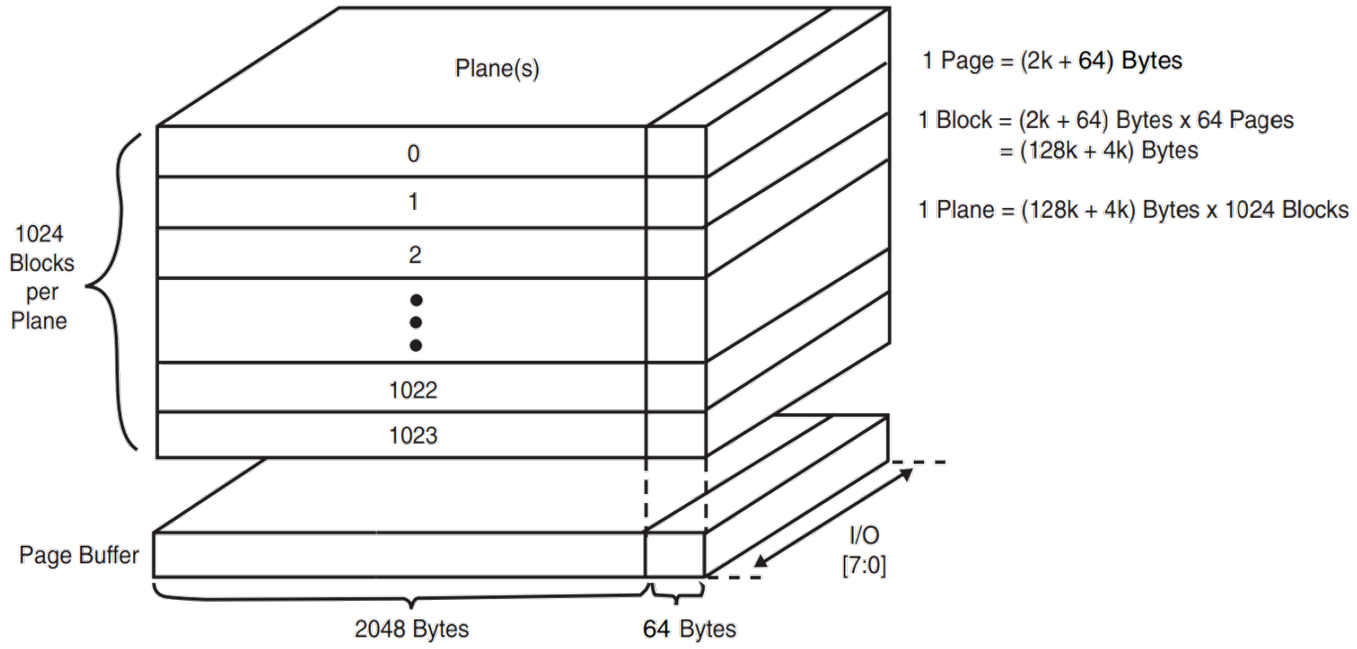
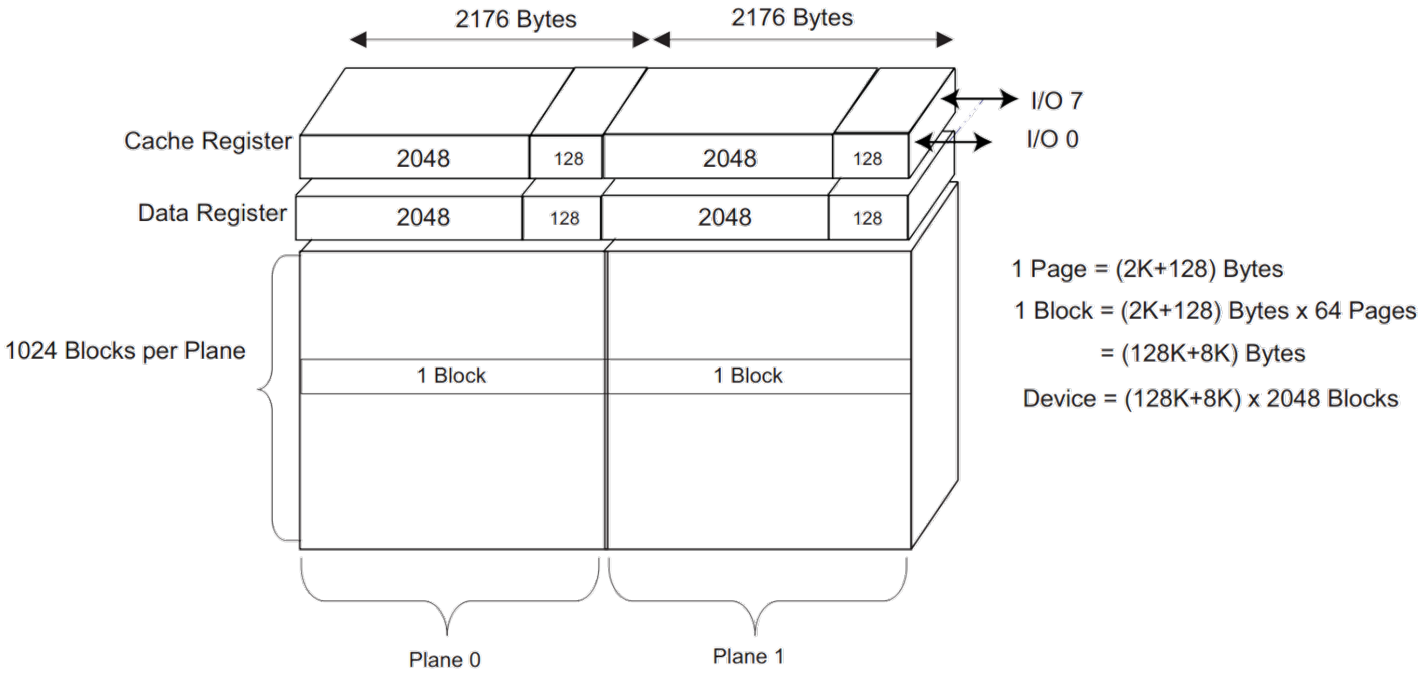


Figure 5. Array Organization — HYN2Gb



1.6 Addressing

1.6.1 Memory Address Phase Cycles

Table 4 provides the memory organization and the address bit requirements for each devices supported.

Table 4. Memory Array Organization and Address Bit Requirements

Density Page Size	Device and Array Organization											Address bits
	Page Size	LUN	Planes	#block per Plane	Page per Block	Spare Byte per Page	Spare Byte per NOP	NOP	Partial Word Size	CA Bits	PA Bits	BA Bits
HYN1Gb	2KB	1	1	1024	64	64	16 (Def.)	4	512B	12	6	10
HYN2Gb	2KB	1	2	1024	64	128	32 (Def)	4	512B	12	6	11

Table 5 provides the address phase cycles for the X8 mode of operation.

Table 5-1. Address Phase Cycles for X8 Mode of Operation -HYN1Gb

Bus Cycle	Name	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
1st	Col Add 1 (C1)	CA[7]	CA[6]	CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]
2nd	Col Add 2 (C2)	L	L	L	L	CA[11]	CA[10]	CA[9]	CA[8]
3rd	Row Add 1 (R1)	BA[1]	BA[0]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
4th	Row Add 2 (R2)	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]

Table 5-2. Address Phase Cycles for X8 Mode of Operation -HYN2Gb

Bus Cycle	Name	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
1st	Col Add 1 (C1)	CA[7]	CA[6]	CA[5]	CA[4]	CA[3]	CA[2]	CA[1]	CA[0]
2nd	Col Add 2 (C2)	L	L	L	L	CA[11]	CA[10]	CA[9]	CA[8]
3rd	Row Add 1 (R1)	BA[1]	BA[0]	PA[5]	PA[4]	PA[3]	PA[2]	PA[1]	PA[0]
4th	Row Add 2 (R2)	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
5th	Row Add 3 (R3)	L	L	L	L	L	L	L	BA[10]

Note

5. Block address concatenated with page address = actual page address, also known as the row address.

Legend:

CAx = Column Address bit.

PAx = Page Address bit.

BAx = Block Address bit.

1.7 Mode Selection

Table 6. Mode Selection[7]

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read Mode	Command Input	High	Low	Low	Rising	High	X
	Address Input	Low	High	Low	Rising	High	X
Program or Erase Mode	Command Input	High	Low	Low	Rising	High	High
	Address Input	Low	High	Low	Rising	High	High
Data Input		Low	Low	Low	Rising	High	High
Data Output (on going)		Low	Low	Low	High	Falling	X
Data Output (suspended)		X	X	X	High	High	X
Busy Time in Read		X	X	X	High	High[9]	X
Busy Time in Program		X	X	X	X	X	High
Busy Time in Erase		X	X	X	X	X	High
Write Protect		X	X	X	X	X	Low
Stand By		X	X	High	X	X	0V / V_{CC}[8]

Notes
6. X can be V_{IL} or V_{IH}. High = Logic level high, Low = Logic level low.
7. WP# should be biased to CMOS high or CMOS low for stand-by mode.
8. During Busy Time in Read, RE# must be held high to prevent unintended data out.

2. Bus Operation

There are six standard bus operations that control the device: Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby (see Table 6).

Typically glitches less than 5ns on Chip Enable, Write Enable, and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

The Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable high, Address Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (program/erase) the Write Protect pin must be high. See Figure 17 and Table 29 for details of the timing requirements.

2.2 Address Input

The Address Input bus operation allows the insertion of the memory address. For the HYN2Gb device, five write cycles are needed to nput the addresses. For the HYN1Gb, four write cycles are needed to input the addresses. If necessary, a 5th dummy address cycle can be issued to HYN1Gb, which will be ignored by the NAND device without causing problems.Addresses are accepted with Chip Enable low, Address Latch Enable high, Command Latch Enable low, and Read Enable high and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation(program/erase) the Write Protect pin must be high. See Figure 18 and Table 29 for details of the timing requirements.

2.3 Data Input

The Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serial and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable high, and Write Protect high and latched on the rising edge of Write Enable. See Figure 19 and Table 29 for details of the timing requirements.

2.4 Data Output

The Data Output bus operation allows data to be read from the memory array and to check the Status Register content, and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable high, Address Latch Enable low, and Command Latch Enable low. See Figure 20 and Table 29 for details of the timings requirements.

2.5 Write Protect

The Hardware Write Protection is activated when the Write Protect pin is low. In this condition, modify operations do not start and the content of the memory is not altered. The Write Protect pin is not latched by Write Enable to ensure the protection even during power up.

2.6 Standby

In Standby, the device is deselected, outputs are disabled, and power consumption is reduced.

3. Command Set

Table 7. Command Set

Command	CMD Cycle #1	# of Valid Addr. Cycles	Data Input Cycles	CMD Cycle #2	CMD Cycle #3	CMD Cycle #4	Valid While Selected LUN is Busy	Valid While Other LUNs is Busy	Notes
RESET	FFh	0					Yes	Yes	
READ ID	90h	1					No	Yes	
READ ONFI SIGNATURE	90h	1					No	Yes	
READ PARAMETER PAGE	ECh	1					No	No	
READ UNIQUE ID	EDh	1					No	No	
GET FEATURES	EEh	1					No	No	
SET FEATURES	EFh	1	4				No	No	
READ STATUS REGISTER	70h	0					Yes	Yes	
READ STATUS ENHANCED	78h	3					Yes	Yes	
RANDOM DATA OUTPUT	05h	2		E0h			No	Yes	
RANDOM DATA INPUT	85h	2	Optional				No	Yes	
READ MODE	00h	0					No	Yes	
PAGE READ	00h	5		30h			No	Yes	
PAGE PROGRAM	80h	5	Yes	10h			No	Yes	
BLOCK ERASE	60h	3		D0h			No	Yes	
COPY BACK READ	00h	5		35h			No	Yes	[10.1]
COPY BACK PROGRAM	85h	5	Optional	10h			No	Yes	[10.1]
LEGACY OTP AREA ENTRY	29h-17h-04h-19h		No				No	No	
LEGACY OTP PROTECTION	4Ch-03h-1Dh-41h-80h	5(00h,00h, 00h, 00h,00h)	Yes	10h			No	No	[10]
PAGE REPROGRAM	8Bh	5	Yes	10h			No	Yes	[10.1]
MULTIPLANE PAGE REPROGRAM	8Bh		Yes	11h	8Bh	10h	No	No	[10.1]
MULTIPLANE BLOCK ERASE	60h	3		60h	D0h		No	No	[10.1]
ONFI MULTIPLANE BLOCK ERASE	60h	3		D1h	60h	D0h	No	No	[10.1]
MULTIPLANE COPY BACK PROGRAM	85h	5		11h	81h	10h	No	No	[10.1]
ONFI MULTIPLANE COPY BACK PROGRAM	85h	5		11h	85h	10h	No	No	[10.1]
Block Lock Operations for Volatile Block Protection									
VOLATILE LOCK ALL	2Ah						No	Yes	
BLOCK UNLOCK UPPER	24h	3					No	Yes	
BLOCK UNLOCK LOWER	23h	3					No	Yes	
LOCK DOWN COMMAND	2Ch						No	Yes	
BLOCK PROTECTION STATUS	7Ah	3					No	Yes	
Block Lock Operations for Permanent Block Protection									
PROGRAM PBP SETTINGS	4Ch-03h-1Dh-41h-80h	5(00h,00h,00h, 0Yh,00h)		10h			No	No	[10]
PBP LOCK DOWN	4Ch-03h-1Dh-41h-80h	5(00h,00h,00h, 1Yh,00h)		10h			No	No	[10]

Note

9. If the device is in OTP mode, the OTP protection setup command is locking the OTP and not permanently protecting block group 0. Vice-versa, If the device is not in OTP mode, the OTP protection setup command is not1 locking the OTP but is permanently protecting block group 0. See Section 4.2. Permanent Block Protection (PBP) Overview.

9.1 Supported for HYN2G08UKTCC1 device only

3.1 Page Read

Page Read is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read and serial page read. Random read mode is enabled when the page address is changed. All data within the selected page are transferred to the data registers. The system controller may detect the completion of this data transfer (tR) by analyzing the output of the R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25 ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# signal makes the device output the data, starting from the selected column address up to the last column address.

The device may output random data in a page instead of the sequential data by writing Random Data Output command. The column address of next data, which is going to be out, may be changed to the address that follows Random Data Output command. Random Data Output can be performed as many times as needed.

3.2 Page Program

A page program cycle consists of a serial data loading period in which up to 2 kB (x8) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports Random Data Input within a page. The column address of next data, which will be entered, may be changed to the address that follows the Random Data Input command (85h). Random Data Input may be performed as many times as needed.

The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks.

Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O0) may be checked. The internal write verify detects only errors for 1's that are not successfully programmed to 0's. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 26 and Figure 29 detail the sequence.

The device is programmable by page, but it also allows multiple partial page programming of a word or consecutive bytes up to 2 kB (x8) in a single page program cycle.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in table 33. Both main data and user spare will be input at the same time for NOP operation; otherwise, data is not guaranteed.

If a Page Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.3 Multiplane Program (HYN2Gb)

The HYN2Gb devices support Multiplane Program, making it possible to program two pages in parallel, one page per plane.

A Multiplane Program cycle consists of a double serial data loading period in which up to 4352 bytes (×8) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. The address for this page must be in the 1st plane (BA[0]=0). The device supports Random Data Input exactly the same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (t_{DBSY}). Once it has become ready again, the '81h' command must be issued, followed by 2nd page address (5 cycles) and its serial data input. The address for this page must be in the 2nd plane (BA[0]=1). The Program Confirm command (10h) starts parallel programming of both pages.

Figure 31 describes the sequences using the legacy protocol. In this case, the block address bits for both planes are the same except for the bit(s) that select the plane. Figure 31-2 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (t_{DBSY}). In case of failure in either page program, the fail bit of the Status Register will be set. Refer to Section 3.9. Read Status Register for further info.

The number of consecutive partial page programming operations (NOP) within the same page must not exceed the number indicated in table 33. Pages may be programmed in any order within a block.

If a Multiplane Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.4 Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only the block address bits are valid while the page address bits are ignored.

The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by the execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the Status Register.

The system controller can detect the completion of an erase by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O0) may be checked. Figure 32 details the sequence.

If a Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted block is erased under continuous power conditions before that block can be trusted for further programming and reading operations.

3.5 Multiplane Block Erase (HYN2Gb)

Multiplane Block Erase allows the erase of two blocks in parallel, one block per memory plane.

The Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See table 33 for performance information.

For the Multiplane Block Erase operation, the address of the first block must be within the first plane (BA[0] = 0) and the address of the second block in the second plane (BA[0] = 1). See Figure 33 for a description of the legacy protocol. In this case, the block address bits for both planes are the same except for the bit(s) that select the plane. Figure 35 describes the sequences using the ONFI protocol. For both addresses issued in this protocol, the block address bits must be the same except for the bit(s) that select the plane.

The user can check operation status by monitoring R/B# pin or reading the Status Register (command 70h or 78h). The Read Status Register command is also available during Dummy Busy time (t_{DBSY}). In case of failure in either erase, the fail bit of the Status Register will be set.

If a Multiplane Block Erase operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted blocks are erased under continuous power conditions before those blocks can be trusted for further programming and reading operations.

3.6 Copy Back Program (HYN2Gb)

The copy back feature supported by HYN2Gb is intended to quickly and efficiently rewrite data stored in one page without utilizing an external memory.Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is greatly improved.The benefit is especially obvious when a portion of a block needs to be updated and the rest of the block also needs to be copied to the newly assigned free block. The operation for performing a copy back is a sequential execution of page-read (without mandatory serial access) and Copy Back Program with the address of destination page. A read operation with the ‘35h’ command and the address of the source page moves the whole page of data into the internal data register. Because of the sub plane structure of the device, copy-back read requires additional read time of 30μs for Multi-Plane

operation and 15µs for 2KB Page-single Plane. As soon as the device returns to the Ready state, optional data read-out is allowed by toggling RE# (see Figure 36), or the Copy Back Program command (85h) with the address cycles of the destination page may be written. The Program Confirm command (10h) is required to actually begin programming.

The source and the destination pages in the Copy Back Program sequence must belong to the same device plane (same BA[0] for HYN2Gb). Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (t_{PROG}) specification.

The data input cycle for modifying a portion or multiple distinct portions of the source page is allowed as shown in Figure 37.

If a Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted page is not used for further reading or programming operations until the next uninterrupted block erase is complete.

3.6.1 Multiplane Copy Back Program (HYN2Gb)

The device supports Multiplane Copy Back Program with exactly the same sequence and limitations as the Page Program. Multiplane Copy Back Program must be preceded by two single page Copy Back Read command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).

Multiplane Copy Back cannot cross plane boundaries — the contents of the source page of one device plane can be copied only to a destination page of the same plane.

The Multiplane Copy Back Program sequence represented in Figure 38 shows the legacy protocol. In this case, the block address bits select the respective blocks for each plane. Figure 39 describes the sequence using the ONFI protocol.

If a Multiplane Copy Back Program operation is interrupted by hardware reset, power failure or other means, the host must ensure that the interrupted pages are not used for further reading or programming operations until the next uninterrupted block erases are complete for the applicable blocks.

3.7 Read Status Register

The Status Register is used to retrieve the status value for the last operation issued. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired.

If the Read Status Register command is issued during multiplane operations then Status Register polling will return the combined status value related to the outcome of the operation in the two planes according to the following table.

Status Register Bit	Composite Status Value
Bit 0, Pass/Fail	OR

In other words, the Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

The command register remains in Status Read mode until further commands are issued. Therefore, if the Status Register is read during a random read cycle, the read command (00h) must be issued before starting read cycles.

The Read Status Register command should not be used for concurrent operations in multi-die stack configurations (single CE#). “Read Status Enhanced” must be used instead.

Using the READ STATUS (70h) command for interleaved operations will result in bus contention since the status will be reported by more than one die simultaneously.

3.8 Read Status Enhanced - HYN2Gb

Read Status Enhanced is used to retrieve the status value for a previous operation in the specified plane.

Figure 41 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence to retrieve the status of the die and the plane of interest.

The command register remains in Status Read mode until further commands are issued. The Status Register is dynamic; the user is not required to toggle RE# / CE# to update it.

3.9 Read Status Register Field Definition

Table 8 below lists the meaning of each bit of the Read Status Register and Read Status Enhanced.

Table 8. Read Status Register

SR Bit	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
0[10, 11]	Pass: “0” Fail: “1”	Pass / Fail	Pass / Fail	Not Used	Pass/Fail
1	Reserved	Not Used	Not Used	Not Used	Not Used
2	Reserved	Not Used	Not Used	Not Used	Not Used
3[12]	OTP Not Protected: “0” OTP Protected: “1”	Not Used	Not Used	Not Used	Not Protected/ Protected
4[13]	1: (Flag 1*) Page Recommended to Rewrite 1: (Flag 2) Page Uncorrectable 0: Normal mode	Not Used	Not Used	Flag 1 (default) or Flag 2	Not Used
5[14]	Busy: “0” Ready: “1”	Not Used	Program in progress/ Completed	Not Used	Not Used
6	Busy: “0” Ready: “1”	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
7[15]	Protected: “0” Not Protected: “1”	Write Protect	Write Protect	Write Protect	Write Protect

Notes

10. SR[0] value is 0 when power-up with VPE=L, else don’t care; SR[0] value is a don’t care after read operation.
11. Bit 0: This bit is only valid for Program and Erase operations. If cleared to zero, then the last command was successful. If set to one, then the last command failed.
12. Bit 3: This bit indicates whether the OTP is lock down, and should be cleared to zero, when not in OTP mode, or FF command is issued, or on power up. This bit should be set to one after lock down command is issued, or when OTP operation (program/erase/erase) command is issued and OTP is lock down.
13. Bit 4: This bit indicates if the last page read contained a high number of ECC errors.
    - The Flag 1(default) or Flag 2 mode, is selectable using the Set Feature command (see Table 17 on page 24).
    - Flag 1 mode: When set to 1, this bit[4] indicates that the page read had a high ECC error count. When such situation occurs, the user is recommended to re-program the page read.
    - Flag 2 mode: When set to one, this bit[4] indicates that the page read had more ECC errors than the internal ECC engine could correct.
14. Bit 5: If set to one then there is no array operation in progress. If cleared to zero, then there is a command being progressed.
15. Bit 7: If set to one, then the device is not write protected. If cleared to zero, then the device is write protected. This bit will always be valid regardless of state of the R/B#. For Status Enhanced command, signal follows WP pin and also indicate protection of the block specified in the 78h command address field.

3.10 Reset

The Reset feature is executed by writing FFh to the command register. If the device is in the Busy state during random read, program, or erase mode, the Reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data may be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high or value 60h when WP# is low. If the device is already in reset state a new Reset command will not be accepted by the command register. The R/B# pin transitions to low for t_{RST} after the Reset command is written. Refer to Figure 42 for further details.

Reset (FFh) command is required after power-on as a first command and must be issued to all CE#s.

3.11 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Note: If you want to execute Read Status command (0x70) after Read ID sequence, you should input dummy command (0x00) before Read Status command (0x70).

For the HYN2Gb device, five read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. For the HYN1Gb device, four read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, and 4th cycle ID, respectively.
The command register remains in Read ID mode until further commands are issued to it. Figure 43 shows the operation sequence, while Table 9 to Table 13 explain the byte meaning.

Table 9. Read ID for Supported Configurations

Density	Spare Area	V_{CC}	1st	2nd	3rd	4th	5th
1 Gb	64 Bytes	3.3V	01h	F1h	00h	1Dh	-
2 Gb	128 Bytes	3.3V	01h	DAh	00h	95h	46h

Table 10. Read ID Bytes

Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type
4th	Page Size, Block Size, Spare Size, Organization
5th	Plane Number

3rd ID Data

Table 11. Read ID Byte 3 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell type	2-level cell 4-level cell 8-level cell 16-level cell				0 0 0 1 1 0 1 1	
Reserved	0	0	0	0		

4th ID Data

Table 12. Read ID Byte 4 Description

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (without spare area)	2 KB 4 KB						0 1 1 0
Block Size (without spare area)	128 KB 256 KB	0 0		0 1 1 0			
Spare Area Size Byte / 512 bytes	16B 32B					0 1	
Reserved	Reserved Reserved Reserved Reserved	0 1 0 1			0 0 1 1		
Organization	×8		0				

5th ID Data

Table 13. Read ID Byte 5 Description — HYN2Gb

	Description	I/O7	I/O6 I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
ECC Level [1]	1 bit / 512 bytes 2 bits / 512 bytes 4 bits / 512 bytes 8 bits / 512 bytes				0 0 0 1 1 0 1 1
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1	
Plane Size (Without Spare Area)	64 Mb 128 Mb 256 Mb 512 Mb 1 Gb 2 Gb 4 Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0		
Reserved		0			

1. The ECC requirement for this on-die ECC device family is 0 bit (1 bit recommended). It is designed to make it backward compatible with existing nodes (4X-nm/3X-nm) and will work with application processors that have 1-bit, 4 bits, or 8 bits ECC engine.

3.12 Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h is entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 44 shows the operation sequence.

3.13 Read Parameter Page

The device supports the ONFI Read Parameter Page operation, initiated by writing ECh to the command register, followed by an address input of 00h. The host may monitor the R/B# pin or wait for the maximum data transfer time (t_R) before reading the Parameter Page data. The command register remains in Parameter Page mode until further commands are issued to it. If the Status Register is read to determine when the data is ready, the Read Command (00h) must be issued before starting read cycles. Figure 45 shows the operation sequence, while Table 14 explains the parameter fields.

Table Paramete Page Description

Byte	O/M	Description	Values
Revision Information and Features Block			
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh, 4Eh, 46h, 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h, 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	HYN1Gb: 10h, 00h HYN2Gb: 18h, 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command	HYN1Gb: 34h, 00h HYN2Gb: 3Ch, 00h
10-31		Reserved (0)	00h
Manufacturer Information Block			
32-43	M	Device manufacturer (12 ASCII characters)	53h, 50h, 41h, 4Eh, 53h, 49h, 4Fh, 4Eh, 20h, 20h, 20h, 20h
44-63	M	Device model (20 ASCII characters)	HYN1Gb: 53h, 33h, 34h,4Dh, 4Ch, 30h,31h, 47h, 33h,20h, 20h, 20h,20h, 20h, 20h,20h, 20h, 20h,20h, 20h HYN2Gb: 53h, 33h, 34h,4Dh, 4Ch, 30h,32h, 47h, 33h,20h, 20h, 20h,20h, 20h, 20h,20h, 20h, 20h,20h, 20h
64	M	JEDEC manufacturer ID	01h
65-66	O	Date code	00h
67-79		Reserved (0)	00h
Memory Organization Block			
80-83	M	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	M	Number of spare bytes per page	HYN1Gb: 40h, 00h HYN2Gb: 80h, 00h
86-89	M	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	M	Number of spare bytes per partial page	HYN1Gb: 10h, 00h HYN2Gb: 20h, 00h
92-95	M	Number of pages per block	40h, 00h, 00h, 00h

Table Paramete Page Description (Continued)

Byte	O/M	Description	Values
96-99	M	Number of blocks per logical unit (LUN)	HYN1Gb: 00h, 04h, 00h,00h HYN2Gb: 00h, 08h, 00h,00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	HYN1Gb: 22h HYN2Gb: 23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	HYN1Gb: 14h, 00h HYN2Gb: 28h, 00h
105-106	M	Block endurance	08h, 04h (–40°C to 85°C)
107	M	Guaranteed valid blocks at beginning of target	08h
108-109	M	Block endurance for guaranteed valid blocks	00h, 00h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	00h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	HYN1Gb: 00h HYN2Gb: 01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00h
115-127		Reserved (0)	00h
Electrical Parameters Block			
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, should be 1	3Fh, 00h
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	00h, 00h
133-134	M	t_{PROG} Maximum page program time (µs)	58h, 02h
135-136	M	t_{BERS} Maximum block erase time (µs)	10h, 27h
137-138	M	t_R Maximum page read time (µs)	HYN1Gb:FAh, 00h HYN2Gb:C2h, 01h

Table Paramete Page Description (Continued)

Byte	O/M	Description	Values
139-140	M	t_{CCS} Minimum Change Column setup time (ns)	C8h, 00h
141-163		Reserved (0)	00h
Vendor Block			
164-253	M	Vendor specific	00h
254-255	M	Integrity CRC	HYN1Gb: 85h, 89h HYN2Gb: 05h, 48h
Redundant Parameter Pages			
256-511	M	Value of bytes 0-255	Repeat Value of bytes 0-255
512-767	M	Value of bytes 0-255	Repeat Value of bytes 0-255
768+	O	Additional redundant parameter pages	FFh

Note
16. O" Stands for Optional, "M" for Mandatory.

3.14 Read Unique ID

The device supports the ONFI Read Unique ID function, initiated by writing EDh to the command register, followed by an address input of 00h. The host must monitor the R/B# pin or wait for the maximum data transfer time (t_R) before reading the Unique ID data. The first sixteen bytes returned by the flash is a unique value. The next sixteen bytes returned are the bit-wise complement of the unique value. The host can verify the Unique ID was read correctly by performing an XOR of the two values. The result should be all ones. The command register remains in Unique ID mode until further commands are issued to it. Figure 46 shows the operation sequence, while Table 15 shows the Unique ID data contents.

Table 15. Unique ID Data Description

Byte	Description
0-15	Unique ID
16-31	ID Complement
32-47	ID Complement
48-63	Unique ID
64-79	Unique ID
80-95	ID Complement
96-111	ID Complement
112-127	Unique ID
⋮	⋮
n*64-(n*64+15)	Unique ID
(n*64+16)-(n*64+31)	ID Complement
(n*64+32)-(n*64+47)	ID Complement
(n*64+48)-(n*64+63)	Unique ID
⋮	⋮
448-463	Unique ID
464-479	ID Complement
480-495	ID Complement
496-511	Unique ID

3.15 One-Time Programmable (OTP)

The device contains a one-time programmable (OTP) area, that consists of one block (64 pages), which is accessed in two different ways:

1. Legacy vendor command method
2. SET FEATURE method

3.15.1 OTP Access

Legacy Vendor Method: The OTP area is located in block #6.

The OTP entry/program/read sequences are as follows:

Entry: 29h - 17h - 04h - 19h

Program: 80h - 00h - 00h - 80h - 01h - 00h - 10h

Read: 00h - 00h - 00h - 80h - 01h - 00h - 30h

SET FEATURE Method: Issue SET FEATURE (EFh) command followed by feature address 90h and the data

P1 = 09h, P2 = 00h, P3 = 00h, and P4 = 00h (See “SET FEATURES, GET FEATURES ONFI Commands” Section for more details on P1/P2/P3/P4 definition)

Once in OTP mode, all subsequent Page Read and Page Program commands are applied to the OTP area. ERASE commands are not valid in OTP mode.

Copyback and Reprogram commands shown in the commands Set are not supported in OTP mode.

3.15.2 OTP Protection

Legacy Vendor Method: Issue OTP protection vendor command sequence 4Ch-03h-1Dh-41h-80h followed by an address of 00h/00h/00h/00h/00h and 10h command.

SET FEATURE Method: Issue SET FEATURE (EFh) command followed by feature address 90h and the data

P1 = 0Bh, P2 = 00h, P3 = 00h, and P4 = 00h.

The status register read command can be used to poll the status register to determine when the programming operation is completed and verify that the OTP area is protected.

The OTP protection sequences described above assume the device is in OTP mode.

3.15.3 OTP Exit

Legacy Vendor Method: Issue the Reset (FFh) command to exit the OTP mode

SET FEATURE Method: Issue SET FEATURE (EFh) command with feature address 90h and the data

P1 = 08h, P2 = 00h, P3 = 00h, and P4 = 00h

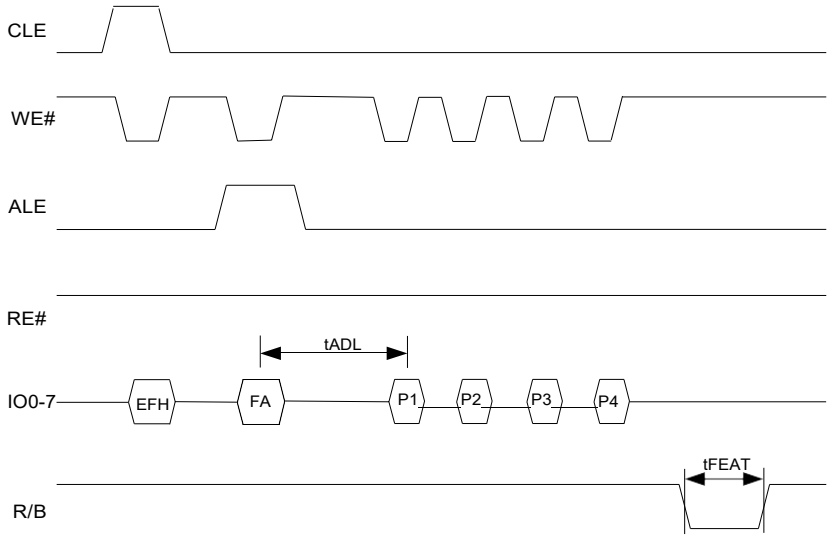
The OTP area is of a single erase block size (64 pages), and hence only row addresses between 00h and 3Fh are allowed. The Block Erase command is not allowed in the OTP mode.

3.16 Feature Operations

3.16.1 Set Features

The Set Features function modifies the settings of a particular feature. For example, this function can be used to enable a feature that is disabled at power-on. Feature settings are volatile across power cycles. Feature setting value is retained across resets unless otherwise specified in the Features table.

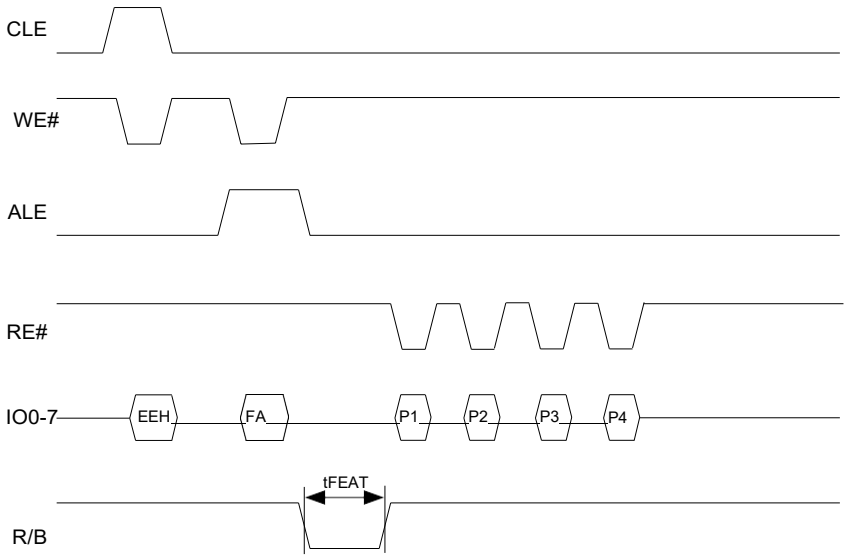
Figure 6. Set Features Timing[17, 18, 19]



3.16.2 Get Features

The Get Features function is the mechanism the host uses to determine the current settings for a particular feature. This function will return the current settings for the feature (including modifications that may have been previously made with the Set Features function). After reading the first byte of data, the host must complete reading all desired data before issuing another command (including Read Status or Read Status Enhanced). Figure 10 defines the Get Features behavior and timings.

Figure 7. Get Features Timing[20, 21, 22]



Notes

17.FA Feature address identifying feature to modify settings for.
18. P1-P4 Parameters identifying new settings for the feature specified.
19. P1 Sub feature parameter 1, P2 Sub feature parameter 2, P3 Sub feature parameter 3, P4, Sub Feature Parameter 4
20.FA Feature address identifying feature to return parameters for.
21.P1-P4 Current settings/parameters for the feature identified by argument P1.
22.P1 Sub feature parameter 1 setting, P2 Sub feature parameter 2 setting, P3 Sub feature parameter 3 setting, P4 Sub Feature Parameter 4 setting.

3.16.3 Feature Parameter Definitions

Table 16. Feature Address Definition

Feature Address	Description
00h	Reserved
01h	Timing Mode
02h-7Fh	Reserved
80h-FFh	Vendor specific

Table 17. Feature Address 90h-Array Operation Mode (P1 Register)[23, 24]

Bits	Field Name	Function	Default Value	Description
7	Reserved		0	
6	Reserved		0	
5	Reserved		0	
4	ECC_STATUS_SEL	ECC Status register Flag Select	0	0: Flag1 (Default) 1: Flag2 This bit selects the ECC status register Flag.
3	Reserved		1	1：This bit must always be set to "1"
2	Reserved		0	
1	OTP_LOCK_EN	OTP Protection Enable	0	1: Set OTP Protection (Lock). 0: Power on value The OTP protection is irreversible and becomes effective only if OTP mode is enabled.
0	OTP_MODE_EN	OTP Mode Enable	0	0: Normal (Array operation) 1: OTP mode enable

Notes
23. P2/P3/P4 are 00h.
24. A software reset command (FFh) does not alter the content of the 90h feature register.

4. Security Features

The security features below provide block protection from program and erase operations.

Two security methods are supported:

- Volatile Block Protection (VBP).

The VBP parameter settings are volatile. Power cycling will reset the settings to the default status (all blocks protected if VPE pin is high). This VBP method can protect one range of contiguous blocks.

This method requires use of a Volatile Protection Enable (VPE) input pin. To activate the VBP method using the VPE input, the host must power up the device with VPE input high during the Power-On Reset (POR) period and issue a set of commands to set the VBP parameter settings which consist of a Lower Boundary Address (LB_ADD) and an Upper Boundary Address (UB_ADD).

■ Permanent Block Protection (PBP)

The PBP parameter settings are non-volatile. These settings will be maintained after a power cycle. The PBP method can protect up to 64 blocks (block 0 to 63) organized in groups of 4 contiguous blocks. Each group can be protected individually and are permanently protected. Once a group is protected, the group can no longer be unprotected.

4.1 Volatile Block Protection (VBP) Overview

The VBP feature can protect all blocks, or one selected range of contiguous blocks, from erase and program operations. The VBP parameter settings are reset to default value after a power-cycle (all blocks protected if VPE input is high) and must be re-programmed by the host.

The VPE input level, latched during Power-On Reset (POR), determines whether the VBP is enabled or disabled. If the VPE input is low at power-on, the VBP feature is disabled and the Write Protect (WP#) input controls the protection of all blocks. If the VPE input is high at power-on, all blocks are protected from programming or erasing even if the WP# input is high. VPE must be high (VPE=H) when issuing all VBP function commands. See Figure 49 and Figure 50.

The Unlock Block commands (23h & 24h) are used to unprotect a range of blocks. The Unlock Block commands set the protection registers (UB_ADD and LB_ADD).

Once the selected blocks are unprotected, those blocks can be protected again by using a Lock All Blocks (2Ah) commands or by asserting WP# low for more than 100ns.

Once the selected blocks are unprotected, the host can issue a Lock-down command (2Ch) to lock the VBP protection range configuration until the next power off to on cycle.

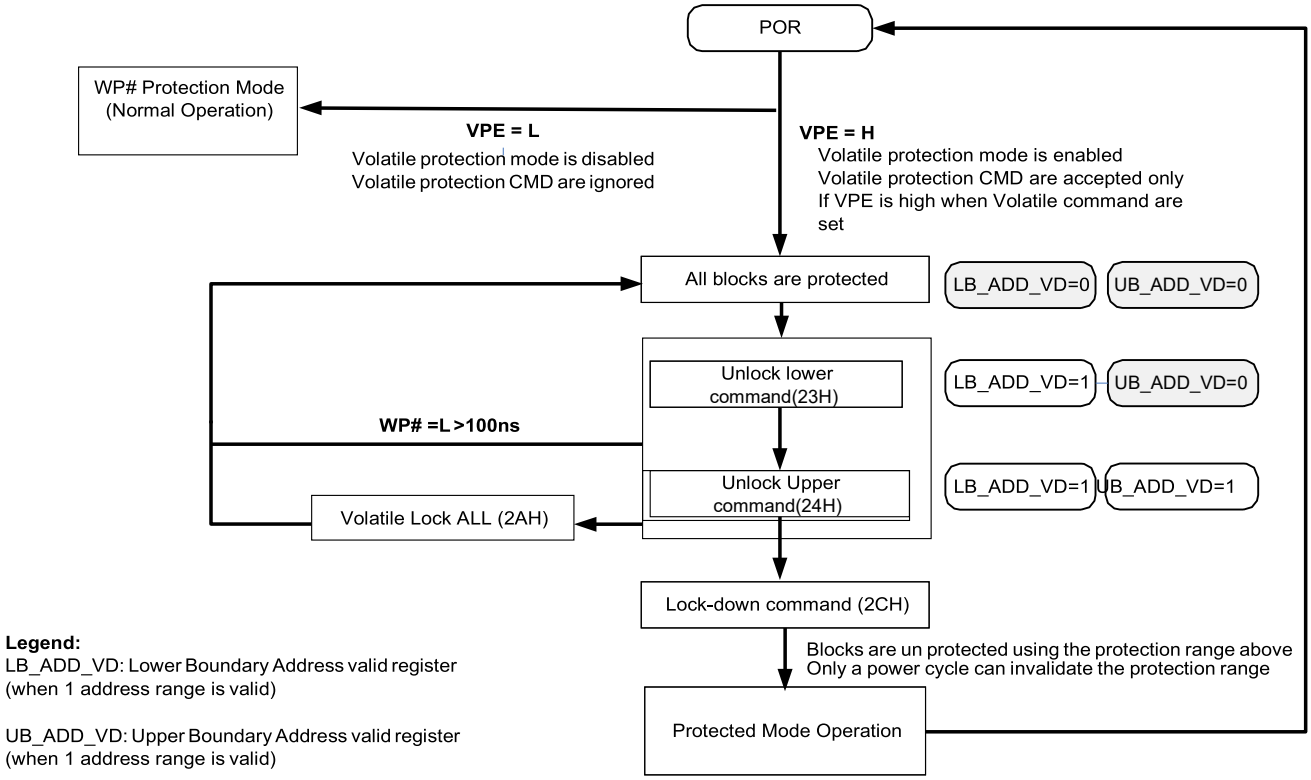
After, the Lock-down command is issued:

■ VPE signal value and the VBP commands are ignored until the next power cycle.

■ WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

Figure 8. provides an overview of the VBP mechanism.

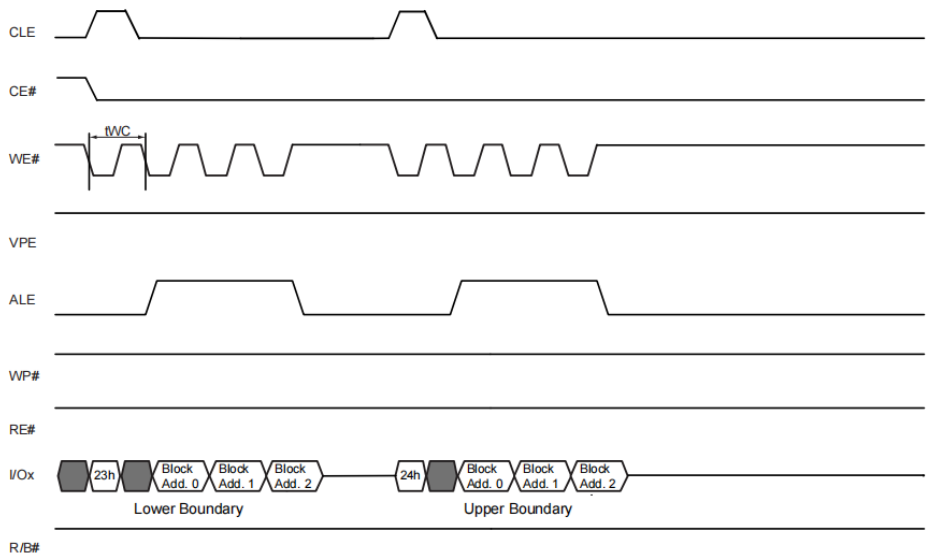
Figure 8. VBP flowchart



4.1.1 VBP Unlock Block (23h and 24h) Commands Waveforms

The Unlock Block commands define the range of blocks to be unprotected. The Unlock Lower command (23h) sets the lower block address, and must be followed by the Unlock Upper command (24h) that sets the upper block address (see Figure 9).

Figure 9. Waveforms for Block Unprotect



To unprotect the complementary range of block (see Figure 9), the host can set an invert-bit in the Unlock command address field (see Table 18). If the invert-bit is set to 0, the unprotected area is within and inclusive of the upper and lower block addresses; if the bit is set to 1, the unprotected area is outside and exclusive of the upper and lower block addresses.

Table 18. Address Definition of Unlock Block

Address Cycle Mapping									
	Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
Block Address 1	1st	BA[1]	BA[0]	L	L	L	L	L	Invert Bit (31)
Block Address 2	2nd	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
Block Address 3	3rd	L	L	L	L	L	L	BA[11]	BA[10]

Note
25.The Invert bit is set by 24h command to select whether the unprotected range is inside or outside of the range boundary. The bit is a don't care for the 23h command.

Figure 10. Unlock Range Option

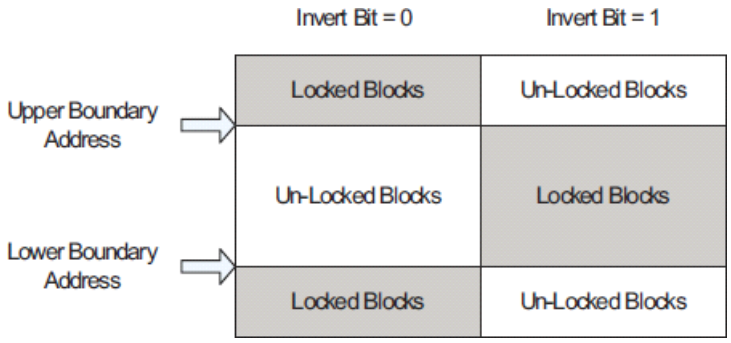


Table 19 illustrates how internally the blocks are being protected for single plane operations (shaded area) when the lower and upper addresses are respectively set to 1 and 4.

Table 19. Single Plane Block Protection Example [26]

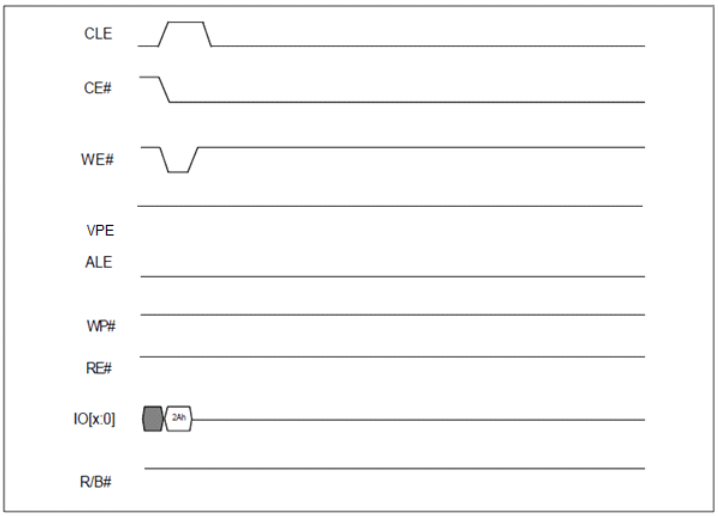
Single Plane Operation	
Block 0	Block 1
Block 2	Block 3
Block 4	Block 5

Note
26.Shaded boxes are protected by VBP.

4.1.2 VBP Lock All (2Ah) Command Waveforms

The Lock All command (2Ah) can be used to protect all the blocks in the device. This command is useful to program a new unprotected range as shown in Figure 11.

Figure 11. Waveforms for Lock All Blocks



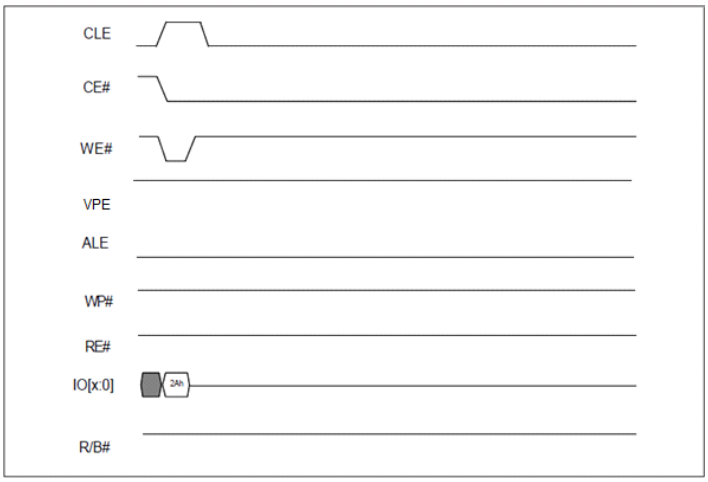
4.1.3 VBP Lock-down (2Ch) Command Waveforms

The Lock-down Command (2Ch) maintains the block protection parameters at the time the command is issued; the protected blocks cannot be unprotected and the unprotected blocks cannot be protected by software. Once the Lock-down command is issued, only a power off to power on cycle will change the block protection status by returning to the default state (all blocks protected state if VPE input is high on power on). The WP# input and VPE input must be high before issuing the Lock-down command.

After, the Lock-down command is issued:

- VPE signal value and the VBP commands are ignored until the next power cycle or hardware reset.
- WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

Figure 12. Waveforms for the Lock-down Command



4.2 Permanent Block Protection (PBP) Overview

The Permanent Block Protection (PBP) feature provides protection of up to sixteen groups (64 blocks total) from program and erase operations.

The device ships from the factory with no blocks protected by the PBP method.

Because this block protection is permanent, a power-on to power-off sequence does not affect the block protection status after the PBP command is issued.

The PBP method is used to select a group of blocks in the main array to be protected from program and erase operation. Multiple groups of blocks can be protected. Once a group of blocks is protected, the group of blocks can no longer be unprotected.

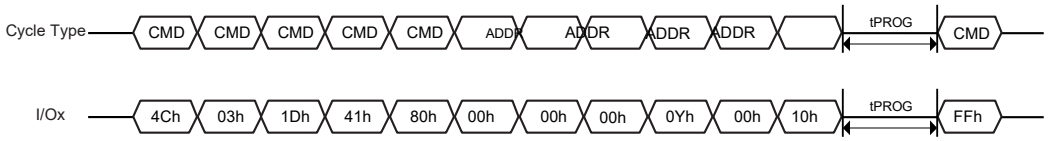
Additional unprotected groups can still be protected using the PBP sequence until the host issues a Permanent Block Protection Lock-down (PBPLDL) command.

When this PBPLDL command is issued, all groups of blocks protected by PBP are permanently protected from program and erase operations and a PBP operation can no longer be used to protect additional groups.

Issuing of the PBPLD sequence will both protect and lock down the protected group. Each PBP and PBPLDL sequence must be exited using the reset command (FFh).

The timing diagram in Figure 13 shows the PBP sequence.

Figure 13. Timing Diagram for the PBP Sequence



The group of blocks being protected is determined by the value of Y (see Table 20) on the fourth address cycle.

During PBP PGM busy, if FFh or power-off occurs, PBP cannot be guaranteed.

Table 20. Fourth Address Cycle (ADDR 4) Protection Scheme Table

Y Value	Protected Group	Protected Blocks
0000	0	0,1,2,3
0001	1	4,5,6,7
0010	2	8,9,10,11
0011	3	12,13,14,15
0100	4	16,17,18,19
0101	5	20,21,22,23
0110	6	24,25,26,27
0111	7	28,29,30,31
1000	8	32,33,34,35
1001	9	36,37,38,39
1010	10	40,41,42,43
1011	11	44,45,46,47
1100	12	48,49,50,51
1101	13	52,53,54,55
1110	14	56,57,58,59
1111	15	60,61,62,63

Note27: Maximum number of PBP and PBPLDL sequences allowed are 16. Any generated sequence is considered as one attempt. The user should avoid issuing a sequence to protect a group that was previously protected.

Table 21. PBP and PBPLDL Sequences

Description	Entry Sequence				CMD Cycle	Address Cycles	CMD Cycle	Read Status or Monitor RB# Output Cycles	Reset (Exit)
PBP sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h, 00h,00h, 0Yh,00h	10h	70h or 78h (Program Operation forces RDBY low)	FFh
PBPLDL sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h, 00h,00h, 1Y,00h	10h	70h or 78h (Program Operation forces RDBY low)	FFh

4.2.1 Block Protection Status Read command (7Ah) Waveform

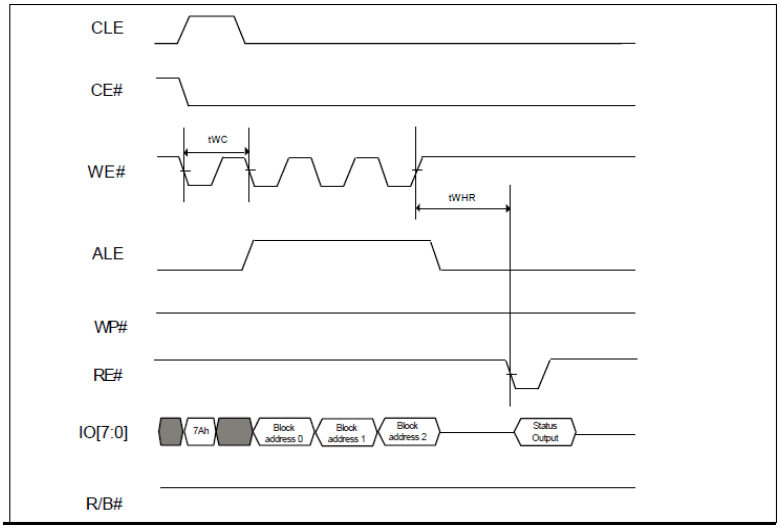
Figure 14 shows the Block Protection Status Read waveform. The Block Protection Status Read command (7Ah) is followed by 3 address cycles and one data cycle.

This register indicates whether a given block (addressed in the Block protection read address command field: BA[11:0]) is locked-down, locked or unlocked using the VBP or PBP protection methods.

Table 22.

Address Cycle Mapping for Block Protection Read Command (7Ah)									
	Bus Cycle	IO[7]	IO[6]	IO[5]	IO[4]	IO[3]	IO[2]	IO[1]	IO[0]
Block Address 0	1st	BA[1]	BA[0]	L	L	L	L	L	L
Block Address 1	2nd	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
Block Address 2	3rd	L	L	L	L	L	L	BA[11]	BA[10]

Figure 14. Waveforms for Block Protection Status Read Operation



4.2.2 Block Lock Status Register

This register indicates whether a given block (addressed in the Block protection read address command field is locked-down, locked or unlocked using the VBP or PBP protection methods.

Table 23 provides the BLS register definition.

Table 23. Block Lock Status Register

Bits	Function	Field Name	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	PBP Lock Down Status	PBP lock down Status	0	0: The PBP block range is not locked down by PBP 1: The PBP block range is locked down by PBP
3	Permanent Block Protection Status	Permanent Block Protect	1	0: The address selected block is locked by PBP 1: The address selected block is not locked by PBP
2	Volatile Block Protection Status	VBP Block-unlock	1	0: The address selected block is locked by VBP 1: The address selected block is not locked by VBP
1		VBP Not Locked-down	1	0: The VBP block range is locked down 1: The VBP block range is not locked down
0		VBP Lock-down	0	0: The VBP block range is not locked down 1: The VBP block range is locked down

5. Signal Descriptions

5.1 Data Protection and Power On / Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.8V.

The power-up and power-down sequence is shown in Figur49, Figure 50, and Figure 51.

The Ready/Busy signal will be valid within 100 µs after the power supplies have reached the minimum values (as specified on). The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B# becomes valid. Issuing of FFh command after Power Up Sequence allows Auto CAM read of the device. Each target (CE) will be busy for a maximum of 2 ms after the RESET command (FFh) is issued.

The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command. In the case where multi LUNs shared the same CE, Read Status Enhanced command should be used instead of READ STATUS. During this busy time, the device executes the initialization process (cam reading), and dissipates a current ICC0 (50 mA max), in addition, it disregards all commands excluding Read Status Register (70h).

Each NAND die (LUN) draws less than 10 mA for over 1 ms before the execution of the first RESET command (FFh) after the device is powered up. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50 mA.

At the end of this busy time, the device defaults into “read setup”, thus if the user decides to issue a page read command, the 00h command may be skipped.

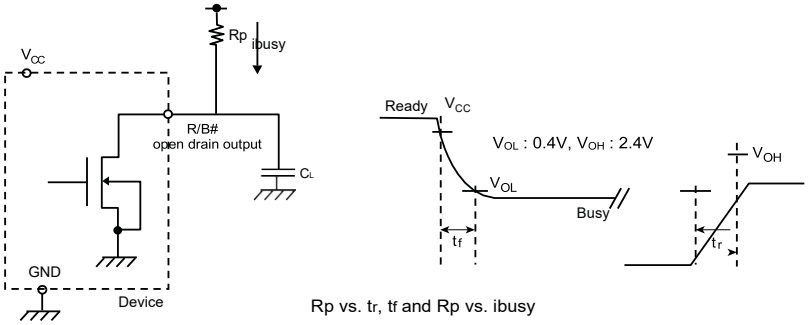
The WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down.

5.2 Ready/Busy

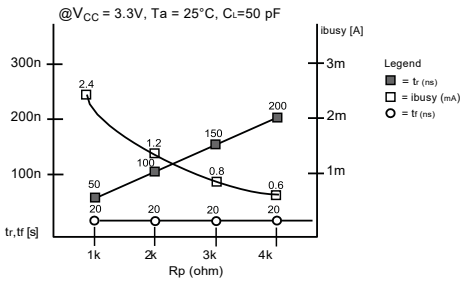
The Ready/Busy output provides a method of indicating the completion of a page program, erase, copyback, or read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, or erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because the pull-up resistor value is related to t_r (R/B#) and the current drain during busy (ibusy), and output load capacitance is related to t_f, an appropriate value can be obtained with the reference chart shown in Figure 15.

For example, for a particular system with 20 pF of output load, t_f from V_{CC} to V_{OL} at 10% to 90% will be 10 ns, whereas for a particular load of 50 pF, SkyHigh measured it to be 20 ns as shown in Figure 15.

Figure 15. Ready/Busy Pin Electrical Application



Rp vs. tr, tf and Rp vs. ibusy



Rp value guidence

$$Rp\ (min.) = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

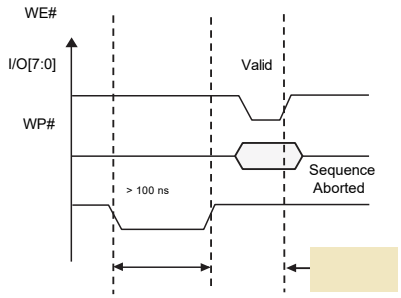
where I_L is the sum of the input currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr.

5.3 Write Protect Operation

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100 ns. Switching WP# low during this time is equivalent to issuing a Reset command (FFh). The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for t_{RST} (similarly to Figure 42). At the end of this time, the command register is ready to process the next command, and the Status Register bit I/O6 will be cleared to 1, while I/O7 value will be related to the WP# value.

Erase and program operations are enabled or disabled by setting WP# to high or low respectively, before issuing the setup commands (80h or 60h). The level of WP# will be set t_{WW} ns before raising the WE# pin for the set up command, as explained in Figure 52 and Figure 53.

Figure 16. WP Low Timing Requirements during Erase Command Sequence



6. Electrical Characteristics

6.1 Valid Blocks

Table 24. Valid Blocks

Device	Symbol	Min	Typ	Max	Unit
HYN1G08UKTCA1	N_{VB}	1004	—	1024	Blocks
HYN2G08UKTCC1	N_{VB}	2008	—	2048	Blocks

6.2 Absolute Maximum Ratings

Table 25. Absolute Maximum Ratings[28,29,30]

Parameter	Symbol	Value	Unit
Ambient Operating Temperature (Industrial Temperature Range)	T_A	-40 to +85	°C
Ambient Operating Temperature (Industrial Plus Temperature Range)	T_A	-40 to +105	°C
Temperature under Bias	T_{BIAS}	-50 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input or Output Voltage	V_{IO} (34)	-0.6 to +4.6	V
Supply Voltage	V_{CC}	-0.6 to +4.6	V

Notes

28.Except for the rating "Operating Temperature Range", stresses above those listed in the table *Absolute Maximum Ratings[33, 35]* "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

29.Minimum Voltage may undershoot to -2V during transition and for less than 20 ns during transitions.

30.Maximum Voltage may overshoot to V_{CC} +2.0V during transition and for less than 20 ns during transitions.

6.3 Recommended Operating Conditions

Table 26. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Vcc Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Supply Voltage	Vss	0	0	0	V

6.4 AC Test Conditions

Table 27. AC Test Conditions

Parameter	Value
Input Pulse Levels	0.0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (2.7 V–3.6 V)	1 TTL Gate and CL = 50 pF

6.5 AC Characteristics

Table 28. AC Characteristics[31, 32, 33]

Parameter	Symbol	Min	Typ	Max	Unit
ALE to RE# delay	t_{AR}	10	—	—	ns
ALE hold time	t_{ALH}	5	—	—	ns

Notes

31.The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.

32.If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 µs.

33. CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either t_{COH} or t_{RHOH} will be met.

Table 29. AC Characteristics[34, 35, 36]

Parameter	Symbol	Min	Typ	Max	Unit
ALE setup time	t_{ALS}	10	—	—	ns
Address to data loading time	t_{ADL}	70	—	—	ns
CE# low to RE# low	t_{CR}	10	—	—	ns
CE# hold time	t_{CH}	5	—	—	ns
CE# high to output High-Z	t_{CHZ}	—	—	30	ns
CLE hold time	t_{CLH}	5	—	—	ns
CLE to RE# delay	t_{CLR}	10	—	—	ns
CLE setup time	t_{CLS}	10	—	—	ns
CE# access time	t_{CEA}	—	—	25	ns
CE# high to output hold	t_{COH} (38)	15	—	—	ns
CE# high to ALE or CLE don't care	t_{CSD}	10	—	—	ns
CE# setup time	t_{CS}	15	—	—	ns
Data hold time	t_{DH}	5	—	—	ns
Data setup time	t_{DS}	7	—	—	ns
Data transfer from cell to register (Single Plane)	t_R	—	45	250	µs
Data transfer from cell to register (Multi Plane)		—	55	450	µs
Output High-Z to RE# low	t_{IR}	0	—	—	ns
Read cycle time	t_{RC}	20	—	—	ns
RE# access time	t_{REA}	—	—	16	ns
RE# high hold time	t_{REH}	7	—	—	ns
RE# high to output hold	t_{RHOH} (38)	15	—	—	ns
RE# high to WE# low	t_{RHW}	100	—	—	ns
RE# high to output High-Z	t_{RHZ}	—	—	100	ns
RE# low to output hold	t_{RLOH}	5	—	—	ns
RE# pulse width	t_{RP}	10	—	—	ns
Ready to RE# low	t_{RR}	20	—	—	ns
Reset time (Read/Program/Erase)	t_{RST}	—	—	5/10/500	µs
WE# high to busy	t_{WB}	—	—	100	ns
Write cycle time	t_{WC}	20	—	—	ns
WE# high hold time	t_{WH}	7	—	—	ns
WE# high to RE# low	t_{WHR}	60	—	—	ns
WE# high to RE# low for Random Data Output	t_{WHR2}	200	—	—	ns
WE# pulse width	t_{WP}	10	—	—	ns
Write protect time	t_{WW}	100	—	—	ns

Notes

34.The time to Ready depends on the value of the pull-up resistor tied to R/B# pin.

35.If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5 µs.

36. CE# low to high or RE# low to high can be at different times and produce three cases. Depending on which signal comes high first, either t_{COH} or t_{RHOH} will be met.

6.6 DC Characteristics

Table 30. DC Characteris tics and Operating [37, 38, 39, 40]

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Power On Current		I_{CC0}	FFh command input after power on	—	—	50 per device	mA
Operating Current	Sequential Read	I_{CC1}	$t_{RC} = t_{RC}$ (min) CE# = V_{IL}, Iout = 0 mA	—	25	35	mA
	Program	I_{CC2}	Normal	—	25	35	mA
	Erase	I_{CC3}	—	—	15	30	mA
Standby Current, (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/Vcc	—	—	1	mA
Standby Current, (CMOS)		I_{CC5}	CE# = V_{CC}-0.2, WP# = 0/V_{CC} VPE= 0/V_{CC}	—	20	100	µA
Input Leakage Current		I_{LI}	V_{IN} = 0 to V_{CC}(max)	—	—	±10	µA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to V_{CC}(max)	—	—	±10	µA
Input High Voltage		V_{IH}	—	V_{CC} x 0.8	—	V_{CC} + 0.3	V
Input Low Voltage		V_{IL}	—	-0.3	—	V_{CC} x 0.2	V
Output High Voltage		V_{OH}	I_{OH} = -400 µA	2.4	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Output Low Current (R/B#)		$I_{OL(R/B\#)}$	V_{OL} = 0.4V	8	10	—	mA
Erase and Program Lockout Voltage		V_{LKO}	—	—	1.8	—	V

Notes
37. All V_{CC} pins, and V_{SS} pins respectively, are shorted together.
38. Values listed in this table refer to the complete voltage range for V_{CC} and to a single device in case of device stacking.
39. All current measurements are performed with a 0.1 µF capacitor connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin.
40. Standby current measurement can be performed after the device has completed the initialization process at power up. Refer to Section 5.1 for more details.

6.7 Pin Capacitance

Table 31. Pin Capacitance (TA = 25°C, f = 1.0 MHz)[41]

Parameter	Symbol	Test Condition	Min	Max	Unit
Input	C_{IN}	V_{IN} = 0V	—	10	pF
Input / Output	C_{IO}	V_{IL} = 0V	—	10	pF

Note
41. For the stacked devices version the Input is 10 pF x [number ofstacked chips] and the Input/Output is 10 pF x [number of stacked chips].

6.8 Thermal Resistance

Table 32. Thermal Resistance[42]

Parameter	Description	TSOP48	Unit
Theta J_A	Thermal Resistance (Junction to Ambient)	40	°C/W

Note
42. Test conditions follow standard methods and procedures for measuring thermal impedance in accordance with EIA/JESD51.

6.9 Program / Erase Characteristics

Table 33. Program / Erase Characteristics[43]

Parameter		Description	Min	Typ	Max	Unit
Program Time [44, 45]		t_{PROG}	—	350	600	µs
Number of partial Program Cycles in the same page	Main + Spare	NOP	—	—	4	Cycle
Block Erase Time		t_{BERS}	—	4	10	ms
Busy time for SET FEATURES and GET FEATURES operations		t_{FEAT}[48]			1	µs
Power on Reset Time		t_{POR}			3	ms

Notes

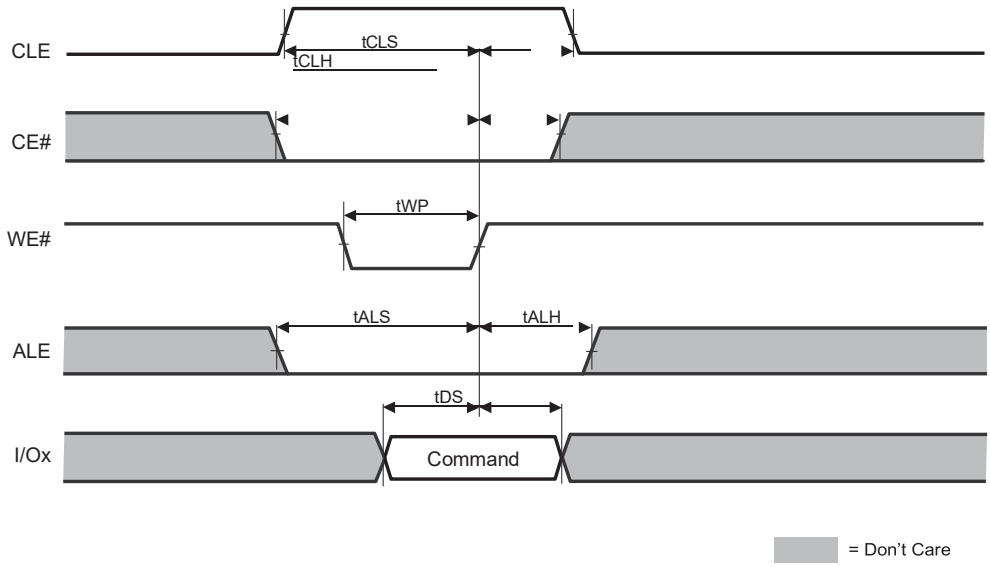
43. Typical program time is defined as the time within which more than 50% of the whole pages are programmed (V_{CC} = 3.3V, 25°C).
44. Copy Back Read and Copy Back Program for a given plane must be between odd address pages or between even address pages for the device to meet the program time (t_{PROG}) specification. Copy Back Program may not meet this specification when copying from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page).
45. t_{PROG} for PBP/OTP has a typical value of 500 µs and a max value of 800 µs.
46. tFEAT (busy time for SET FEATURES) spec for OTP protection has a typical value of 500 µs and a max value of 800 µs.

7. Timing Diagrams

7.1 Command Latch Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/ erase) the Write Protect pin must be high.

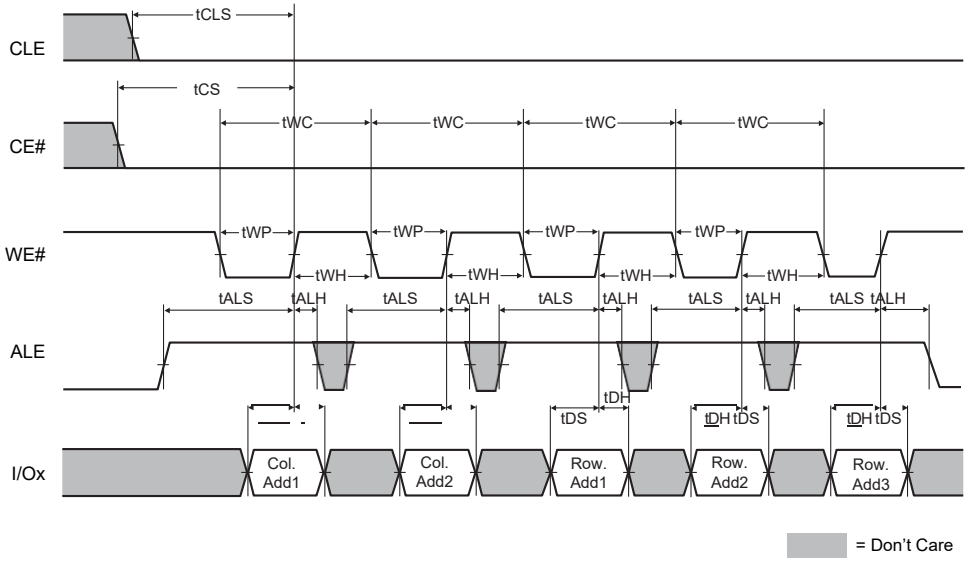
Figure 17. Command Latch Cycle



7.2 Address Latch Cycle

Address Input bus operation allows the insertion of the memory address. To insert the 27 (×8 Device) addresses needed to access the 1 Gb, four write cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low, and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modify operation (write/erase) the Write Protect pin must be high.

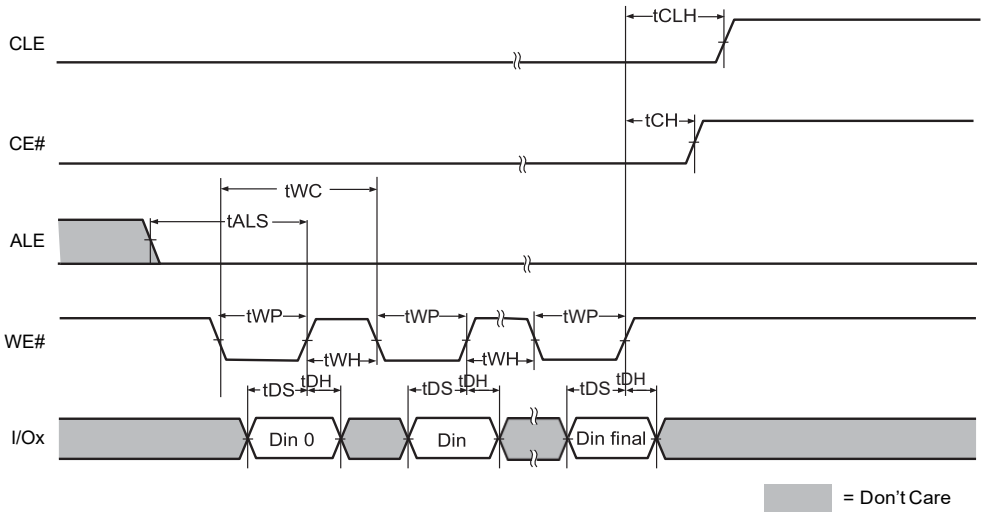
Figure 18. Address Latch Cycle



7.3 Data Input Cycle Timing

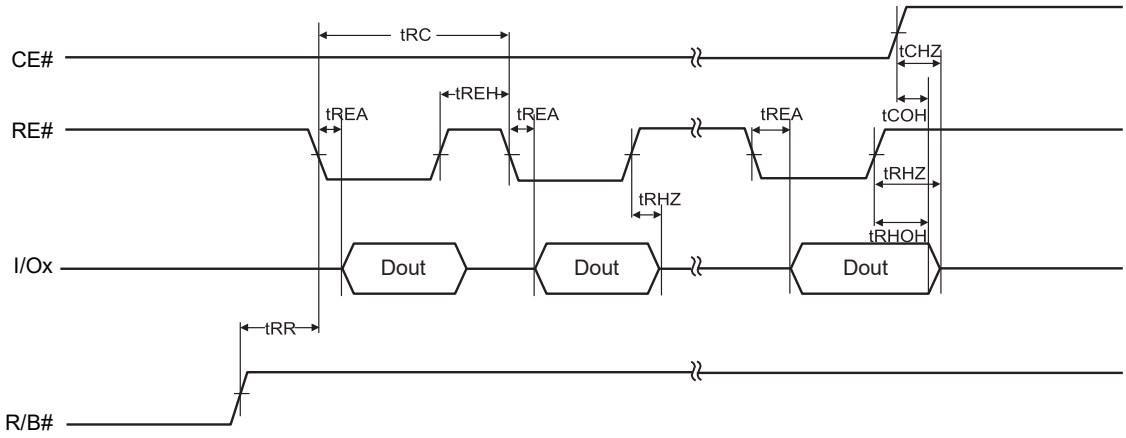
Data Input bus operation allows the data to be programmed to be sent to the device. The data insertion is serially, and timed by the Write Enable cycles. Data is accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

Figure 19. Input Data Latch Cycle



7.4 Data Output Cycle Timing (CLE=L, WE#=H, ALE=L, WP#=H)

Figure 20. Data Output Cycle Timing[47, 48, 49]

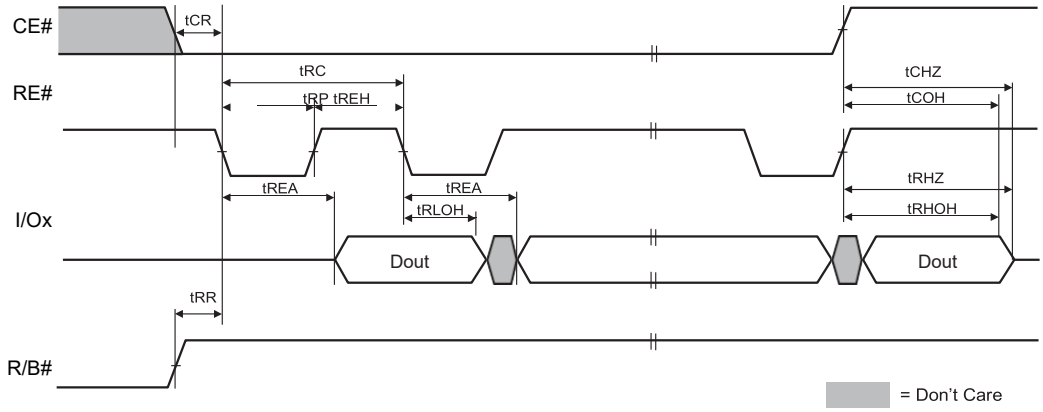


Notes

47. Transition is measured at ± 200 mV from steady state voltage with load.
48. This parameter is sampled and not 100% tested.
49. t_{RHOH} starts to be valid when frequency is lower than 33 MHz.

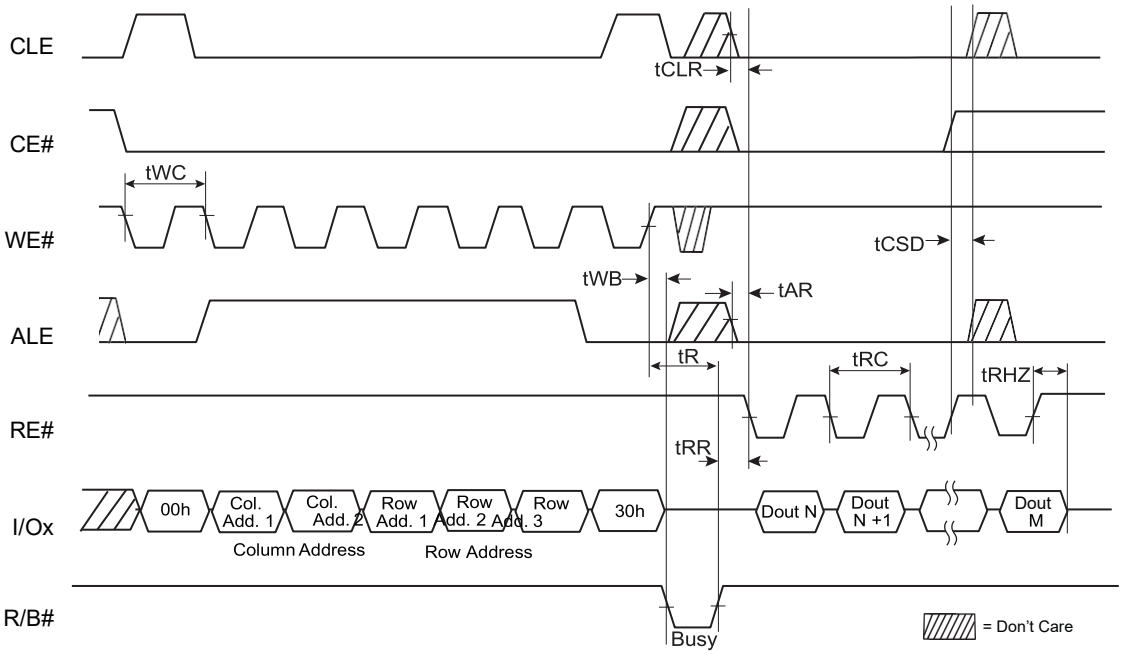
7.5 Data Output Cycle Timing (EDO Type, CLE=L, WE#=H, ALE=L)

Figure 21. Data Output Cycle Timing (EDO)[50, 51, 52, 35]



7.6 Page Read Operation

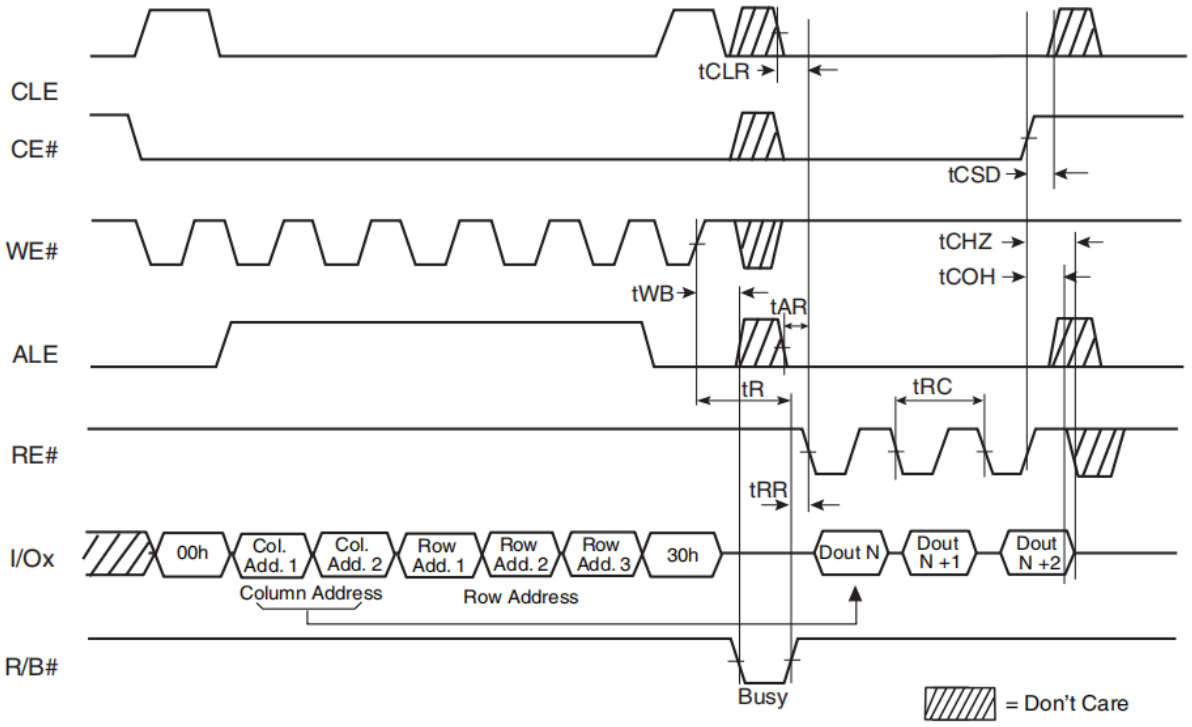
Figure 22. Page Read Operation (Read One Page)[54]



Notes
50. Transition is measured at ± 200 mV from steady state voltage with load.
51. This parameter is sampled and not 100% tested.
52. t_{RLOH} is valid when frequency is higher than 33 MHz.
53. t_{RHOH} starts to be valid when frequency is lower than 33 MHz.
54. If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.

7.7 Page Read Operation (Interrupted by CE#)

Figure 23. Page Read Operation Interrupted by CE#



7.8 Page Read Operation Timing with CE# Don't Care

Figure 24. Page Read Operation Timing with CE# Don't Care

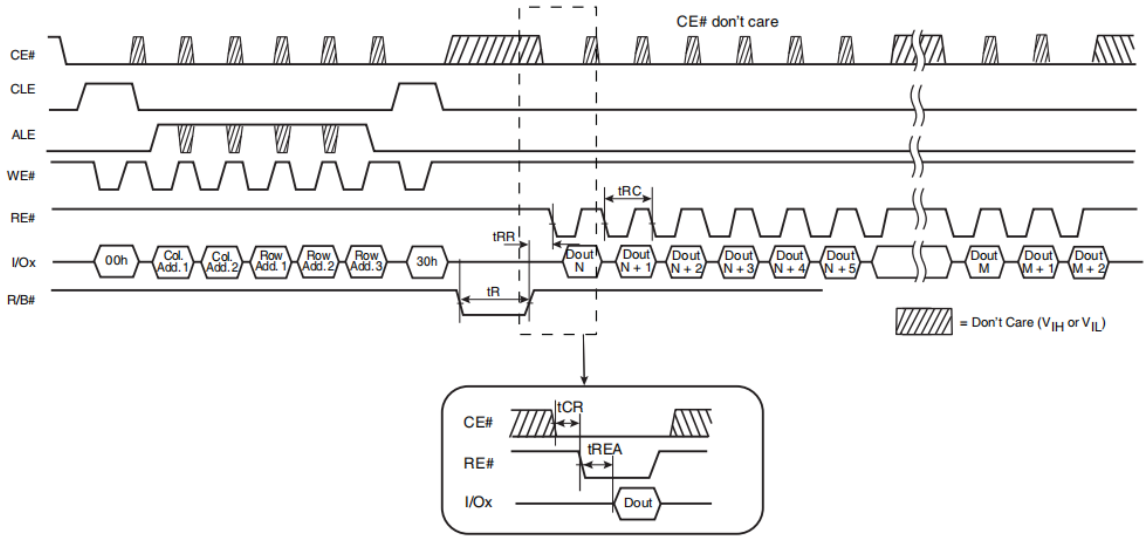
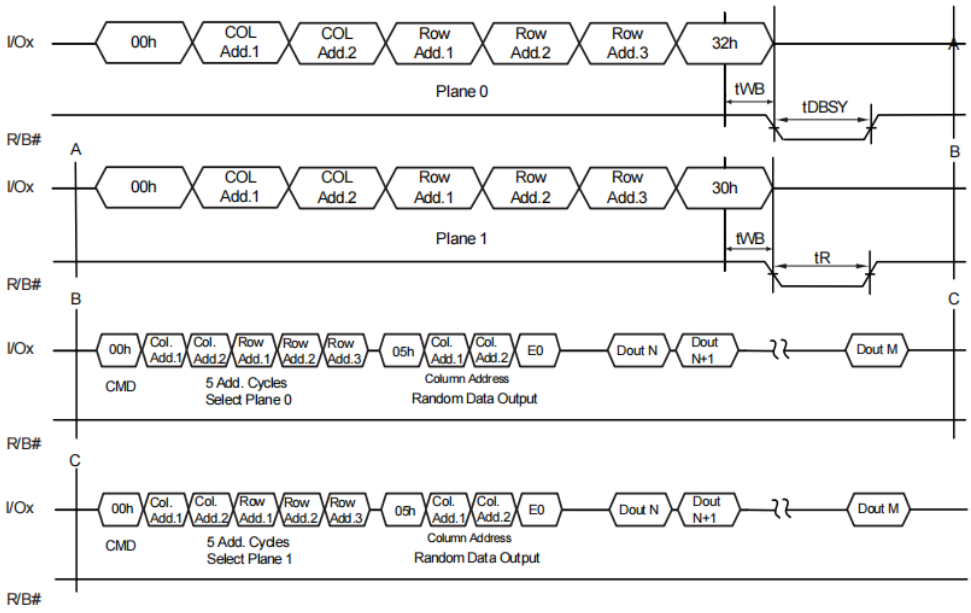
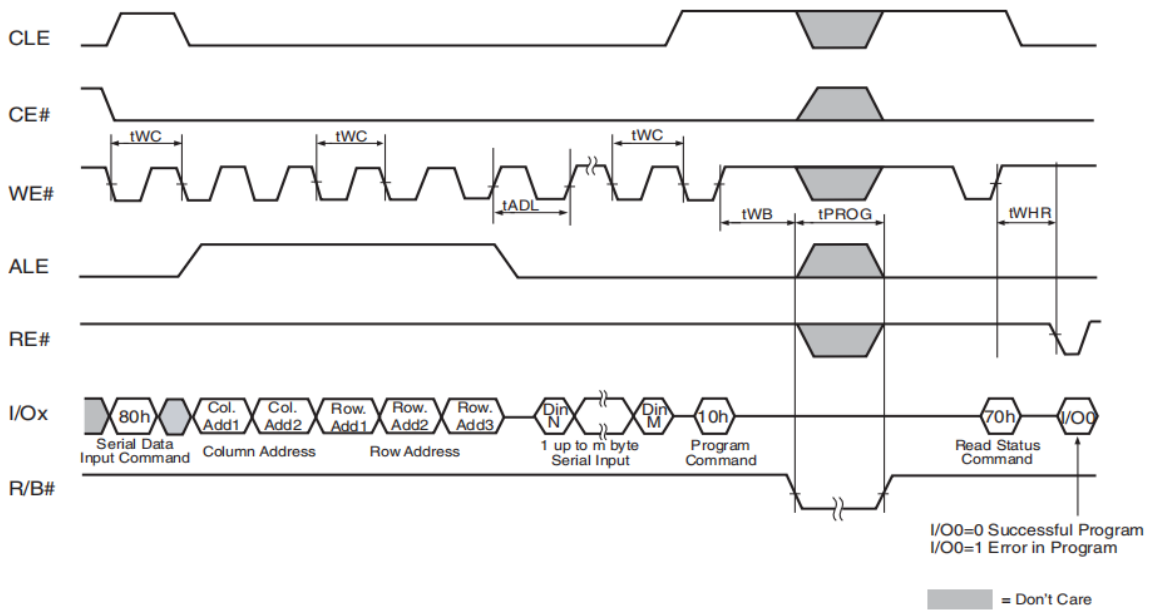


Figure 25. Multiplane Page Read Operation



7.9 Page Program Operation

Figure 26. Page Program Operation[55]



Note

55. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

7.10 User Spare Program

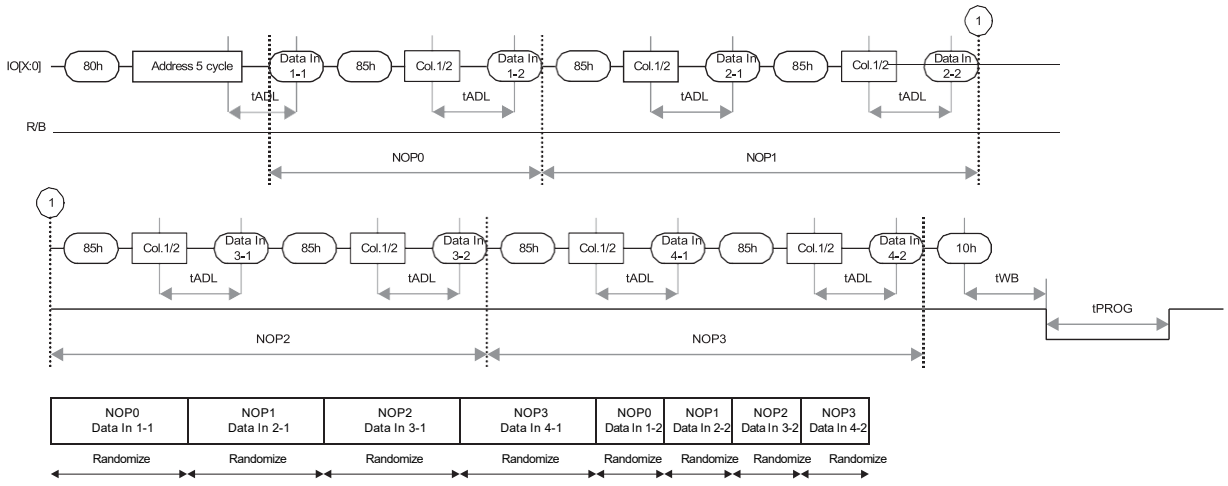
The number of consecutive partial page programming operations within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte) in the case of 2KB Page. Number of Program (NOP) refers to main area that is divided and programmed in each number of partial program operation.

During NOP program, data that is designated to user spare area must use random data input to change column address. Because NOP is allowed in maximum of 4 times, user spare area is also divided into 4 regions to match up to each NOP area. Main data is divided using NOP, and randomized while programming the data. Although user spare that is included in each NOP is also randomized, randomization done between main data and user spare are different as shown in Figure 27. Therefore, for each NOP, column address change should match up correct NOP with NOP user spare.

First, input 512 bytes of data for NOP0; then, input user spare data for NOP0 after changing of column address using Random Data Input. After programming data, use Random Data Input to return back to starting address of NOP1 main data. Secondly, input 512 bytes of NOP1 data, using Random Data Input to change column address to user spare data for NOP1 input. After programming user spare data for NOP1, return to starting address of NOP2 main data. NOP2 and NOP3 must follow the same process. Both main data and user spare should be input at the same time for NOP operation; otherwise, data is not guaranteed.

If user decide to follow the same order as programming order during data out, read out NOP0 area first, then use Random Data Output to change column address to read out NOP0 user spare area.

Figure 27. Random Data Input Timings



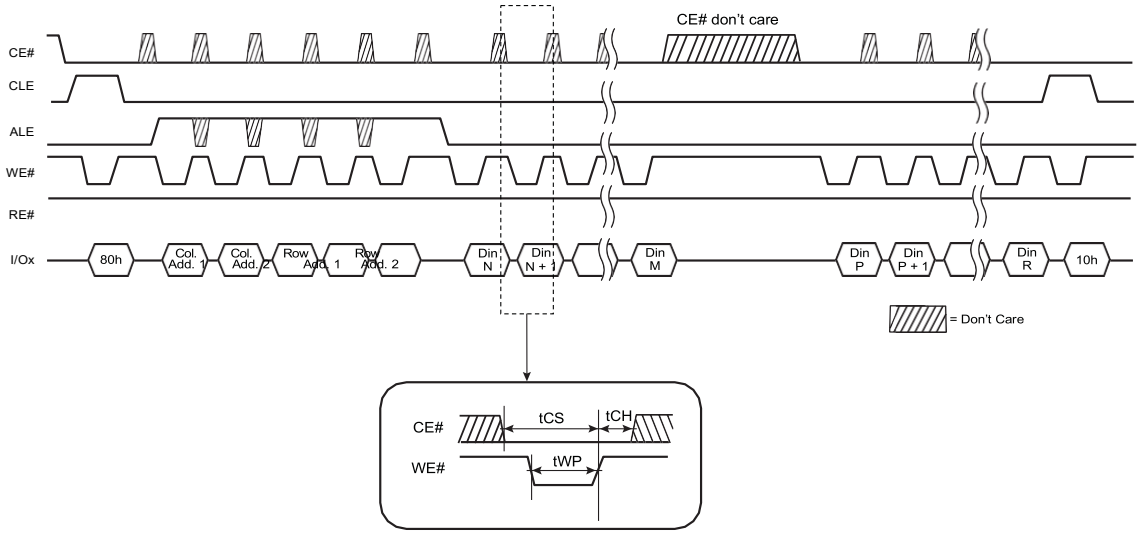
7.11 Small Data Input Guidelines

Small data input is allowed within an NOP provided that it meets the following conditions:

- Data size must be a minimum of 4 bytes or greater within single NOP.
- Data input column address must start from xxxx0h, xxx4h, xxx8h, and xxxCh.

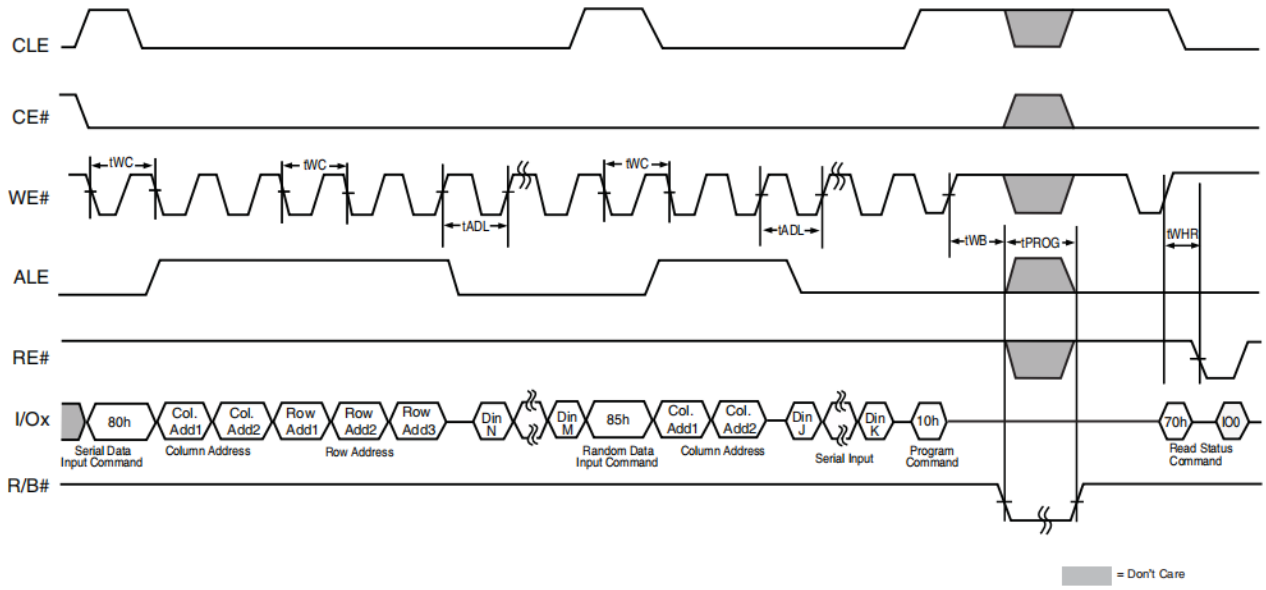
7.12 Page Program Operation Timing with CE# Don't Care

Figure 28. Page Program Operation Timing with CE# Don't Care



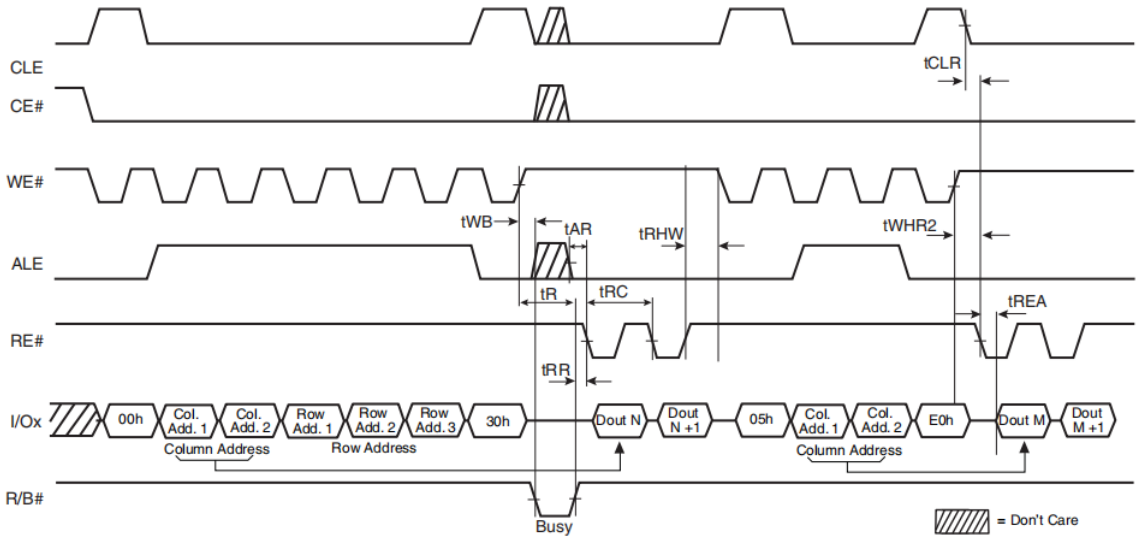
7.13 Page Program Operation with Random Data Input

Figure 29. Random Data Input[58]



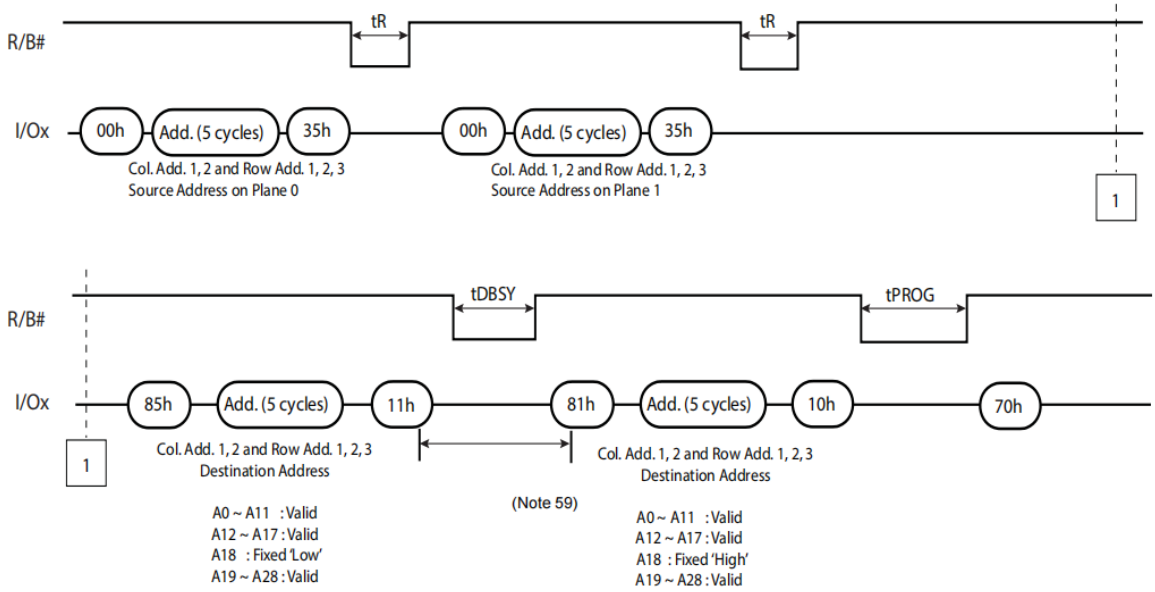
7.14 Random Data Output In a Page

Figure 30. Random Data Output



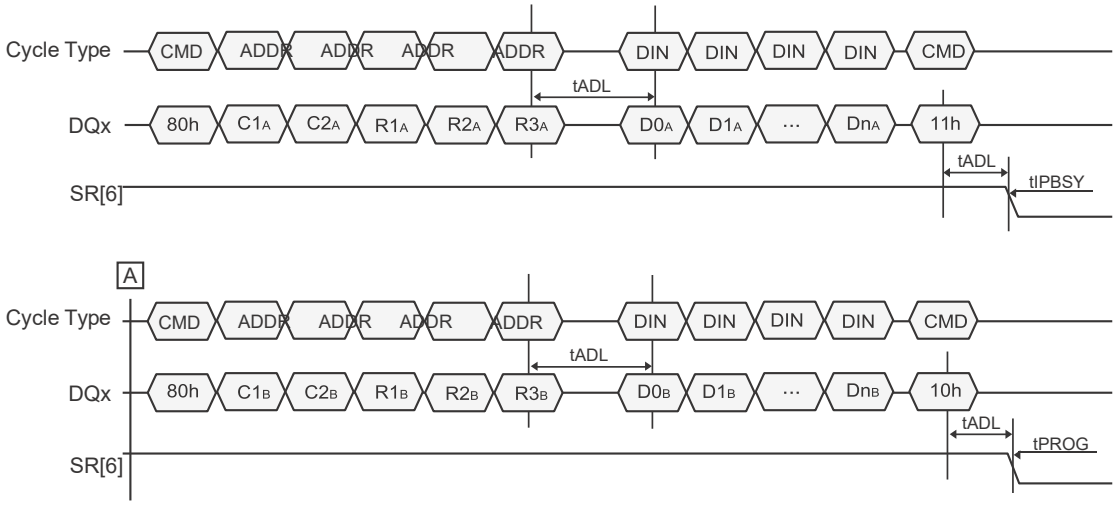
7.15 Multiplane Page Program Operation

Figure 31. Multiplane Page Program[56, 57, 58]



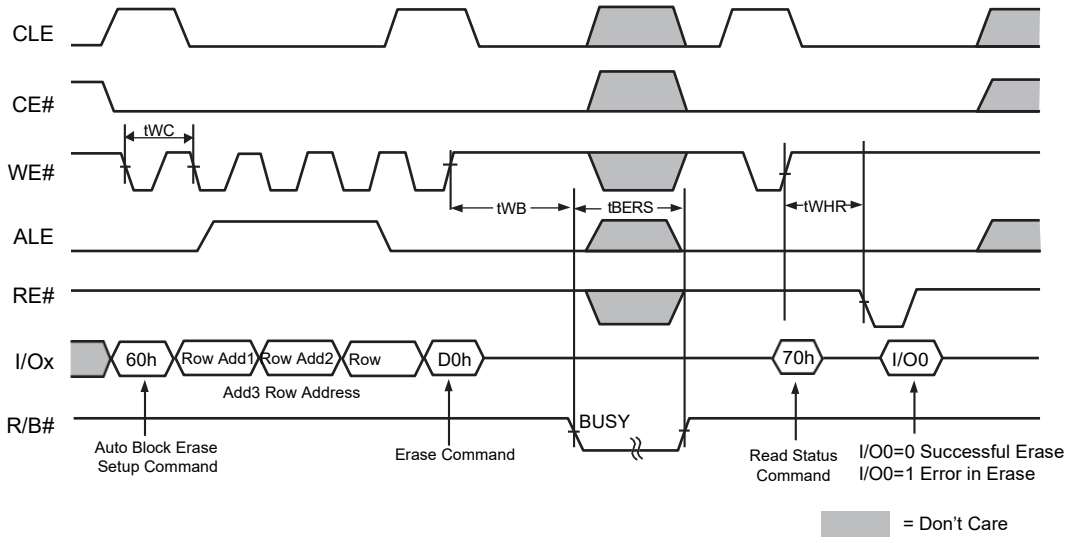
Notes
56. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
57. A18 is the plane address bit for ×8 devices.
58. The block address bits must be the same except for the bit(s) that select the plane.

Figure 31-2. Multiplane Page Program (ONFI 1.0 Protocol)[59,60, 61, 62, 63, 64, 65]



7.16 Block Erase Operation

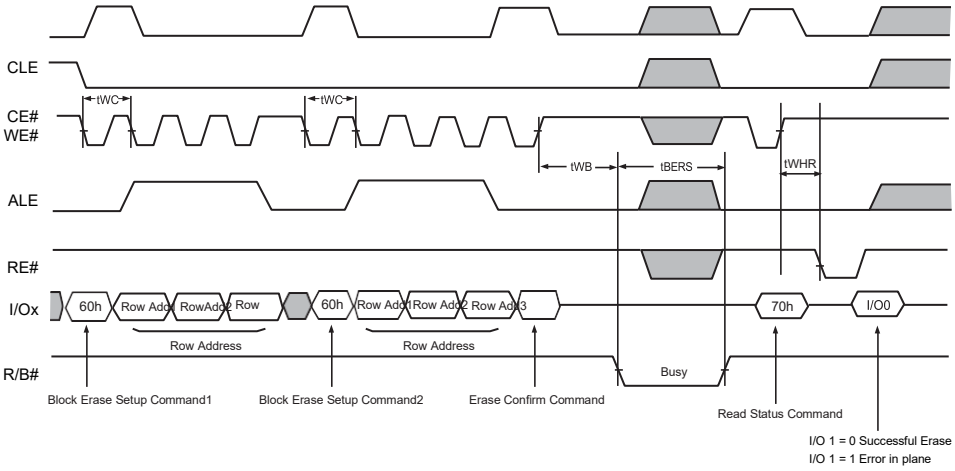
Figure 32. Block Erase Operation (Erase One Block)



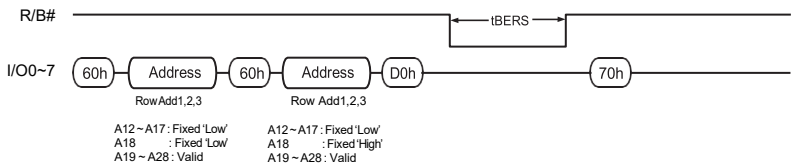
Notes
59. C1A-C2A Column address for page A. C1A is the least significant byte.
60. R1A-R3A Row address for page A. R1A is the least significant byte.
61. D0A-DnA Data to program for page A.
62. C1B-C2B Column address for page B. C1B is the least significant byte.
63. R1B-R3B Row address for page B. R1B is the least significant byte.
64. D0B-DnB Data to program for page B.
65. The block address bits must be the same except for the bit(s) that select the plane.

7.17 Multiplane Block Erase

Figure 33. Multiplane Block Erase[66, 67]



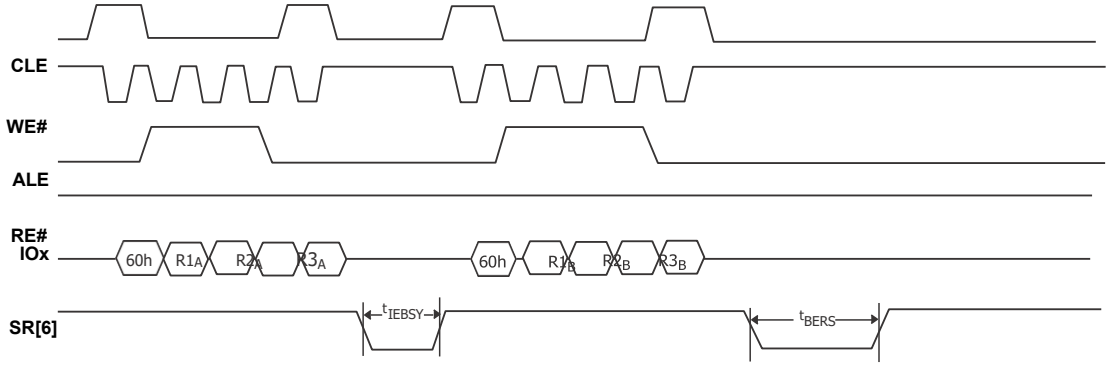
Ex.) Address Restriction for Multiplane Block Erase Operation



Notes

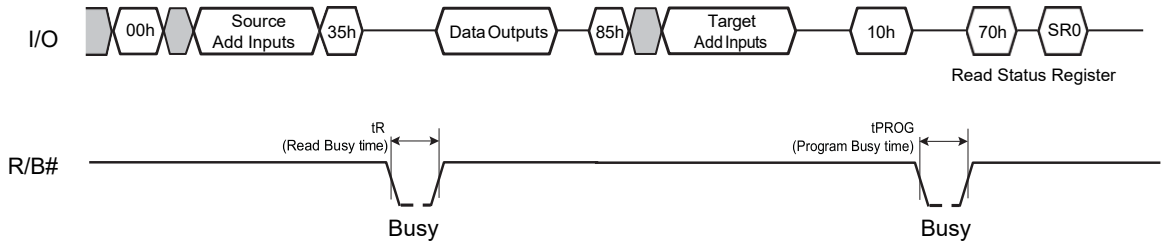
66. A18 is the plane address bit for ×8 devices.
67. The block address bits must be the same except for the bit(s) that select the plane.

Figure 35. Multiplane Block Erase (ONFI 1.0 Protocol)[68, 69, 70]



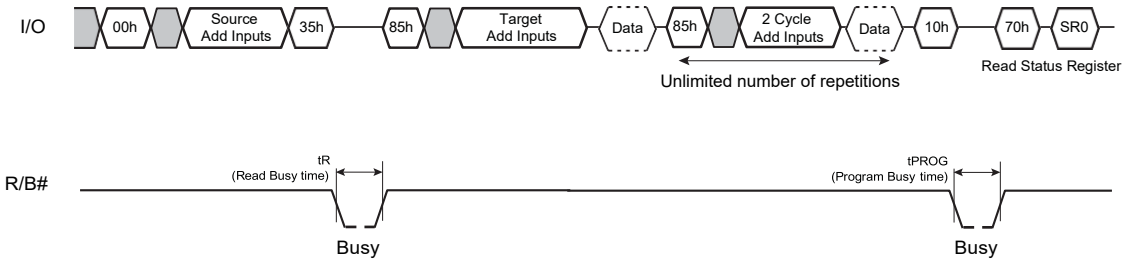
7.18 Copy Back Read With Optional Data Readout

Figure 36. Copy Back Read with Optional Data Readout



7.19 Copy Back Program Operation With Random Data Input

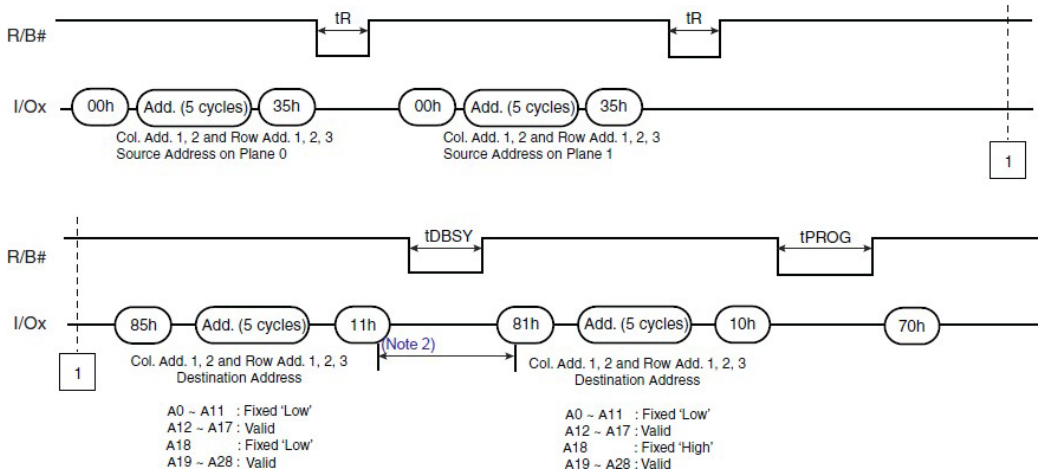
Figure 37. Copy Back Program with Random Data Input

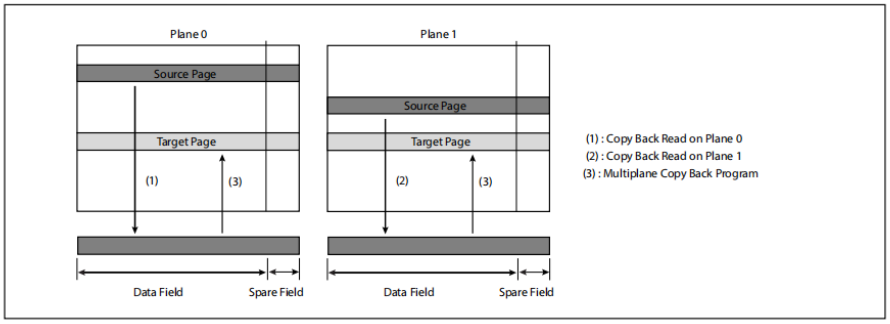


Notes
68. R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
69. R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
70. The block address bits must be the same except for the bit(s) that select the plane.

7.20 Multiplane Copy Back Program

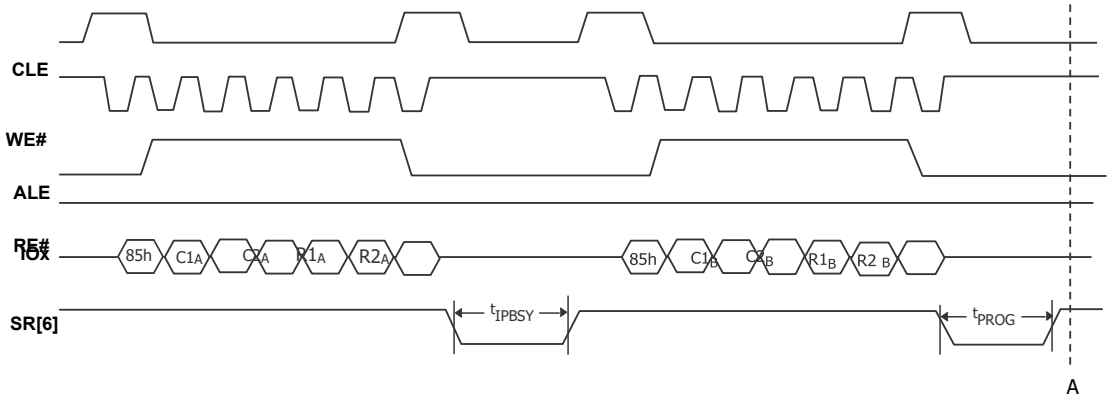
Figure 38. Multiplane Copy Back Program[71, 72, 73, 74]





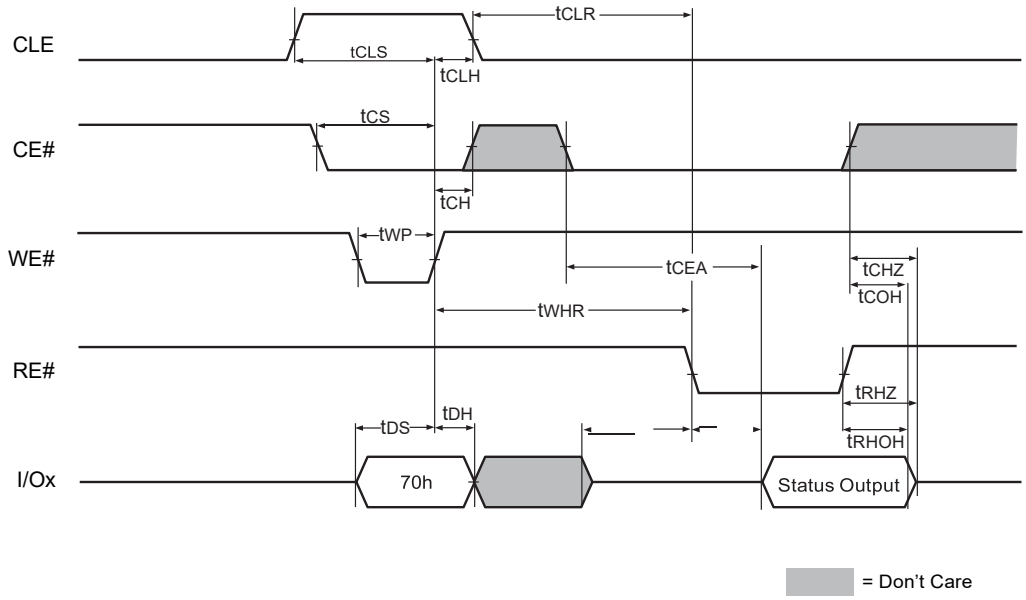
Notes
71. Copy Back Program operation is allowed only within the same memory plane.
72. Any command between 11h and 81h is prohibited except 70h, 78h, and FFh.
73. A18 is the plane address bit for ×8 devices.
74. The block address bits must be the same except for the bit(s) that select the plane.

Figure 39. Multiplane Copy Back Program (ONFI 1.0 Protocol) [75, 76, 77, 78, 79]



7.21 Read Status Register Timing

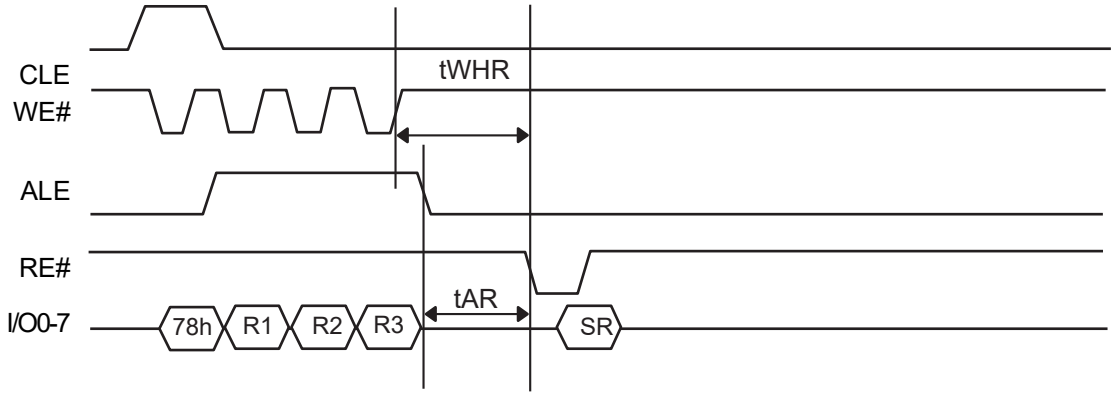
Figure 40. Read Status Cycle



Notes
75. C1A-C2A Column address for page A. C1A is the least significant byte.
76. R1A-R3A Row address for page A. R1A is the least significant byte.
77. C1B-C2B Column address for page B. C1B is the least significant byte.
78. R1B-R3B Row address for page B. R1B is the least significant byte.
79. The block address bits must be the same except for the bit(s) that select the plane.

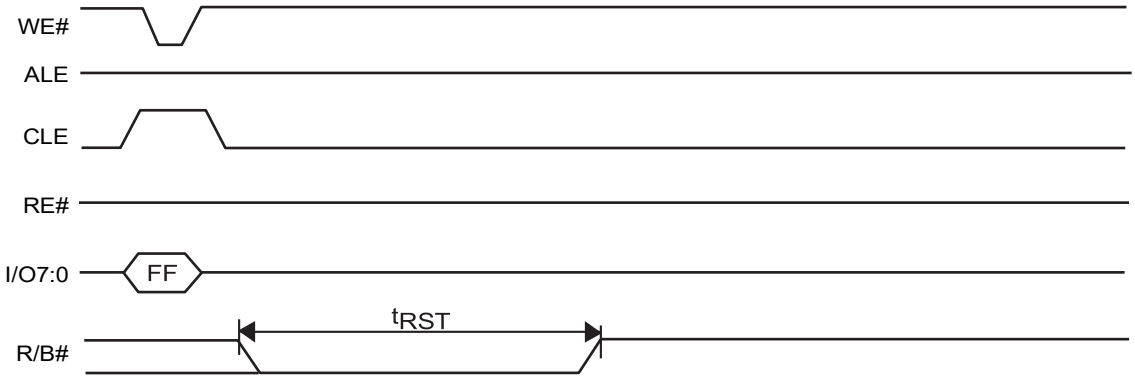
7.22 Read Status Enhanced Timing

Figure 41. Read Status Enhanced Timing



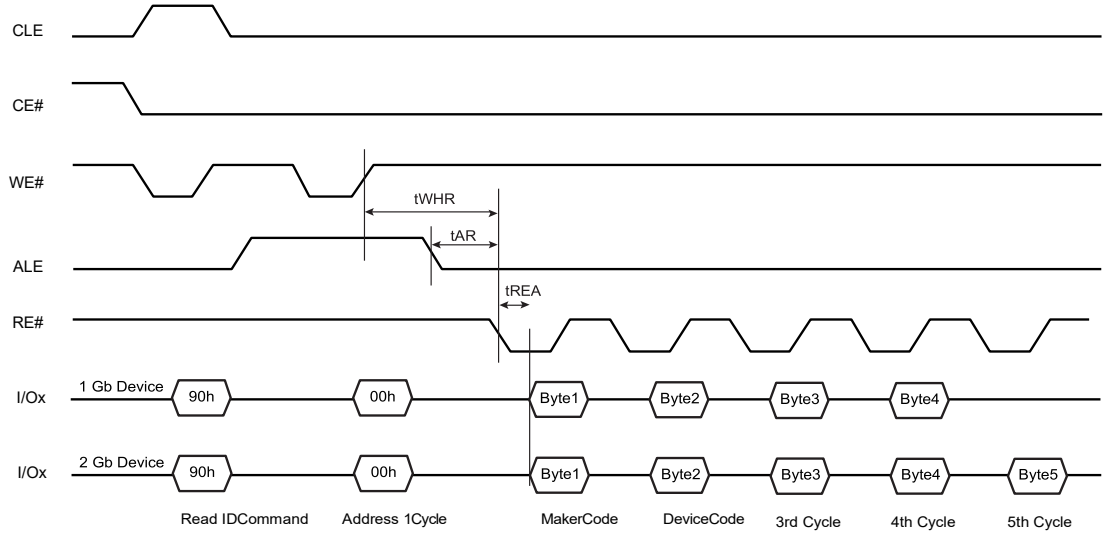
7.23 Reset Operation Timing

Figure 42. Reset Operation Timing



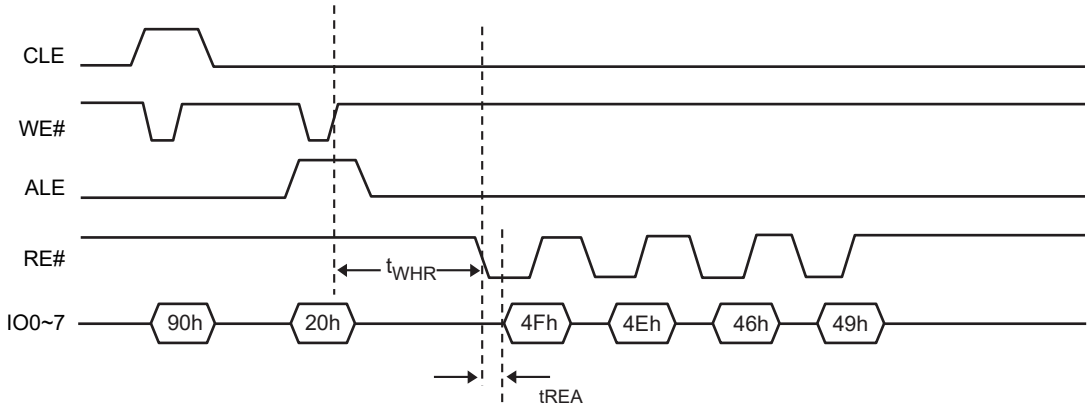
7.24 Read ID Operation Timing

Figure 43. Read ID Operation Timing



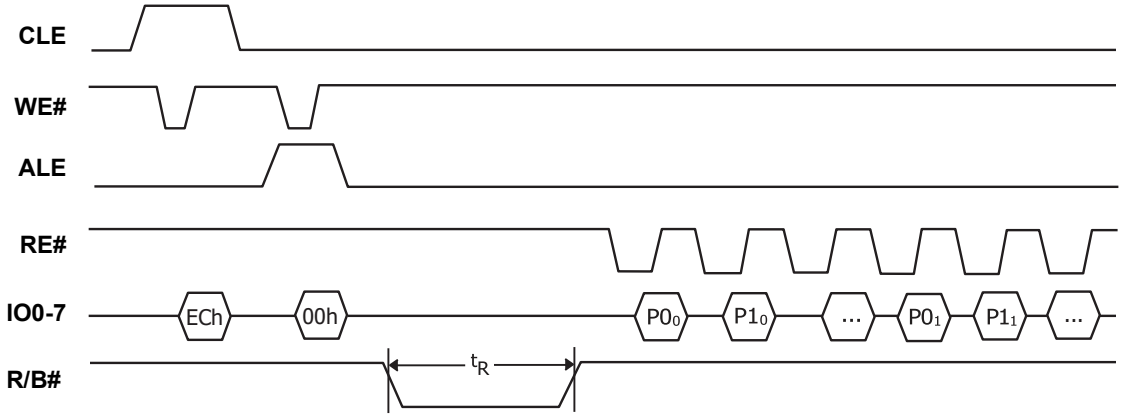
7.25 Read ONFI Signature Timing

Figure 44. ONFI Signature Timing



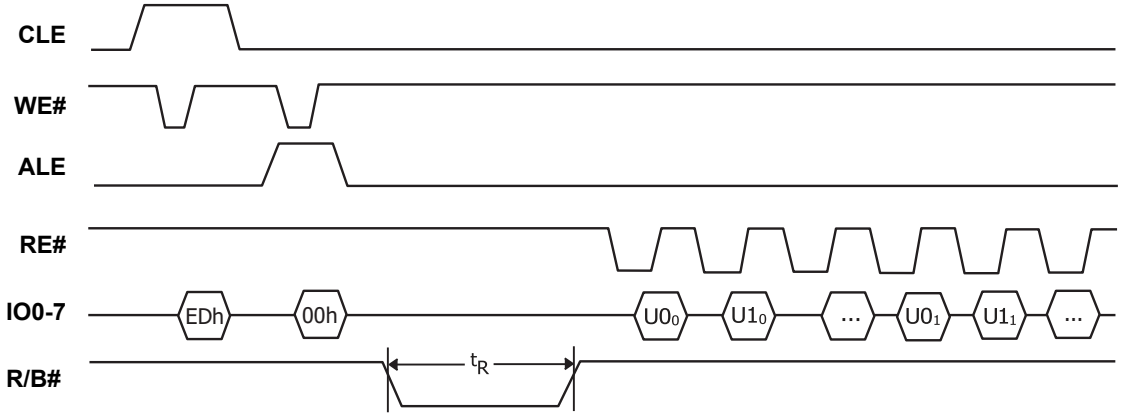
7.26 Read Parameter Page Timing

Figure 45. Read Parameter Page Timing[80]



7.27 Read Unique ID Timing

Figure 46. Read Unique ID Timing

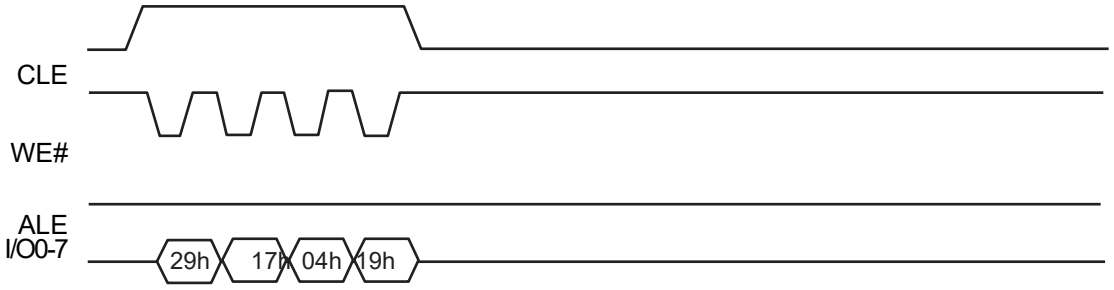


Note

80.If Status Register polling is used to determine completion of the read operation, the Read Command (00h) must be issued before data can be read from the page buffer.

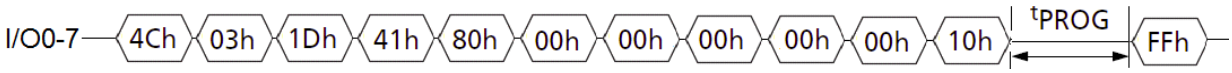
7.28 OTP Entry Timing

Figure 47. OTP Entry Timing



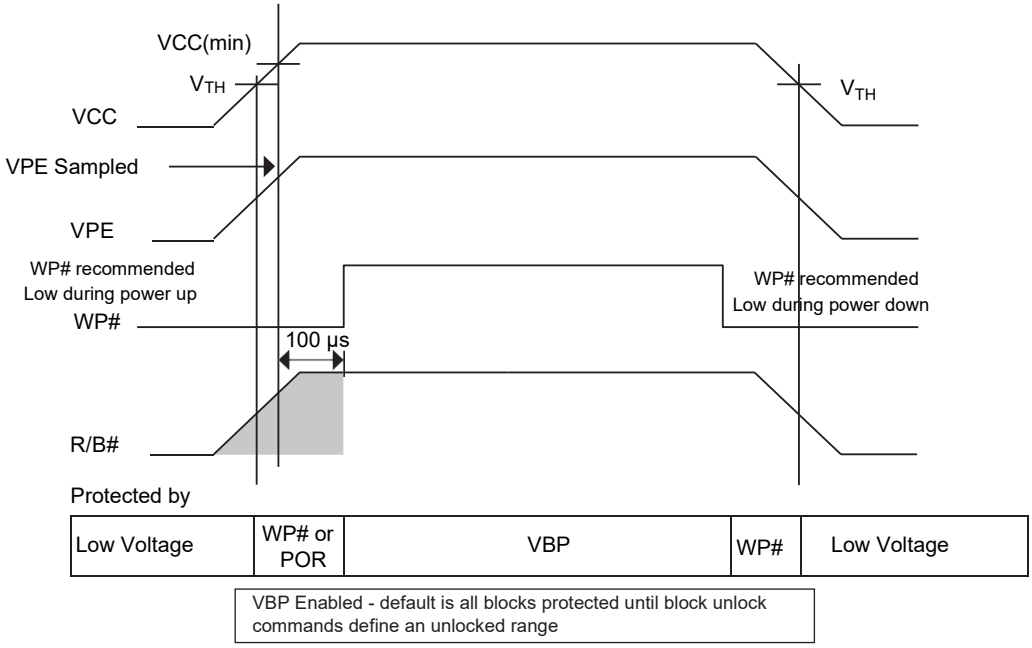
7.29 Legacy OTP Protection Timing

Figure 48. Legacy OTP Protection Timing



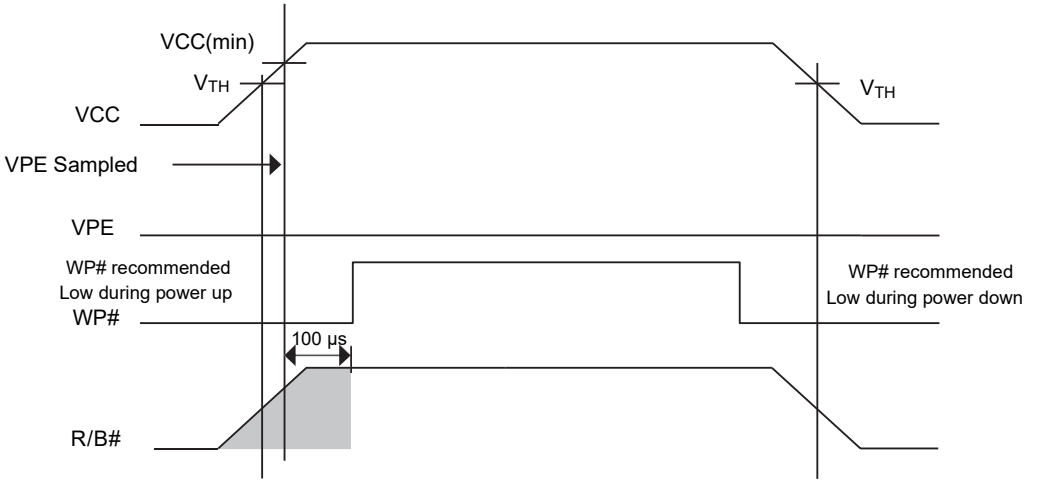
7.30 Power On and Data Protection Timing

Figure 49. VPE High at Power up Timing[81, 82, 83]



Notes
81.V_{TH} = 1.8 Volts (Typ).
82.The VPE pin must be sampled between V_{TH} and V_{CC} (min).
83.During power up, VCC and VPE slopes are equal.

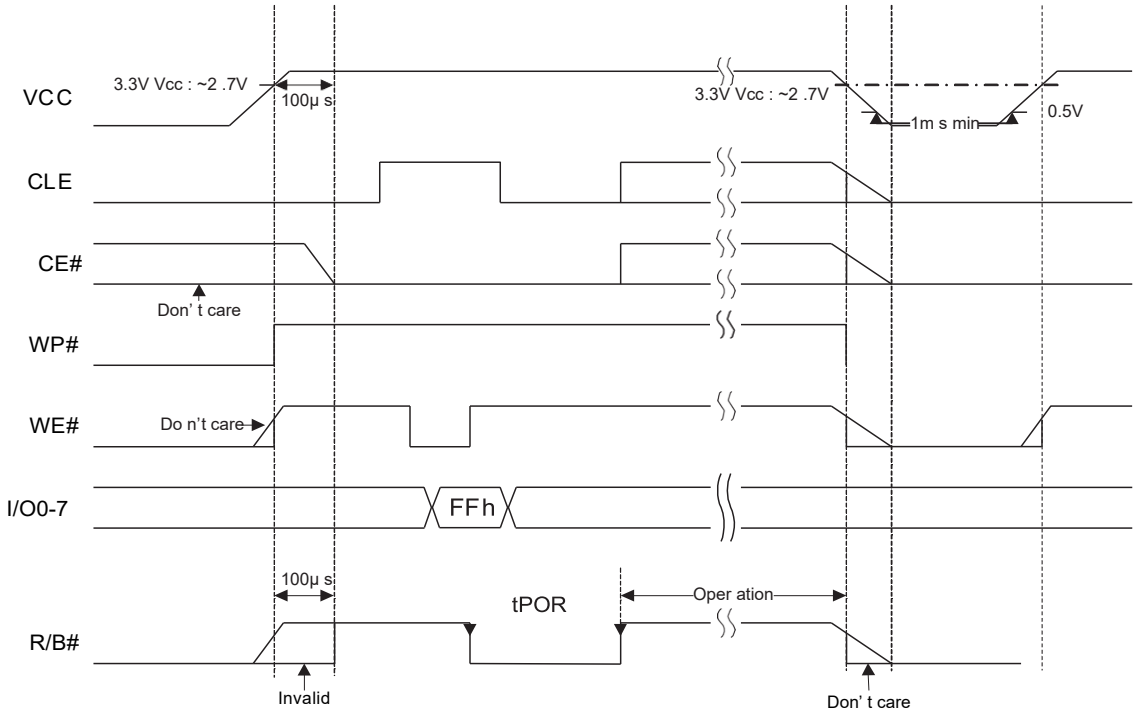
Figure 50. VPE LOW at Power up Timing



Protected by

Low Voltage	WP# or POR	Method other than VBP	WP#	Low Voltage

Figure 51. Device Initialization[84, 85]



Notes

84. Reset (FFh) command is required after power-on and R/B# = high as a first command.
85. During Power-On, VCC should rise monotonically and must remain greater than VLKO (Low VCC Lock-Out Voltage) to execute the initialization process successfully.

7.31 WP# Handling

Figure 52. Program Enabling / Disabling Through WP# Handling

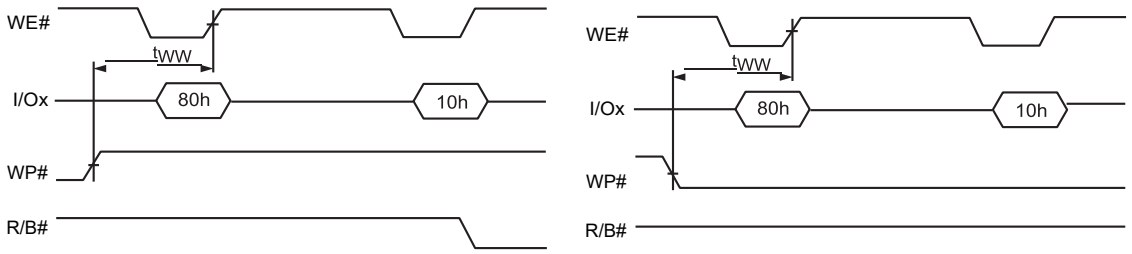
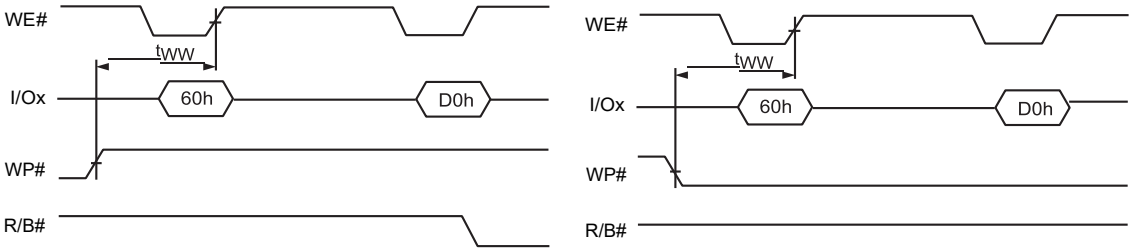


Figure 53. Erase Enabling / Disabling Through WP# Handling

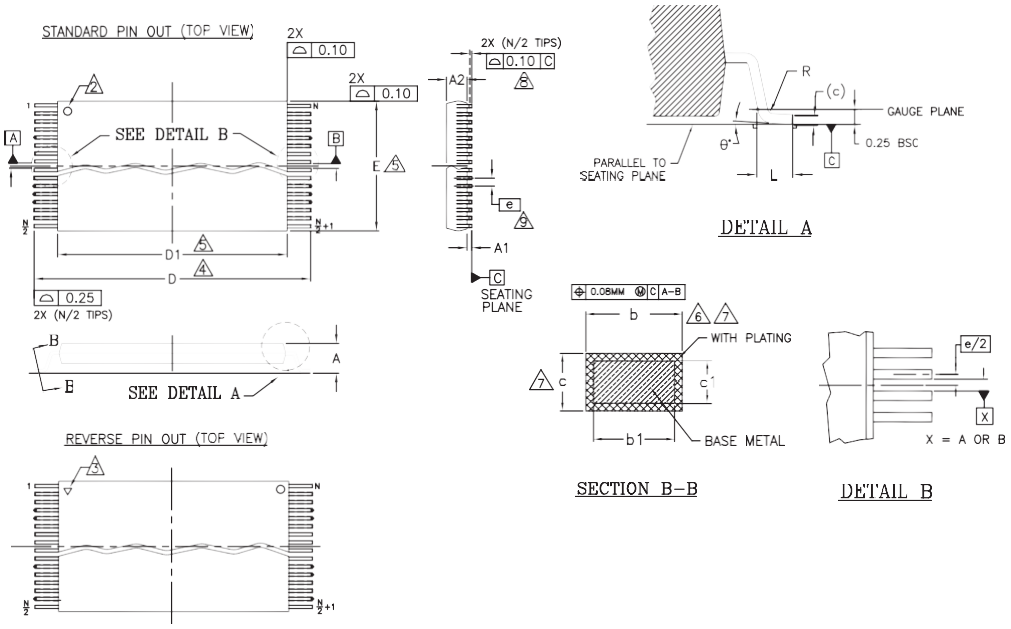


8. Physical Interface

8.1 Physical Diagram

8.1.1 48-Pin Thin Small Outline Package (TSOP)

Figure 54. TS/TSR 48 — 48-lead Plastic Thin Small Outline, 12 x 20 mm, Package Outline



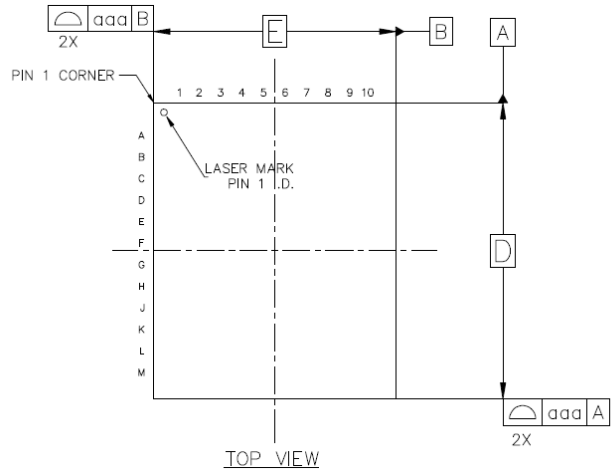
PACKAGE	TS/TSR 48		
JEDEC	MO-142 (D) DD		
SYMBOL	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	---	8
R	0.08	---	0.20
N	48		

NOTES:

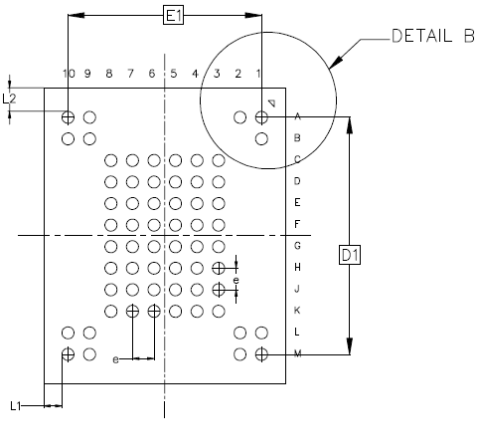
1. DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

5006 \ f16-038 \ 6.5.13

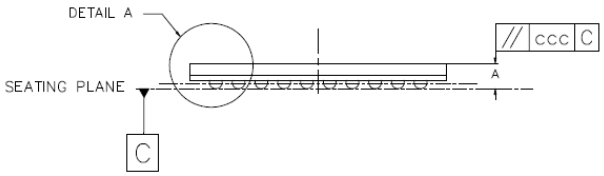
8.1.2 63-ball BGA PACKAGE TYPE



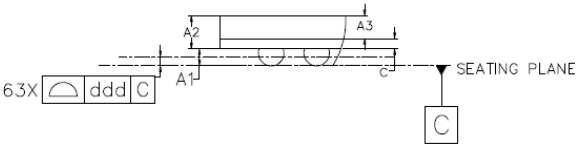
TOP VIEW



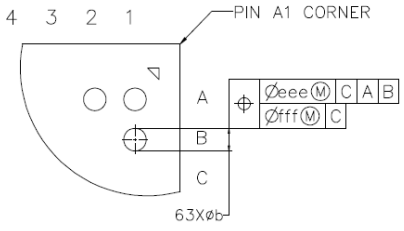
BOTTOM VIEW



SIDE VIEW



DETAIL A(2:1)



DETAIL B(2:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.88	0.96
A1	0.25	0.30	0.35
A2	0.53	0.58	0.63
A3	0.40 BASIC		
c	0.15	0.18	0.21
D	10.90	11.00	11.10
D1	8.80 BASIC		
E	8.90	9.00	9.01
E1	7.20 BASIC		
e	0.80 BASIC		
b	0.40	0.45	0.50
L1	0.675REF		
L2	0.875REF		
aaa	0.15		
ccc	0.15		
ddd	0.15		
eee	0.15		
fff	0.08		

9. System Interface

To simplify system interface, CE# may be unasserted during data loading or sequential data reading as shown in Figure 55. By operating in this way, it is possible to connect NAND flash to a microprocessor.

Figure 55. Program Operation with CE# Don't Care

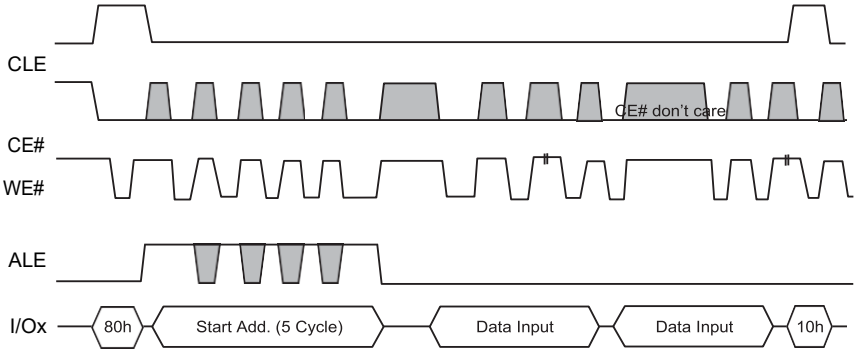


Figure 56. Read Operation with CE# Don't Care

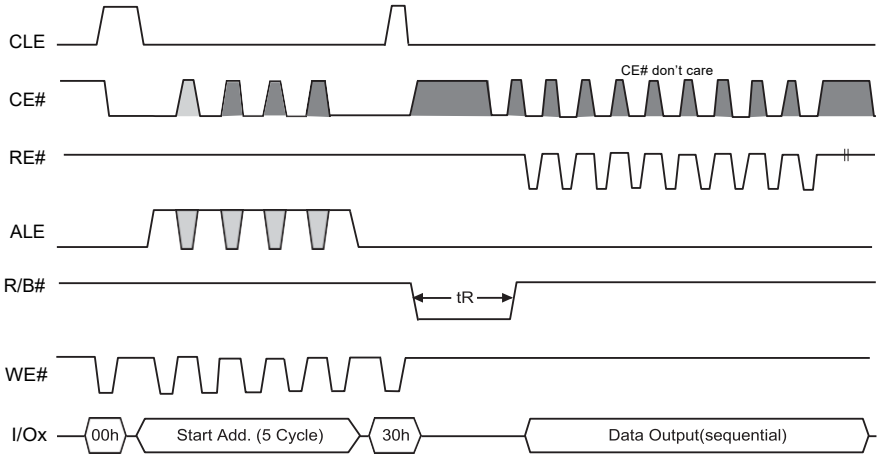
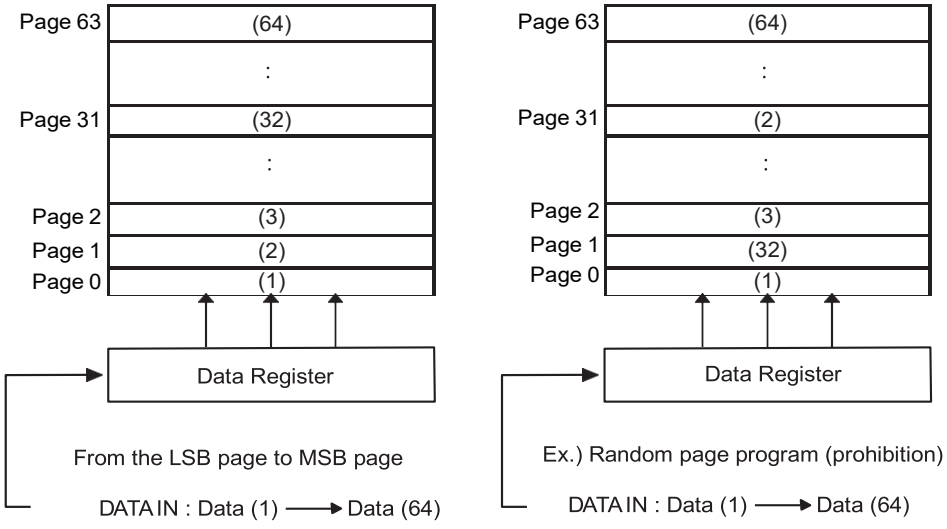


Figure 57. Page Programming Within a Block



10. Error Management

10.1 System Bad Block Replacement

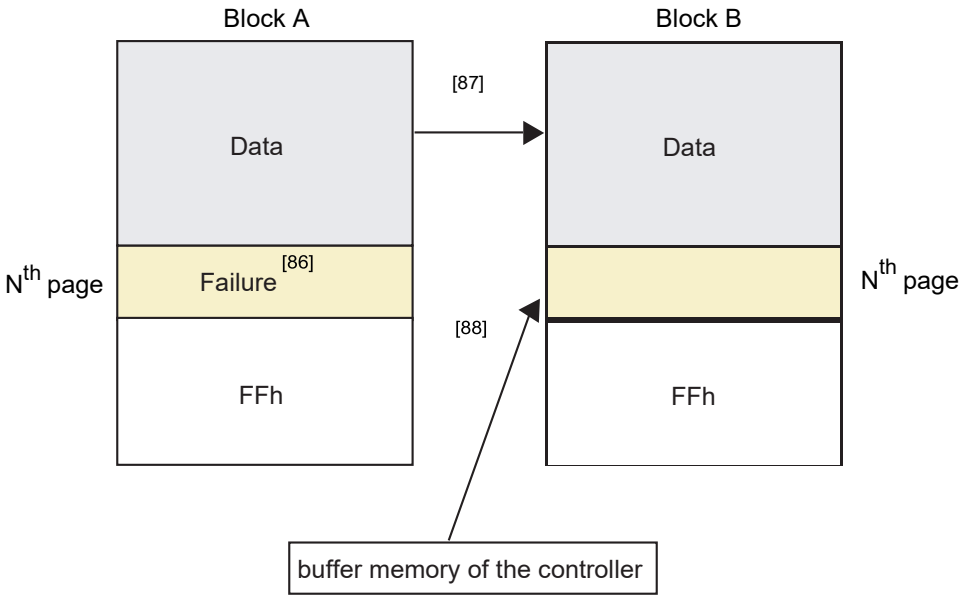
Over the lifetime of the device, additional Bad Blocks may develop. In this case, each bad block has to be replaced by copying any valid data to a new block. These additional Bad Blocks can be identified whenever a program or erase operation reports “Fail” in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. Refer to Table 34 and Figure 58 for the recommended procedure to follow if an error occurs during an operation.

Table 34. Block Failure

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	Check Read Status Register

Figure 58. Bad Block Replacement

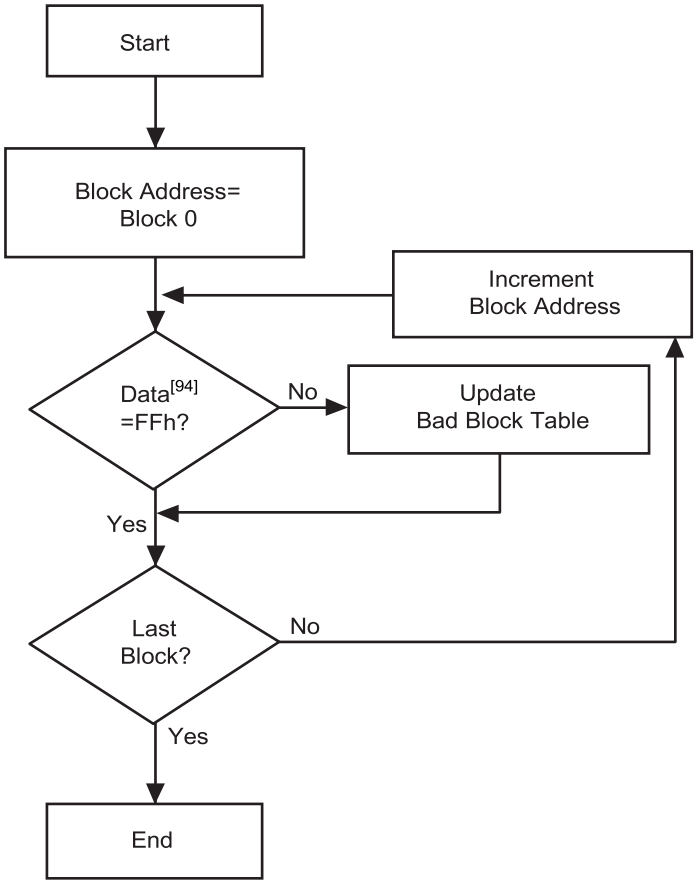


Notes
86.An error occurs on the Nth page of Block A during a program operation.
87.Data in Block A is copied to the same location in Block B, which is a valid block.
88.The Nth page of block A, which is in controller buffer memory, is copied into the Nth page of Block B.
89.Bad block table should be updated to prevent from erasing or programming Block A.

10.2 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased (FFh). The Bad Block Information is written before shipping. Any block where the 1st byte in the spare area of the 1st or 2nd or last page does not contain FFh is a Bad Block. That is, if the first page has an FF value and should have been a non-FF value, then the non-FF value in the second page or the last page will indicate a bad block.The Bad Block Information must be read before any erase is attempted, as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information, it is recommended to create a Bad Block table following the flowchart shown in Figure 59. The host is responsible to detect and track bad blocks, both factory bad blocks and blocks that may go bad during operation. Once a block is found to be bad, data should not be written to that block. Blocks 0-7 are guaranteed good at the time of shipment.

Figure 59. Bad Block Management Flowchart[90]



Note
90. Check for FFh at the 1st byte in the spare area of the 1st, 2nd, and last pages.

11. Document History Page

Publication Version:	V1.0 05/19/2022
Note:	Initial release
V1.2 2022.12	ADD BGA63