
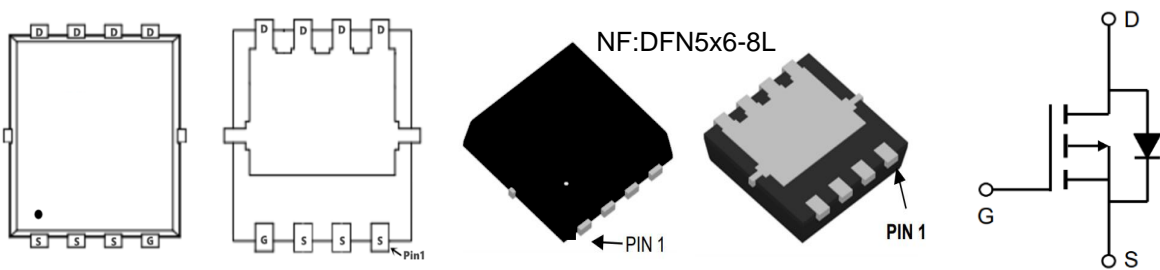


**TM70P03NF**

**P-Channel Enhancement Mosfet**

<p><b>General Description</b></p> <ul style="list-style-type: none"> <li>• Low <math>R_{DS(ON)}</math></li> <li>• RoHS and Halogen-Free Compliant</li> </ul> <p><b>Applications</b></p> <ul style="list-style-type: none"> <li>• Load switch</li> <li>• PWM</li> </ul>	<p><b>General Features</b></p> <p><math>V_{DS} = -30V</math> <math>I_D = -70A</math></p> <p><math>R_{DS(ON)} = 6m\Omega(\text{typ.}) @ V_{GS} = -10V</math></p> <p>100% UIS Tested 100% <math>R_g</math> Tested</p> 
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NF:DFN5x6-8L

Marking: 70P03F

**Absolute Maximum Ratings** ( $T_A = 25^\circ C$  Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current@-10V <sup>1</sup>	$I_D$	$T_C=25^\circ C$	-70
		$T_C=75^\circ C$	-40
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	-175	A
Single Pulse Avalanche Energy <sup>3</sup>	<b>EAS</b>	31	mJ
Avalanche Current	$I_{AS}$	-70	A
Total Power Dissipation <sup>4</sup>	$T_C=25^\circ C$	<b>P<sub>D</sub></b>	31.2
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>1</sup>	$R_{\theta JA}$	61	$^\circ C/W$
Thermal Resistance from Junction-to-Case <sup>1</sup>	$R_{\theta JC}$	4	$^\circ C/W$

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P-Channel Enhancement Mosfet

Electrical Characteristics  $T_c = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$V_{DS} = -24V, V_{GS} = 0V$	-	-	-1	$\mu A$
	$T_J=55^\circ\text{C}$		-	-	-5	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance <sup>2</sup>	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -12A$	-	6	8.8	m $\Omega$
		$V_{GS} = -4.5V, I_D = -8A$	-	9	14	
Forward Transconductance	$g_{fs}$	$V_{DS} = -5V, I_D = -20A$	-	28	-	S
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V, f = 1\text{MHz}$	-	4320	-	pF
Output Capacitance	$C_{oss}$		-	529	-	
Reverse Transfer Capacitance	$C_{rss}$		-	487	-	
<b>Switching Characteristics</b>						
Gate Resistance	$R_g$	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0\text{MHz}$	-	4.0	-	$\Omega$
Total Gate Charge	$Q_g$	$V_{GS} = -10V, V_{DS} = -15V, I_D = -15A$	-	45	-	nC
Gate-Source Charge	$Q_{gs}$		-	8.5	-	
Gate-Drain Charge	$Q_{gd}$		-	12.8	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 2.5\Omega, I_D = -15A$	-	18.9	-	nS
Rise Time	$t_r$		-	15.7	-	
Turn-Off Delay Time	$t_{d(off)}$		-	64.8	-	
Fall Time	$t_f$		-	36.5	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	$I_S = -1A, V_{GS} = 0V$	-	-	-1	V
Continuous Source Current <sup>1,5</sup>	$I_S$	$V_G = V_D = 0V$ , Force Current	-	-	-70	A

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -25A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



# TM70P03NF

# P-Channel Enhancement Mosfet

## Typical Characteristics

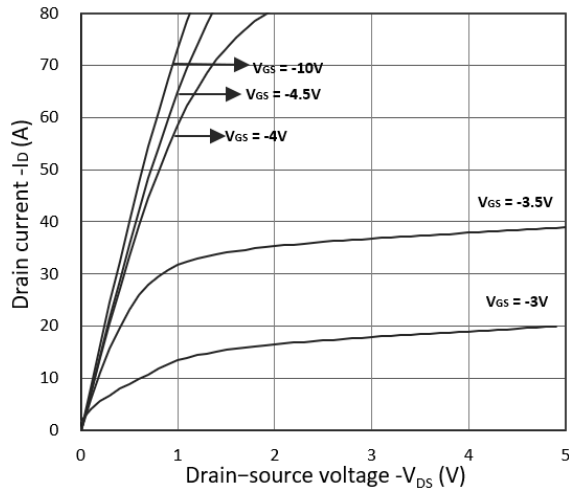


Figure 1. Output Characteristics

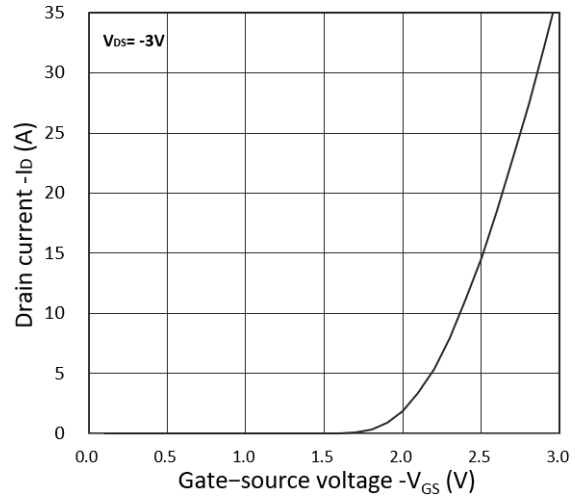


Figure 2. Transfer Characteristics

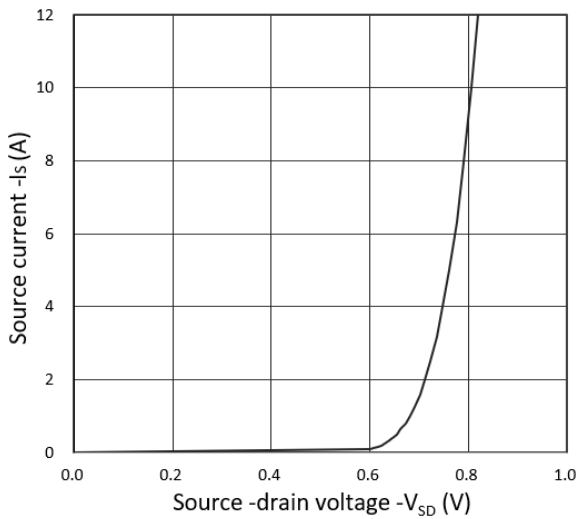


Figure 3. Forward Characteristics of Reverse

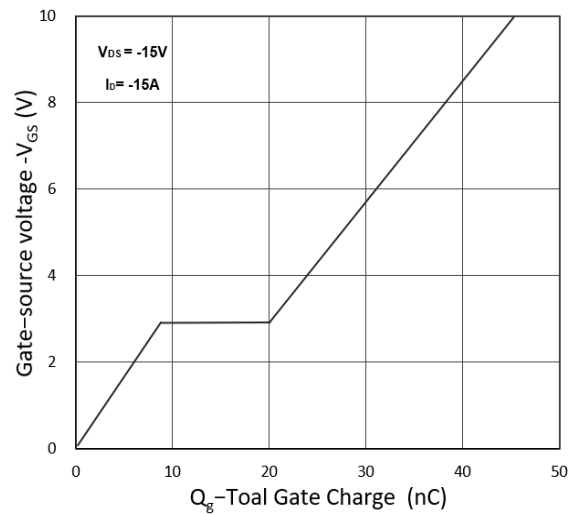


Figure 4. Gate Charge Characteristics

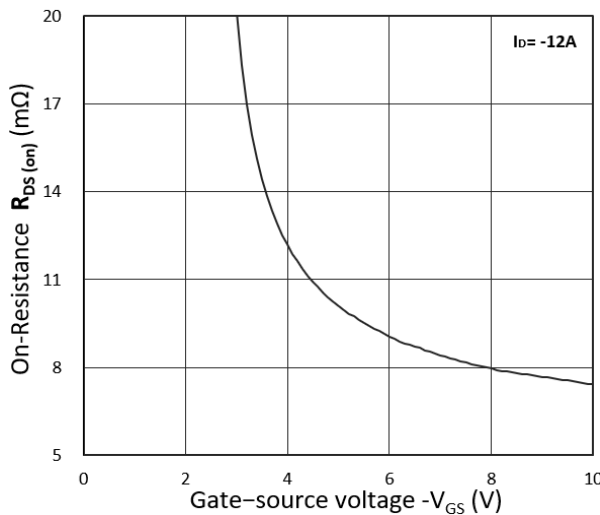


Figure 5.  $R_{DS(on)}$  vs.  $V_{GS}$

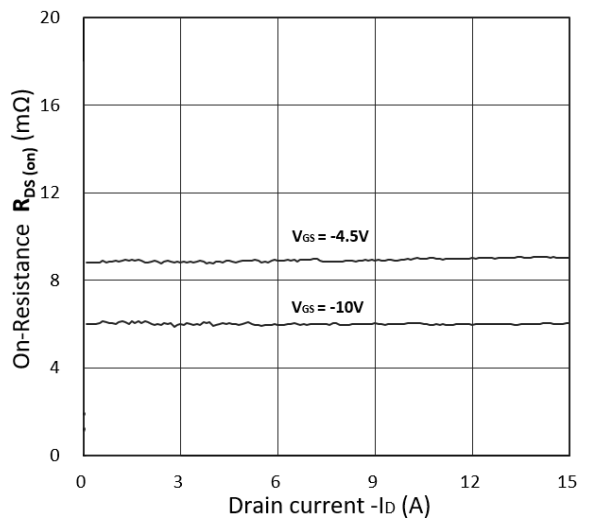


Figure 6.  $R_{DS(on)}$  vs.  $I_D$

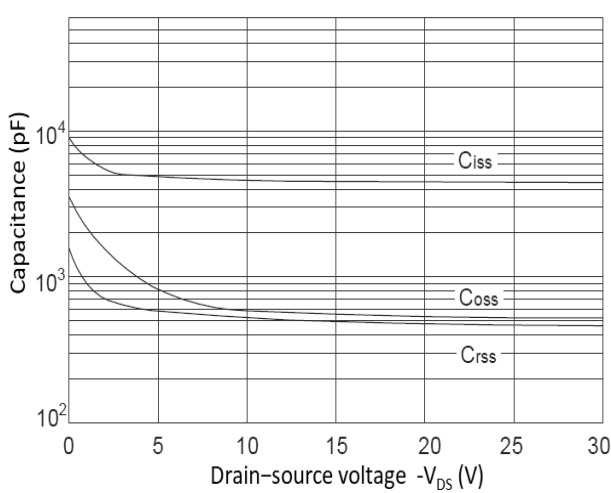


Figure 7. Capacitance Characteristics

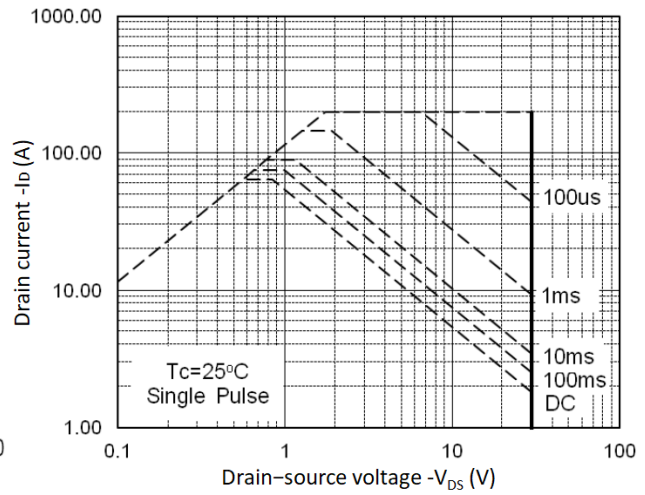


Figure 8. Safe Operating Area

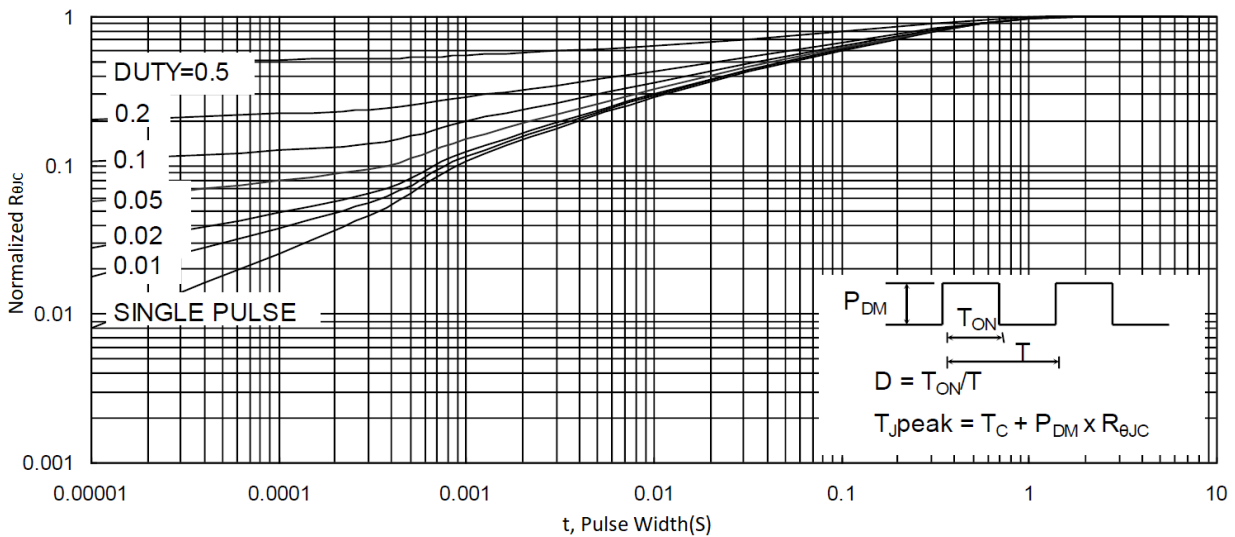


Figure 9. Normalized Maximum Transient Thermal Impedance

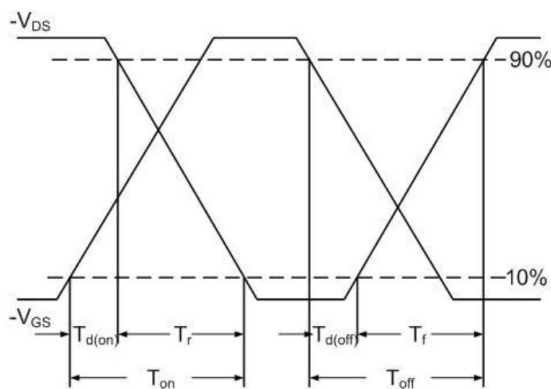


Figure 10. Switching Time Waveform

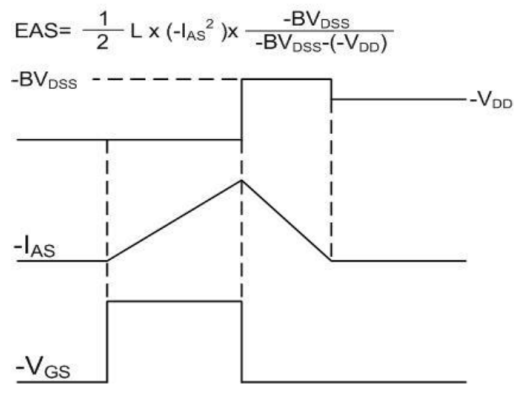
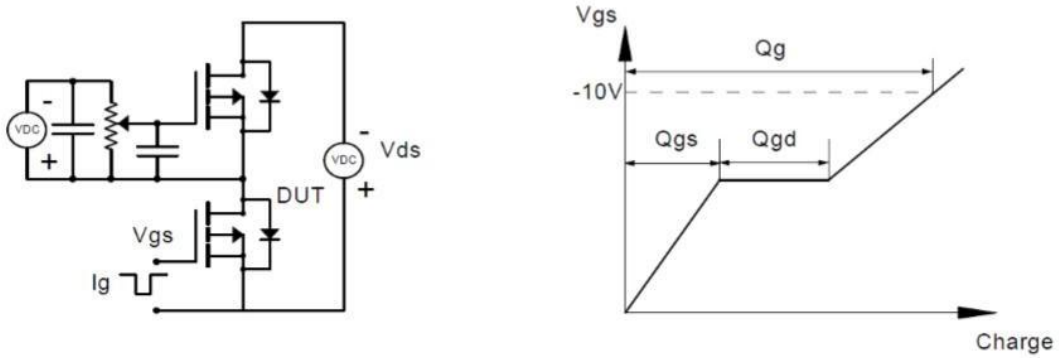


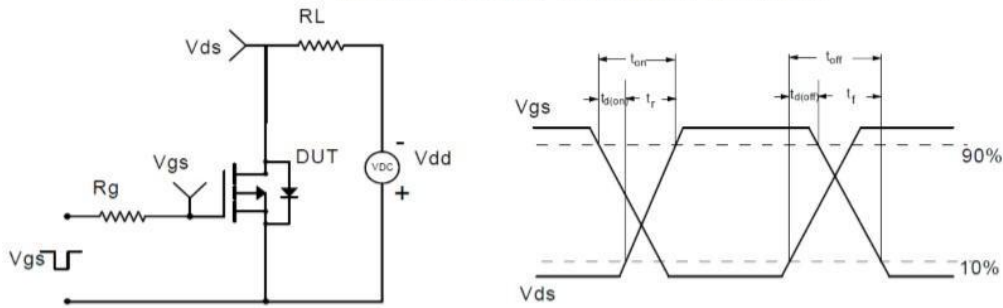
Figure 11. Unclamped Inductive Switching  
Waveform

Test Circuit

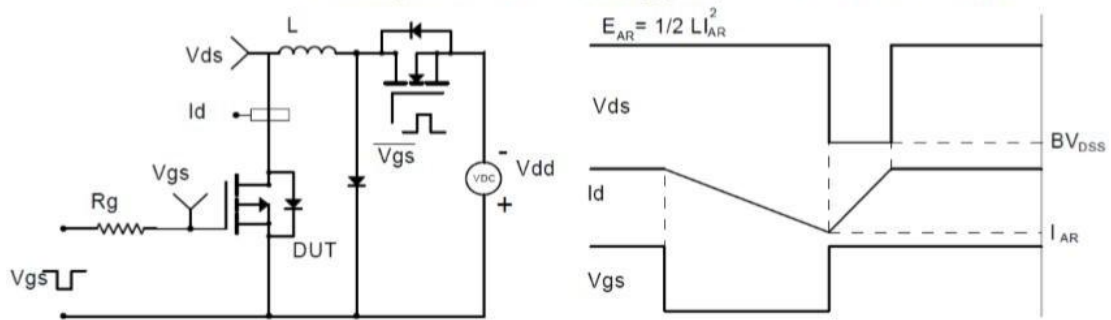
Gate Charge Test Circuit & Waveform



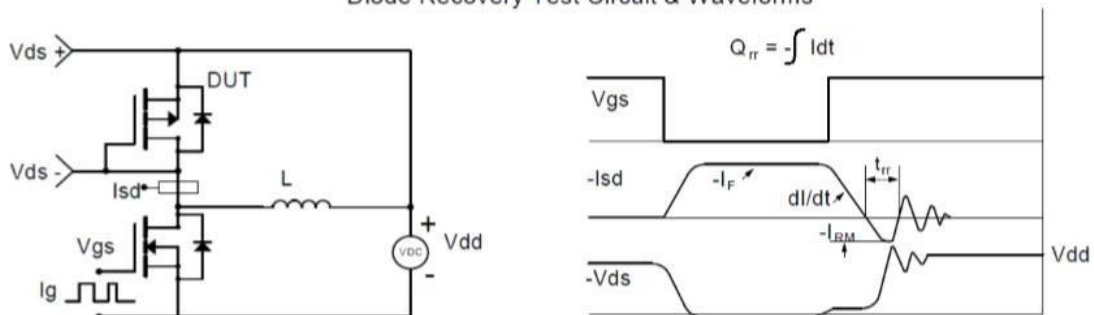
Resistive Switching Test Circuit & Waveforms



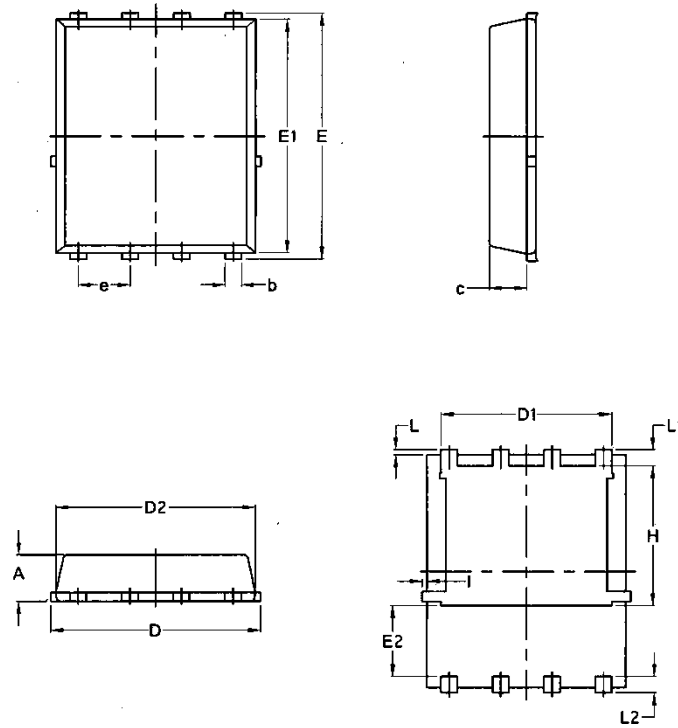
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



## Package Mechanical Data: DFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
l	/	0.18	/	0.0070