



UNI-SEMICONDUCTOR CO., LTD

宇力半导体有限公司



U5115S-6S Data Sheet

V 3.1

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High Current IO+/- 1.0/1.2A HALF-BRIDGE DRIVER

General Description

The U5115S/U5116S Fully operated to +280V is high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels.

The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 280 volts.

Product Summary

V _{OFFSET}	280V max
I _{O+/-}	1.0 A / 1.2A
V _{CCon/off (typ.)}	8V & 7V
t _{on/off (typ.)}	600 & 280ns
Deadtime (typ.)	280 ns
Work Tem	-40 ~150 °C

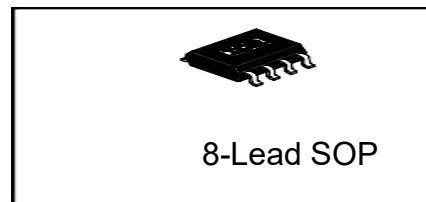
Key Features

- Integrated DBOOT(FR107)
- Floating channel designed for bootstrap operation
- Fully operational to +280V
- Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 7 to 20V
- Undervoltage lockout
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels

Applications

- Home appliances
- Industrial applications and drives
- Motor drivers
- DC, AC, PMDC and PMAC motors
- Induction heating
- HVAC

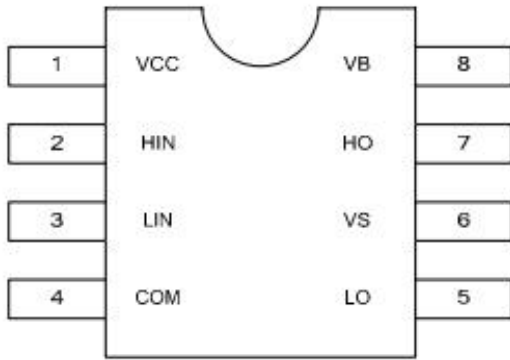
Package



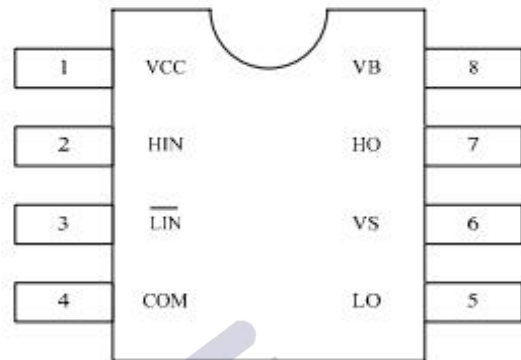
Products Information

Base Part Number	Package Type	Standard OUT		V _{OFFSET}	Logic Control
		IO+	IO-		
U5115S	SOP8	1.0A	1.2A	280V	HIN & $\overline{\text{LIN}}$
U5116S	SOP8	1.0A	1.2A	280V	HIN & LIN

Pin Assignments



U5116S



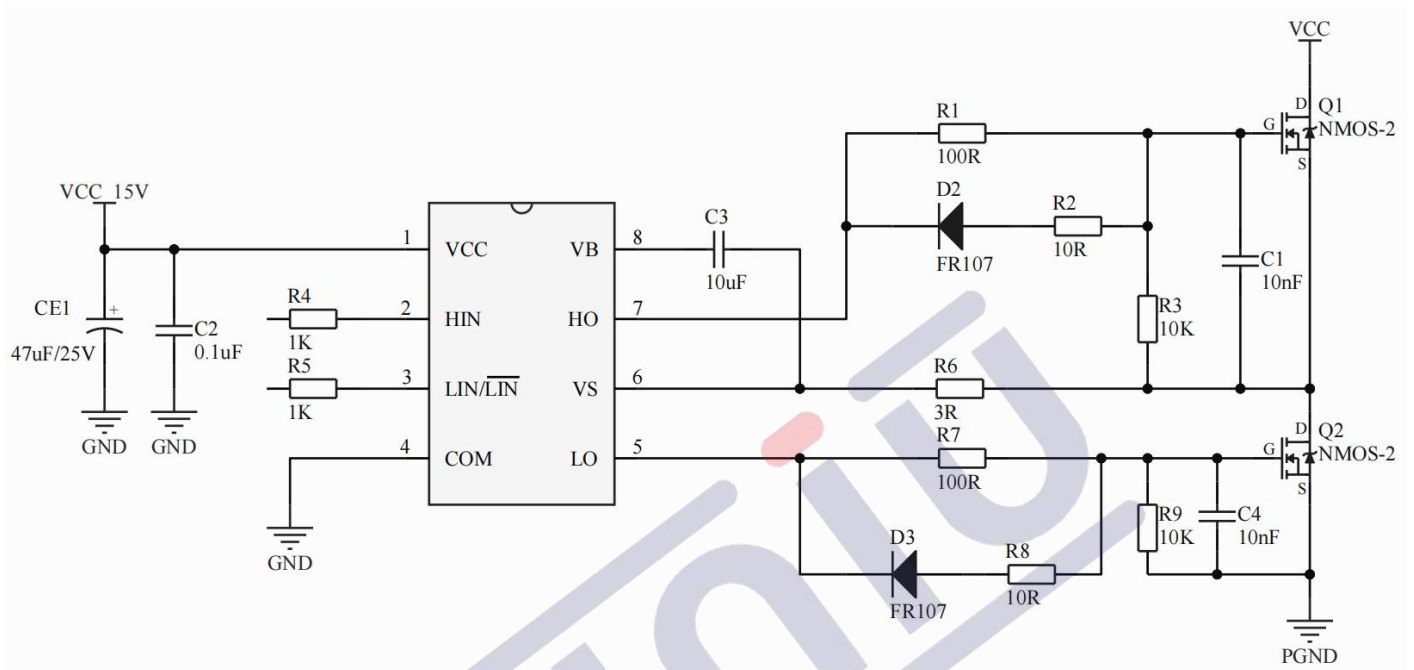
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Pin Function

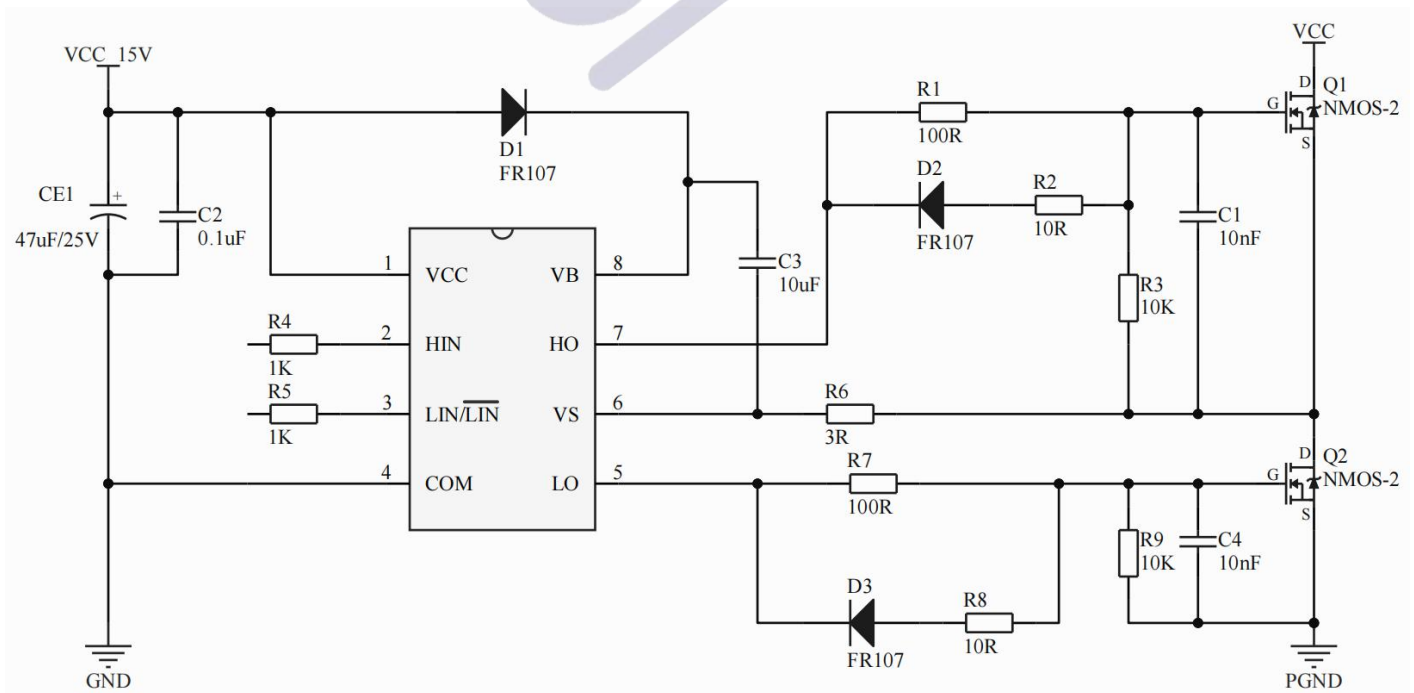
Number	Symbol	Type	Description
1	VCC	P	Low side and logic fixed supply
2	HIN	I	Logic input for high side gate driver outputs (HO), in phase
3	LIN	I	Logic input for low side gate driver outputs (LO), in phase
	$\overline{\text{LIN}}$	I	Logic input for low side gate driver outputs (LO), out of phase
4	COM	P	Low side return
5	LO	O	Low side gate drive output
6	VS	P	High side floating supply return
7	HO	O	High side gate drive output
8	VB	P	High side floating supply

Typical Connection

NO-DBOOT(FR107) Application



DBOOT(FR107) Application



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
VB	High side floating absolute voltage	-0.3	280	V
VS	High side floating supply offset voltage	VB-15	VB+0.3	
VHO	High side floating output voltage	VS-0.3	VB+0.3	
VLO	Low side output voltage	-0.3	V _{cc} +0.3	
V _{cc}	Low side and logic fixed supply voltage	-0.3	25	
VIN	Logic input voltage (HIN & LIN)	-0.3	V _{cc} +0.3	
dVS/dt	Allowable offset supply voltage transient	—	55	V/ns
P _D	Package power dissipation @ TA ≤ +25°C , DIP-8	—	1	W
	Package power dissipation @ TA ≤ +25°C , SOIC-8	—	0.625	
R _{thJA}	Thermal resistance, junction to ambient , DIP-8	—	125	°C/W
	Thermal resistance, junction to ambient , SOIC-8	—	200	
TJ	Junction temperature	-35	150	°C
TS	Storage temperature	-55	175	
TL	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	VS + 7	VS + 20	V
VS	High side floating supply offset voltage	-20.8	200	
VHO	High side floating output voltage	VS	VB	
VLO	Low side output voltage	0	V _{CC}	
V _{CC}	Low side and logic fixed supply voltage	7	20	
VIN	Logic input voltage (HIN&LIN)	0	V _{CC}	
TA	Ambient temperature	-40	150	°C

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 12V$, Typical Connection Figure 1 and $T_A = 25^\circ C$ unless otherwise specified.

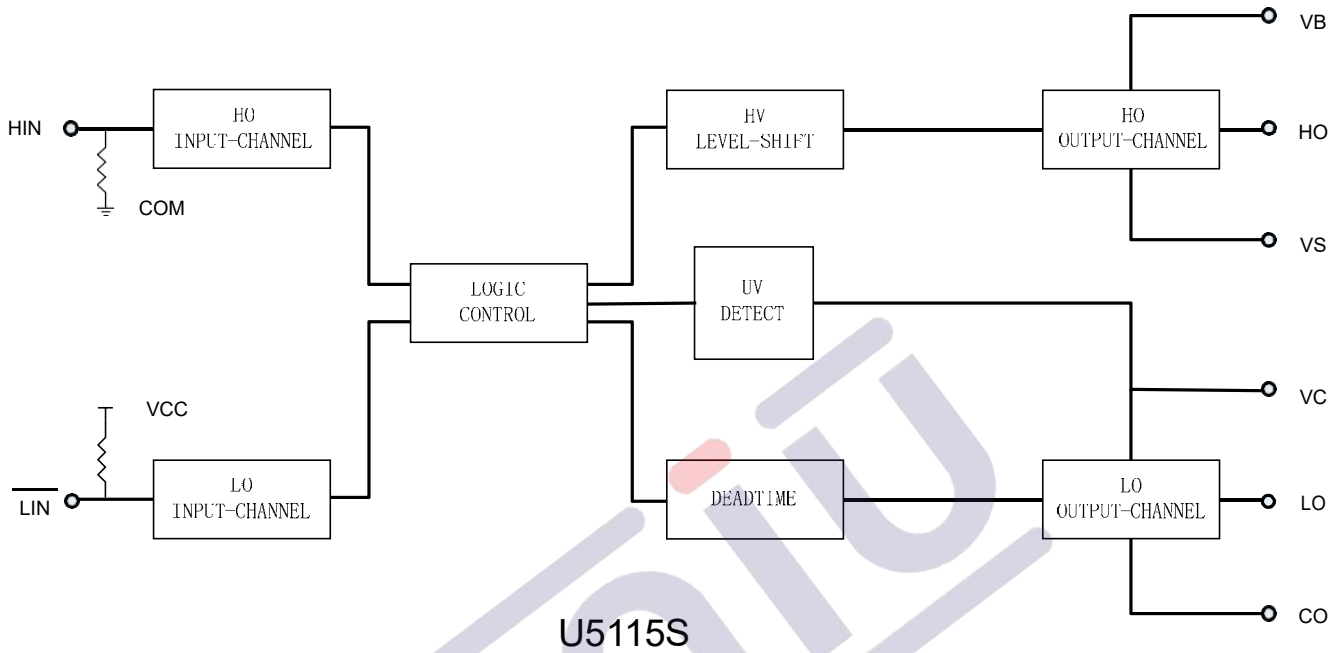
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	600	700	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	280	400		$V_S = 90V$
t_r	Turn-on rise time	—	600	750		
t_f	Turn-off fall time	—	190	300		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	220	280	330		
MT	Delay matching, HS & LS turn-on/off	—	—	60		

Electrical Characteristic

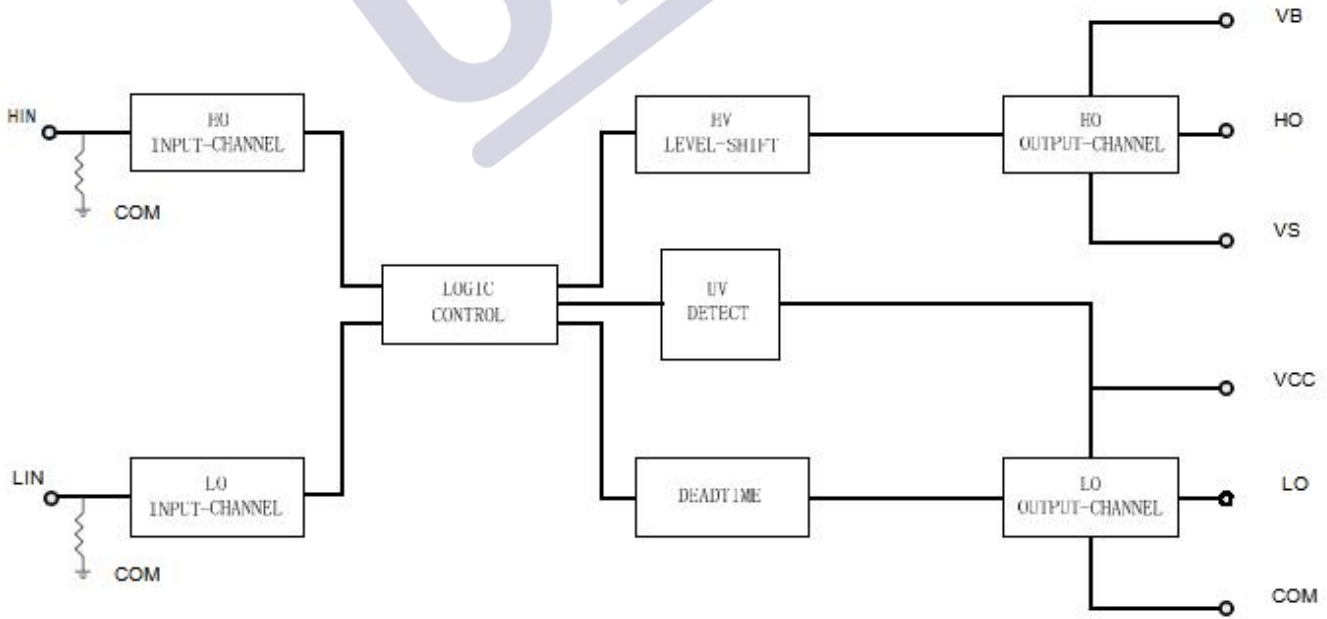
$V_{CC} = V_{BS} = V_{BIAS} = 15V$, $T_A = 25^{\circ}C$, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{CCUV+}	VCC supply under-voltage positive going threshold (U5115S)	8.6	9.4	10.2	V	
V_{CCUV-}	VCC supply under-voltage negative going threshold (U5115S)	8.0	8.8	9.6		
V_{CCHYS}	VCC supply under-voltage lockout hysteresis (U5115S)	0.4	0.6	—		
V_{CCUV+}	VCC supply under-voltage positive going threshold (U5116S)	6.4	7.2	8.0		
V_{CCUV-}	VCC supply under-voltage negative going threshold (U5116S)	6.0	6.8	7.6		
V_{CCHYS}	VCC supply under-voltage lockout hysteresis (U5116S)	0.3	0.4	—		
IQCC	Quiescent VCC supply current	—	300	500	uA	$V_{in} = 0V$ or 5V
IQBS	Quiescent VBS supply current	—	100	200		$V_{in} = 0V$ or 5V
ILK	Offset supply leakage current	—	—	50		$V_B = V_S = 90V$
V_{IH}	Logic "1" (HO) & Logic "0" (LO) input voltage	2.5	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" (HO) & Logic "1" (LO) input voltage	—	1.6	—		$V_{CC} = 10V$ to 20V
IIN+	Logic "1" input bias current	—	3	10	uA	$V_{IN} = 5V$ $L_{IN} = 0V$
IIN-	Logic "0" input bias current	—	—	1		$V_{IN} = 5V$ $L_{IN} = 0V$
VOH	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_o = 0A$
VOL	Low level output voltage, V_O	—	—	100		$I_o = 0A$
IO+	Output high short circuit pulsed current	—	1000	—	mA	$V_O = 0V$ $V_{IN} = V_{IH}$ $PW \leq 10 \mu s$
IO-	Output low short circuit pulsed current	—	1200	—		$V_O = 15V$ $V_{IN} = V_{IL}$ $PW \leq 10 \mu s$

Block Diagram

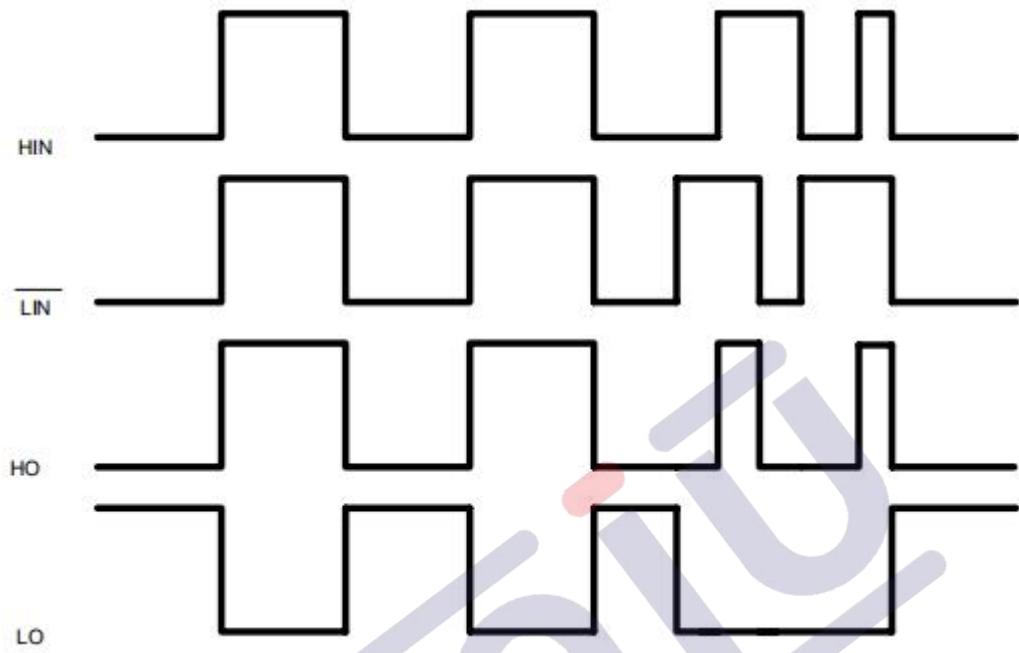


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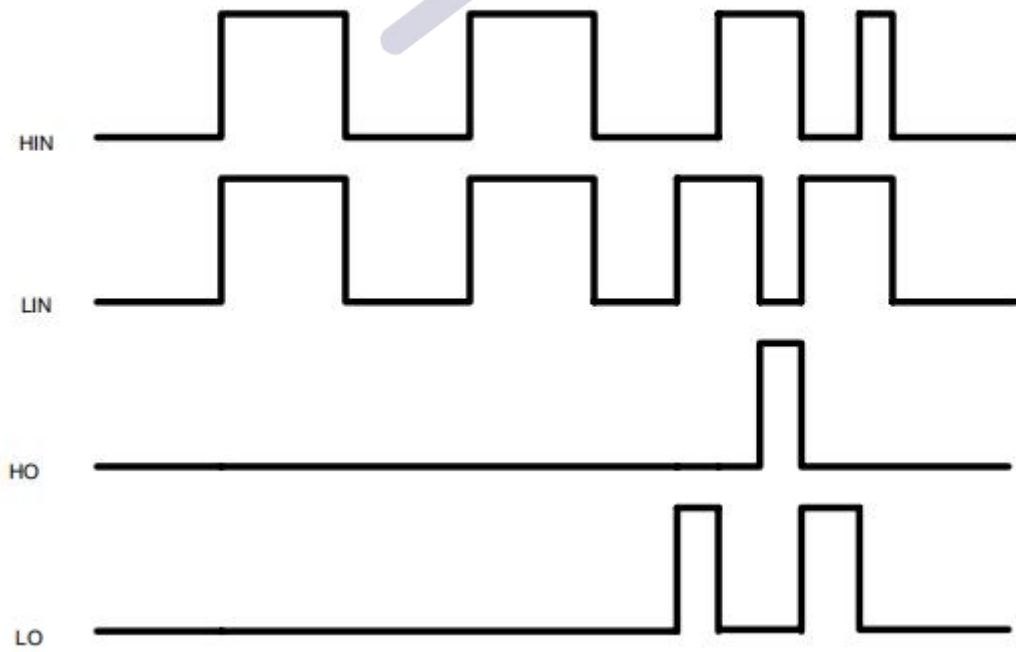


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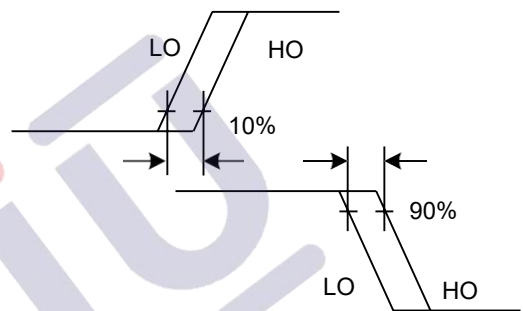
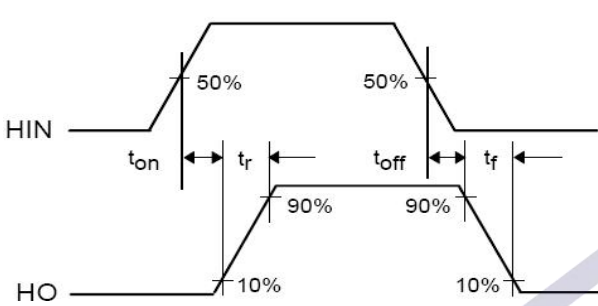
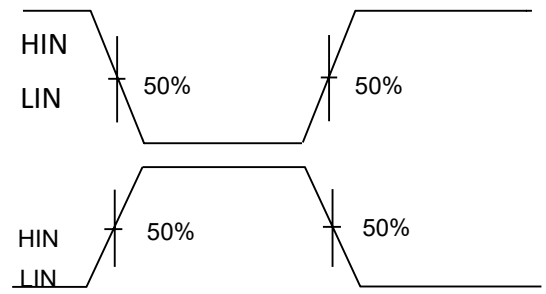
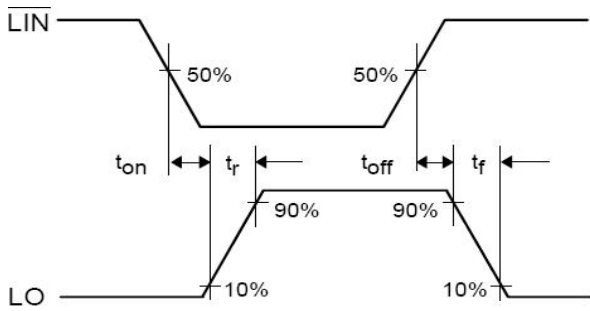
Time waveform



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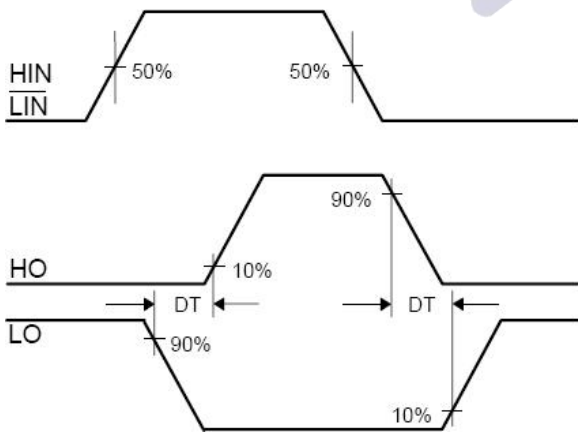


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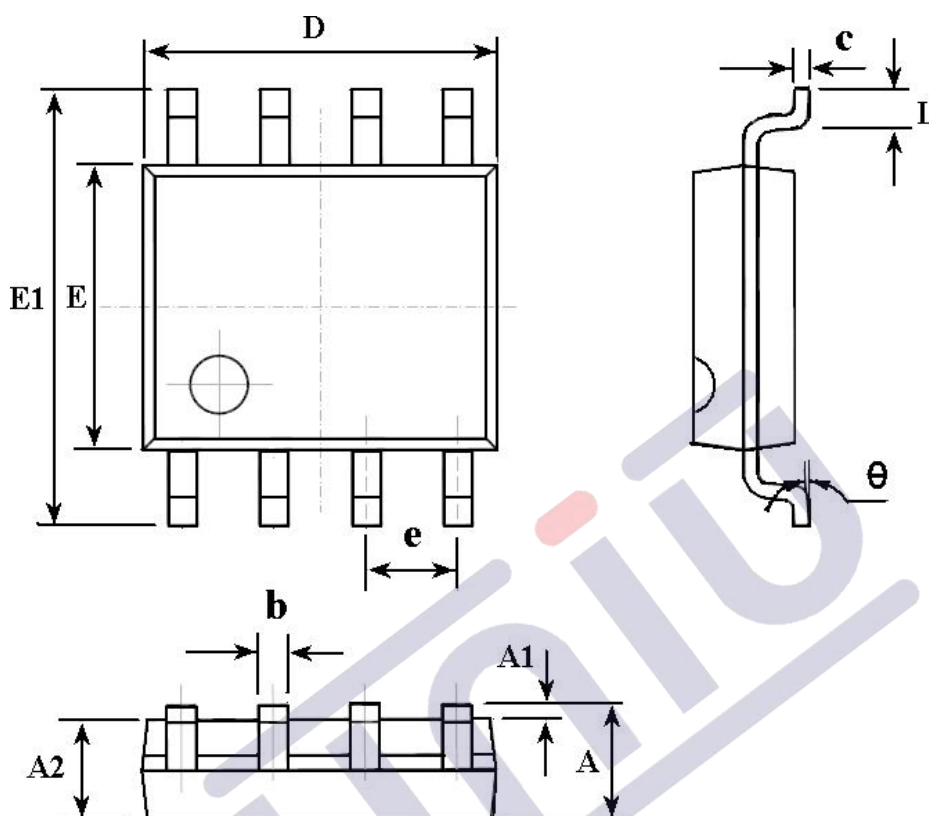
Switching Time Waveform Definitions

Delay matching time Definitions



Deadtime Waveform Definitions

Packaging information SOP8



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2019/05/11	2.0	Change the package
2021/10/18	3.0	Layout adjustment
2022/06/11	3.1	Change the header

2.免责声明

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