ZHEJIANG UNIU-NE Technology CO.,LTD

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U3315-6 Data Sheet

V 3.0

High Current IO+/- 1.2/1.5A 3-PHASE BRIDGE DRIVER

General Description

U3315/6 is a high-speed 3-phase gate driver for power MOSFET and IGBT devices with three independent high and low side referenced output channels. Built-in dead time protection and shoot- through protection prevent damage to the half-bridge. The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. A novel high-voltage BCD process and common-mode noise canceling technique provide stable operation of high-side drivers under high dV/dt noise conditions while achieving excellent negative transient voltage tolerance. low-PW consumption isincluded so that standby mode may be used to set thechip into a low quiescent current state to realize long battery lifetime.

Key Features

- Floating channel designed for bootstrap operation
- Fully operational to +300 V
- Tolerant to negative transient voltage
- Gate drive supply range from 4.5V to 20V
- Independent 3 half-bridge drivers
- Low side output out of phase with inputs. High side outputs out of phase
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity

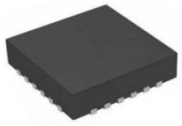
Applications

- E-BIKE/electric power tool 3-phase motor driver
- Battery-powered mini/micro motor control
- General purpose inverter

Product Summary

V_{OFFSET}	300V max
I_O+/-	1.2 A / 1.5A
VCC	4.5V to 20V
$t_{on/off}$ (typ.)	220 & 110ns
Work Tem	-40 ~150 ℃

Package



QFN24

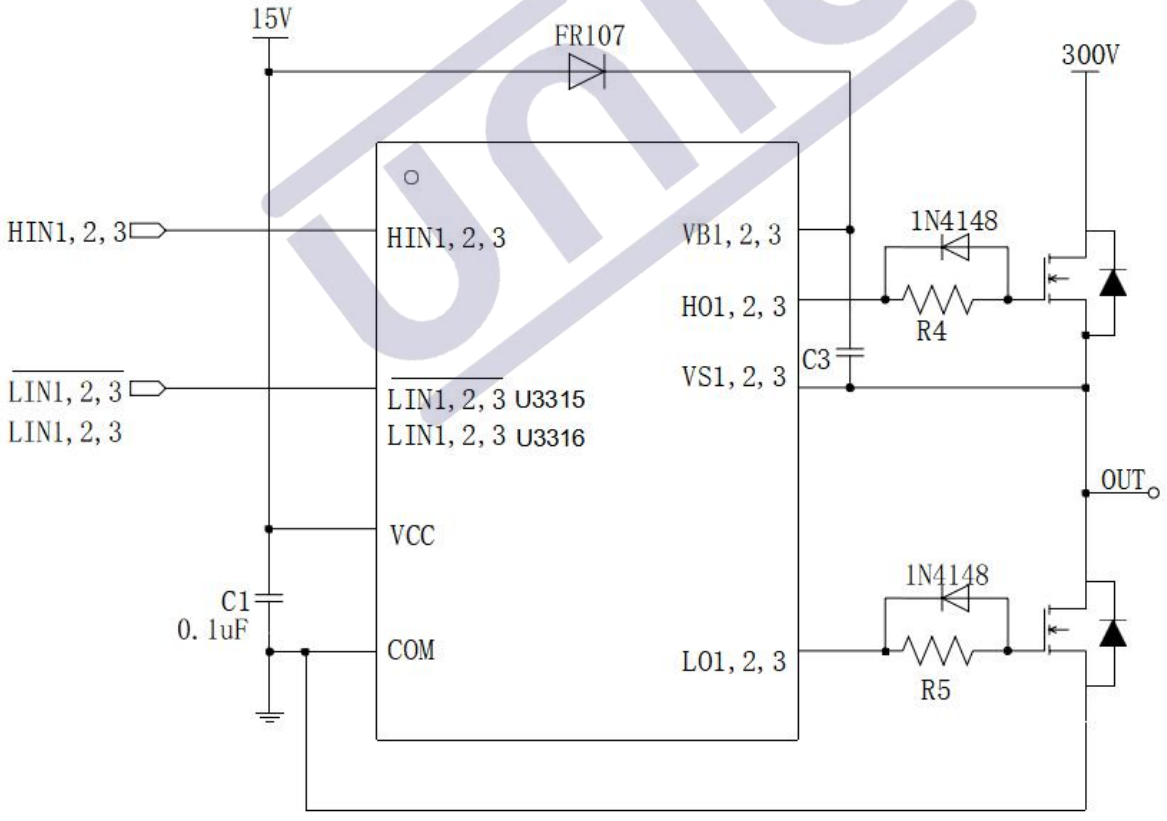
20-PIN TSSOP

Products Information

Base Part Number	Package Type	Standard OUT		V_{OFFSET}	Logic Control
		IO+	IO-		
U3315	QFN24	1.2A	1.5A	300V	HIN & $\overline{\text{LIN}}$
U3316	QFN24	1.2A	1.5A	300V	HIN & LIN

Base Part Number	Package Type	Standard OUT		V_{OFFSET}	Logic Control
		IO+	IO-		
U3315	TSSOP20	1.2A	1.5A	300V	HIN & $\overline{\text{LIN}}$
U3316	TSSOP20	1.2A	1.5A	300V	HIN & LIN

Typical Application

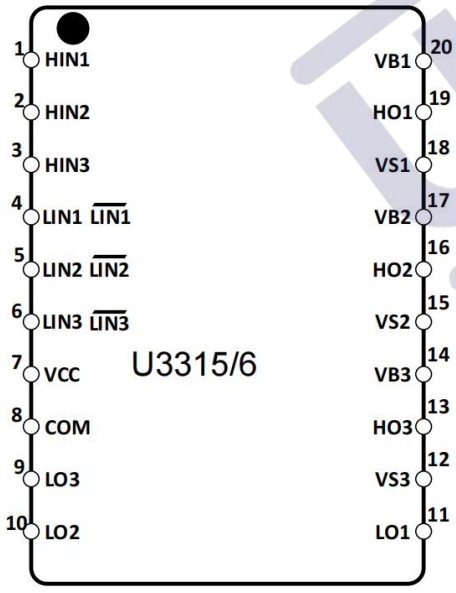


Pin Function

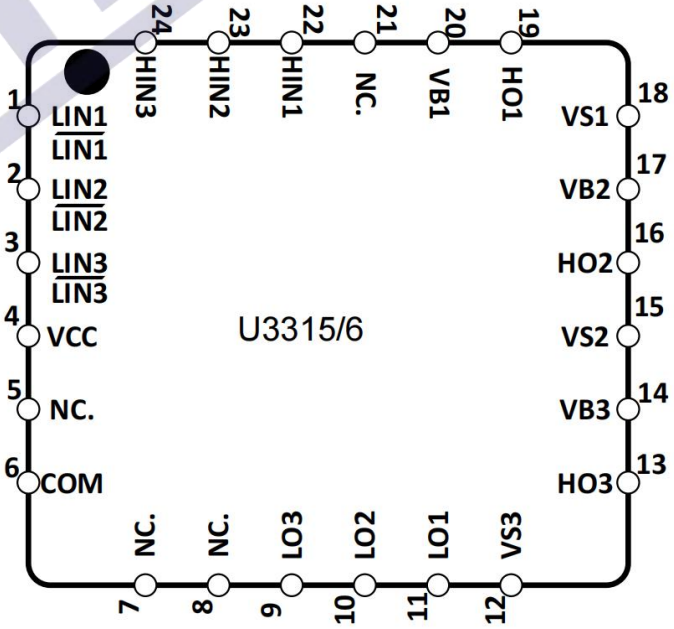
Number	Symbol	Description
1	VCC	Low side and logic fixed supply
2	HIN1,2,3	Logic inputs for high side gate driver outputs(HO1,2,3),in phase
3	U3316 LIN1,2,3	Logic inputs for high side gate driver outputs(LO1,2,3),in phase
4	U3315 $\overline{\text{LIN1,2,3}}$	Logic inputs for high side gate driver outputs(LO1,2,3),out of phase
5	COM	Logic Ground
6	VB1,2,3	High side floating supply
7	HO1,2,3	High side gate driver outputs
8	VS1,2,3	High voltage floating supply returns
9	LO1,2,3	Low side gate driver output

Packages

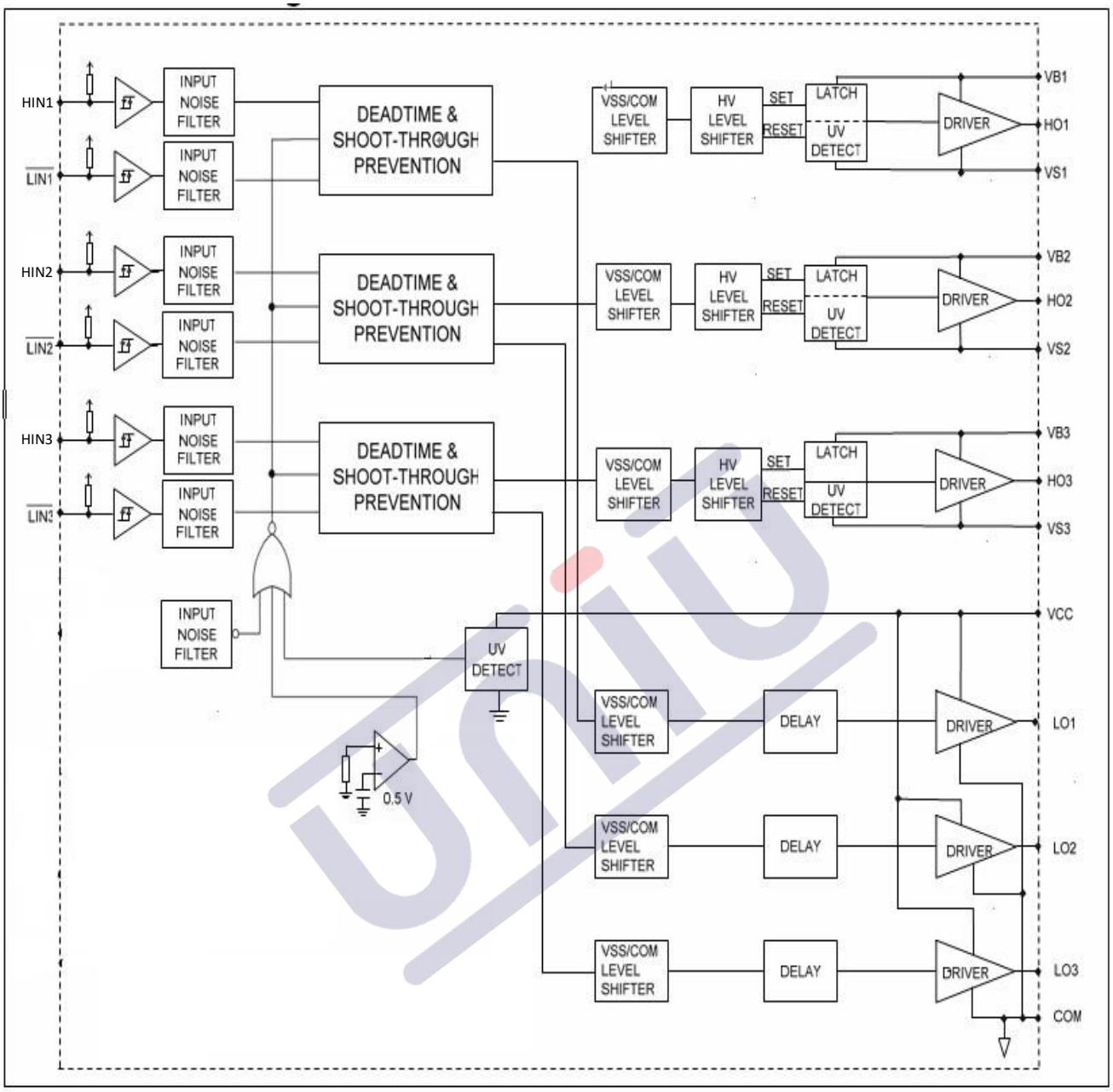
20-PIN TSSOP



QFN24



Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
VS	High side offset voltage		VB 1,2,3-25	VB 1,2,3+ 0.3	V
VB	High side floating supply voltage		-0.3	300	
VHO	High side floating output voltage		VS1,2,3 -0.3	VB 1,2,3+ 0.3	
VCC	Low side and logic fixed supply voltage		-0.3	25	
COM	Logic ground		VCC- 25	VCC+0.3	
VLO1,2,3	Low side output voltage		-0.3	VCC+0.3	
VIN	Input voltage		COM-0.3	Lower of (COM+15) or (VCC+ 0.3)	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
PD	Package power dissipation @ TA ≤+25 °C	TSSOP20	—	1.5	W
		QFN24	—	1.6	
RthJA	Thermal resistance, junction to ambient	TSSOP20	—	83	°C/W
		QFN24	—	78	
TJ	Junction temperature		—	150	°C
TS	Storage temperature		-55	150	
TL	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure . For proper operation the device should be used within the recom- mended conditions. All voltage parameters are absolute referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min	Max	Units
VB1,2,3	High side floating supply voltage	VS1,2,3+4.5	VS1,2,3+20	V
VS1,2,3	High side floating supply offset voltage	Note 1	260	
VHO1,2,3	High side output voltage	VS1,2,3	VB1,2,3	
VLO1,2,3	Low side output voltage	0	VCC	
VCC	Low side and logic fixed supply voltage	4.5	20	
VIN	Logic input voltage	COM	COM + 5	
TA	Ambient temperature	-40	125	°C

Note 1: Logic operational for VS of COM

Electrical Characteristic

(V_{CC}–COM)=(V_B–V_S)=15V. Ambient temperature T_A=25ºC unless otherwise specified. The $V_{IN,TH,}$ V_I, and I_{IN} parameters are referenced to COM and are applicable to all channels. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to, COM. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
Quiescent VCC supply current	I_{QVCC1}	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, V_{ENB}=0	210	330	450	μA
Quiescent VCC supply current in standby mode	I_{QVCC2}	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, V_{ENB}=5	-	46	80	
operating VCC supply current	I_{VCCOP}	$f_{LIN1,2,3}$=20KH, $f_{HIN1,2,3}$=20KH,	-	1500	-	
VCC supply under-voltage positive going threshold	V_{CCUV+}	-	2.9	4.2	5.5	V
VCC supply under-voltage negative going threshold	V_{CCUV-}	-	2.5	3.8	5.1	
VCC supply under-voltage lockout hysteresis	V_{CCHYS}	-	-	0.4	-	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}	-	2.5	3.8	4.5	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}	-	2.2	3.5	4.5	
High side VBS supply under-voltage lockout hysteresis	V_{BSUVHS}	-	-	0.3	-	
High side quiescent VBS supply current	I_{QBS}	V_{BS}=15V	25	45	65	μA
Offset supply leakage current	I_{LK}	V_B=V_S=260V V_{CC}=0V	-	-	10	
Logic Input Section						
Logic HIGH input voltage HIN1,2,3, LIN1,2,3 and ENB	V_{IH}	-	2.5	-	-	V
Logic LOW input voltage HIN1,2,3, LIN1,2,3 and ENB	V_{IL}	-	-	-	0.8	
Input positive going threshold	$V_{IN,TH+}$	-	-	1.9	-	
Input negative going threshold	$V_{IN,TH-}$	-	-	1.4	-	
Logic HIGH input bias current	I_{IN+}	V_{IN}=5V	-	50	-	μA
Logic LOW input bias current	I_{IN-}	V_{IN}=0	-	0	-	
Gate Driver Output Section						
High side output HIGH short-circuit pulse current	I_{HO+}	V_{HO}=V_S=0	-	1.2	-	A
High side output LOW short-circuit pulse current	I_{HO-}	V_{HO}=V_B=15V	-	1.5	-	
Low side output HIGH short-circuit pulse current	I_{LO+}	V_{LO}=0	-	1.2	-	
Low side output LOW short-circuit pulse current	I_{LO-}	V_{LO}=V_{CC}=15V	-	1.5	-	
Allowable negative VS voltage for HIN1,2,3 signal propagation to HO1,2,3	V_{SN}	V_{BS}=15V	-	-12	-	V

Electrical Characteristic

(V_{CC}–COM)=(V_B–V_S)=15V ,$V_{S1,2,3}$=COM, and C_{load}=1nF unless otherwise specified, ambient temperature T_A=25ºC.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	t_{on}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	-	220	260	ns
Turn-off propagation delay	t_{off}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3=0}$, $V_{S1,2,3}$=0	-	110	140	
Turn-on rise time	t_r	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	-	37	-	
Turn-off fall time	t_f	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0	-	30	-	
Dead time	DT	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0 and 5V, without external dead time	-	100	-	
Dead time matching (all six channels)	MDT	without external dead time	-	-	50	
Delay matching (all six channels)	MT	external dead time > 1000ns	-	-	50	
Output pulse-width matching	PM	external dead time > 1000ns, PW_{IN}=10μs, PM=PW_{OUT}–PW_{IN}	-	-	50	

LOW SIDE POWER SUPPLY: VCC

VCC is the low side supply and it provides power to both input logic and low side output power stage. The built-in under- voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than V_{CCUV+} =4.2V is present, shown as Figure. 1. The U3315/6 shuts down all the gate driver outputs, when the VCC supply voltage is below V_{CCUV-} =3.8 V, shown as Figure. 1. This prevents the external power devices against extremely low gate voltage levels during on-state which may result in excessive power dissipation.

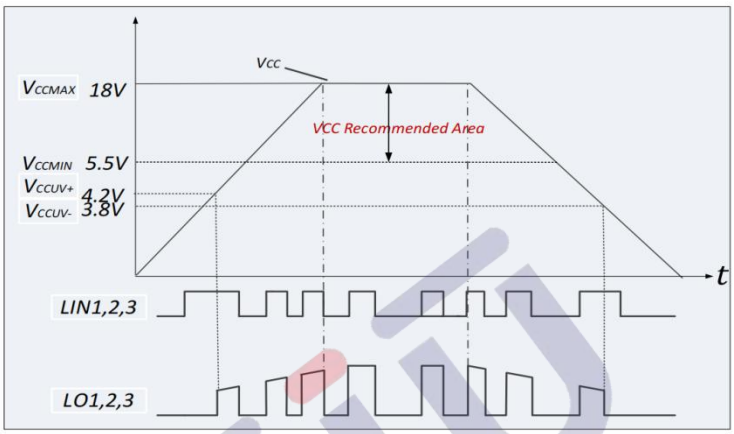


Figure. 1 VCC supply UVLO operating area

HIGH SIDE POWER SUPPLY: VBS (VB1-VS1, VB2-VS2, VB3-VS3)

VBS is the high side supply voltage. The total high side circuitry may float with respect to COM following the external high side power device emitter/source voltage. Due to the internal low power consumption, the entire high side circuitry may be supplied by bootstrap topology connected to VCC, and it may be powered with small bootstrap capacitors. The device operating area as a function of the supply voltage is given in Figure. 2.

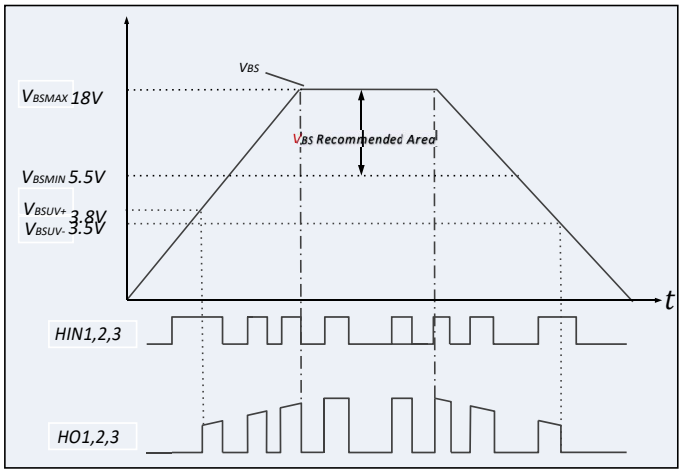


Figure. 2 VBS supply UVLO operating area

LOW SIDE AND HIGH CONTROL INPUT LOGIC: HIN&LIN (HIN1, 2, 3/LIN1, 2, 3)

The Schmitt trigger threshold of each input is designed low enough to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Input Schmitt trigger and advanced noise filtering provide noise rejection of short input pulses. An internal pull-down resistor of about 200kΩ (positive logic) pre-biases each input during VCC supply start-up state. The minimum recommended input pulse-width is 300ns for proper operation of the driver.

SHOOT-THROUGH PREVENTION

The U3315/6 is equipped with shoot-through protection circuitry (also known as cross conduction prevention circuitry). Figure. 3 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. When the inputs controlling both high-side and low-side drivers are both logic HIGH, then both driver outputs are pulled down to logic LOW to shut down two power devices in the same bridge.

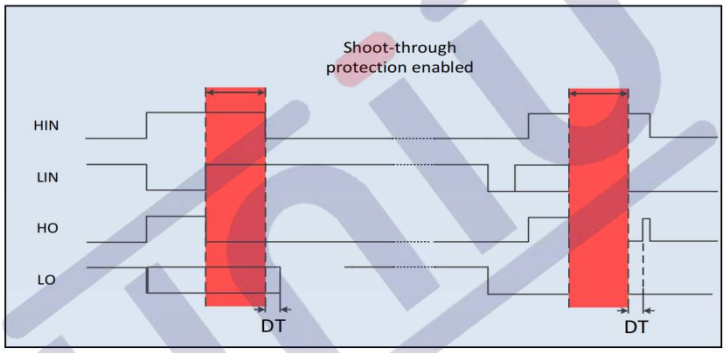


Figure. 3 Shoot-through prevention

DEAD TIME PROTECTION

The U3315/6 features integrated fixed dead time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off. This is done to ensure that the power switch has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT. External dead times larger than DT are not modified by the gate driver. Figure. 4 illustrates the dead time period and the relationship between the output gate signals.

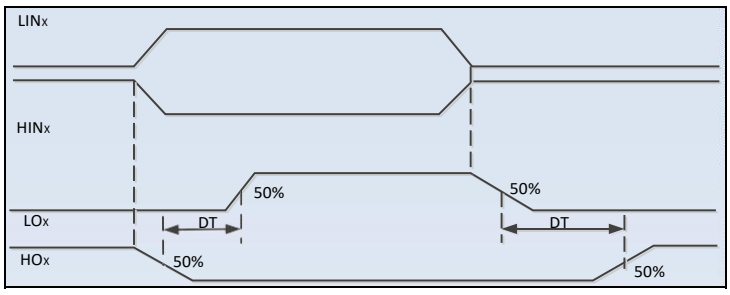
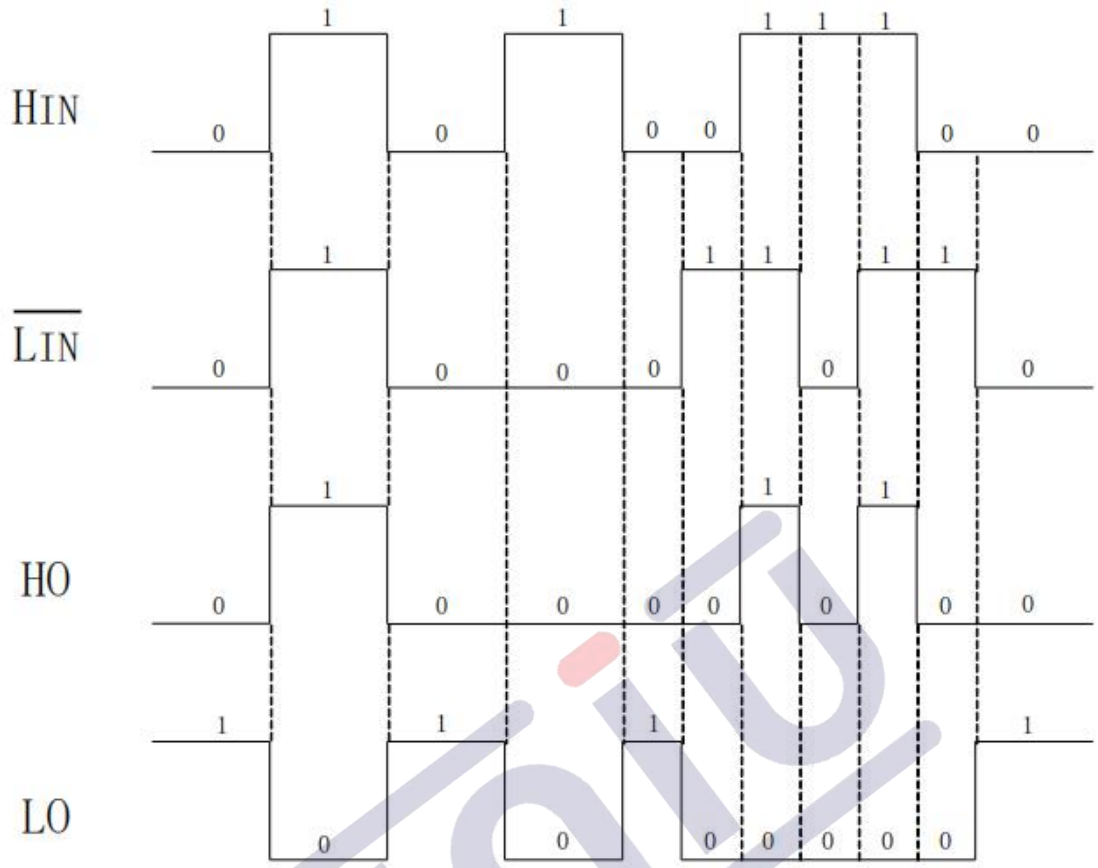


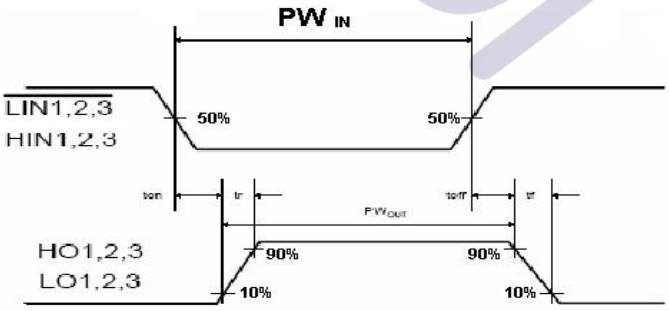
Figure. 4 Dead time protection

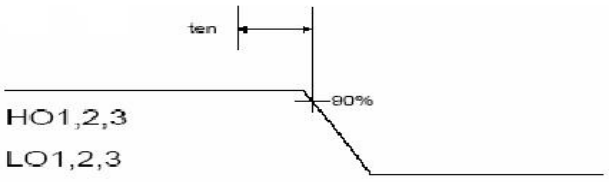
GATE DRIVER (HO1, 2, 3/ LO1, 2, 3)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive power devices such as IGBT and power MOSFET. Low side outputs (i.e. LO1, 2, 3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are only changed at the edge of the respective inputs. After releasing from an under- voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output. In contrast, after releasing from an under-voltage condition of the VCC supply, the low side outputs may directly switch to the state of their respective inputs without the additional constraints of the high side driver.

Typical Performance Characteristics

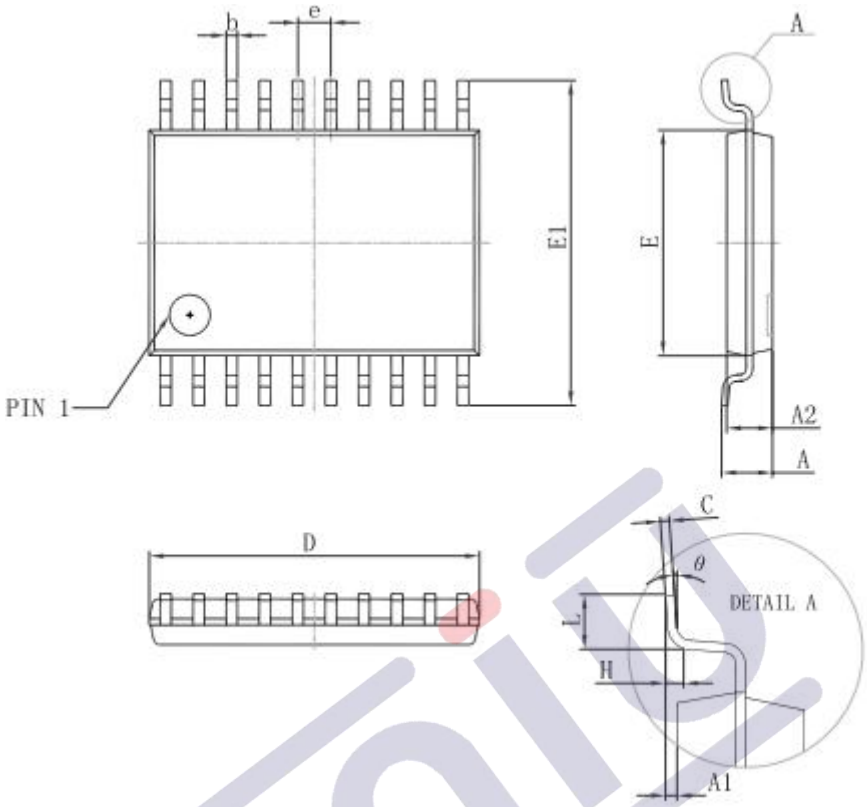






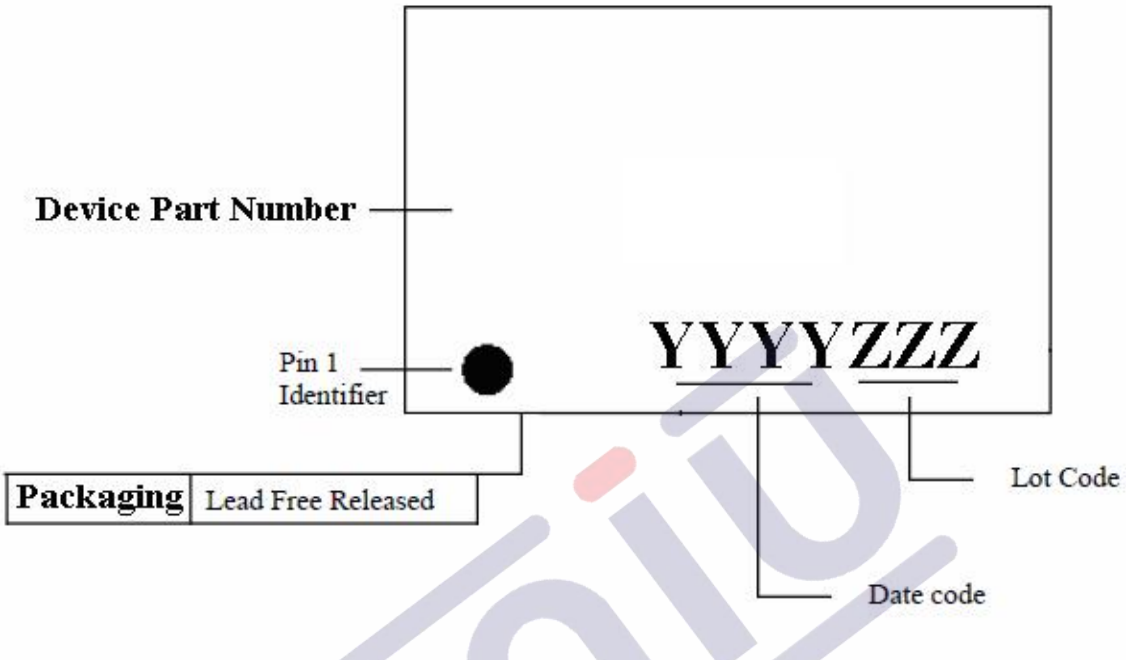
Mechanical Dimensions

TSSOP20

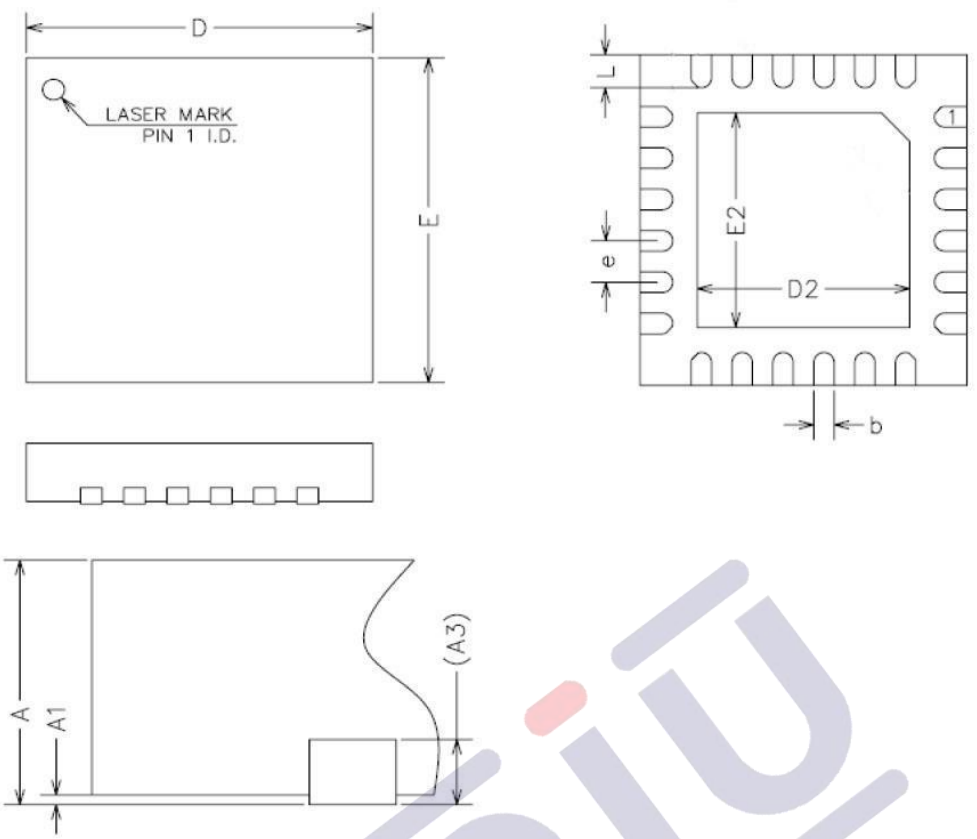


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Ordering Information



24 PINS, QFN



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.50	2.65	2.80
E		4.00 BSC	
E2	2.50	2.65	2.80
e		0.50 BSC	
L	0.35	0.40	.0.45

Notes:

1. All dimensions refer to JEDEC MO-220 WGGD-6
2. All dimensions are in mm

1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2019/05/21	2.0	Change the package
2021/10/19	3.0	Layout adjustment

2.免责声明

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