AiP74HC/HCT123
Dual Retriggerable Monostable Multivibrator with Reset

Product Specification

Specification Revision History:

Version	Date	Description
2012-06-A1	2012-06	New
2021-07-A2	2021-07	Add Typical Application Circuit And Application Note
2021-11-A3	2021-11	Modify Ordering Information; Modify ambient temperature to -40℃~+105℃ and add electrical characteristics of -40℃~+105℃
2021-12-A4	2021-12	Modify Ordering Information

1、General Description

The AiP74HC/HCT123 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL).

The AiP74HC/HCT123 are dual retriggerable monostable multivibrators with output pulse width control by three methods:

1. The basic pulse is programmed by selection of an external resistor (R_{EXT}) and capacitor (C_{EXT}).
2. Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\overline{A}$) or the active HIGH-going edge input (nB). By repeating this process, the output pulse period (nQ=HIGH, $n\overline{Q}$=LOW) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on input $n\overline{RD}$, which also inhibits the triggering.
3. An internal connection from $n\overline{RD}$ to the input gates makes it possible to trigger the circuit by a HIGH-going signal at input $n\overline{RD}$.

Features:

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100% duty factor
- Direct reset terminates output pulse
- Specified from -40℃ to +105℃
- Packaging information: DIP16/SOP16/TSSOP16

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC123DA16.TB	DIP16	74HC123	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HCT123DA16.TB	DIP16	74HCT123	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
AiP74HC123SA16.TB	SOP16	74HC123	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HCT123SA16.TB	SOP16	74HCT123	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
AiP74HC123TA16.TB	TSSOP16	74HC123	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74HCT123TA16.TB	TSSOP16	74HCT123	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC123SA16.TR	SOP16	74HC123	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HCT123SA16.TR	SOP16	74HCT123	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
AiP74HC123TA16.TR	TSSOP16	74HC123	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
AiP74HCT123TA16.TR	TSSOP16	74HCT123	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

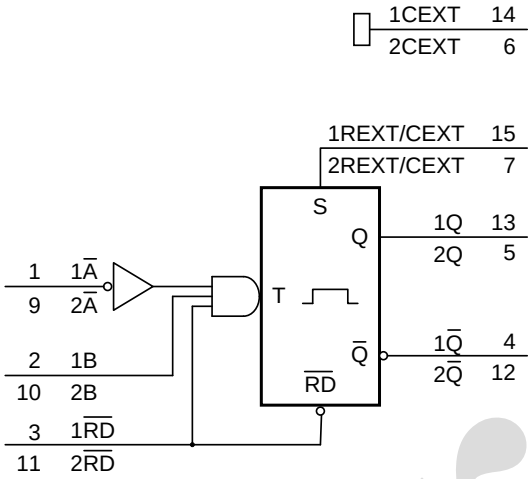


Figure 1. Logic symbol

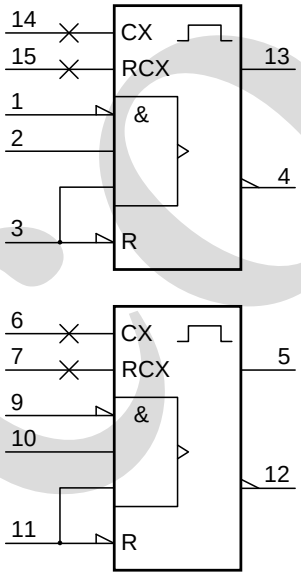


Figure 2. IEC logic symbol

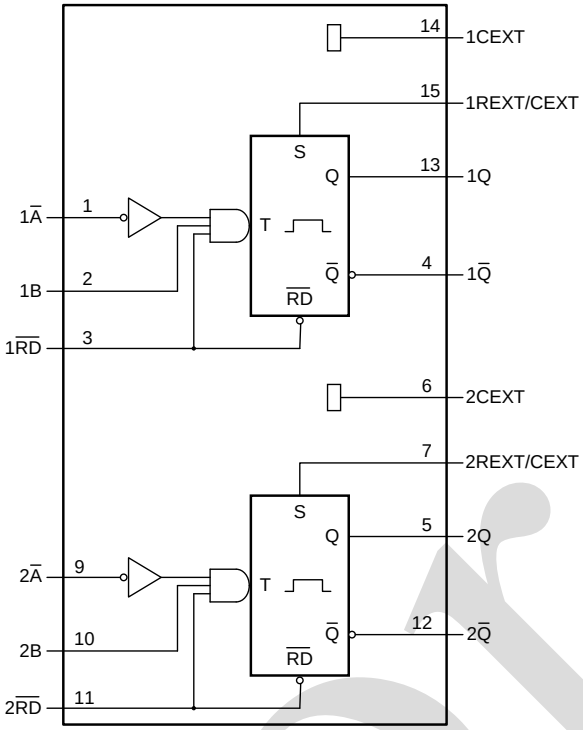


Figure 3. Functional diagram

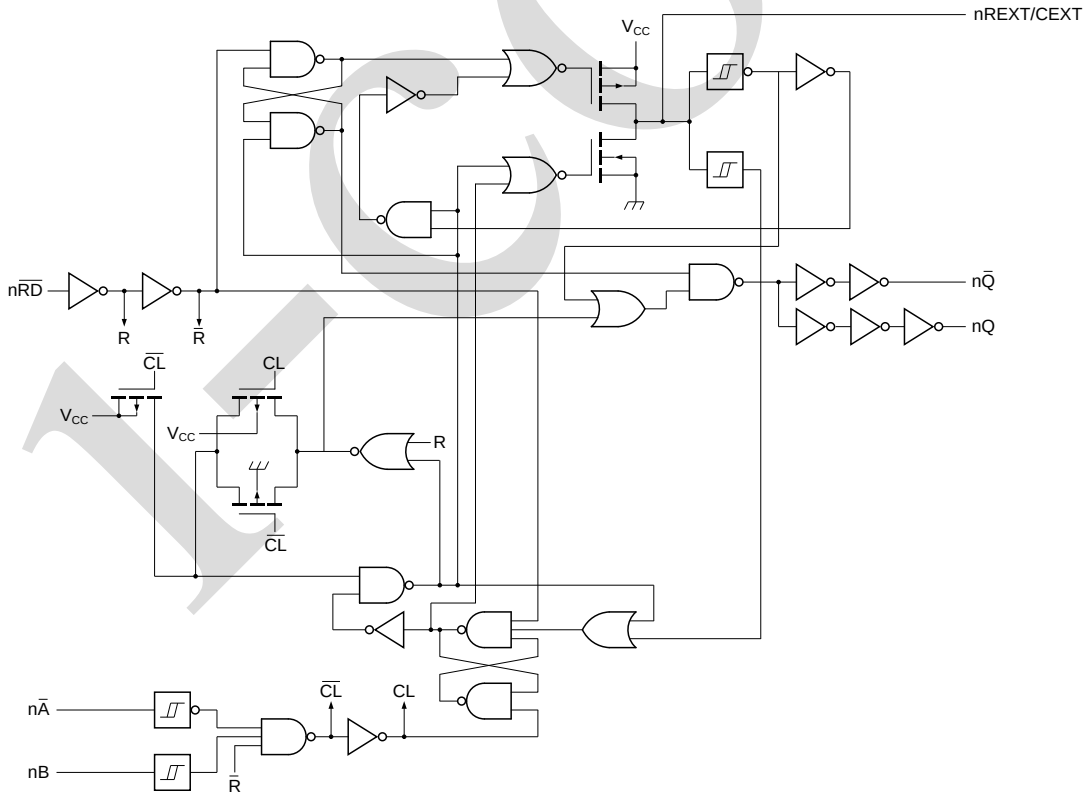
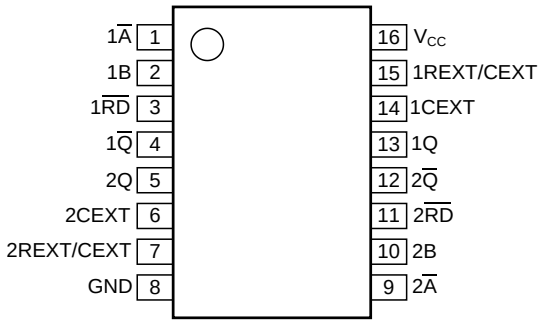


Figure 4. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1$\overline{A}$	negative-edge triggered input 1
2	1B	positive-edge triggered input 1
3	1$\overline{RD}$	direct reset LOW and positive-edge triggered input 1
4	1$\overline{Q}$	active LOW output 1
5	2Q	active HIGH output 2
6	2CEXT	external capacitor connection 2
7	2REXT/CEXT	external resistor and capacitor connection 2
8	GND	ground (0V)
9	2$\overline{A}$	negative-edge triggered input 2
10	2B	positive-edge triggered input 2
11	2$\overline{RD}$	direct reset LOW and positive-edge triggered input 2
12	2$\overline{Q}$	active LOW output 2
13	1Q	active HIGH output 1
14	1CEXT	external capacitor connection 1
15	1REXT/CEXT	external resistor and capacitor connection 1
16	V_{CC}	supply voltage

2.4、Function Table

Input			Output	
n$\overline{RD}$	**n$\overline{A}$**	**nB**	**nQ**	**n$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊓
H	↓	H	⊓	⊓
↑	L	H	⊓	⊓

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.

[2] ↑=LOW-to-HIGH transition; ↓=HIGH-to-LOW transition.

[3]  =one HIGH level output pulse;  =one LOW level output pulse.

[4] If the monostable was triggered before this condition was established, the pulse will continue as programmed.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	except for pins nREXT/CEXT; V_O= -0.5V to (V_{CC}+0.5V)		-	±25	mA
supply current	I_{CC}	-		-	50	mA
ground current	I_{GND}	-		-	-50	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

[1] For DIP16 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP16 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP16 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
supply voltage	V_{CC}	-		2.0	5.0	6.0	V
input voltage	V_I	-		0	-	V_{CC}	V
output voltage	V_O	-		0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	$n\overline{RD}$ input	V_{CC}=2.0V	-	-	625	ns/V
			V_{CC}=4.5V	-	1.67	139	ns/V
			V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-		-40	-	+105	℃
AiP74HCT123							
supply voltage	V_{CC}	-		4.5	5.0	5.5	V
input voltage	V_I	-		0	-	V_{CC}	V
output voltage	V_O	-		0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	$n\overline{RD}$ input	V_{CC}=2.0V	-	-	-	ns/V
			V_{CC}=4.5V	-	1.67	139	ns/V
			V_{CC}=6.0V	-	-	-	ns/V
ambient temperature	T_{amb}	-		-40	-	+105	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-4mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA
input capacitance	C_I	-		-	3.5	-	pF
AiP74HCT123							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	4.5	-	V
			I_O=-4mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	0	0.1	V
			I_O=4mA	-	0.15	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±0.1	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	pins $n\bar{A}$, nB	-	35	125	uA
			pin $n\bar{R}D$	-	50	180	uA
input capacitance	C_I	-		-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4mA; V_{CC}=4.5V	3.84	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	-	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
AiP74HCT123							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4mA	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	pins $n\bar{A}$, nB	-	-	160	uA
			pin $n\bar{R}D$	-	-	225	uA

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-4mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=4mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
AiP74HCT123							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-4mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=4mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	pins $n\bar{A}$, nB	-	-	170	uA
			pin $n\bar{R}D$	-	-	245	uA

3.3.4、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V); C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
propagation delay	t_{pd}	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6[1]	V_{CC}=2.0V	-	83	255	ns
			V_{CC}=4.5V	-	30	51	ns
			V_{CC}=5.0V; C_L=15pF	-	26	-	ns
			V_{CC}=6.0V	-	24	43	ns
		$\overline{nRD}$(reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=2.0V	-	66	215	ns
			V_{CC}=4.5V	-	25	43	ns
			V_{CC}=5.0V; C_L=15pF	-	20	-	ns
			V_{CC}=6.0V	-	19	37	ns
transition time	t_t	see Figure 6[1]	V_{CC}=2.0V	-	19	75	ns
			V_{CC}=4.5V	-	7	15	ns
			V_{CC}=6.0V	-	6	13	ns
pulse width	t_W	$n\overline{A}$ LOW; see Figure 7	V_{CC}=2.0V	100	8	-	ns
			V_{CC}=4.5V	20	3	-	ns
			V_{CC}=6.0V	17	2	-	ns
		nB HIGH; see Figure 7	V_{CC}=2.0V	100	17	-	ns
			V_{CC}=4.5V	20	6	-	ns
			V_{CC}=6.0V	17	5	-	ns
		$\overline{nRD}$ LOW; see Figure 8	V_{CC}=2.0V	100	14	-	ns
			V_{CC}=4.5V	20	5	-	ns
			V_{CC}=6.0V	17	4	-	ns
		nQ HIGH and $n\overline{Q}$ LOW; V_{CC}=5.0V; see Figure 7, 8[2]	C_{EXT}=100nF; R_{EXT}=10kΩ	-	450	-	us
			C_{EXT}=0pF; R_{EXT}=5kΩ	-	75	-	ns
retrigger time	t_{rtrig}	$n\overline{A}$, nB; C_{EXT}=0pF; R_{EXT}=5kΩ; V_{CC}=5.0V; see Figure 7[3][4]		-	110	-	ns
external timing resistor	R_{EXT}	see Figure 7	V_{CC}=2.0V	10	-	1000	kΩ
			V_{CC}=5.0V	2	-	1000	kΩ
external timing capacitor	C_{EXT}	V_{CC}=5.0V; see Figure 9[4]		-	-	-	pF
power dissipation capacitance	C_{PD}	per monostable; V_I=GND to V_{CC}[5]		-	54	-	pF
AiP74HCT123							
HIGH to LOW propagation delay	t_{PHL}	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	30	51	ns
			V_{CC}=5V; C_L=15pF	-	26	-	ns

		$\overline{nRD}$(reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	27	46	ns
			V_{CC}=5V; C_L=15pF	-	23	-	ns
LOW to HIGH propagation delay	t_{PLH}	$\overline{nRD}$, $n\overline{A}$, nB to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	28	51	ns
			V_{CC}=5V; C_L=15pF	-	26	-	ns
		$\overline{nRD}$(reset) to nQ or $n\overline{Q}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	23	46	ns
			V_{CC}=5V; C_L=15pF	-	23	-	ns
transition time	t_t	V_{CC}=4.5V; see Figure 6[1]		-	7	15	ns
pulse width	t_W	V_{CC}=4.5V	$n\overline{A}$ LOW; see Figure 7	20	3	-	ns
			nB HIGH; see Figure 7	20	5	-	ns
			$\overline{nRD}$ LOW; see Figure 8	20	7	-	ns
		nQ HIGH and $n\overline{Q}$ LOW; V_{CC}=5.0V; see Figure 7, 8[2]	C_{EXT}=100nF; R_{EXT}=10kΩ	-	450	-	us
			C_{EXT}=0pF; R_{EXT}=5kΩ	-	75	-	ns
retrigger time	t_{rtrig}	$n\overline{A}$, nB; C_{EXT}=0pF; R_{EXT}=5kΩ; V_{CC}=5.0V; see Figure 7[3] [4]		-	110	-	ns
external timing resistor	R_{EXT}	V_{CC}=5.0V; see Figure 9		2	-	1000	kΩ
external timing capacitor	C_{EXT}	V_{CC}=5.0V; see Figure 9[4]		-	-	-	pF
power dissipation capacitance	C_{PD}	per monostable; V_I=GND to V_{CC}-1.5V[5]		-	56	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

[2] For other R_{EXT} and C_{EXT} combinations see Figure 9. If C_{EXT}>10nF, the next formula is valid.

$t_W = K \times R_{EXT} \times C_{EXT}$, where:

t_W=typical output pulse width in ns;

R_{EXT}=external resistor in kΩ; C_{EXT}=external capacitor in pF;

K=constant = 0.45 for V_{CC}=5.0V and 0.55 for V_{CC}=2.0V.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is approximately 7pF.

[3] The time to retrigger the monostable multivibrator depends on the values of R_{EXT} and C_{EXT}. The output pulse width will only be extended when the time between the active-going edges of the trigger input pulses meets the minimum retrigger time. If C_{EXT}>10pF,

the next formula (at V_{CC}=5.0V) for the setup time of a retrigger pulse is valid:

$t_{rtrig}=30+0.19\times R_{EXT}\times C_{EXT}^{0.9}+13\times R_{EXT}^{1.05}$, where:

t_{rtrig}=retrigger time in ns;

C_{EXT}=external capacitor in pF; R_{EXT}=external resistor in kΩ.

The inherent test jig and pin capacitance at pins 15 and 7 (nREXT/CEXT) is 7pF.

[4] When the device is powered-up, initiate the device via a reset pulse, when C_{EXT}<50pF.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i+\sum(C_L\times V_{CC}^2\times f_o)+0.75\times C_{EXT}\times V_{CC}^2\times f_o+D\times 16\times V_{CC}$ where:

f_i=input frequency in MHz; f_o=output frequency in MHz;

D=duty factor in %; C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

C_{EXT}=timing capacitance in pF;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, GND=0V; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
propagation delay	t_{pd}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6[1]	V_{CC}=2.0V	-	-	320	ns
			V_{CC}=4.5V	-	-	64	ns
			V_{CC}=6.0V	-	-	54	ns
		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=2.0V	-	-	270	ns
			V_{CC}=4.5V	-	-	54	ns
			V_{CC}=6.0V	-	-	46	ns
transition time	t_t	see Figure 6[1]	V_{CC}=2.0V	-	-	95	ns
			V_{CC}=4.5V	-	-	19	ns
			V_{CC}=6.0V	-	-	16	ns
pulse width	t_W	$\overline{nA}$ LOW; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		nB HIGH; see Figure 7	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
		$\overline{nRD}$ LOW; see Figure 8	V_{CC}=2.0V	125	-	-	ns
			V_{CC}=4.5V	25	-	-	ns
			V_{CC}=6.0V	21	-	-	ns
AiP74HCT123							
HIGH to LOW propagation delay	t_{PHL}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	64	ns

		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	58	ns
LOW to HIGH propagation delay	t_{PLH}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	64	ns
		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	58	ns
transition time	t_t	V_{CC}=4.5V; see Figure 6[1]		-	-	19	ns
pulse width	t_W	V_{CC}=4.5V	$\overline{nA}$ LOW; see Figure 7	25	-	-	ns
			nB HIGH; see Figure 7	25	-	-	ns
			$\overline{nRD}$ LOW; see Figure 8	25	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +105℃, GND=0V; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC123							
propagation delay	t_{pd}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6[1]	V_{CC}=2.0V	-	-	385	ns
			V_{CC}=4.5V	-	-	77	ns
			V_{CC}=6.0V	-	-	65	ns
		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=2.0V	-	-	325	ns
			V_{CC}=4.5V	-	-	65	ns
			V_{CC}=6.0V	-	-	55	ns
transition time	t_t	see Figure 6[1]	V_{CC}=2.0V	-	-	110	ns
			V_{CC}=4.5V	-	-	22	ns
			V_{CC}=6.0V	-	-	19	ns
pulse width	t_W	$\overline{nA}$ LOW; see Figure 7	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		nB HIGH;	V_{CC}=2.0V	150	-	-	ns

		see Figure 7	V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
		$\overline{nRD}$ LOW; see Figure 8	V_{CC}=2.0V	150	-	-	ns
			V_{CC}=4.5V	30	-	-	ns
			V_{CC}=6.0V	26	-	-	ns
AiP74HCT123							
HIGH to LOW propagation delay	t_{PHL}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	77	ns
		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	69	ns
LOW to HIGH propagation delay	t_{PLH}	$\overline{nRD}$, $\overline{nA}$, nB to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	77	ns
		$\overline{nRD}$(reset) to nQ or $\overline{nQ}$; C_{EXT}=0pF; R_{EXT}=5kΩ; see Figure 6	V_{CC}=4.5V	-	-	69	ns
transition time	t_t	V_{CC}=4.5V; see Figure 6[1]		-	-	22	ns
pulse width	t_W	V_{CC}=4.5V	$\overline{nA}$ LOW; see Figure 7	30	-	-	ns
			nB HIGH; see Figure 7	30	-	-	ns
			$\overline{nRD}$ LOW; see Figure 8	30	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_t is the same as t_{THL} and t_{TLH}.

4、Testing Circuit

4.1、AC Testing Circuit

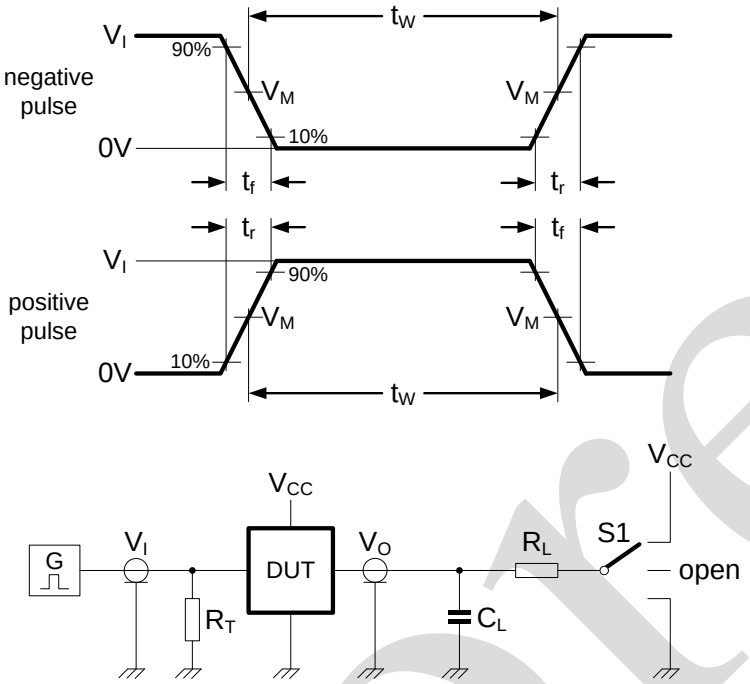


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

4.2、AC Testing Waveforms

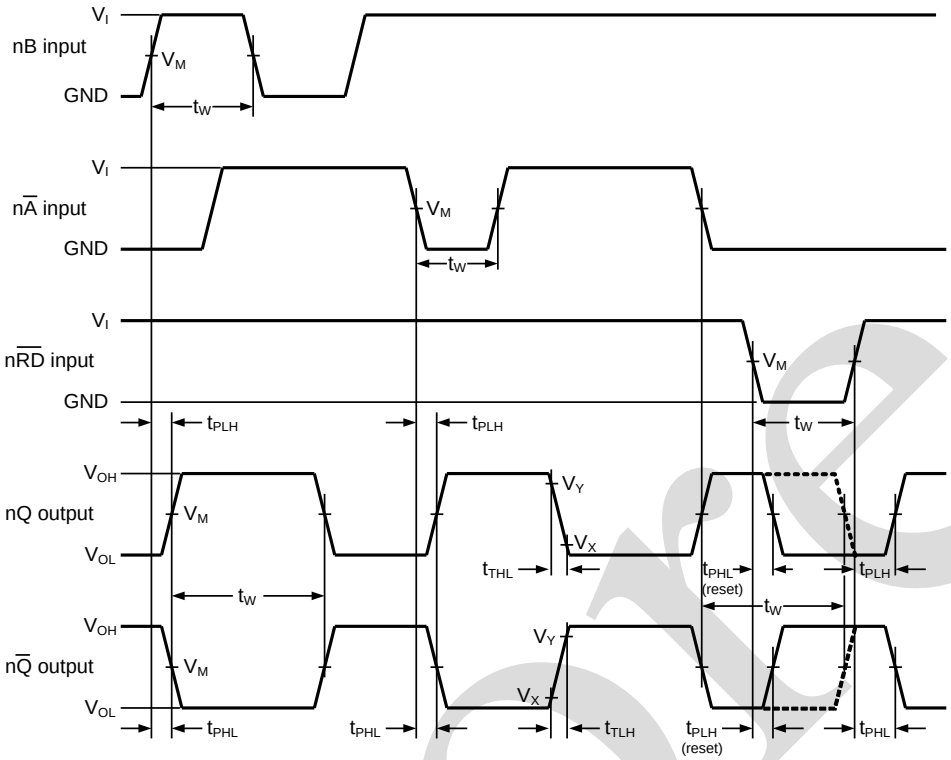


Figure 6. Propagation delays from inputs (nA̅, nB, nR̅D̅) to outputs (nQ, nQ̅) and output transition times

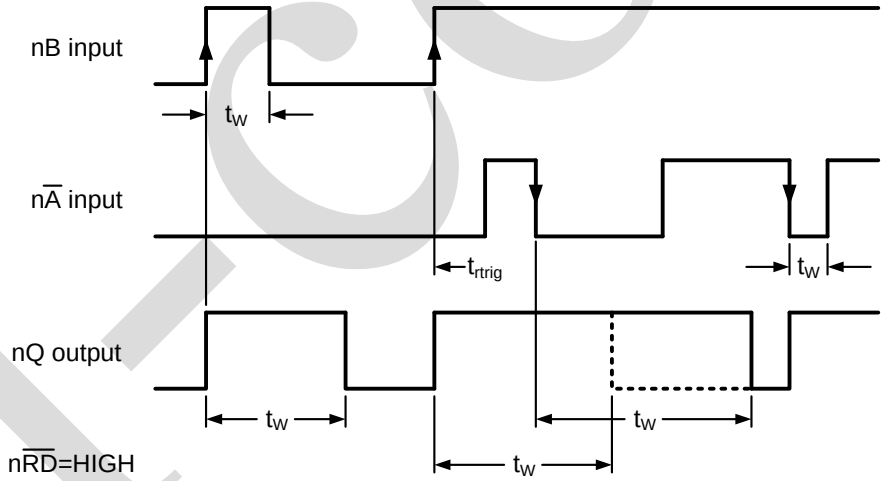


Figure 7. Output pulse control using retrigger pulse

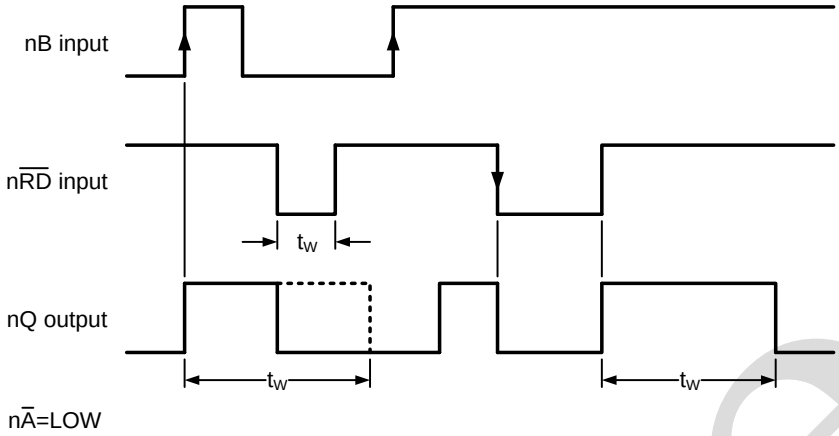
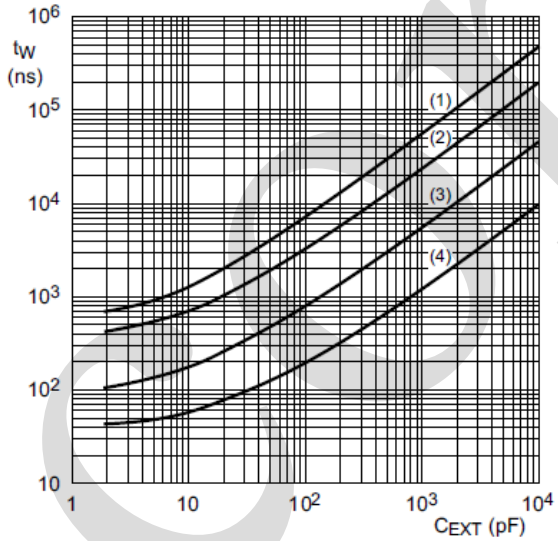


Figure 8. Output pulse control using reset input nRD



V_{CC}=5.0V; T_{amb}=25℃.

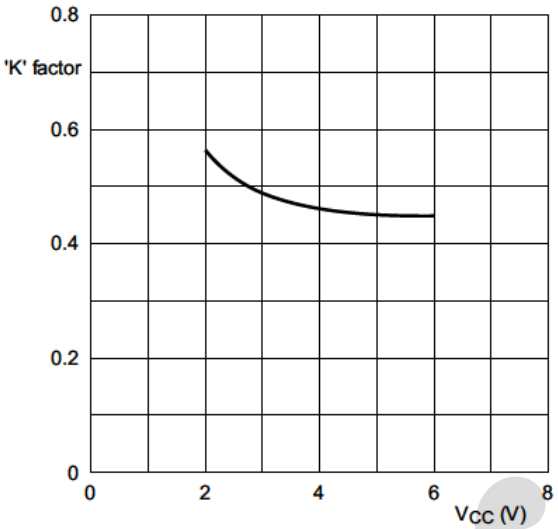
(1) R_{EXT}=100kΩ

(2) R_{EXT}=50kΩ

(3) R_{EXT}=10kΩ

(4) R_{EXT}=2kΩ

Figure 9. Typical output pulse width as a function of the external capacitor value



C_{EXT}=10nF; R_{EXT}=10kΩ to 100kΩ.T_{amb}=25℃.

Figure 10. AiP74HC123 typical 'K' factor as function of V_{CC}

4.3、Measurement Points

Type	Input	Output
	V_M	V_M
AiP74HC123	0.5×V_{CC}	0.5×V_{CC}
AiP74HCT123	1.3V	1.3V

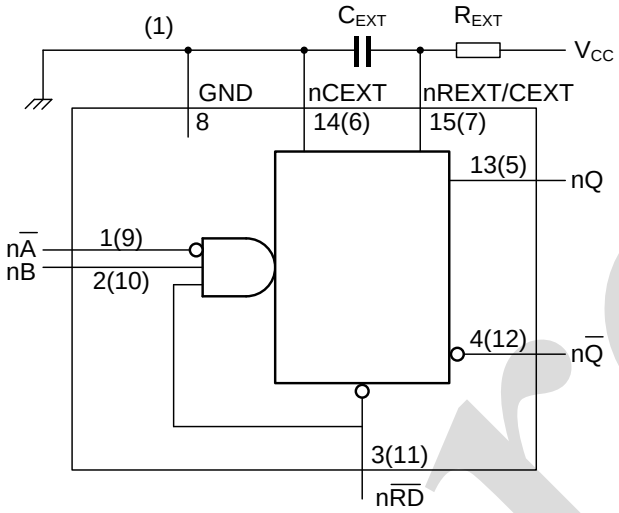
4.4、Test Data

Type	Input		Load		S1 position
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}
AiP74HC123	V_{CC}	6ns	15pF, 50pF	1kΩ	open
AiP74HCT123	3V	6ns	15pF, 50pF	1kΩ	open

5、Typical Application Circuit And Application Note

5.1、Timing component connections

The basic output pulse width is essentially determined by the values of the external timing components R_{EXT} and C_{EXT}.



(1) For minimum noise generation it is recommended to ground pins 6 ($2C_{EXT}$) and 14 ($1C_{EXT}$) externally to pin 8 (GND).

Figure 11. Timing component connections

5.2、Power-up considerations

When the monostable is powered-up it may produce an output pulse, with a pulse width defined by the values of R_{EXT} and C_{EXT}. This output pulse can be eliminated using the circuit shown in Figure 12.

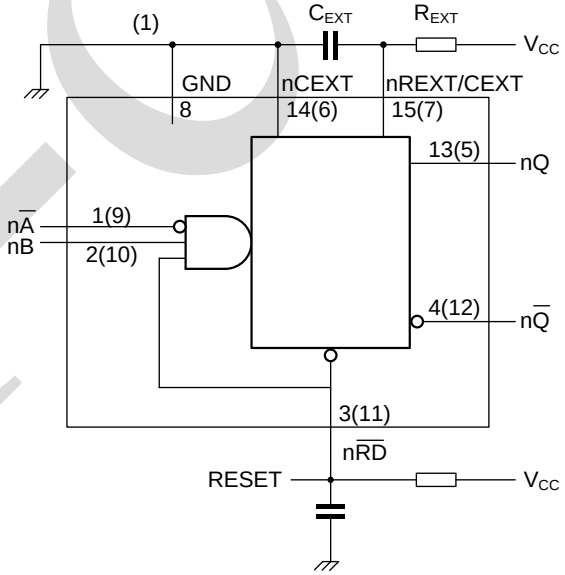


Figure 12. Power-up output pulse elimination circuit

5.3、Power-down considerations

A large capacitor C_{EXT} may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Figure 13.

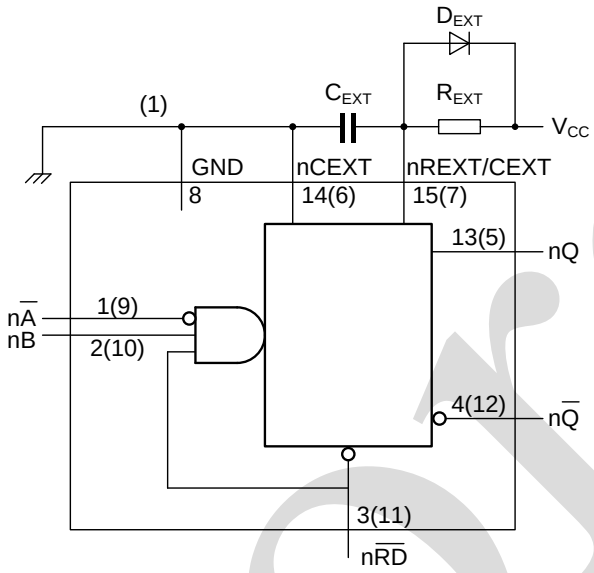
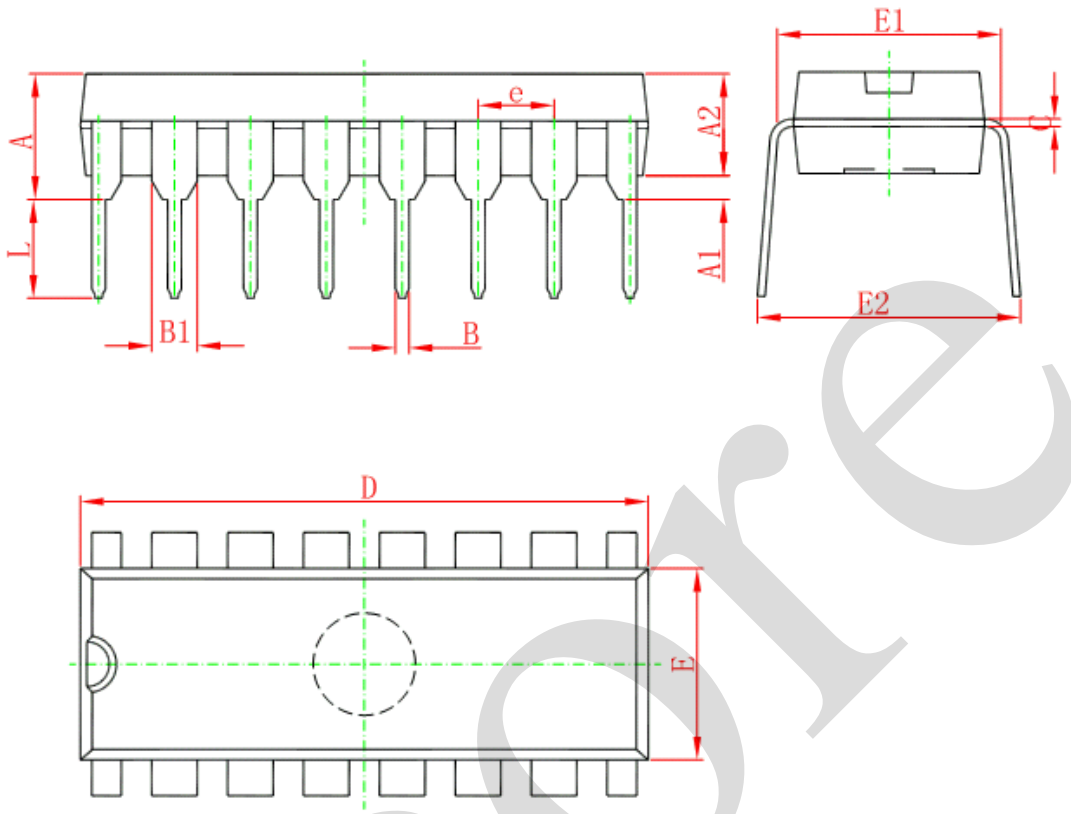


Figure 13. Power-down protection circuit

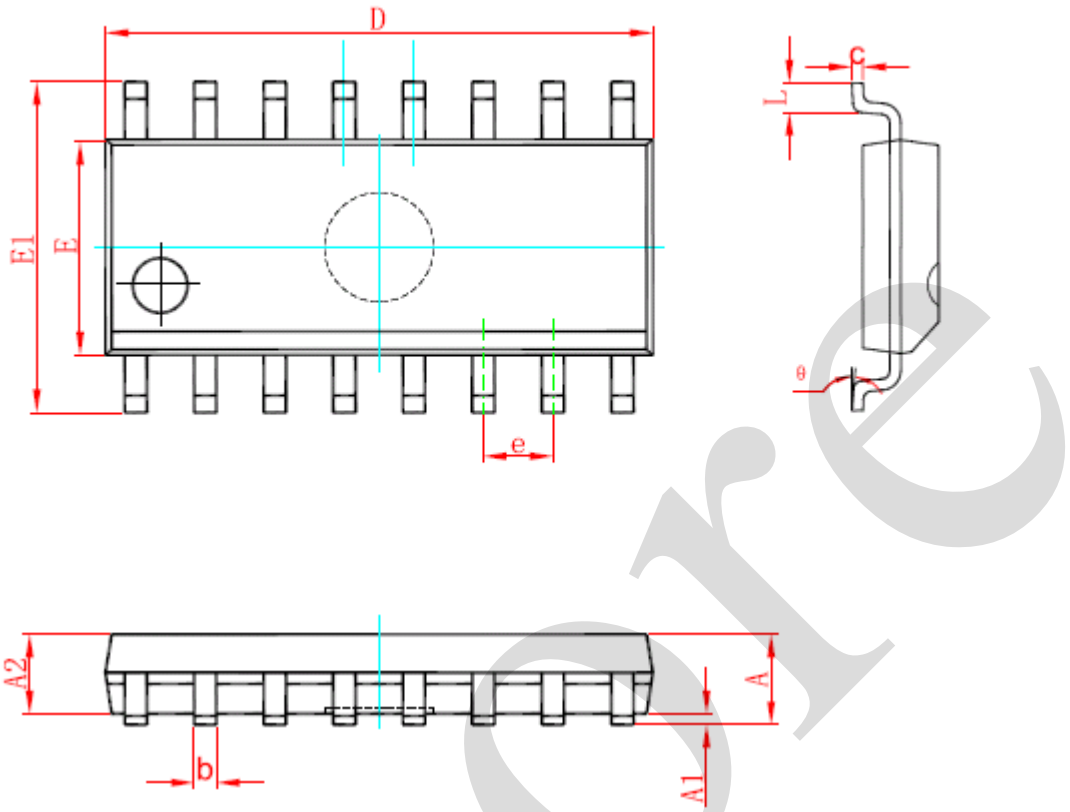
6、Package Information

6.1、DIP16



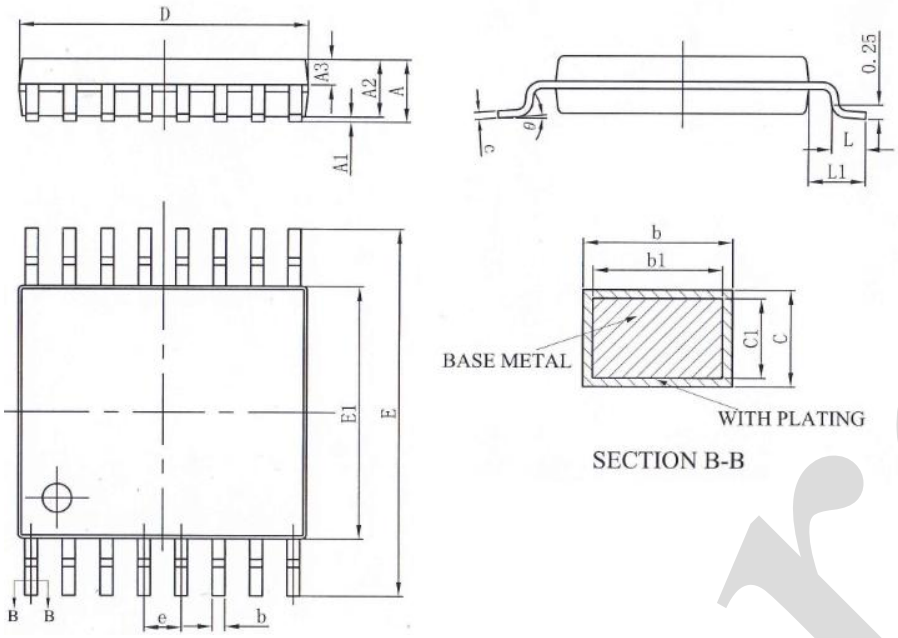
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

6.2、SOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

6.3、TSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.