GENERAL DESCRIPTION

The MX5114D is designed to drive a VCSEL with strong sink current capability from an internal N-MOSFET. The MX5114D provides inverting and noninverting inputs to satisfy requirements for inverting and noninverting input. The inputs of the MX5114D are TTL/CMOS Logic compatible and withstand input voltages up to 20 V regardless of the VDD voltage. The MX5114D has fast switching speed and minimized propagation delays, facilitating high-frequency operation. The MX5114D is available in a 6-pin DFN2*2 package.

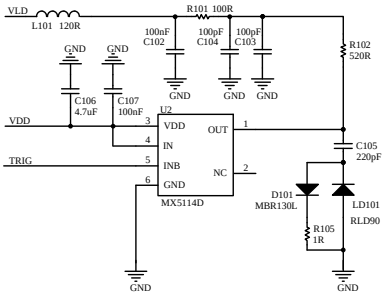
FEATURES

- ♦ 4V to 20V Single Power Supply
- ♦ 15A Peak Current Transient
- ♦ 0.4Ω turn on resistance with internal FET
- ♦ 5ns (Typical) Propagation Delay
- ♦ Matching Delay Time Between Inverting and Noninverting Inputs
- ♦ TTL/CMOS Logic Inputs
- ♦Low Input Capacitance: 2.5pF (Typical)
- ♦–40°C to 125°C Operating Temperature Range
- ♦ 6-Pin DFN2*2

APPLICATIONS

Laser driver without external MOSFET

TYPICAL APPLICATION



GENERAL INFORMATION

Ordering information

Part Number	Description
MX5114D	DFN2*2-6L
MPQ	3000pcs

Package dissipation rating

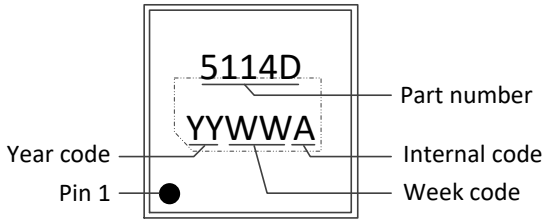
Package	RθJA（℃/W）
DFN2*2-6L	108.1

Absolute maximum ratings

Parameter	Value
VDD to GND	-0.3 to 24V
IN, INB to GND	-0.3 to 24V
OUT to GND	-0.3 to VDD+0.3V
Junction temperature	150℃
Storage temperature, Tstg	-55 to 150℃
Leading temperature （soldering，10secs）	260℃
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Marking information



Recommended operating condition

Symbol	Parameter	Range
VDD	VDD supply voltage	4-20V
Junction temperature		-40~125℃
PD	Power dissipation	0.73W

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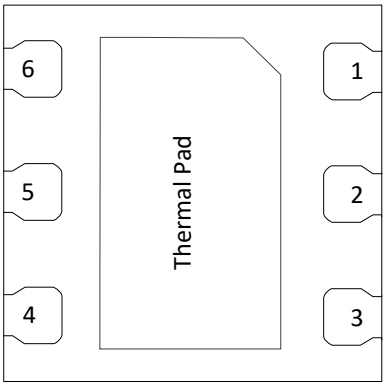
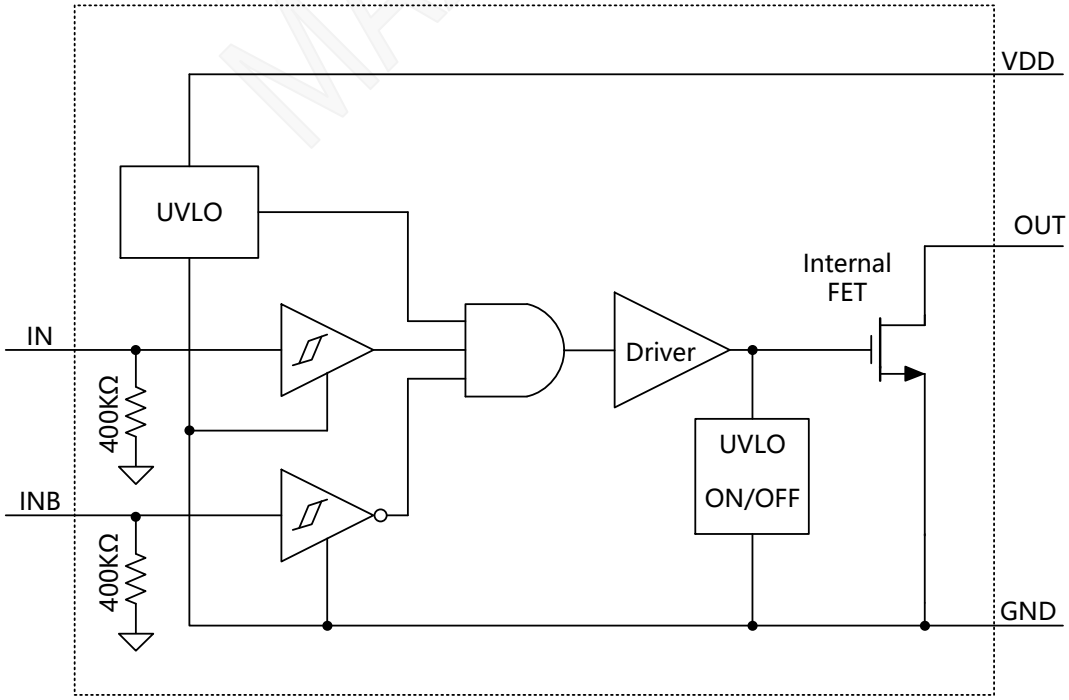
TERMINAL ASSIGMENTS



Pin information (Bottom View)

PIN NO.	PIN name	Description
1	OUT	Open drain of internal FET output pin.
2	NC	No connection.
3	VDD	Gate drive supply Locally decouple to GND using low ESR/ESL capacitor located as close as possible to the IC.
4	IN	Noninverting logic input Connect to VDD when not used.
5	INB	Inverting logic input Connect to GND when not used.
6	GND	Ground All signals are referenced to this ground.
Thermal Pad		No connect.

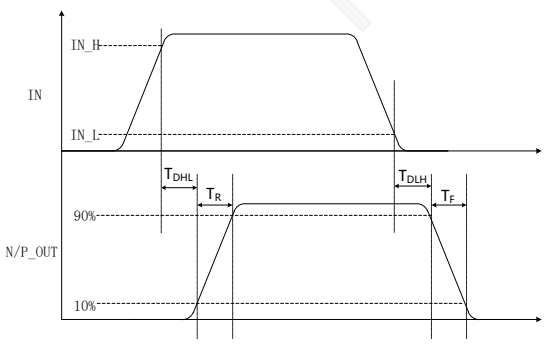
BLOCK DIAGRAM

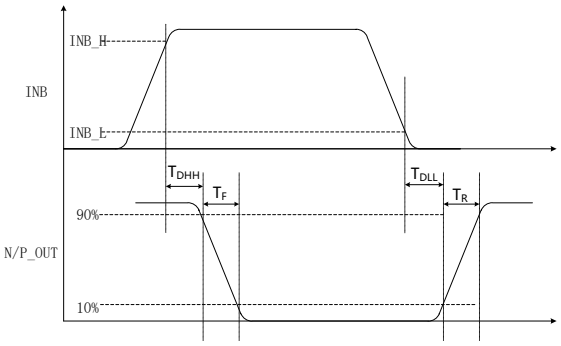


Electrical characteristics

（TA=25℃，VDD=12V, unless otherwise noted）

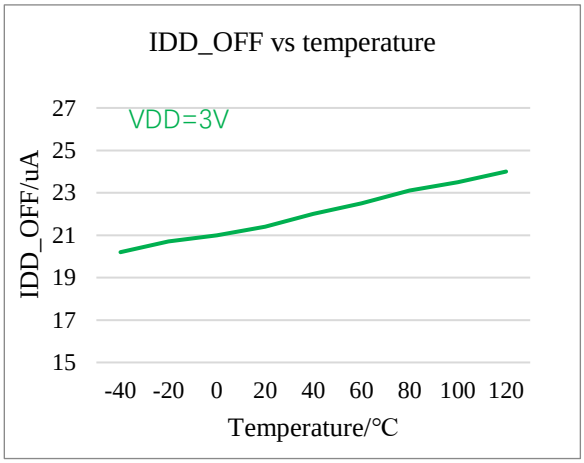
Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
POWER SUPPLY						
IDD	Operation current	VDD=IN=12V，INB=100kHz		70	300	μA
IQ	Quiescent current	VDD=12V		45	250	μA
IQ_IN_H	Quiescent current	VDD=IN=12V		45	250	μA
IQ_INB_L	Quiescent current	VDD=12, INB=0		45	250	μA
I_{DD_OFF}	VDD=3.0V，IN=INB=GND			20	50	μA
	VDD=3.0V，IN=INB=VDD			30	60	μA
U_{VLO_ON}	UVLO rising threshold	VDD rising	3.1	3.3	3.5	V
U_{VLO_OFF}	UVLO falling threshold	VDD falling	3.5	3.85	4.2	V
U_{VLO_HYS}	UVLO threshold hysteresis		0.2	0.5	0.8	V
LOGIC INPUT						
V_{IN_H}	Noninverting input high voltage	IN input rising	1.8	2.1	2.4	V
V_{IN_L}	Noninverting input low voltage	IN input falling	0.9	1.2	1.5	V
V_{INB_H}	Inverting input high voltage	INB input rising	1.8	2.1	2.4	V
V_{INB_L}	Inverting input low voltage	INB input falling	0.9	1.2	1.5	V
R_{INBL}	Inverting input pull down resistor			400		kΩ
R_{INL}	Noninverting input pull down resistor			400		kΩ
N-CHANNEL OUTPUT						
R_{ON}	Output resistance-pulling down @ 4.5V	VDD=4.5V, IIN_OUT=-50mA		0.60	0.85	Ω
	Output resistance-pulling down @ 10V	VDD=10V, IIN_OUT=-50mA		0.40	0.65	Ω
I_{PK}	Peak current	Turn on 50ns and Turn off 30μs		15		A
I_{PKIN}	Internal FET drive capability			7.6A		A
SWITCHING CHARACTERISTICS						
C_{IN}	Input capacitance			2.5		pF
T_{FALL}	Fall time	VDD=12V，No capacitor		2	5	ns
T_{DLH}	Propagation delay, Low to High, noninverting			5	10	ns
T_{DHL}	Propagation delay, High to Low, noninverting			5	10	ns
T_{DHH}	Propagation delay, High to High, inverting			5	10	ns
T_{DLL}	Propagation delay, Low to Low, inverting			6	10	ns



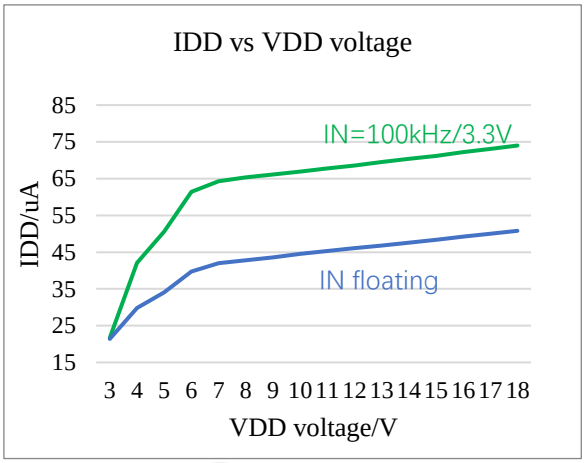


Note：OUT is tied to VDD from a small resistor

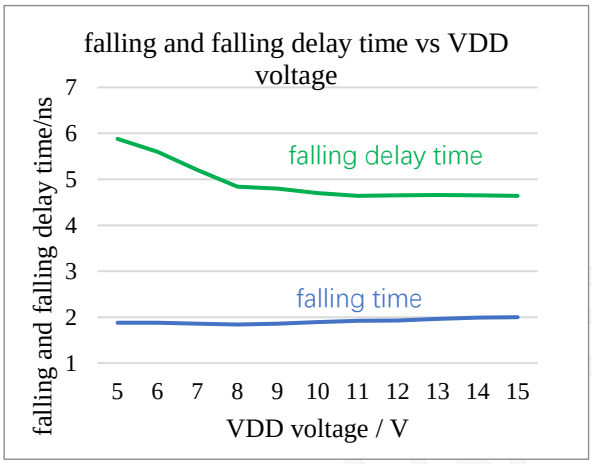
Characteristic plots



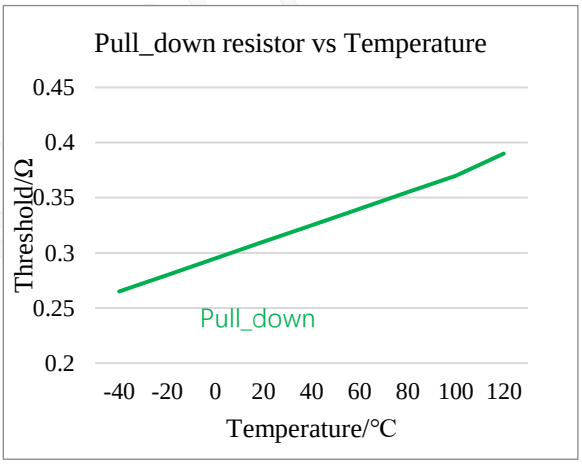
VDD OFF current vs temperature



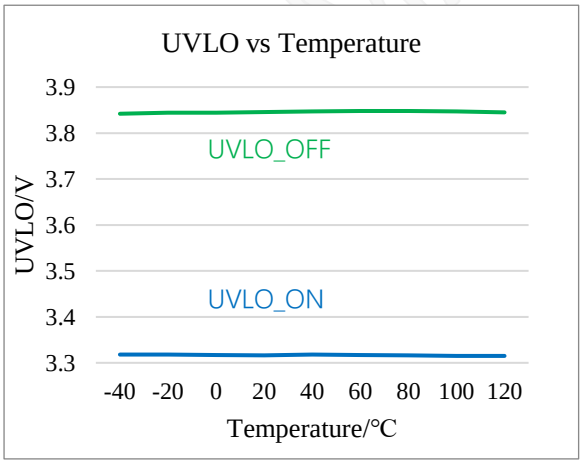
Operation current vs VDD voltage



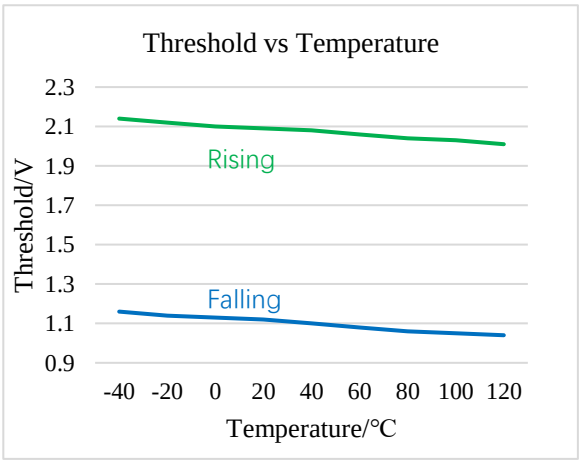
Falling and falling delay time vs VDD voltage



pull down resistor vs temperature



UVLO vs temperature



IN and INB high and low threshold vs temperature

Operation description

The MX5114D is a special purpose circuit for laser driver with 15A peak current capability. Inputs of the MX5114D are CMOS/TTL Logic compatible and can withstand the input voltages up to 20V regardless of the VDD voltage. This allows inputs of the MX5114D to be connected directly to most PWM controllers.

The MX5114D startup logic is optimized to drive ground-referenced N channel FET with an under voltage lockout function to ensure that the IC starts up in an orderly fashion. When VDD is rising, yet below the UVLO level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.5V before the part shuts down. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power switching.

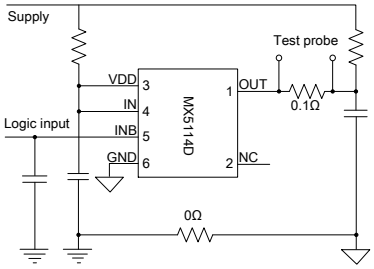
VDD bypass capacitor guidelines

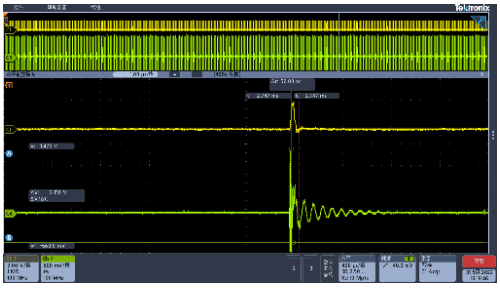
To enable this IC to turn a device on quickly, a local high frequency bypass capacitor, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to the bulk electrolytic capacitance of 10uF to 47uF commonly found on the driver and controller bias circuits.

A typical criterion for choosing the value of bypass capacitor is to keep the ripple voltage on the VDD supply to ⩽5%. This is often achieved with a value ⩾20 times the equivalent load capacitance, defined here as QG/VDD. Ceramic capacitors of 0.1uF to 1uF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

Peak current test

The peak current test is as shown in the figure below, the pulse width is 50ns and the period is 30us. And the test result shown in the second figure. The peak current can be calculated as IPK=1.47V/0.1R=14.7A.





Layout and connection guidelines

The MX5114D family of ToF drivers incorporates fast-reacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 15A to facilitate voltage transition times from under 5ns to over 50ns. The following layout and connection guidelines are strongly recommended:

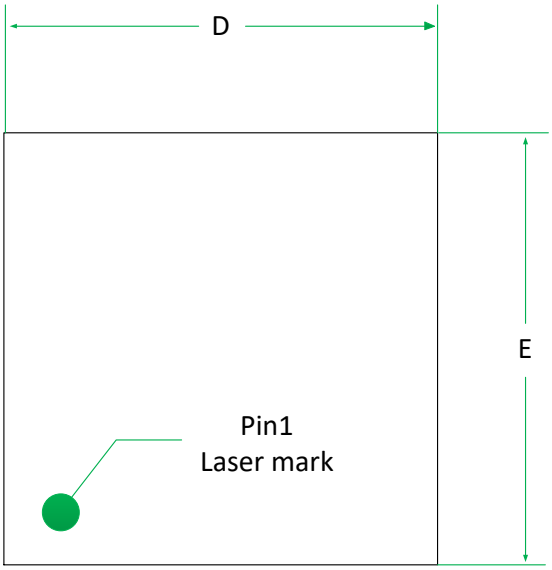
- Keep high current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs pins.
- In noisy environments, it may be necessary to tie inputs of an unused PIN to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long IN, INB, or OUT, leads. For best results, make connections to all pins as short and direct as possible.
- The MX5114D is compatible with many other industry standard drivers. In single input pin IN, there is an internal resistor tied to GND and INB tied to VDD, this should be considered in the PCB layout.

Truth table of logic operation

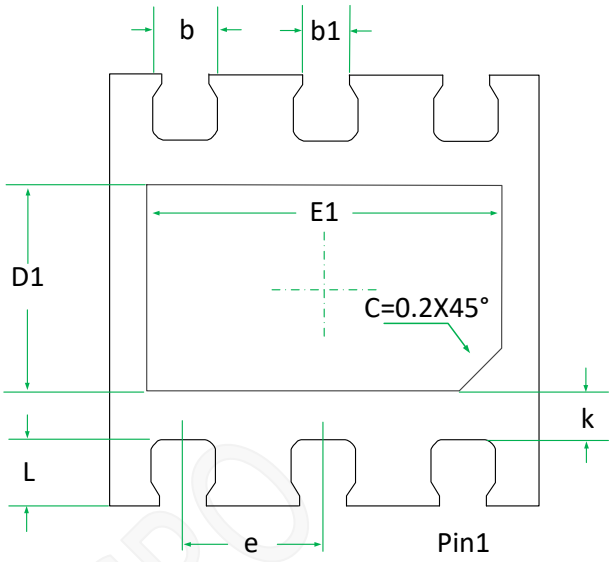
The MX5114D truth table indicates the operational states using the IN and INB input configuration. MX5114D can be used in laser distance test, and only INB and OUT can be used without external NMOSFET. And at this time, the IN should be connected to VDD pin.

IN	INB	OUT
H	H	L
H	L	Open circuit
L	L	L
L	H	L

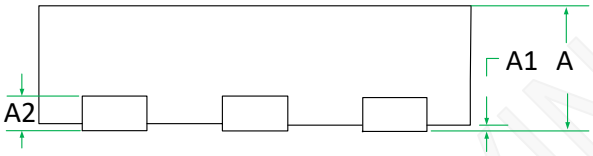
Package information



Top View



Bottom View



Side View

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.02	0.022	0.024
A1	0	0.025	0.050	0	0.001	0.002
A2		0.152BSC			0.006BSC	
D	1.900	2.000	2.100	0.075	0.078	0.083
E	1.900	2.000	2.100	0.075	0.078	0.083
D1	0.860	0.960	1.060	0.034	0.038	0.042
E1	1.550	1.650	1.750	0.061	0.065	0.069
k		0.220BSC			0.008BSC	
b	0.250	0.300	0.350	0.010	0.012	0.014
b1		0.220BSC			0.008BSC	
e		0.650BSC			0.026BSC	
L	0.224	0.300	0.376	0.009	0.012	0.015

DFN2*2-6L for MX5114D

Restrictions on Product Use

- MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.
- In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.
- The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）

V11 Add the peak current test waveform

V12 The INB internal pull up resistor change pull down resistor and the pull down resistor are added in block diagram

V13 add marking information and version information

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