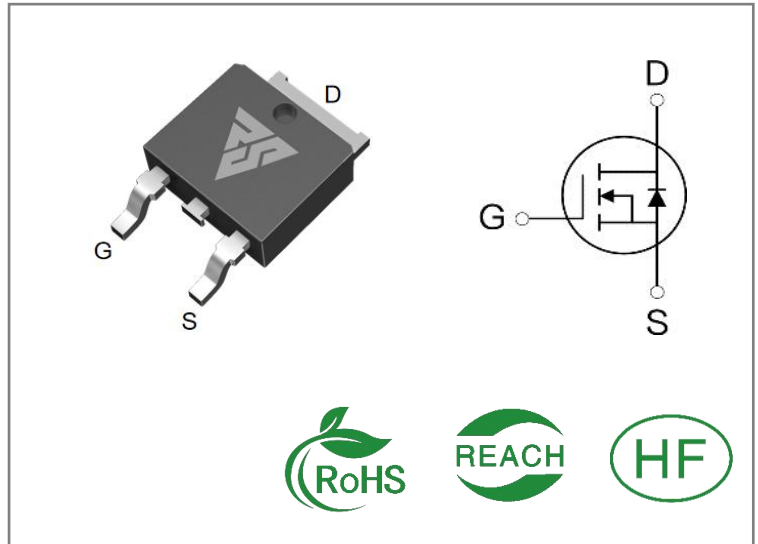


ID	R _{DS(ON)} (Typ)	VDSS
90A	3.7mΩ	20V


Applications:

- Load Switch
- PWM Applications
- Power Managment

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS20N90D	T0-252	RS20N90D	Tape&reel	2500 PCS

Absolute Maximun Ratings T_c= 25°C unless otherwise specified

Symbol	Parameter	RS20N90D	Units
VDSS	Drain-to-Source Voltage	20	V
ID	Continuous Drain Current TC=25°C	90	A
ID	Continuous Drain Current TC=70°C	72	
IDM	Pulsed Drain Current	360	
PD	Power Dissipation	80	W
VGS	Gate- to- Source Voltage	±12	V
EAS	Single Pulse Avalanche Engergy L = 0.5mH, VDD = 10V, RG = 25Ω, Tj = 25°C	240	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS20N90D	Units	Test Conditions
R θ JC	Junction-to-Case	2.1	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 1 5 0 °C
R θ JA	Junction-to-Ambient	62		1 cubic foot chamber, free air.

OFF Characteristics T_J= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	20	--	--	V	VGS=0V, ID=250μA
IDSS	Drain- to- Source Leakage Current	--	--	1	μA	VDS=20V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=12V , VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-12V , VDS=0V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance	--	3.7	5	mΩ	VGS=4.5V, ID=20A
		--	4.7	6	mΩ	VGS=2.5V, ID=15A
VGS(TH)	Gate Threshold Voltage	0.46	0.65	1.0	V	VGS=VDS, ID=250μA

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	6.5	--	nS	VDS=10V ID=2A RG=3Ω VGS=4.5V
trise	Rise Time	--	17	--		
td(OFF)	Turn- OFF Delay Time	--	30	--		
tfall	Fall Time	--	17	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	4800	--	pF	VGS=0V VDS=10V f=1.0MHz
Coss	Output Capacitance	--	700	--		
Crss	Reverse Transfer Capacitance	--	350	--		
Qg	Total Gate Charge	--	27	--	nC	VDS=10V ID=20A VGS=4.5V
Qgs	Gate- to- Source Charge	--	7.0	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	6.5	--		

Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	90	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	360	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=30A,VGS=0V
trr	Reverse Recovery Time	--	35	--	nS	VGS=0V IS=30A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	15	--	nC	

Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

Typical Feature Curve

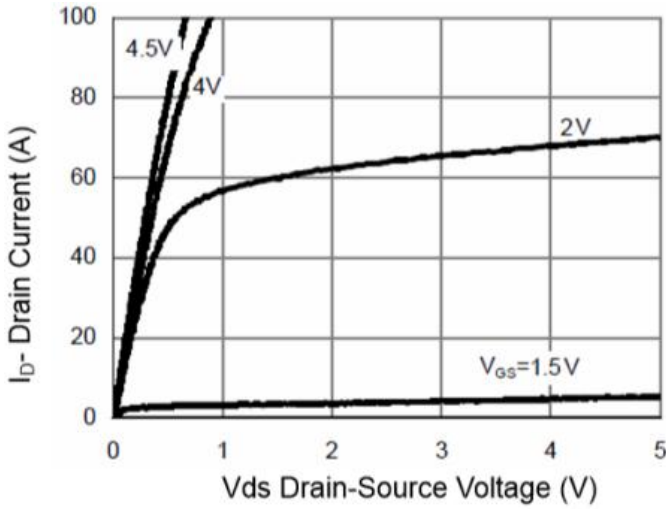


Figure 1 Output Characteristics

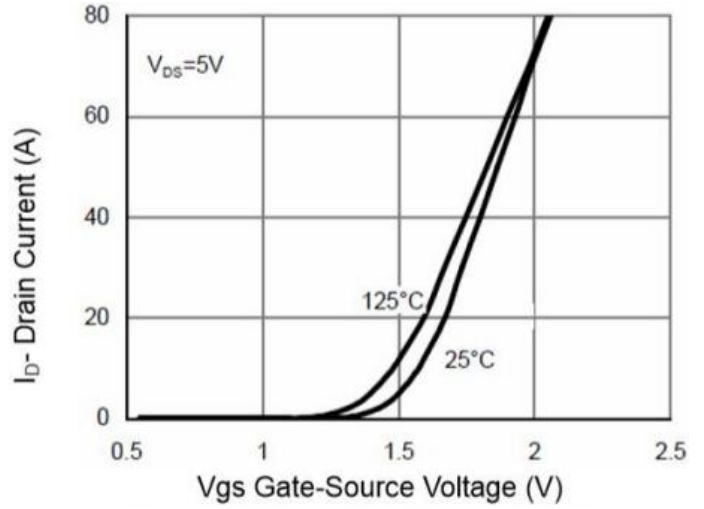


Figure 2 Transfer Characteristics

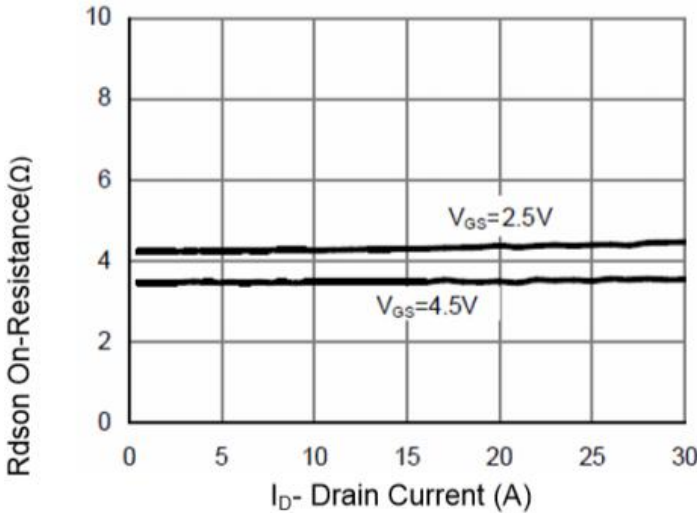


Figure 3 Rdson- Drain Current

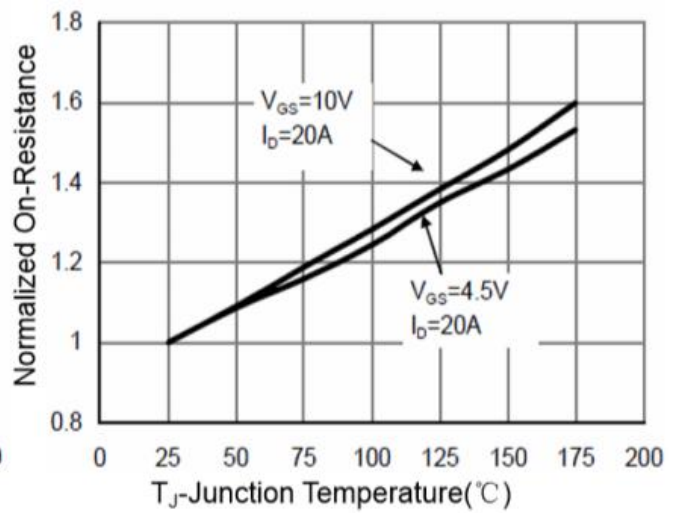


Figure 4 Rdson-Junction Temperature

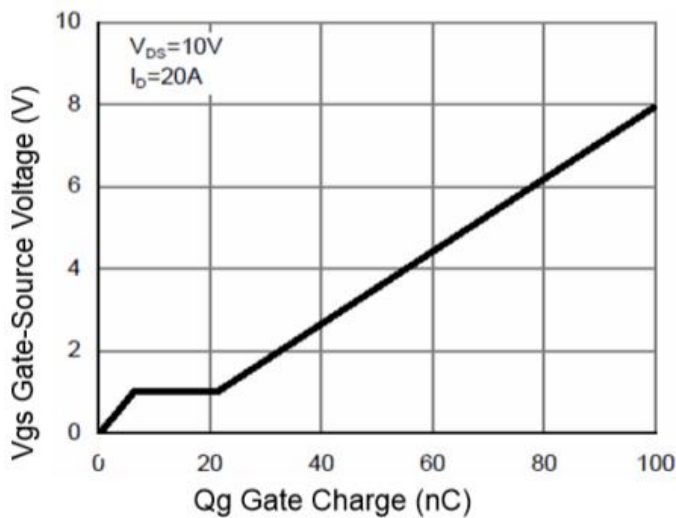


Figure 5 Gate Charge

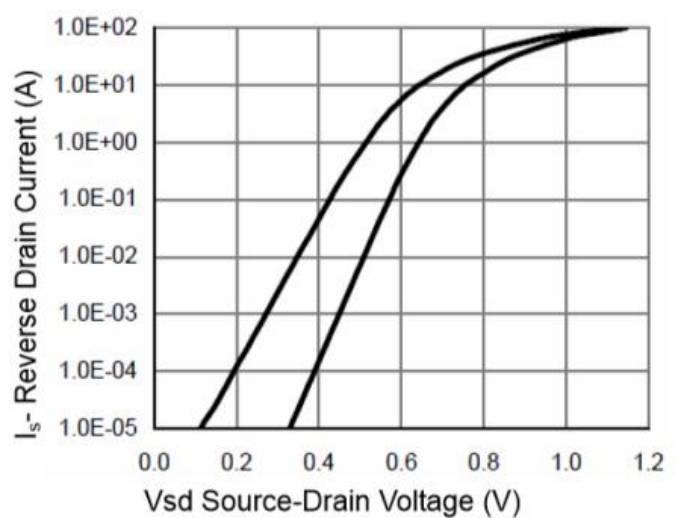


Figure 6 Source- Drain Diode Forward

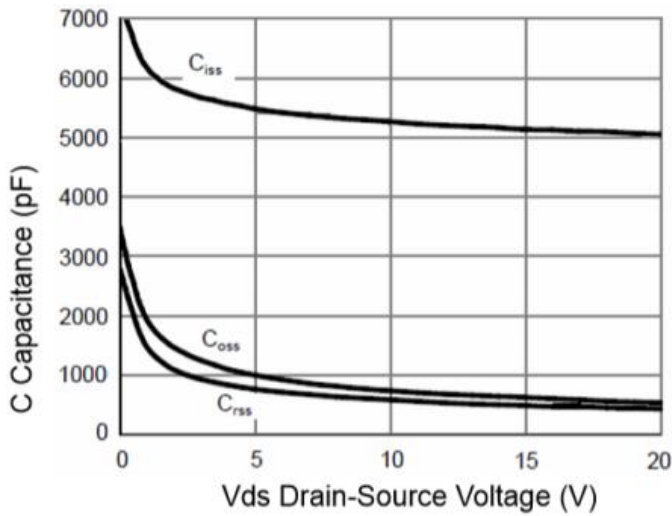


Figure 7 Capacitance vs Vds

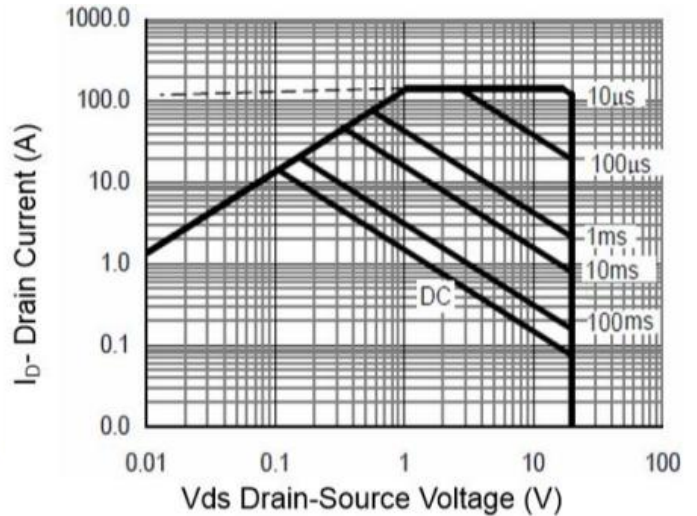


Figure 8 Safe Operation Area

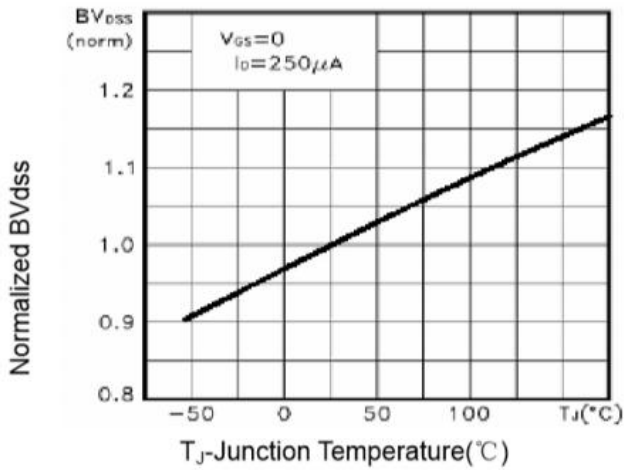


Figure 9 BV_{DSS} vs Junction Temperature

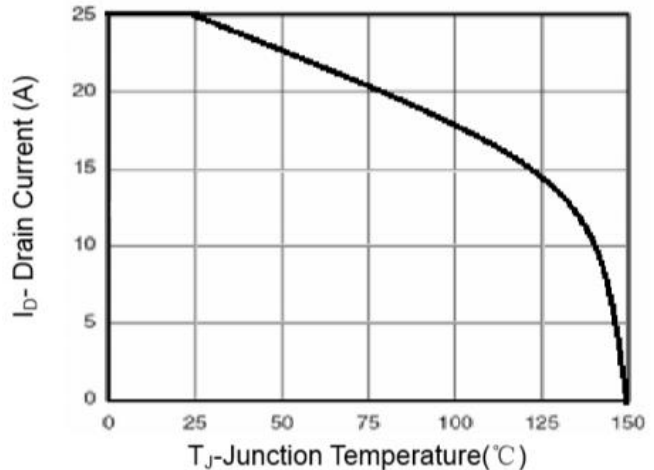


Figure 10 Current vs Junction Temperature

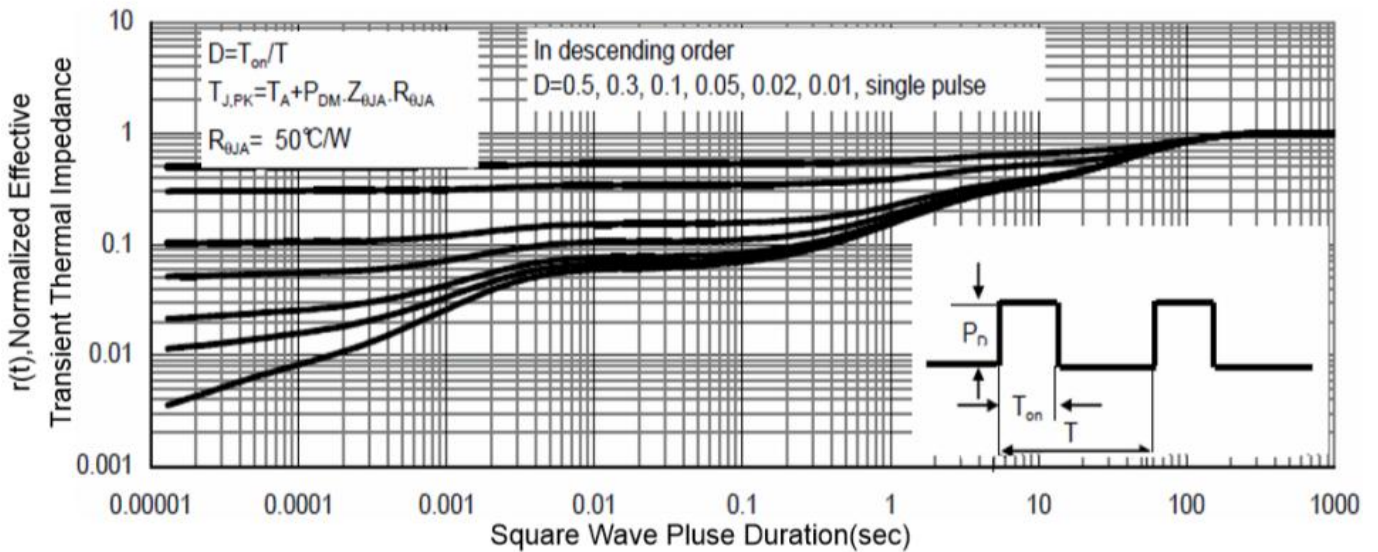


Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuits and Waveforms

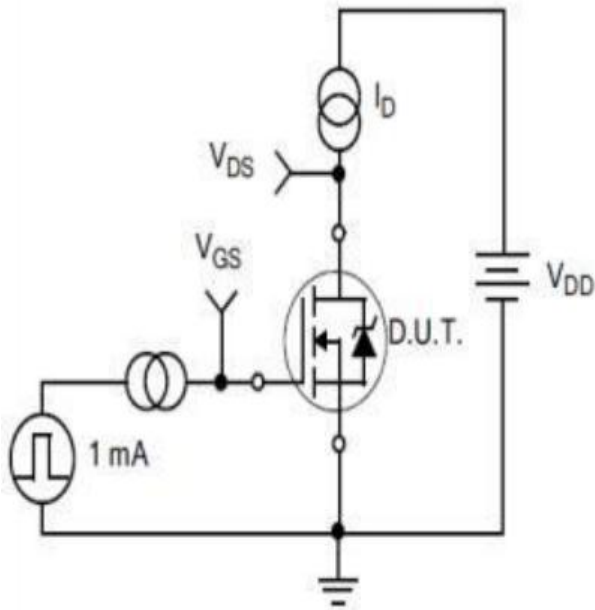


Figure A.
Gate Charge Test Circuit

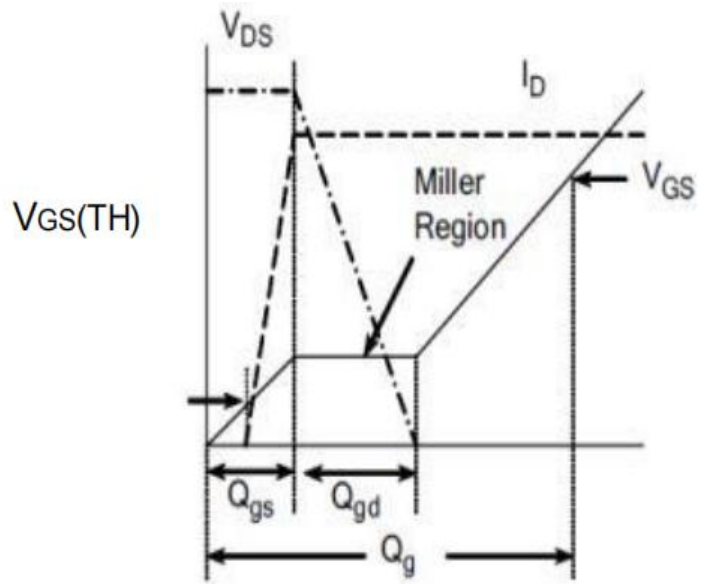


Figure B.
Gate Charge Waveform

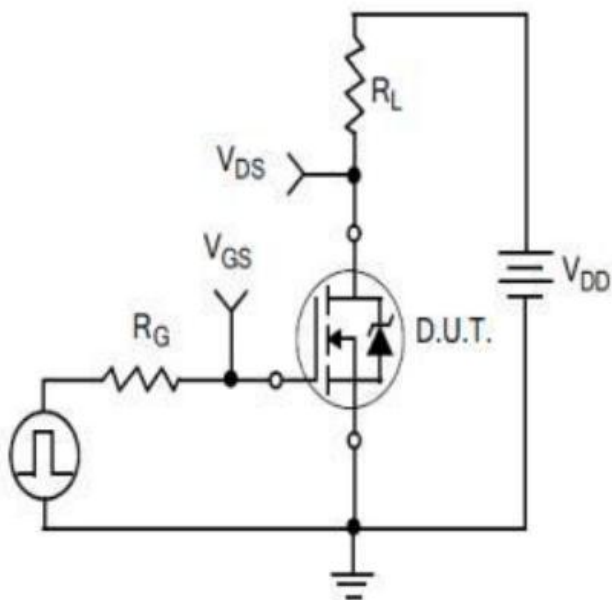


Figure C.
Resistive Switching Test Circuit

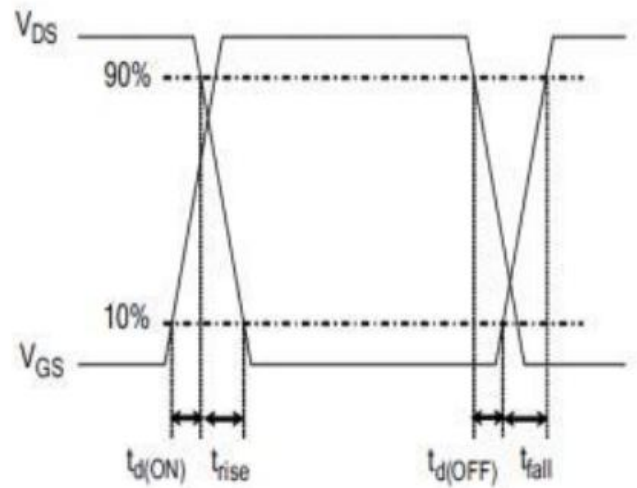


Figure D.
Resistive Switching Waveforms

Test Circuits and Waveforms

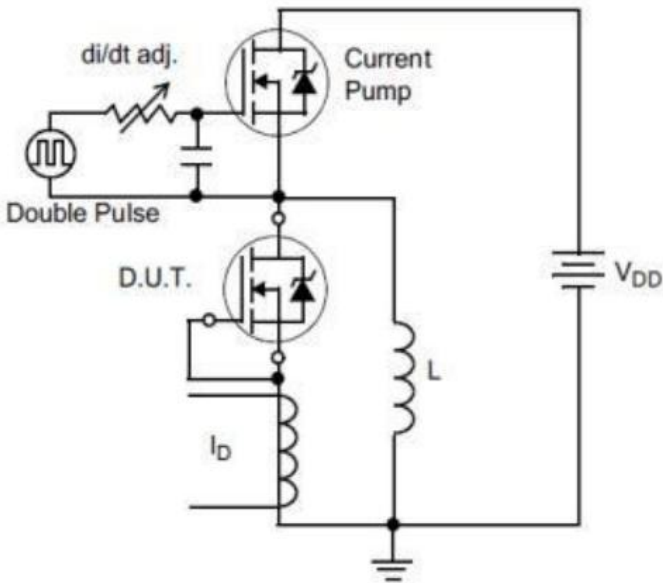


Figure E. Diode Reverse Recovery Test Circuit

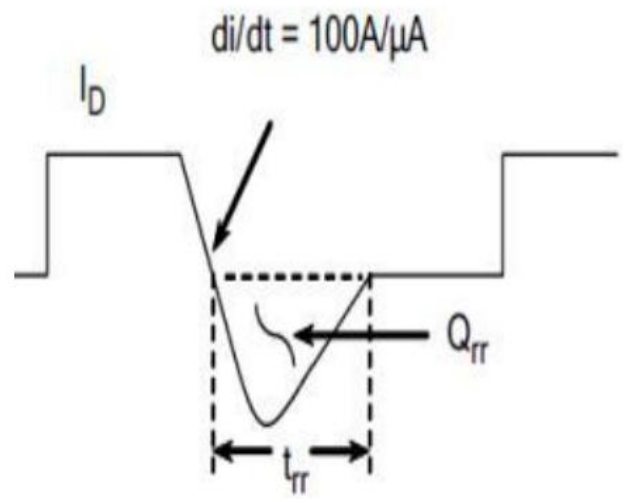


Figure F. Diode Reverse Recovery Waveform

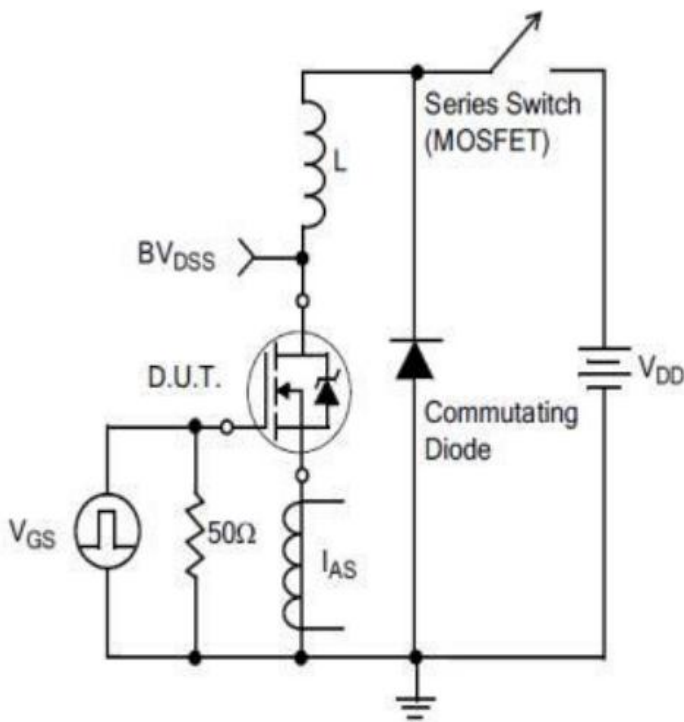
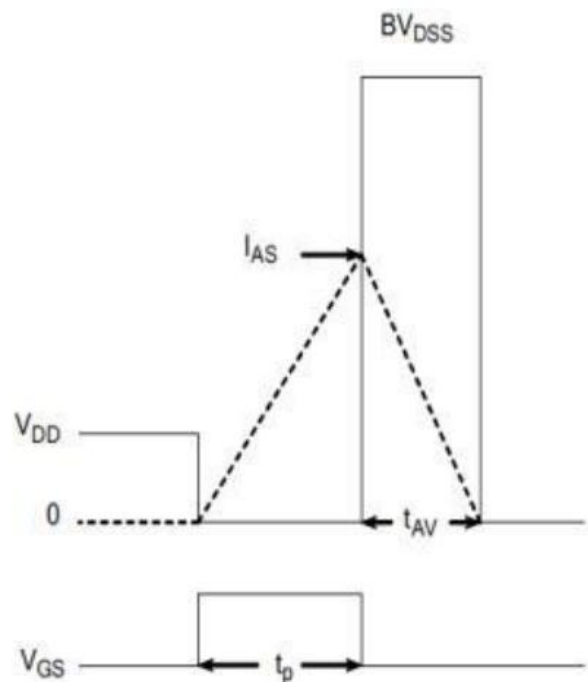


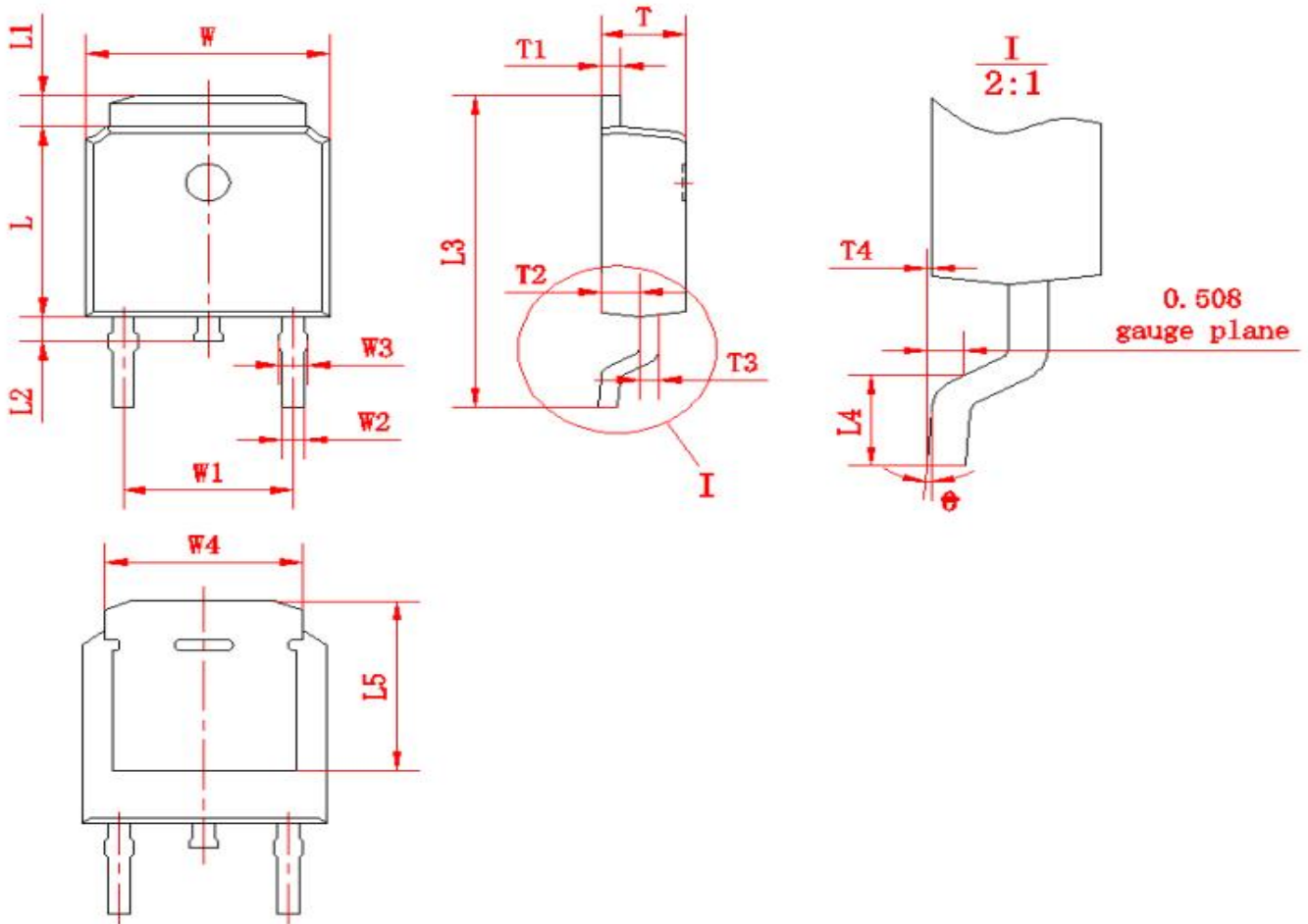
Figure G. Unclamped Inductive Switching Test Circuit



$$EAS = \frac{IAS^2 L}{2}$$

Figure H. Unclamped Inductive Switching Waveforms

Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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