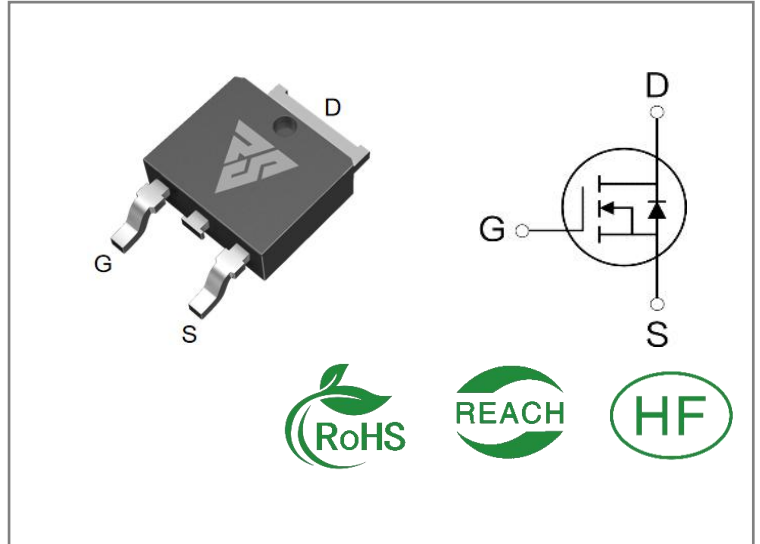


ID	R _{DS(ON)} (Typ)	VDSS
60A	6.2mΩ	30V


Applications:

- Load Switch
- PWM Applications
- Power Management

Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability

Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS30N60D	T0-252	RS30N60D	Tape&reel	2500 PCS

Absolute Maximum Ratings Tc= 25°C unless otherwise specified

Symbol	Parameter	RS30N60D	Units
VDSS	Drain-to-Source Voltage	30	V
ID	Continuous Drain Current TC=25°C	60	A
ID	Continuous Drain Current TC=100°C	35	
IDM	Pulsed Drain Current (Note*1)	140	
PD	Power Dissipation	60	W
VGS	Gate- to- Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy L = 1mH, VDD = 15V, RG = 25 Ω, TC=25°C	70	mJ
TL TPKG	Maximum Temperature for Soldering	300	°C
	Leads at 0.063in(1.6mm)from Case for 10 seconds Package Body for 10 seconds	260	
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the " Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	RS30N60D	Units	Test Conditions
R θ JC	Junction-to-Case	2.5	°C / W	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 °C
R θ JA	Junction-to-Ambient	60		1 cubic foot chamber, free air.

OFF Characteristics TJ= 25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	30	--	--	V	VGS=0V, ID=250 μ A
IDSS	Drain- to- Source Leakage Current	--	--	1	μ A	VDS=30V, VGS=0V
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	VGS=20V, VDS=0V
	Gate- to- Source Reverse Leakage	--	--	-100		VGS=-20V, VDS=0V

ON Characteristics TJ=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	6.2	7.5	m Ω	VGS=10V, ID=25A
		--	11.5	15	m Ω	VGS=4.5V, ID=20A
VGS(TH)	Gate Threshold Voltage	1.0	1.6	3.0	V	VGS=VDS, ID=250 μ A

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	10	--	nS	VDS=15V ID=20A RG=1.8 Ω
trise	Rise Time	--	8	--		
td(OFF)	Turn- OFF Delay Time	--	30	--		
tfall	Fall Time	--	5	--		

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	2000	--	pF	VGS=0V VDS=15V f=1.0MHz
Coss	Output Capacitance	--	280	--		
Crss	Reverse Transfer Capacitance	--	160	--		
Qg	Total Gate Charge	--	23	--	nC	VDS=10V ID=25A VGS=10V
Qgs	Gate- to- Source Charge	--	7	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	4.5	--		

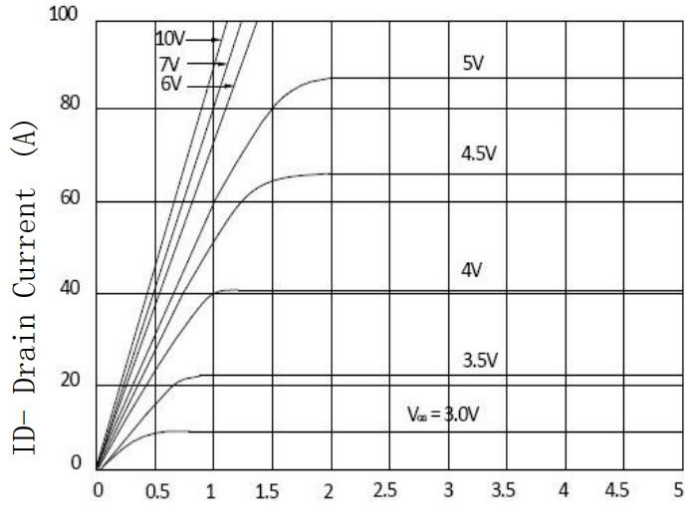
Source- Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	60	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	250	A	
VSD	Diode Forward Voltage	--	--	1.2	V	IS=8A,VGS=0V
trr	Reverse Recovery Time	--	22	--	nS	VGS=0V IS=16A di/dt=100A/μs
Qrr	Reverse Recovery Charge	--	12	--	μC	

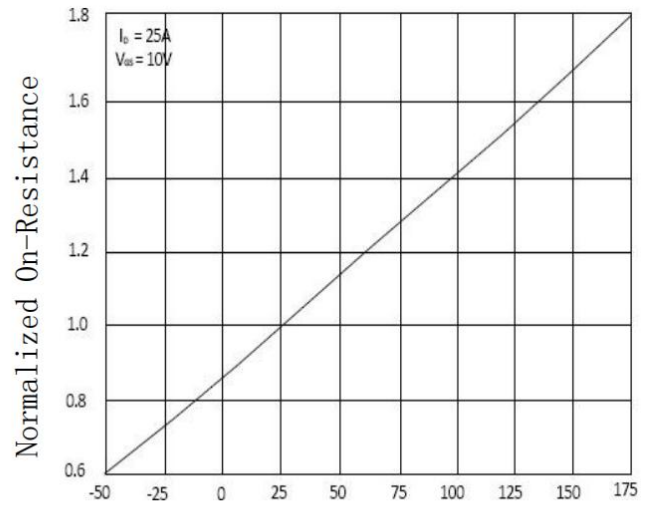
Notes:

- * 1. Repetitive rating, pulse width limited by maximum junction temperature.
- * 2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1\%$

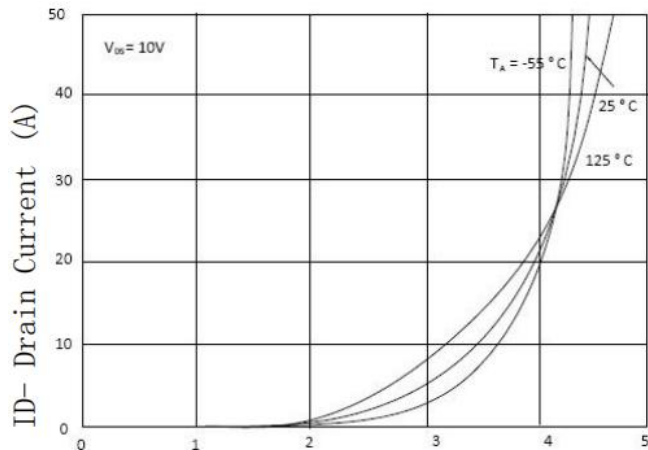
Typical Feature Curve



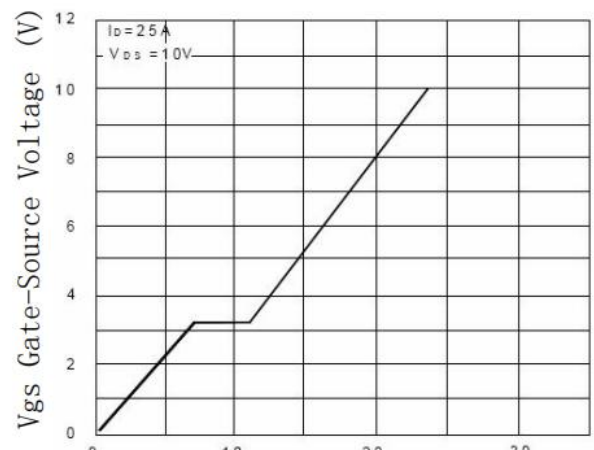
Vds Drain-Source Voltage (V)
Figure 1 Output Characteristics



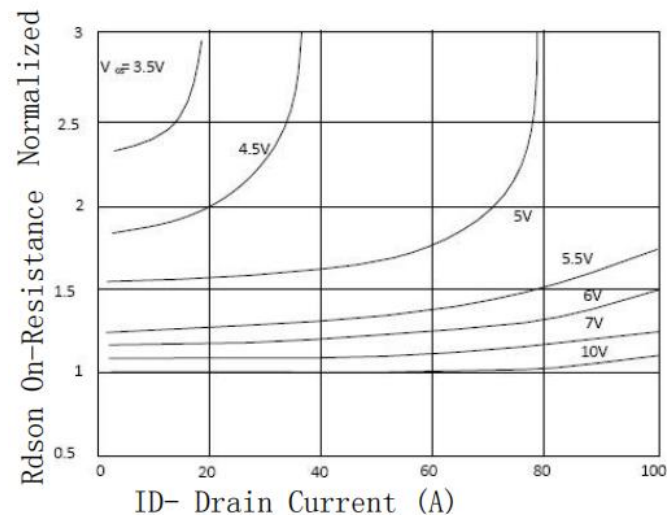
TJ-Junction Temperature (°C)
Figure 4 Rdson-Junction Temperature



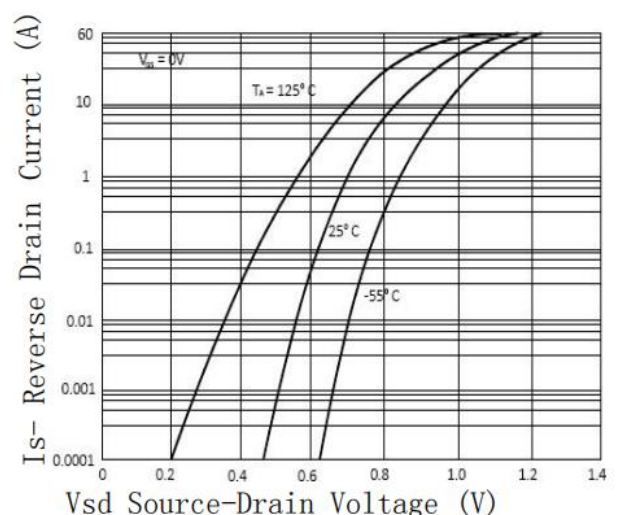
Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics



Qg Gate Charge (nC)
Figure 5 Gate Charge



ID- Drain Current (A)
Figure 3 Rdson- Drain Current



Vsd Source-Drain Voltage (V)
Figure 6 Source- Drain Diode Forward

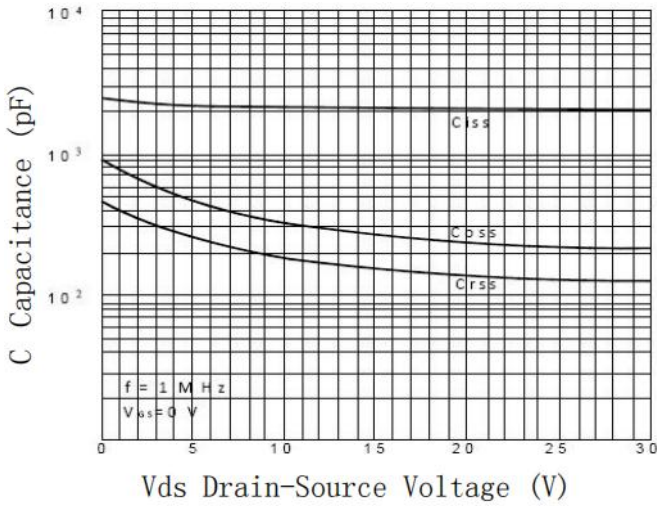


Figure 7 Capacitance vs Vds

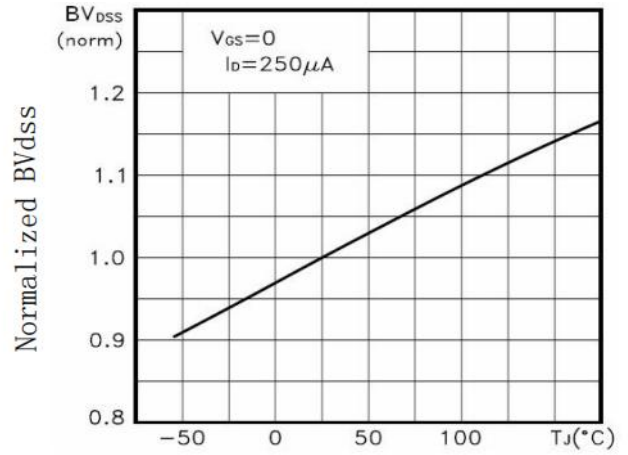


Figure 9 BVdss vs Junction Temperature

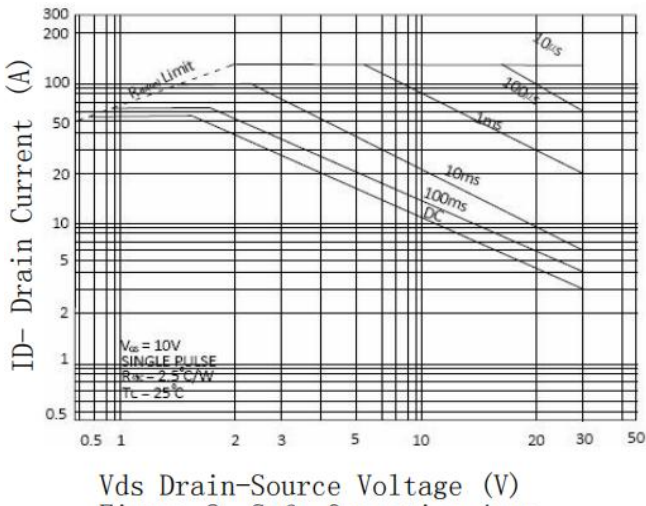


Figure 8 Safe Operation Area

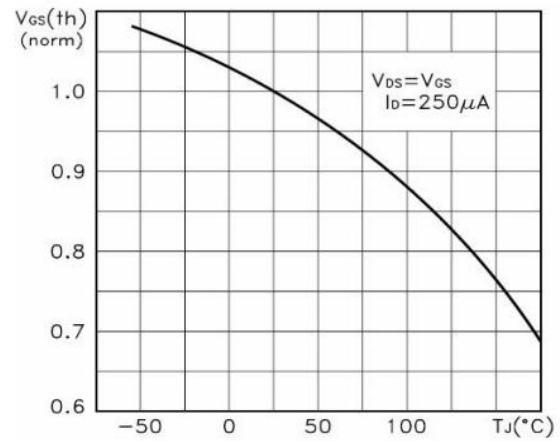


Figure 10 VGS(th) vs Junction Temperature

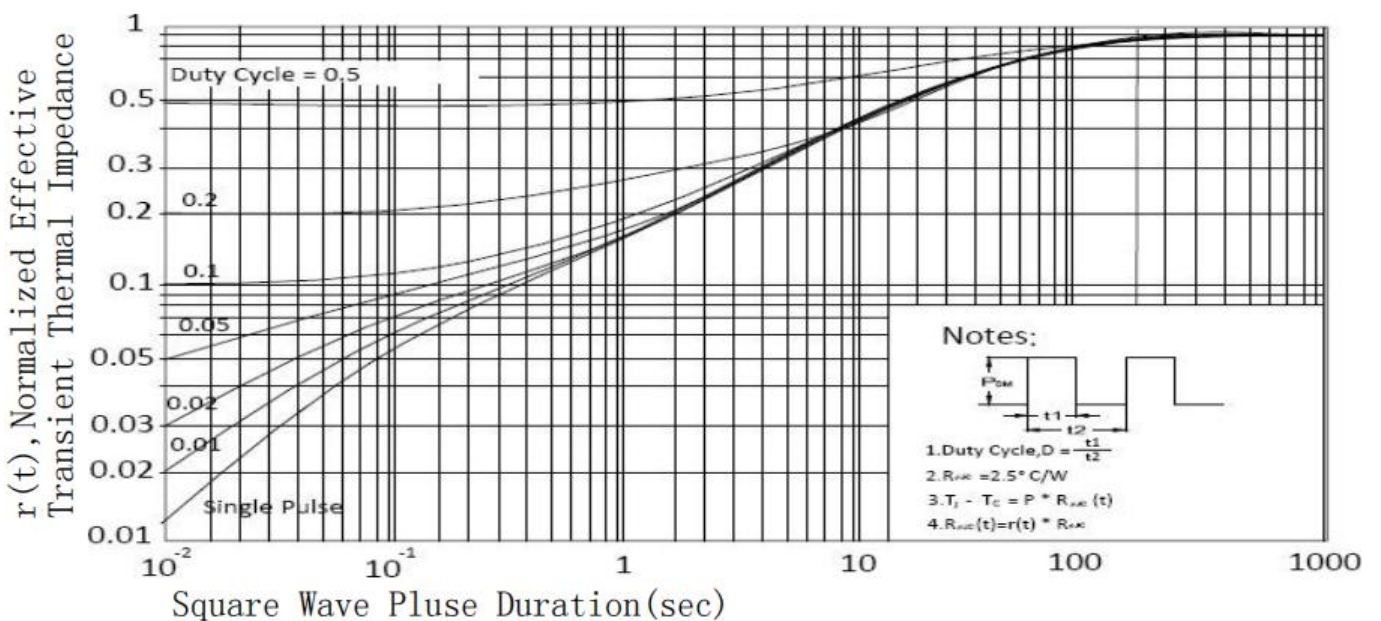


Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuits and Waveforms

Figure A: Gate Charge Test Circuit and Waveform

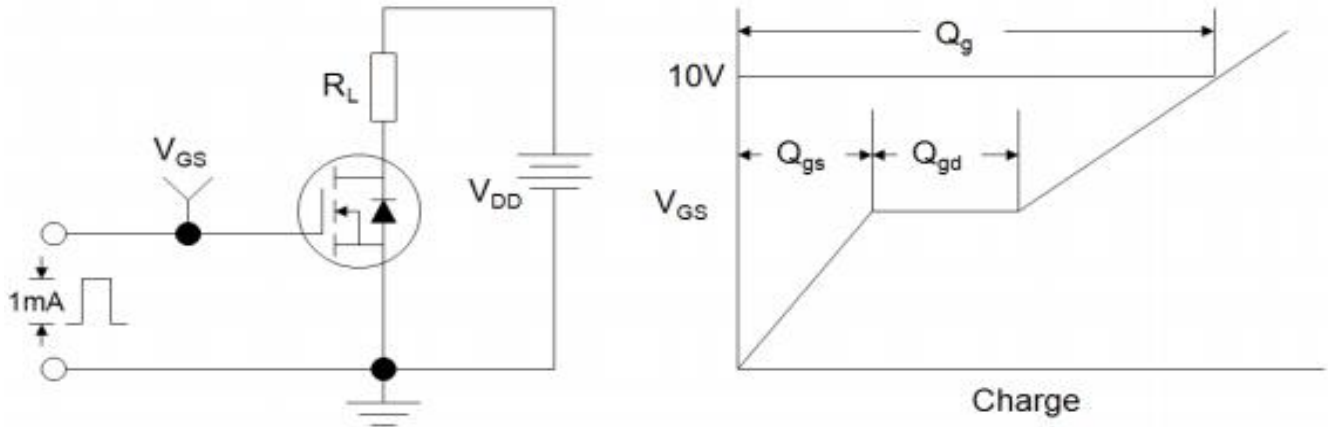


Figure B: Resistive Switching Test Circuit and Waveform

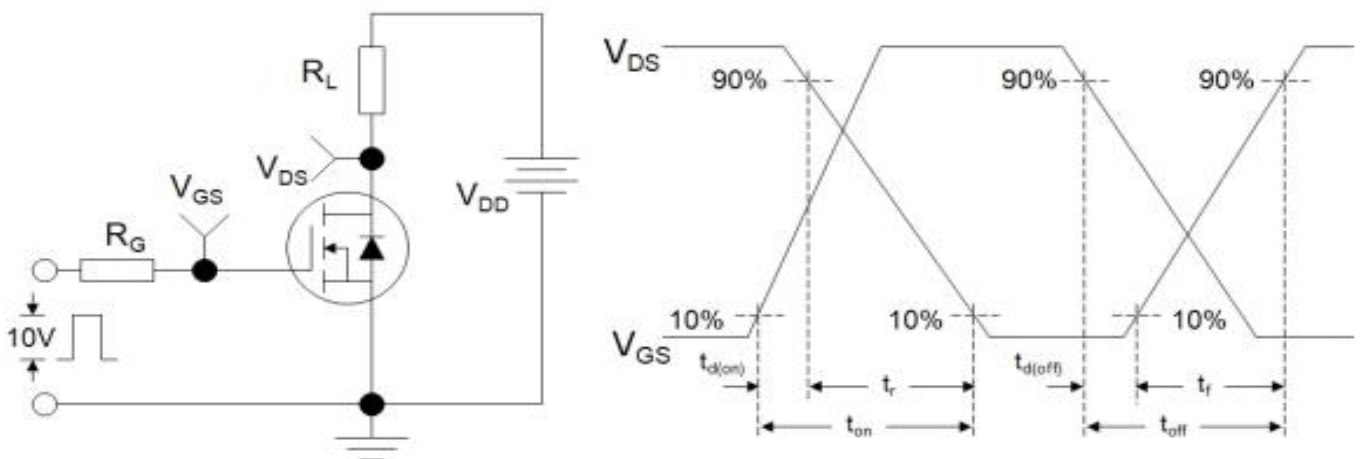
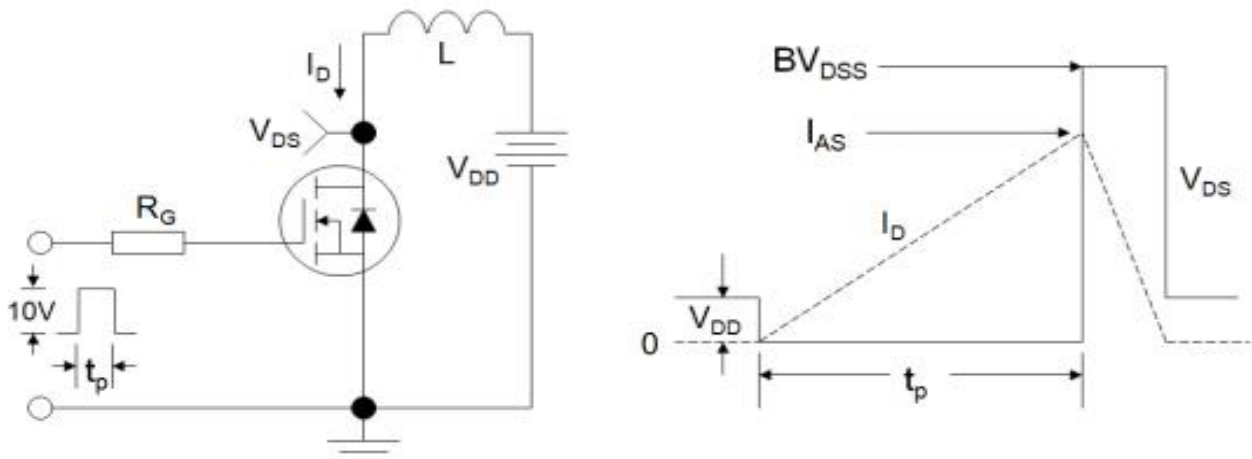
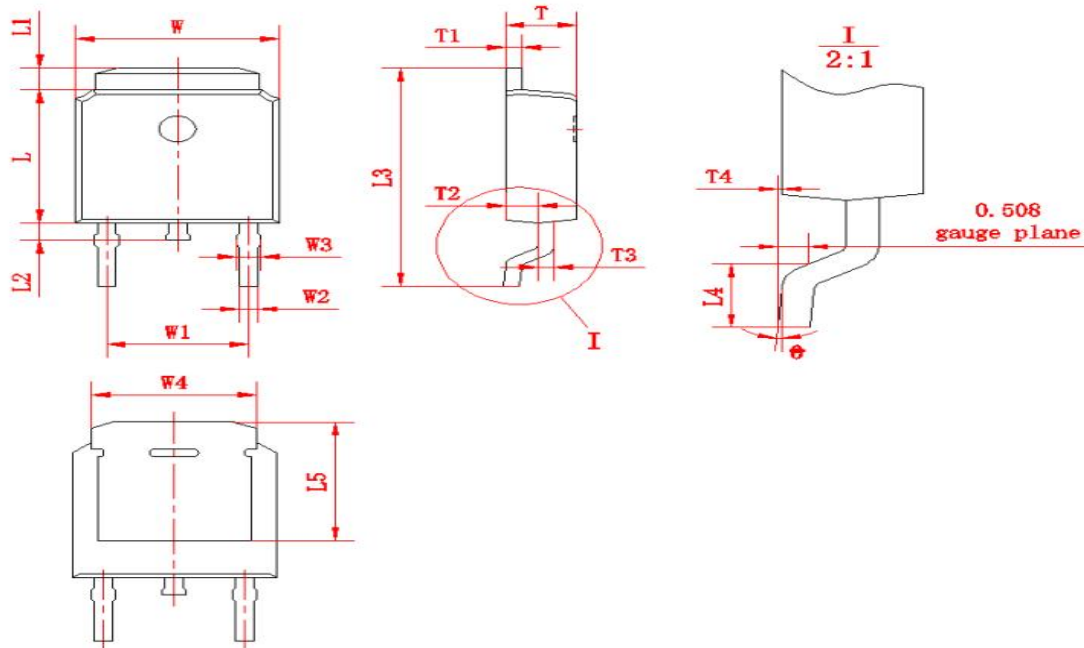


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



Package outline drawing(TO-252 Unit: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.80	1.20	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.6	0.8	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0.00	0.12
W4	(5.3)		L5	(5.20)		0	0	8
L	6.00	6.20	T	2.20	2.40			

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