Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

S6J3200 Series

32-bit Microcontroller TRAVEO™ T1G Family

The TRAVEO™ T1G MCU S6J3200 family features 32-bit RISC microcontrollers with an Arm® Cortex®- R5 core and operates up to 240 MHz. This microcontroller comes with highly-efficient 2D/3D graphic engines with advanced feature-sets for memory saving, safety, and high image quality to help manufacturers take advantage of the lower overall system costs. It also meets the increasingly high levels of performance and quality that industrial, consumer, and automotive applications demand. In addition, this microcontroller offers support for the Cypress HyperBus™ memory interface, a breakthrough that dramatically improves read performance while reducing the number of pins. This microcontroller comes with Ethernet AVB, CAN-FD, a high-speed communication protocol compatible with the conventional CAN, and Secure Hardware Extension (SHE) as a security function.

Features

System
- 32-bit Arm Cortex-R5F CPU core at up to 240 MHz
- GPIO port: Up to 120
- 12-bit A/D converter: Up to 50 channels
- External interrupt: Up to 16 channels
- Base timer: Up to 24 channels
- 32-bit free-run timer: Up to 12 channels
- Built-in CR oscillators
- Real-time clock
- Input capture unit: Up to 24 channels
- Output compare unit: Up to 24 channels
- DMA controller: 16 channels
- Stepper motor controller (SMC): Six units
- JTAG debug interface

Graphics and Display
- 2D graphic engine
- 3D graphic engine (optional)
- Timing generator - TCON
- TTL/RSDS
- FPD-Link – LVDS (optional)
- Video capture (optional)
- Communication: Ethernet AVB MAC (optional)
- CAN-FD: up to four channels
- Multi-function serial interface : up to 12 channels, selec table protocol: UART, CSIO, LIN, and I^2C
- MediaLB: up to one channel (optional)

Memory
- Cypress HyperBus Memory interface
- Dual quad double data rate SPI Flash Interface

Multimedia
- I2S input/output: Up to two units
- PCM to PWM output unit
- Sound mixer (optional): 1 unit x 10 inputs (optional)
- Stereo audio DAC (optional)

Security and Safety
- Secure Hardware Extension
- Safety features, such as MPU, TPU, ECC, and others
- CRC generator: One channel
- Watchdog timer with window function
- Low-voltage detector
- Clock supervisor for all source clocks

Table of Contents

1. Overview ... 3
1.1 Document Definition ... 3
2. Function List ... 4
2.1 Function List ... 4
2.2 Optional Function ... 7
3. Product Description ... 15
3.1 Overview ... 15
3.2 Product Description ... 15
4. Package and Pin Assignment ... 22
4.1 Pin Assignment ... 22
4.2 Package Dimensions ... 39
5. I/O Circuit Type ... 44
5.1 I/O Circuit Type ... 44
5.2 Note ... 51
6. Port Description ... 52
6.1 Port Description List ... 52
6.2 Remark ... 70
7. Precautions and Handling Devices ... 70
7.1 Handling Precautions ... 70
7.2 Handling Devices ... 73
8. Electric Characteristics ... 75
8.1 Absolute Maximum Rating ... 75
8.2 Operation Assurance Condition ... 79
8.3 DC Characteristics ... 84
8.4 AC Characteristics ... 98
8.5 A/D Converter ... 173
8.6 Audio DAC ... 177
8.7 Flash Memory ... 180
9. Abbreviation ... 181
10. Ordering Information ... 183
11. Errata ... 185
12. Appendix ... 190
12.1Application 1: JTAG tool Connection ... 190
13. Major Changes ... 191
13.1Supplementary Information ... 191
Document History ... 214
Sales, Solutions, and Legal Information ... 225

1. Overview

1.1 Document Definition

Following are the related documents of S6J3200.

Table 1-1

Document Type	Definition	Primary User	Document Code
Datasheet	The function and its characteristics are specified quantitatively.	Investigator and hardware engineer	002-05682 Revision (Previous: DS708-00003-Revision)
S6J3200 hardware manual	The function and operation of the S6J3200 series are described.	Software engineer	002-04852 Revision
TRAVEO™ T1G Platform hardware manual	The function and operation of the CPU core platform are described.	Software engineer	002-04854 Revision
Application note	The reference software, sample application, the reference board design, and so on are explained.	Software and hardware engineer	002-09861 Revision 002-09715 Revision 002-04455 Revision 002-04096 Revision 002-12061 Revision 002-04452 Revision 002-09716 Revision 002-11319 Revision 002-02495 Revision

Notes:

- *Refer to all documents for the system development.*
- *"Primary user" is most likely the engineer for whom the document is the most useful.*
- *The description of the datasheet and the S6J3200 hardware manual should precede the duplicated description of TRAVEO™ T1G platform hardware manual.*
- *The TRAVEO™ T1G platform hardware manual is expected to be used as a dictionary of platform specification.*
- *Document code usually includes its revision.*
- *Revised information from the previous revision can be seen the supplementary information.*

2. Function List

2.1 Function List

The table shows the functions which are implemented in S6J3200 series.

Table 2-1

Function	Description	Remark
CPU core	Arm Cortex R5F	
FPU	Available (Double precision and Single precision)	
PPU	Available	
MPU	Available	
TPU	Available	
Endian	Little endian	
Core clock frequency	Option	See 2.2.1 and AC specification on the datasheet.
HPM bus frequency	Option	See AC specification on the datasheet
Resource clock frequency	Option	See AC specification on the datasheet
Embedded CR oscillation	Slow clock:100 kHz, Fast clock: 4 MHz (Center frequency)	See AC specification on the datasheet
PLL	PLL0, 1, 2, 3	
SSCG PLL	SSCG0, 1, 2, 3	
Clock supervisor	Available	
DMA	16 ch	
Boot-ROM	16 Kbytes	
JTAG	Available	
Data cache	16 Kbytes	
Instruction cache	16 Kbytes	
Program FLASH	Option	See 2.2.1
Work FLASH	112 Kbytes	
TC-RAM	Option	See 2.2.1
System-RAM	Option	See 2.2.1
Backup-RAM	16 Kbytes	
Security (SHE)	Option	See 2.2.1
Low latency interrupt	Available	
Power domain	5 domains	
Power supply	5 V +/- 0.5 V, 3.3 V +/- 0.3 V, 1.2 V +/- 0.1 V	
Embedded LDO power supply for 5.0 V	Available	
Low-voltage detection of external power supply	Available	
Low-voltage detection of internal LDO output	Available	
Hardware watchdog timer	Available	
Software watchdog timer	Available	
Package	Option	See 2.2.1
AUTOSAR	AUTOSAR 4.0.3	
General Purpose I/O	Option	See 2.2.3
Quad Position & Revolution Counter (Up/Down Counter)	2 ch	
I/O timer	3 unit x 8 ch	
32 bit Reload timer	14 ch	
Real time clock	Available	Automatic calibration
Sound generator	4 ch	
Sound waveform generator	Option 1 unit x 5 outputs	See 2.2.1

Function	Description	Remark
Sound mixer	Option 1 unit x 10 inputs	See 2.2.1
Stereo audio DAC	Option 1 unit (L and R)	See 2.2.1
PCM-PWM	Option 1 unit (L and R)	See 2.2.1
Base timer	12 units (24 ch)	
Free-run timer	12 ch	
Input Capture Unit	12 unit (24channels of capture)	
Output Compare Unit	12unit (24 channels of compare match)	
Stepping motor controller (SMC)	For 6 gauges	
12 bit-A/D converter	Option 1 unit x 50 input ports (Max)	See 2.2.3
CRC	4 unit	
Programmable CRC	1 unit	
Source clock timer	4 ch	
NMI	Available	
External interrupt	16 ch	
Internal interrupt	512 vectors	
I2S	2 ch	One only supports an output as a function of the sound system.
DDR HSSPI	2 ch	A type of Quad SPI
HyperBus (RPC2)	Option	See 2.2.1 See AC specification on the datasheet.
Multi-function serial interface	12 ch	
CAN-FD	4 ch	
CAN-FD RAM (ECC supported)	16KB/ch It equivalents to 128 message buffer per channel of CCAN module	
Ethernet AVB	Option	See 2.2.1
Media-LB (MOST25)	Option	See 2.2.1
LCD controller	Option 4 COM x 32 SEG (Max)	See 2.2.3
Indicator PWM	1 ch	
MPU for AHB	1 unit	
MPU for AXI	1 unit	
Internal VRAM	Option	See 2.2.1
Graphic engine clock	Option	See 2.2.1
Graphic AXI clock	Option	See 2.2.1
Display clock	Option 64 MHz (ch.0), 50 MHz(ch.1)	See 2.2.1
Display clock source	Graphic display controller clock or external clock	
Target frame rate	60 fps	
Number of display outputs	Option Maximum 2 outputs simultaneously	See 2.2.1
TTL output (RGB888)	Option	See 2.2.1
RSDS/TCON support	1 output	
FPD-Link (LVDS)	Option 1 output, 350 Mbps (Max)	See 2.2.1
Video capture unit	Option	See 2.2.1
Video capture format	ITU656, YCbCr4:4:4, YCbCr4:2:2, RGB888, RGB666	
2D Graphic engine	1 unit	
2.5D support	Available	
Vector drawing on 2D engine	Available	
Warping	Available	
Scale/Rotate/Blend	Available	
2D Driver API	CYPRESS proprietary	

Function	Description	Remark
3D Graphic engine	Option	See 2.2.1
Vector drawing on 3D engine	Option	See 2.2.1
3D Driver API	Option	See 2.2.1

Notes:

- *The options are described in 2.2.*
- *The described specifications in the table which are related the electric characteristics only show the typical values. They don't necessarily include the width of characteristics, errors, and so on. They should be seen in the datasheet in detailed.*
- *Target resolution of graphics is WVGA 800 x 480, WQVGA 480 x 272.*
- *Target capture resolution of graphics is WVGA 800 x 480.*

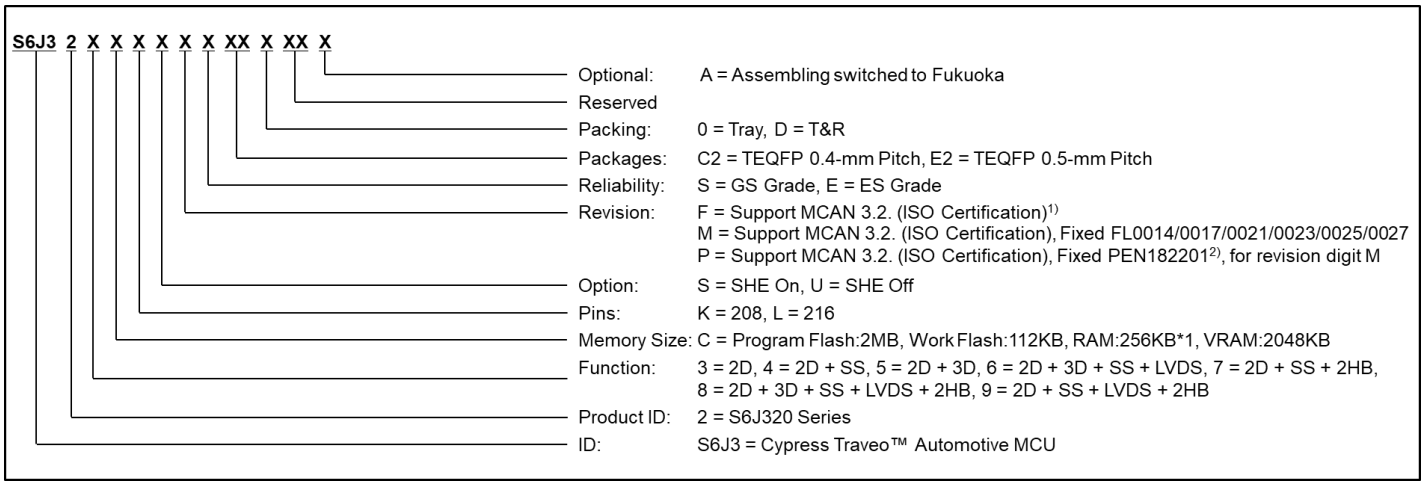
2.2 Optional Function

2.2.1 Basic Option

The following figure shows the optional function and the part number relations of the series.

2.2.1.1 S6J320C

Figure 2-1: Option and Part Number for S6J320C



*1 TCRAM: 128 KB + System-RAM: 128 KB

1) Please contact your Cypress sales representative to receive the customer information CI708-0001
2) Please contact your Cypress sales representative to receive the product errata notification PEN182201

Table 2-2: Function Digit Table

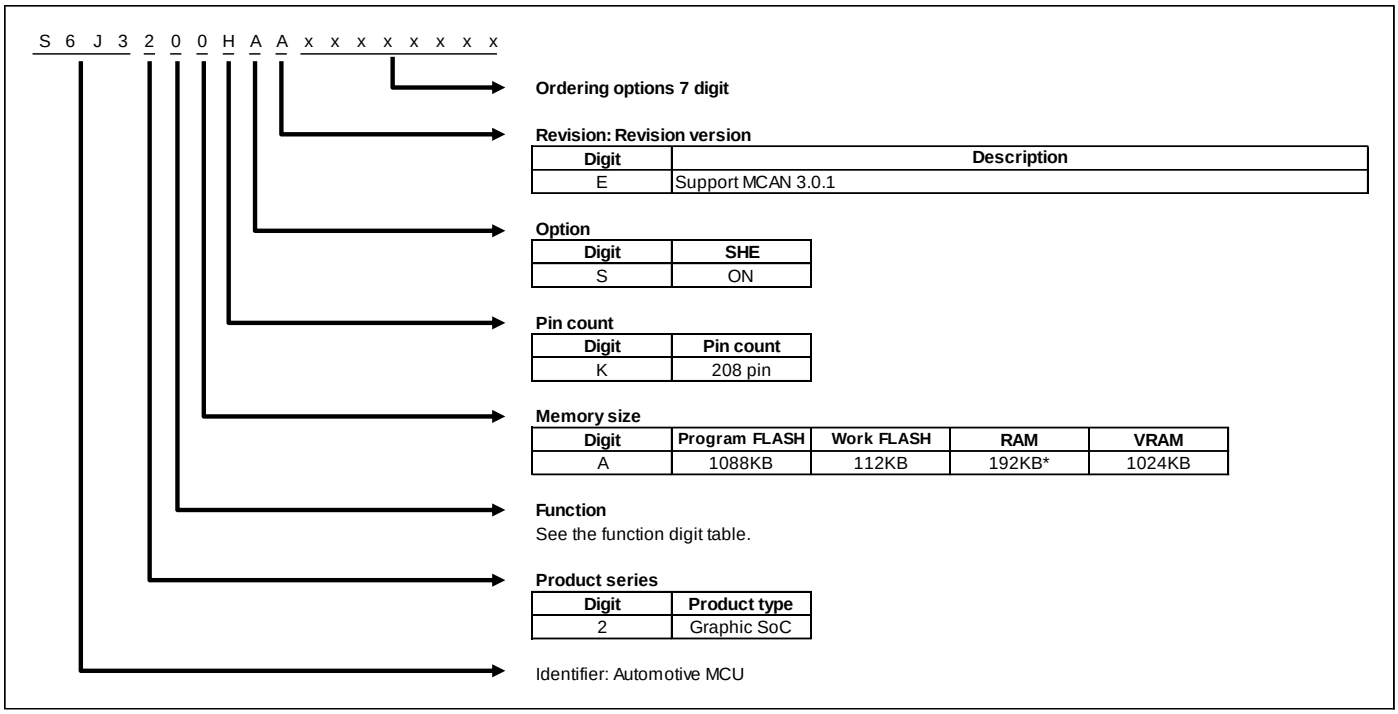
Part Number	S6J32X (X = Function Digit)						
Function Digit	**3**	**4**	**5**	**6**	**7**	**8**	**9**
CPU Clock Maximum	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz	240 MHz
Graphics Clock Maximum	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz
Display Output Support	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1
Video Capture Support	1 unit	1 unit	1 unit	1 unit	1 unit	1 unit	1 unit
Graphic Engine Type	2D	2D	2D, 3D	2D, 3D	2D	2D, 3D	2D
HyperBus Interface	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1, 2	ch.0, 1, 2	ch.0, 1, 2
Sound System	N/A	YES	N/A	YES	YES	YES	YES
FPD-Link	N/A	N/A	N/A	YES	N/A	YES	YES
Media System	YES	YES	YES	YES	YES	YES	YES
Chip Select Output of MFS	YES	YES	YES	YES	YES	YES	YES
I^2C	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *Display Output ch.1 is used for FPD-LINK (LVDS) and DRGB (Digital RGB). The ch.1 of the product which doesn't support FPD-LINK is used for DRGB only.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

2.2.1.2 S6J320A

Figure 2-2: Option and Part Number for S6J320A



* TCRAM: 64 KB + System-RAM: 128 KB

Table 2-3: Function Digit Table

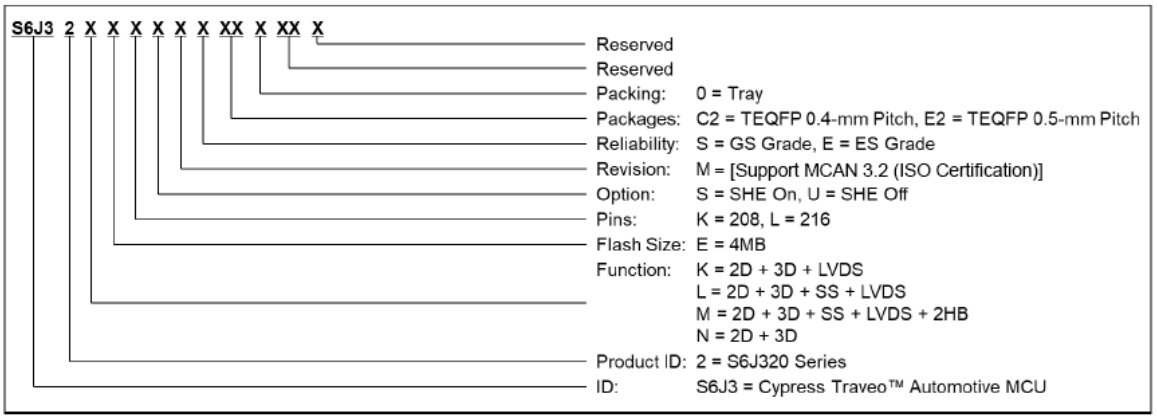
Part Number	S6J32X (X = Function Digit)
Function Digit	**B**
CPU Clock Maximum	160 MHz
Graphics Clock Maximum	160 MHz
Display Output Support	ch.0
Video Capture Support	N/A
Graphic Engine Type	2D
HyperBus Interface	ch.0, 1
Sound System	YES
FPD-Link	N/A
Media System	N/A
Chip Select Output of MFS	N/A
I^2C	MFS ch.16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

2.2.1.3 S6J320E

Figure 2-3: Option and Part Number for S6J320E



*1 TCRAM: 128 KB + System-RAM: 384 KB

Table 2-4: Function Digit Table

Part Number	S6J32X (X = Function Digit)			
Function Digit	**K**	**L**	**M**	**N**
CPU Clock Maximum	240 MHz	240 MHz	240 MHz	240 MHz
Graphics Clock Maximum	200 MHz	200 MHz	200 MHz	200 MHz
Display Output Support	ch.0, 1	ch.0, 1	ch.0, 1	ch.0, 1
Video Capture Support	1 unit	1 unit	1 unit	1 unit
Graphic Engine Type	2D, 3D	2D, 3D	2D, 3D	2D, 3D
HyperBus Interface	ch.0, 1	ch.0, 1	ch.0, 1, 2	ch.0, 1
Sound System	N/A	YES	YES	N/A
FPD-Link	YES	YES	YES	N/A
Media System	YES	YES	YES	YES
Chip Select Output of MFS	YES	YES	YES	YES
I^2C	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17	MFS ch.4, 10, 12, 16, 17

Notes:

- *This table only shows the relation between the optional function and the part numbers. That is, all products are not necessarily available for orders. See the order number on the datasheet, and confirm actual availabilities of products.*
- *The sound system is composed of the sound waveform generator, the sound mixer, the audio DAC, PCM-PWM, and I2S0.*
- *The media system means both Ethernet AVB and Media LB.*
- *The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.*
- *Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB.*
- *Display Output ch.1 is used for FPD-LINK (LVDS) and DRGB (Digital RGB). The ch.1 of the product which doesn't support FPD-LINK is used for DRGB only.*
- *HyperBus Interface ch.0 for MCU and ch.1 for graphic subsystem cannot be used simultaneously.*

2.2.2 ID

ID is specified for each function digit and revision, which is defined in Figure 2-1 through Figure 2-3. The Chip ID can be read from SYSC0_SYSIDR and the Platform ID can be read from SYSC0_SYSPFIDR. For SYSC0_SYSIDR and SYSC0_SYSPFIDR, see the TRAVEO™ T1G Platform hardware manual.

The Graphic subsystem ID can be read from the IPIdentifier register on the graphic subsystem. See the chapter Graphic Subsystem in S6J3200 hardware manual.

Function Digit	Option	Revision	Chip ID	JTAG ID	Platform ID	Graphic Subsystem
3, 4, 5, 6, 7, 8, 9	S and U	A	0x10100000	0x100085CF	0x00110200	N/A
		B	-	-	-	-
		C and D	0x10100100	0x1000C5CF	0x00110200	N/A
		E and F	0x10100101	0x1000C5CF	0x00110200	0x23443420
		H	0x10100102	0x1000C5CF	0x00110200	0x23443470
		J	0x10100103	0x1000C5CF	0x00110200	0x23443480
		M	0x10100104	0x1000C5CF	0x00110200	0x23443490
		P	0x10100104	0x1000C5CF	0x00110200	0x23443490
B	S	A	-	-	-	-
		B	0x10110000	0x100095CF	0x00110200	N/A
		C and D	-	-	-	-
		E	0x10110002	0x100095CF	0x00110200	0x23442450
K	S	M	0x10170000	0x002705CF	0x00110200	0x23443490
L	S			0x002715CF		
M	S			0x002725CF		
N	S			0x002735CF		

2.2.3 Restriction

Some functions have restrictions which depend on package pin counts.

Table 2-5

Function	TEQFP256	TEQFP216	TEQFP208
Analog input port (12 bit-ADC)	AN0 to AN49 (50 ports)	AN0 to AN49 (50 ports)	AN1 to AN3, AN5 to AN17, AN20 to AN49 (46 ports)
SEG port of LCD controller	SEG0 to SEG31 (32 ports)	SEG0 to SEG31 (32 ports)	SEG0 to SEG29 (30 ports)

Function	TEQFP256	TEQFP216	TEQFP208
General Purpose I/O	P0_00, P0_01, P0_02, P0_03, P0_04, P0_05, P0_06, P0_07, P0_08, P0_09, P0_10, P0_11, P0_12, P0_13, P0_14, P0_15, P0_16, P0_17, P0_18, P0_19, P0_26, P0_27, P0_28, P0_30, P0_31, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P2_16, P2_17, P2_19, P2_22, P2_24, P2_25, P2_26, P2_27, P2_28, P2_29, P2_30, P2_31, P3_00, P3_01, P3_02, P3_03, P3_04, P3_05, P3_06, P3_07, P3_08, P3_09, P3_10, P3_11, P3_12, P3_13, P3_14, P3_15, P3_16, P3_17, P3_18, P3_19, P3_20, P3_21, P3_22, P3_23, P3_24, P3_25, P3_26, P3_27, P3_28, P3_29, P3_30, P3_31, P4_00, P4_01, P4_02, P4_03, P4_04, P4_05, P4_06, P4_07, P4_08, P4_09, P4_10, P4_11, P4_12, P4_25, P4_26, P4_27, P4_28, P4_29, P4_30, P4_31, P5_00, P5_01, P5_02, P5_03, P5_04, P5_05, P5_06, P5_07, P5_08, P5_09, P5_10, P5_11, P5_12, P5_13, P5_14, P5_15, P5_16, P5_17, P5_18, P5_19, P5_20, P5_21, P5_22, P5_27, P5_28, P5_29, P5_30, P5_31, P6_00, P6_01, P6_02, P6_03, P6_04, P6_05, P6_06, P6_07, P6_08, P6_09, P6_10, P6_11, P6_12, P6_13, P6_14, P6_15, P6_16, P6_17, P6_18, P6_19, P6_20, P6_21, P6_22, P6_23, P6_24, P6_25, P6_26 (154 ports)	P0_00, P0_01, P0_02, P0_03, P0_04, P0_05, P0_06, P0_07, P0_08, P0_09, P0_10, P0_11, P0_12, P0_13, P0_14, P0_15, P0_16, P0_17, P0_18, P0_19, P0_26, P0_27, P0_28, P0_30, P0_31, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P2_16, P2_17, P2_19, P2_22, P2_24, P2_25, P2_26, P2_27, P2_28, P2_29, P2_30, P2_31, P3_00, P3_01, P3_02, P3_03, P3_04, P3_05, P3_06, P3_07, P3_08, P3_09, P3_10, P3_11, P3_12, P3_13, P3_14, P3_15, P3_16, P3_17, P3_18, P3_19, P3_20, P3_21, P3_22, P3_23, P3_24, P3_25, P3_26, P3_27, P3_28, P3_29, P3_30, P3_31, P4_00, P4_01, P4_02, P4_03, P4_04, P4_05, P4_06, P4_07, P4_08, P4_09, P4_10, P4_11, P4_12, P4_25, P4_26, P4_27, P4_28, P4_29, P4_30, P4_31, P5_00, P5_01, P5_02, P5_03, P5_04, P5_05, P5_06, P5_07, P5_08, P5_09, P5_10, P5_11, P5_12, P5_13, P5_14, P5_15, P5_16, P5_17, P5_18, P5_19, P5_20, P5_21, P5_22, P5_27, P5_28, P5_29, P5_30, P5_31, P6_00 (128 ports)	P0_00, P0_01, P0_04, P0_05, P0_06, P0_07, P0_08, P0_09, P0_10, P0_11, P0_12, P0_13, P0_14, P0_15, P0_16, P0_17, P0_18, P0_19, P0_26, P0_27, P0_28, P0_30, P0_31, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P2_16, P2_17, P2_19, P2_22, P2_25, P2_26, P2_27, P2_29, P2_30, P2_31, P3_00, P3_01, P3_02, P3_03, P3_04, P3_05, P3_06, P3_07, P3_08, P3_09, P3_12, P3_13, P3_14, P3_15, P3_16, P3_17, P3_18, P3_21, P3_22, P3_23, P3_24, P3_25, P3_26, P3_27, P3_28, P3_29, P3_30, P3_31, P4_00, P4_01, P4_02, P4_03, P4_04, P4_05, P4_06, P4_07, P4_08, P4_09, P4_10, P4_11, P4_12, P4_25, P4_26, P4_27, P4_28, P4_29, P4_30, P4_31, P5_00, P5_01, P5_02, P5_03, P5_04, P5_05, P5_06, P5_07, P5_08, P5_09, P5_10, P5_11, P5_12, P5_13, P5_14, P5_15, P5_16, P5_17, P5_18, P5_19, P5_20, P5_21, P5_22, P5_27, P5_28, P5_29, P5_30, P6_00 (120 ports)
PPG triggered input	PPG0/1/2/3/4/5_TIN1, PPG6/7/8/9/10/11_TIN	PPG0/1/2/3/4/5_TIN1, PPG6/7/8/9/10/11_TIN	PPG6/7/8/9/10/11_TIN

Notes:

- *See multiplexed functions on pin assignment sheet.*
- *The optional restriction will be added without notification.*

3. Product Description

3.1 Overview

This section explains the product features of the S6J3200 series. The description of this section should precede the duplicated description on platform manual.

3.2 Product Description

Table 3-1: Product Features

Feature	Description
Technology	55-nm CMOS technology with embedded flash Fully automotive qualified according to ISO/TS 16949 and AEC-Q100
Functional Safety	The product series has some functional safety features suited for ASIL-B application.
Peripherals	See function list.
Power Domain (PD)	See the platform manual and the STATE TRANSITION chapter in detail. The product series supports the power-off control of PD2 (including PD3 and 5), PD4_0, PD4_1, and PD6. The power domain resets of PD3 and PD5 included in PD2 are not supported in the product series, and "0" is always read from the reset factor flags of them. This series does not support partial wakeup for PD6.
Debug and Trace	See the platform manual in detail. – Standard 5-pin JTAG interface – 4k Word Embedded Trace Buffer 4-bit trace support for TEQFP package. Full trace (dedicated 16-bit port) with special bond-out package is planned.
System Control	See the platform manual in detail. Main and sub oscillator is available. – A wide range of 3.6 - 16 MHz is available for main oscillator – 32 KHz is available for sub oscillator Sub clock is enable/disable by register settings
Clock	See the platform manual in detail. CLK_CLKO (Clock Output Function) is not supported. Main Oscillation Stabilization Wait Time (at 4 MHz):8.19 ms (Initial value)
Embedded CR oscillation	See the platform manual in detail. Stabilization time is as followings. – 0.35 ms to 0.8 ms for 4 MHz (Fast clock) – 0.43 ms to 1.28 ms for 100 kHz (Slow clock)
Clock Supervisor	See the platform manual in detail. This product series does not support the clock supervisor output port. (Related register and internal circuit is implemented.)
Reset	See the platform manual in detail. Following resets are not mounted on this device or not supported. – INITX: INITX is issued by simultaneous assert of RSTX and MODE, but this product series does not support INITX. – SRSTX (and nSRST pin) The product series does not support EX5VRST and writing EX5VRSTCNT bits in SYSC0_SPECFGR has no effect.
Hardware Watchdog	See the platform manual in detail. Hardware watchdog function stops during PSS mode. In the related register of HWDG_CFG, the bit ALLOWSTOPCLK is always read as 1 (HWDG_CFG.ALLOWSTOPCLK=1). The product series does not support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.)

Feature	Description
Software Watchdog	See the platform manual in detail. The product series doesn't support Watchdog Counter Monitor Output port. (Related register and internal circuit is implemented.)
Standby Mode	See the platform manual in detail. Standby mode with 5 V single power supply is available. Turning off the 3.3-V supply and the external 1.2-V supply in standby mode is available. The long term pulse of the indicator PWM can be outputted during RTC Standby mode.
PLL / SSCG PLL	See the platform manual in detail. Use case assumption is following. – PLL ➢ Sound system clock ➢ Sound frequency master clock ➢ Peripherals ➢ Display clock ➢ Trace clock – SSCG ➢ CPU core ➢ GDC core ➢ HyperBus ➢ DDR-HSSPI Product supports down spread and center spread modes with the conditions defined in chapter "Internal Clock Timing" on the datasheet.
External Interrupts	See the platform manual in detail.
NMI	See the platform manual in detail. 1 NMI pin.
Memory Protection	MPU16 AHB: See the platform manual in detail. MPU for AXI: ch.0 (Supervise Ethernet) MPU for AHB: ch.1 (Supervise Media LB) Additional MPU for Graphic sub system, MediaLB and Ethernet AVB. They are described on the chapter of MPU for AHB and MPU for AXI. To configure Lock or Unlock for both MPUXn_UNLOCK and MPUHn_UNLOCK, – Lock: 0x112ABB56 – Unlock: 0xACCABB56
Peripheral Protection	See the platform manual in detail. Protected peripherals are described in the base address map.
Internal Memories System RAM	See the platform manual in detail. 1 wait cycle is necessary for RAM read at over 160 MHz. No need to insert wait cycles for RAM write.
Internal Memories TCRAM	See the platform manual in detail.
Internal Memories Backup RAM	16 KB Backup RAM can only be operated in RUN mode (normal operation mode). In other mode the memory content should be retained, but it cannot be operated. SLEEP control for Backup RAM is not supported and cannot be used.
Internal Memories VRAM	ECC region is shared with user region. Memory size available for user program become less when ECC is enabled. User can define ECC enabled area and ECC disabled area. Single error correction, double error detection (SECDED) ECC support per 32-bit word.

Feature	Description
Embedded Program/Work Flash Memory	Embedded Program flash can be accessed with 0-wait-cycle if CPU frequency is 80 MHz or less. 0-wait-cycle: 80 MHz or less. 1-wait-cycle: 160 MHz or less. 2-wait-cycle: more than 160 MHz. The maximum frequency should be referred in datasheet. Erase suspend is supported. Reading and writing to the other sector are possible when Flash Erase is suspended. Serial Flash programing and Parallel Flash programing are supported. Margin mode is not supported.
Security	Chip erase function is available for flash memory. The function of "MK_CEER" is not supported. (MK_CEER = not selectable) For details, see the platform manual and chapter "Security"
Internal Power Domain	PD1: Always ON PD2: Cortex R5F platform/ GDC/ additional peripherals PD4: Backup RAM in Always On domain PD6: Peripherals in Always On domain * The chapter of the block diagram explains in detail.
Power Supply	External 5 V, 3 V, 1.2 V is required. Built in LDO provides internal 1.2 V for Always On region (PD1). External 1.2-V power supply control pin is supported. External 3.3-V power supply should be controlled by GPIO. There are constraints of power on/off sequence.
Low-voltage Detection	LVD for external voltage is supported. LVD for internal voltage is supported. See the specification of the detected level on the datasheet.
Low-voltage Detection for RAM Retention (RVD)	RVD for RAM retention is effective during the standby mode only. That is, it is only for the Backup RAM of 16 KB that the function is available.
Resource inter-connect	The output signal of some resources can be inputted to the other resource.
I/O Ports	5-V GPIO 3-V GPIO Multi input level and multi output drivability Pull-up, pull-down function is available. Resource input and output is multiplexed. +B input is allowed many pins of 3.3 V, 5 V, and 3.3 V/5 V I/O domain.
A/D Converter	12-bit resolution, 1 unit 50 channels of analog input for TEQFP256 and TEQPF216 46 channels of analog input for TEQFP208 24 channels of them are shared with the SMC for TEQFP256/216/208 External trigger and timer trigger are available. The description of the A/D converter function should be referred in the S6J3200 hardware manual. Though the chapter of I/O port in TRAVEO™ T1G PF V3 hardware manual describes another A/D converter function, do not refer it.
CRC	See the platform manual in detail.
Programmable CRC	DMA support
Sound Generator	Produces sound/melody with varying frequency and amplitude for convenient duration Square wave sound output Automatic linear amplitude increment or decrement Interrupt request generated when specified sound length has ended

Feature	Description
Sound Waveform Generator	Sine waveform, saw-tooth waveform and Square waveform are generated with easy configuration of the parameters which specified sound sources. Fade-in and Fade-out control for reverberation.
Sound Mixer	The input channels of 0-4 are reserved for waveform generator. Mixing different sampling frequency sounds. Mixing Internal sounds and External I2S input sounds. Saturating addition function for keeping sound quality. Cut a specific frequency data by digital filter. LPF is support by FIR filter. Fade-in and Fade-out control.
PCM-PWM	Conversion of PCM audio streaming to Pulse Width Modulated signals. Supports 2 output channels for stereo and mono data Up to 16-bit output sample resolution Support for half and full H-bridges
Audio DAC	The sound source of the fixed 48 kHz sampling frequency can be outputted. 1unit, L/R channels support. BTL connection is available.
I2S	2 ch. – I2S0 can output sound sources which are processed by Sound System. – I2S1 can input sound sources which are processed by Sound System. See the "Sound System Configuration" of S6J3200 hardware manual in detail.
Base Timer	See the platform manual in detail. A unit consists of a pair of 16-bit base timers. 12 units, that is, 24 channels of base timers are available.
Reload Timer	See the platform manual in detail.
I/O Timer	See the platform manual in detail.
Quad Position & Revolution Counter (Up/Down Counter)	See the platform manual in detail.
Multi-functional Serial (MFS)	See the platform manual in detail. 5 ports of MFS only support I^2C. Note – Not all pins support I2C. Only pins which have the I2C I/O characteristics support it. See the datasheet in detail. The I^2C is not designed to be hot swappable. The availability of chip select function can be seen at Function Digit Table. Chip Select Input is not supported. CTS/RTS is not mounted (hardware flow control is not supported for this series.) WUCR function is not supported for this product.
CAN-FD	Flexible data rate is supported. 16 KB/ch of message RAM is available. The clock output from CAN pre-scaler is supplied to every CAN. ECC error generation function of the message RAM is not supported for this device. Therefore, CAN FD ECC Error Insertion Control Register (FDFECR) is not writeable. See the platform manual in detail
Real Time Clock (RTC) with Auto-calibration	See the platform manual in detail.

Feature	Description
DDR High Speed SPI	ch.0: HSSPI as a MCU peripheral ch.1: HSSPI on graphic subsystem See the platform manual in detail
HyperBus I/F	ch.0: HyperBus as a MCU peripheral ch.1: HyperBus on graphic subsystem ch.2: HyperBus on graphic subsystem The following register is not supported and cannot be used. – Controller Status Register (HYPERBUSIn_CSR) – Interrupt Enable Register (HYPERBUSIn_IEN) – Interrupt Status Register (HYPERBUSIn_ISR) – Write Protection Register (HYPERBUSIn_WPR) – Test Register (HYPERBUSIn_TEST) GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic Sub System. See the "HyperBus Interface Port Configuration" of S6J3200 hardware manual in detail.
Stepper Motor Control (SMC)	Each channel has four motor drivers with high output capability
External Interrupt Capture Unit (EICU)	See the platform manual in detail.
Ethernet AVB	10/100 Mbps MII-Interface Supports Audio-Video Bridging (AVB) ETHERNETn_revision_reg : 0x30070106 (Initial value) for after revision B ETHERNETn_designcfg_debug6: 0x0302000E (Initial value) See 0 in details.
MediaLB	MOST25 (512FS) 3 wires Maximum 15 ch is available.
LCD Controller	TEQFP256: 4 com x 32 seg TEQFP216: 4 com x 32 seg TEQFP208: 4 com x 30 seg LCDC pins are initialized with Reset. (Stop LCDC alternating current output). Duty and Static of segment output is supported. (SEG23/ST0, SEG24/ST1, SEG25/ST2, SEG26/ST3, SEG27/ST4, SEG28/ST5, SEG29/ST6, SEG30/ST7, SEG31/ST8)
SHE	See the platform manual in detail.
Source Clock Timer	See the platform manual in detail.
Graphics Subsystem	Variable setting about GDC clock. (Asynchronous with CPU clock) Two drawing engines for “2D drawing” and “3D drawing”. Parallel processing support. CPU can direct access to VRAM. Programmable panel timing controller with RGB888 and RSDS support.
FPD-Link Converter	LFCTRL and FRANGE bit of CTRL1. See chapter FPD-Link Converter about function. -These register bit are supported for revision M, P. -These register bit are not supported for revision F and J. These bit are reserved bit(Access type is R0,W0. Initial value is 0).

Feature	Description
Power Supply Control (PSC)	PSC (PSC_1) output is used for external 1.2-V power supply module control and automatically switched with the following condition. "High": Request to supply VCC12 - "Power ON Reset" is released - CPU wakes up from PSS shutdown mode "Low": Request to stop supplying VCC12 - CPU transfers from RUN mode to PSS shutdown mode. For timing chart of output signals include PSC in detail, see the "S6J3200 hardware manual" and chapter "State Transition"

3.2.1 Ethernet

The following functions are not supported.

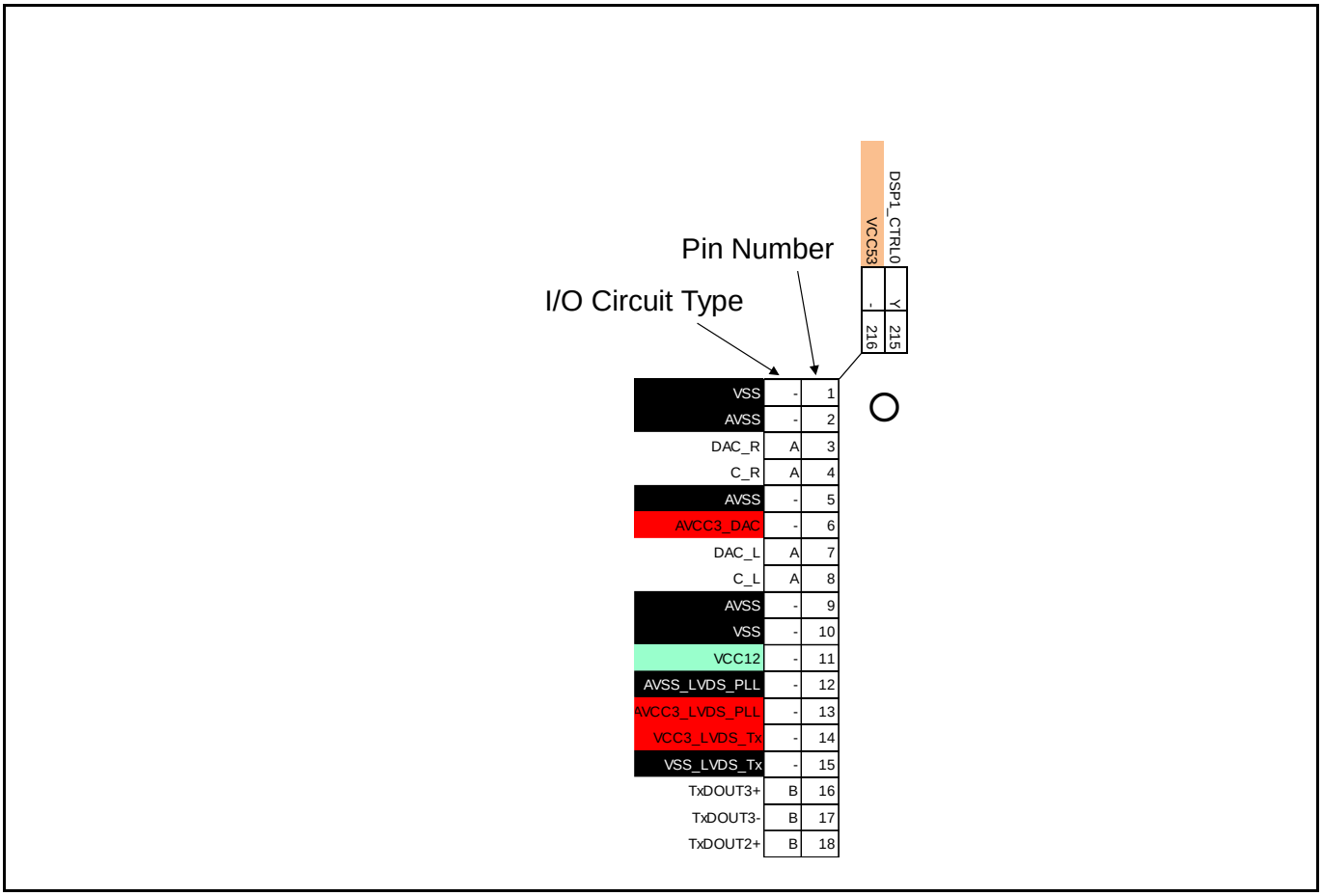
Functions	Remark
External FIFO Interface	
Additional Low Latency TX FIFO Interface for DMA configurations	
MAC Transmit Block - half-duplex - collision - back_pressure	
MAC Filtering Block - external address match - Wakeup On Lan	
Energy Efficient Ethernet support	
LPI Operation in Cadence IP	
PHY Interface - GMII - SGMII - TBI	
10/100/1000 Operation - 1000 M	
SGMII Operation	
Jumbo Frames	
Physical Control Sub-Layer	

4. Package and Pin Assignment

4.1 Pin Assignment

The characters next to the pin number in the pin assignment drawing specify the I/O circuit type.

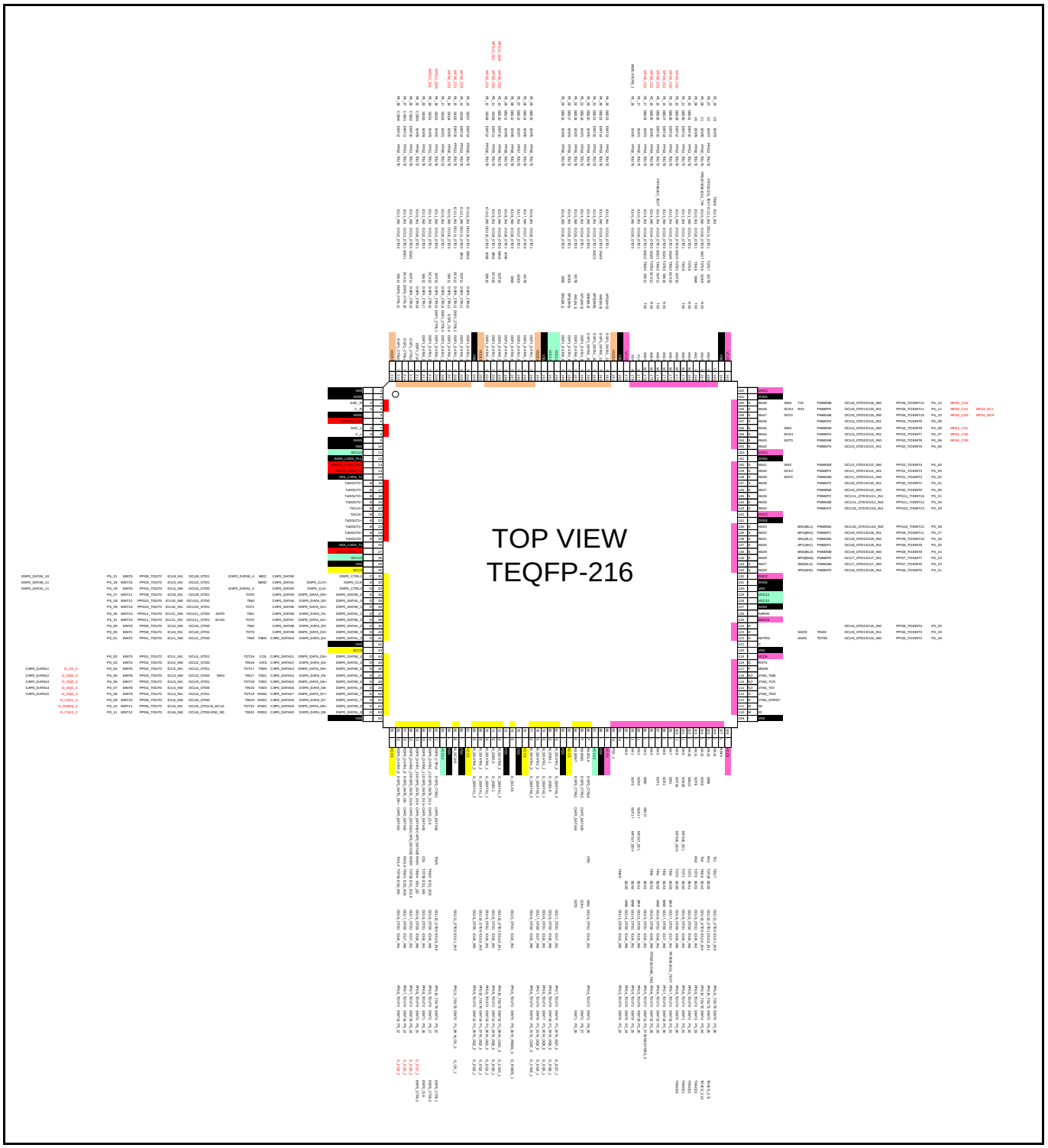
Figure 4-1: Pin Number and I/O Circuit Type



Function Digit	TEQFP-216	TEQFP-208	TEQFP-256
S6J328, S6J329, S6J32M	Figure 4-2	Figure 4-9	Figure 4-17
S6J327	Figure 4-3	Figure 4-10	-
S6J326, S6J32L	Figure 4-4	Figure 4-11	-
S6J325, S6J32N	Figure 4-5	Figure 4-12	-
S6J324	Figure 4-6	Figure 4-13	-
S6J323	Figure 4-7	Figure 4-14	-
S6J32K	Figure 4-8	Figure 4-15	-
B	-	Figure 4-16	-

4.1.1 TEQFP-216 Pin Assignment

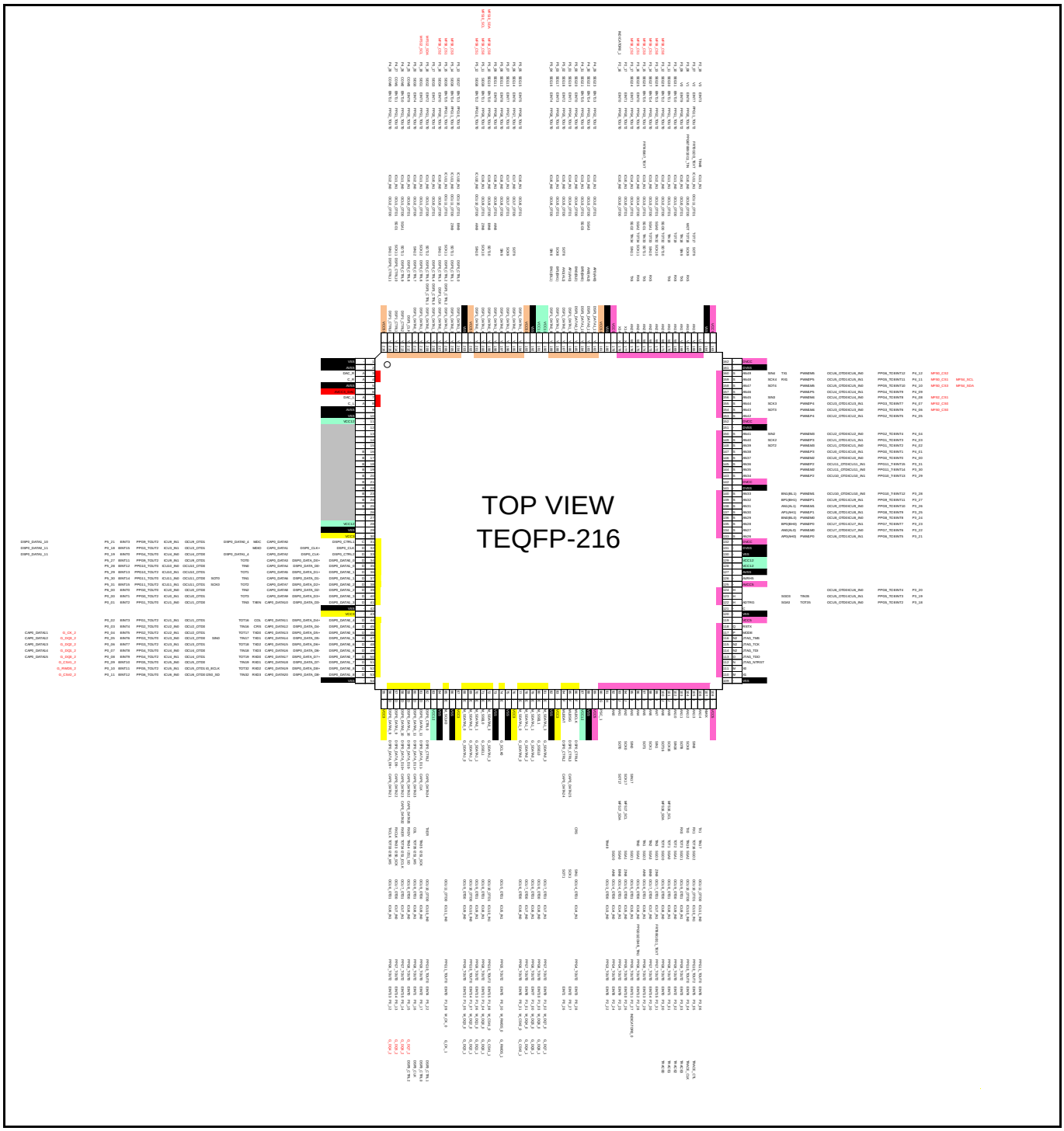
Figure 4-2: TEQFP-216 (S6J328CLxx, S6J329CLxx, S6J32MELxx)



Note:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*

Figure 4-3: TEQFP-216 (S6J327CLxx)



Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
12 to 27	Set to ground

Figure 4-4: TEQFP-216 (S6J326CLxx, S6J32LELxx)

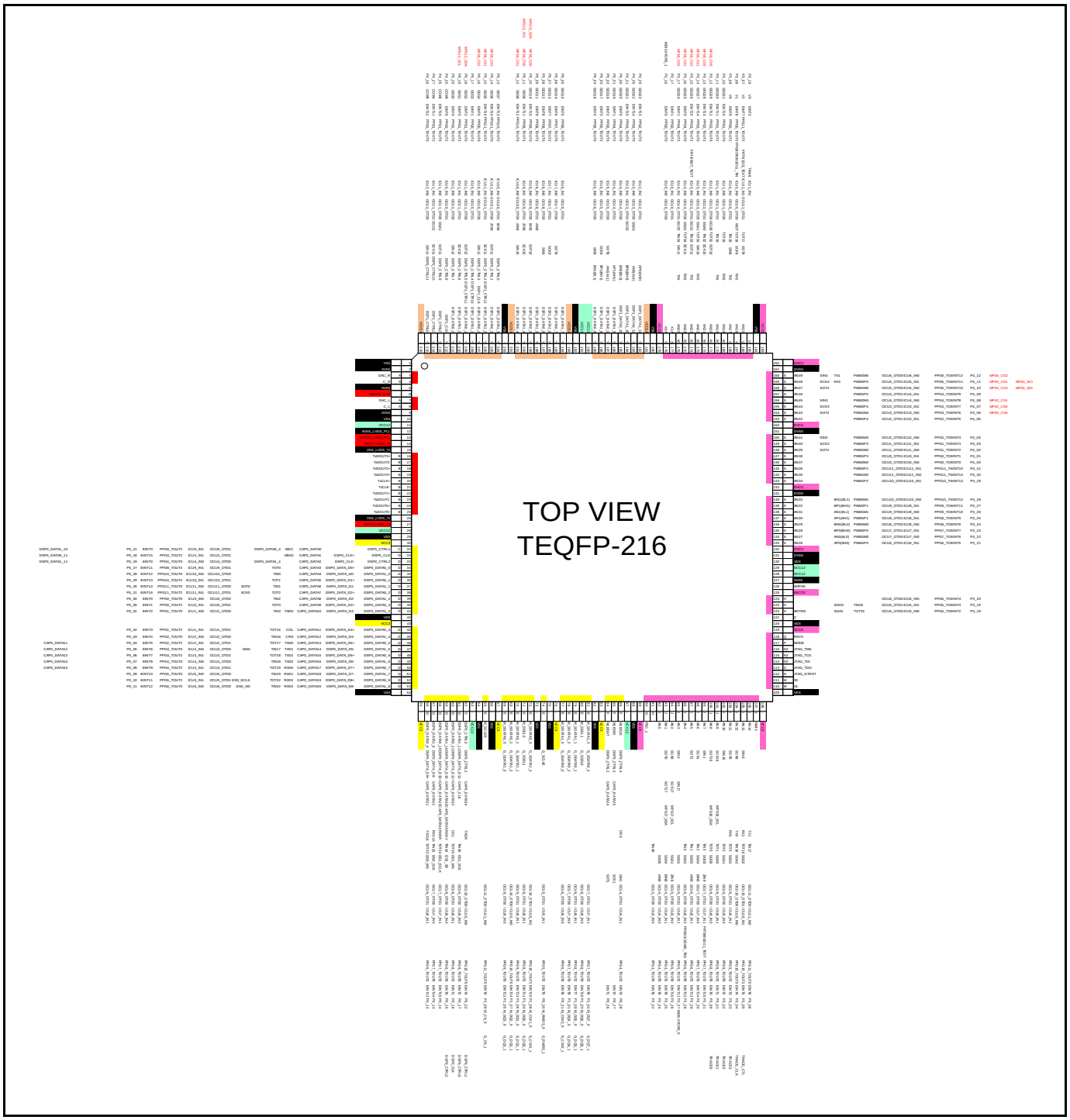
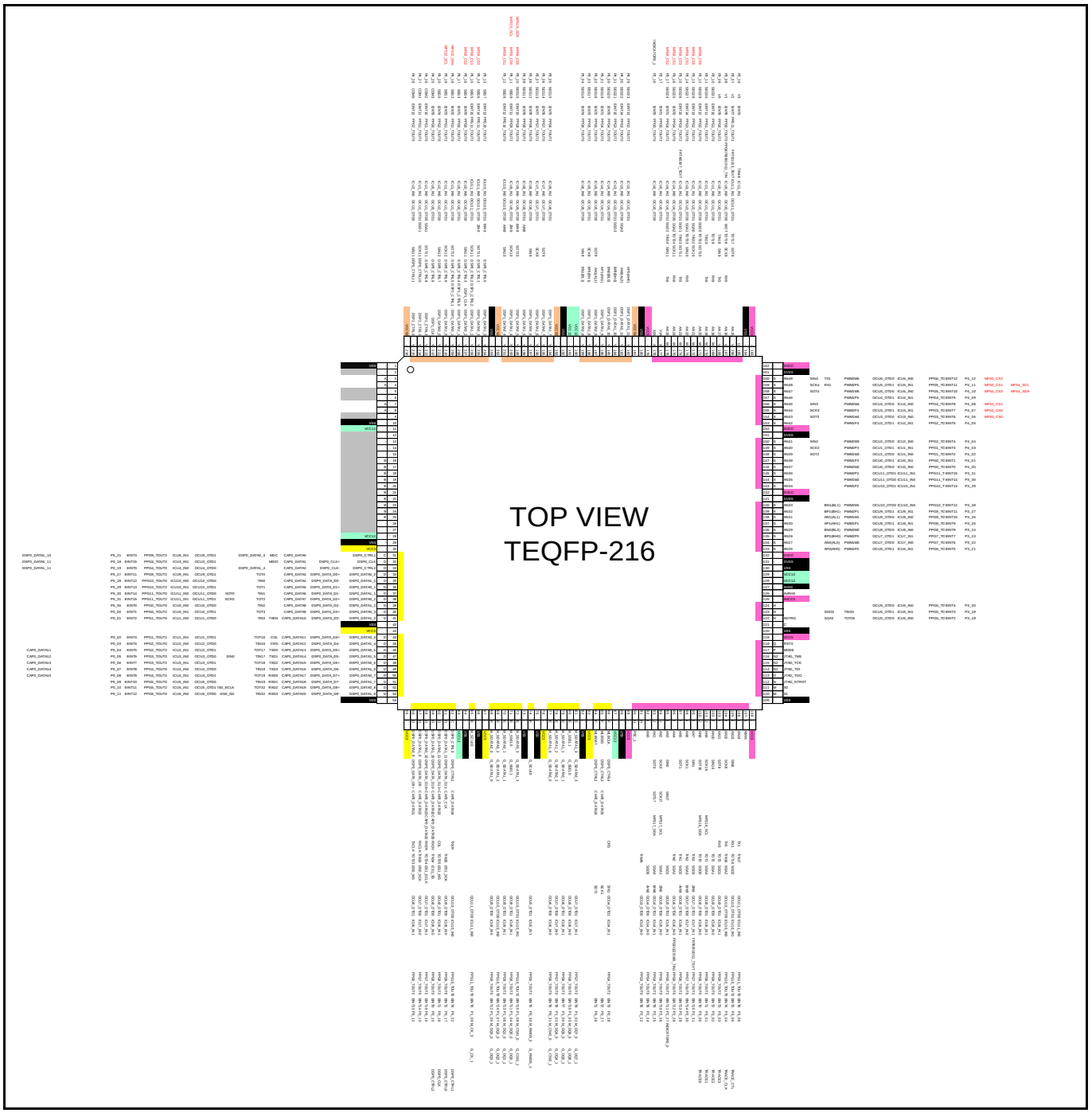


Figure 4-5: TEQFP-216 (S6J325CLxx, S6J32NELxx)

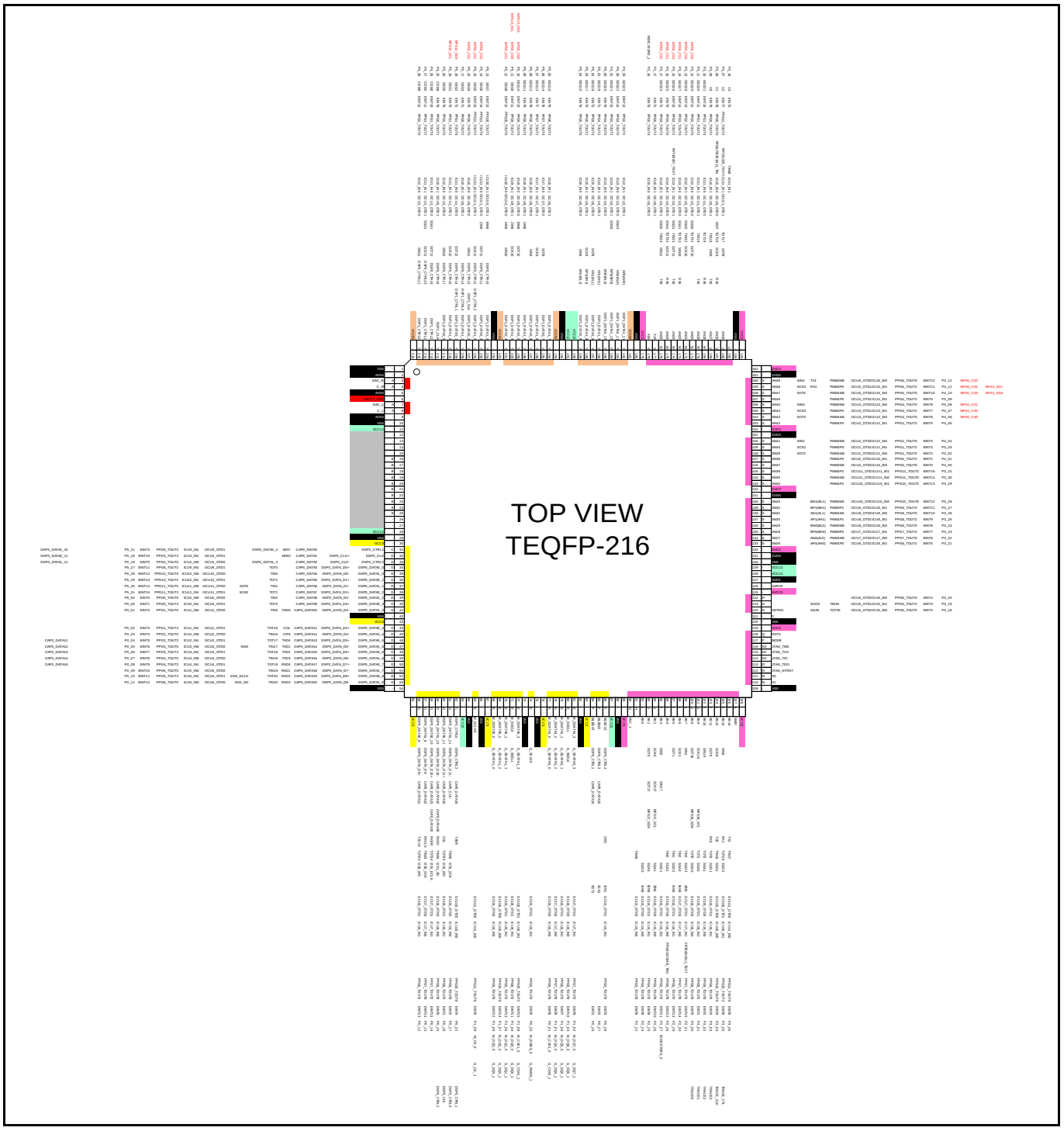


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9, and 12 to 27	Set to ground
3, 4, 7, 8	Open

Figure 4-6: TEQFP-216 (S6J324CLxx)

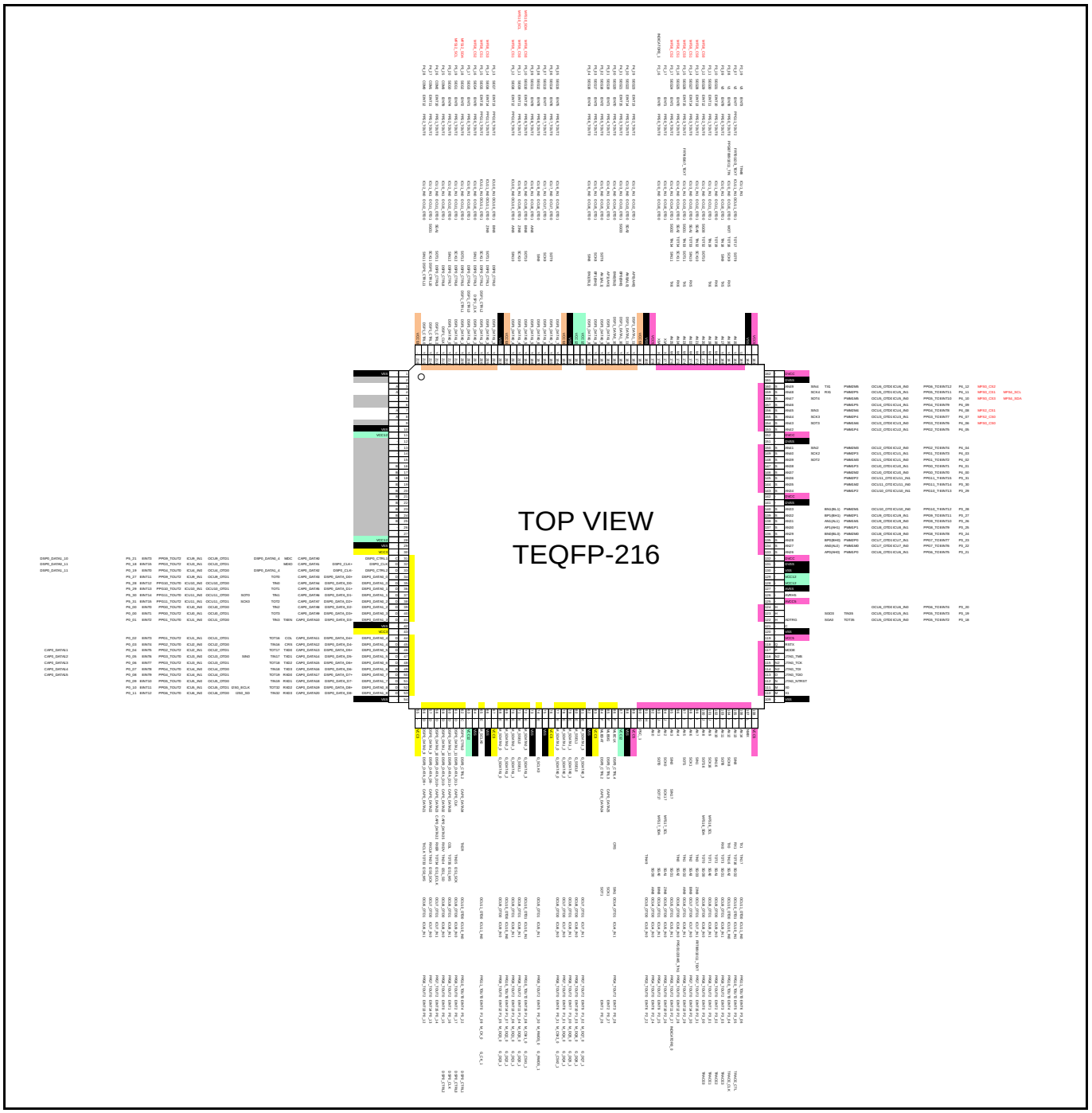


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
12 to 27	Set to ground

Figure 4-7: TEQFP-216 (S6J323CLxx)

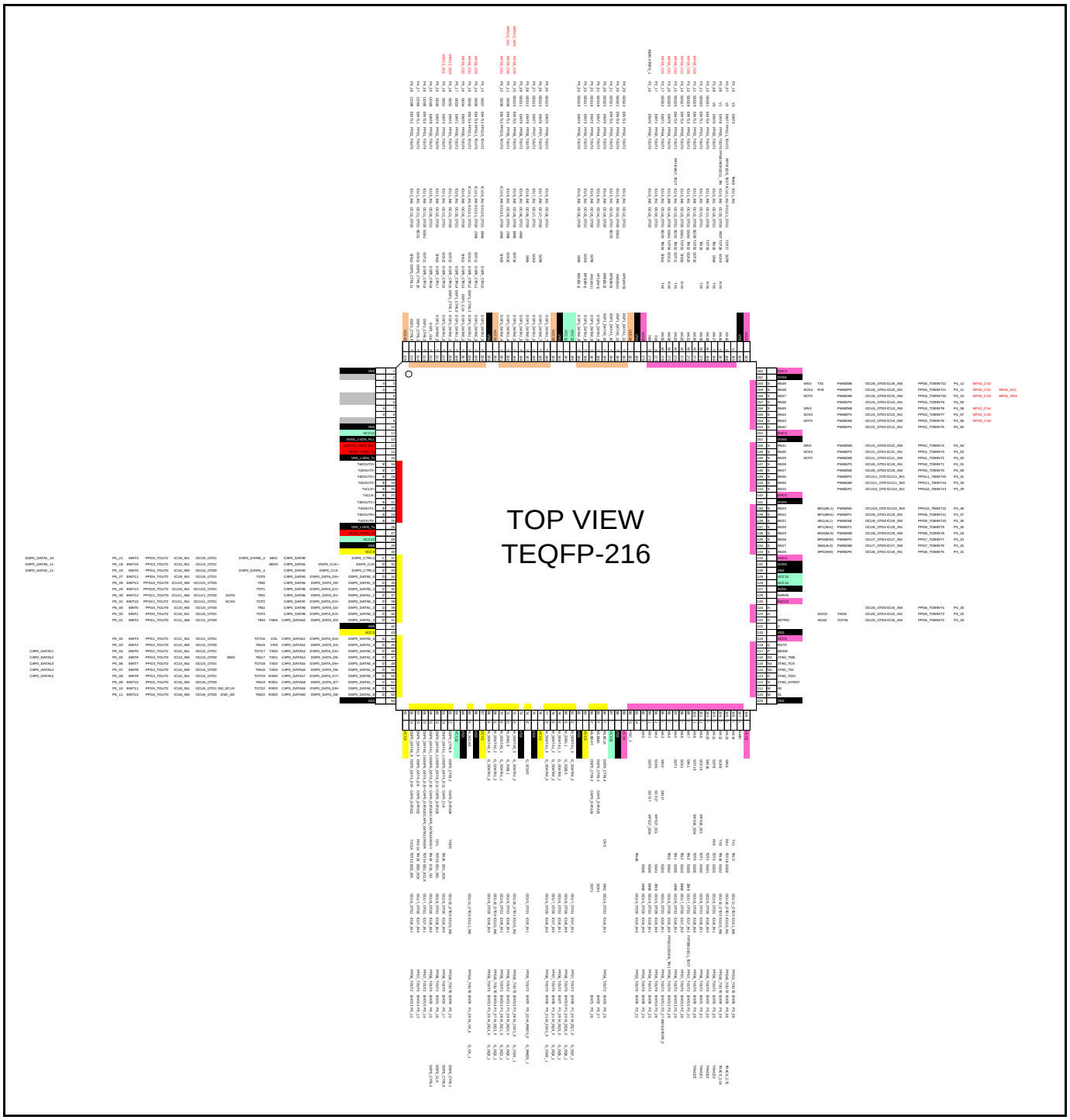


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9, and 12 to 27	Set to ground
3, 4, 7, 8	Open

Figure 4-8: TEQFP-216 (S6J32KELxx)



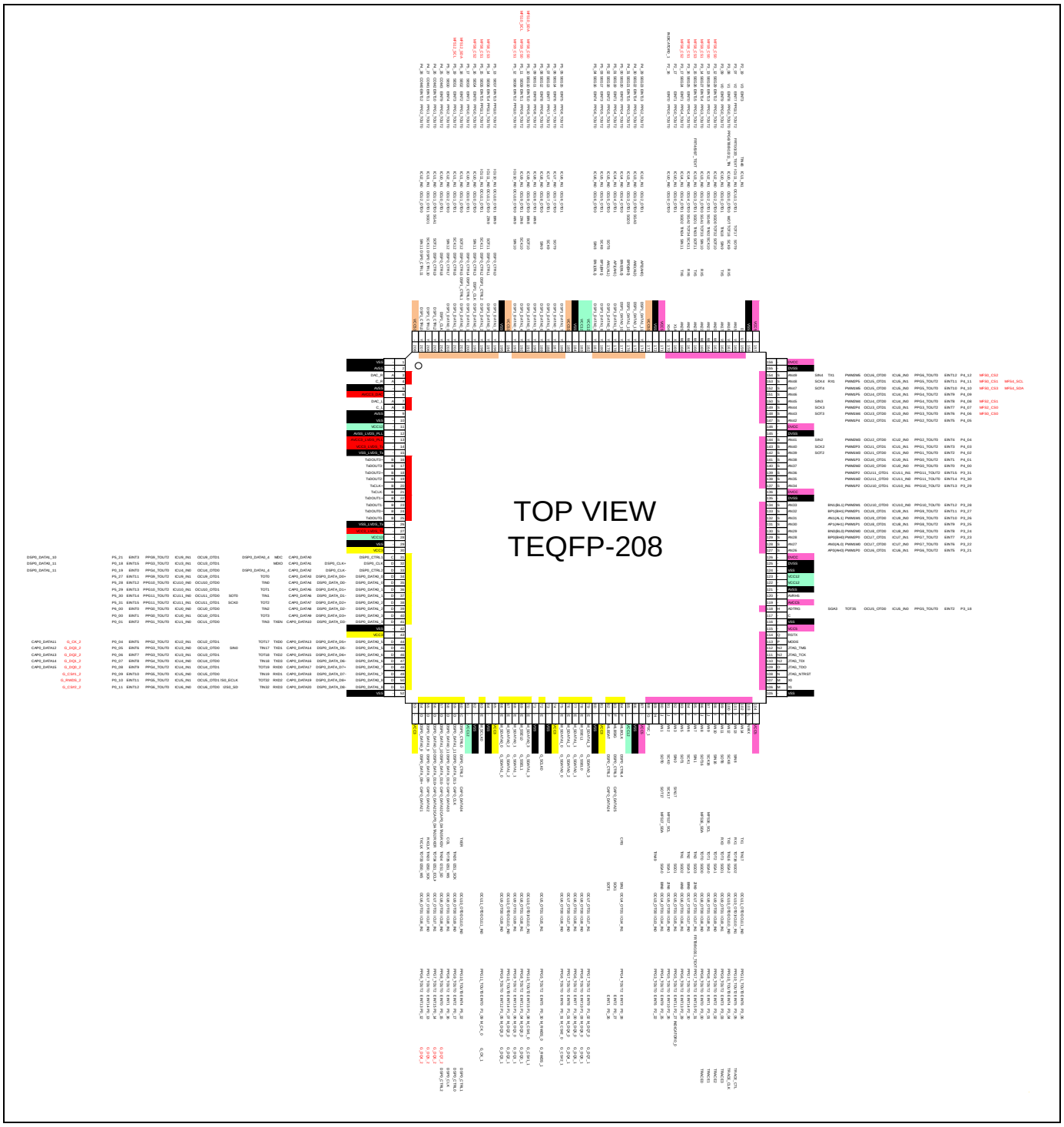
Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9	Set to ground
3, 4, 7, 8	Open

4.1.2 TEQPF-208 Pin Assignment

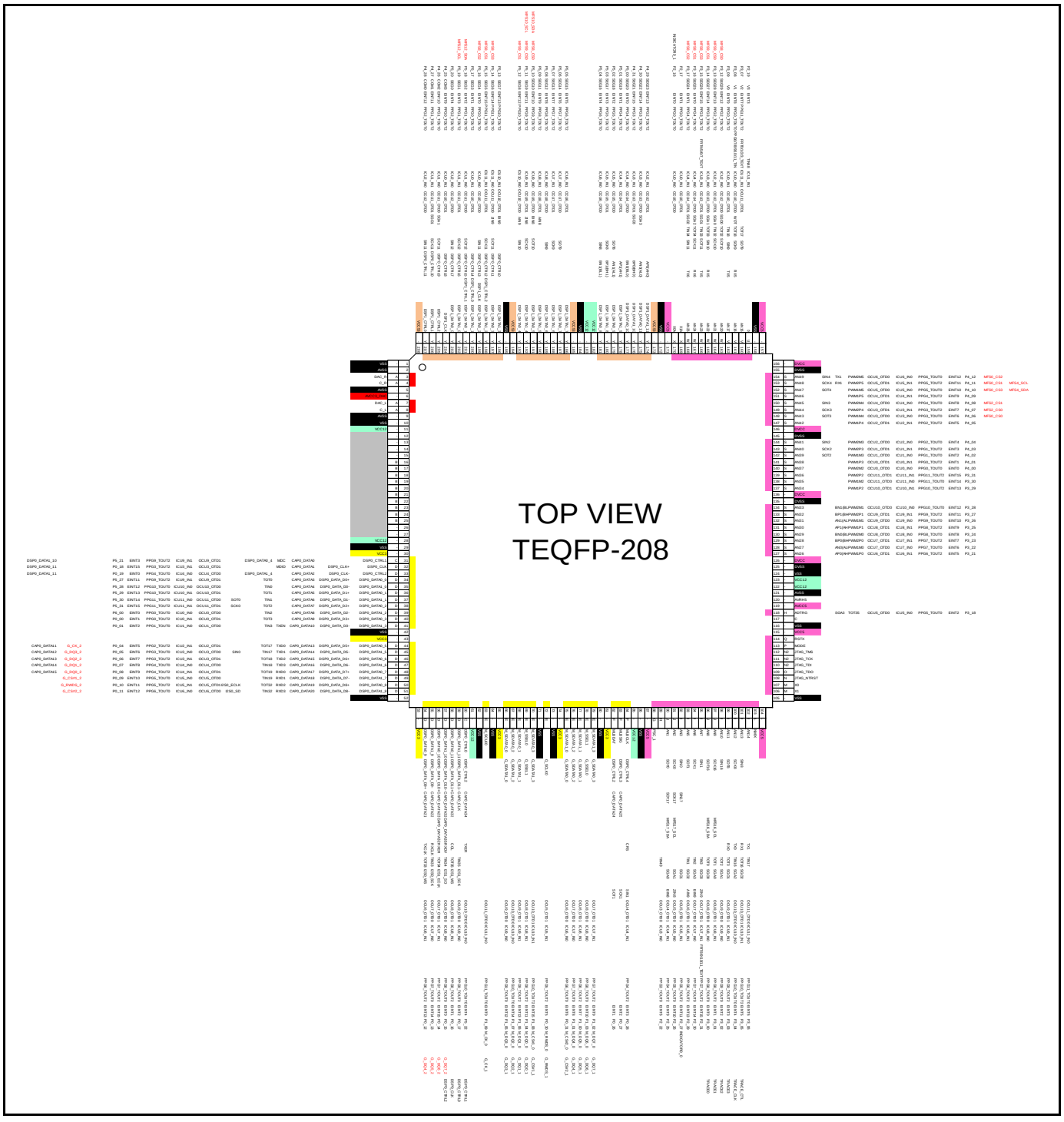
Figure 4-9: TEQFP-208 (S6J328CKxx, S6J329CKxx, S6J32MEKxx)



Note:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*

Figure 4-10: TEQFP-208 (S6J327CKxx)

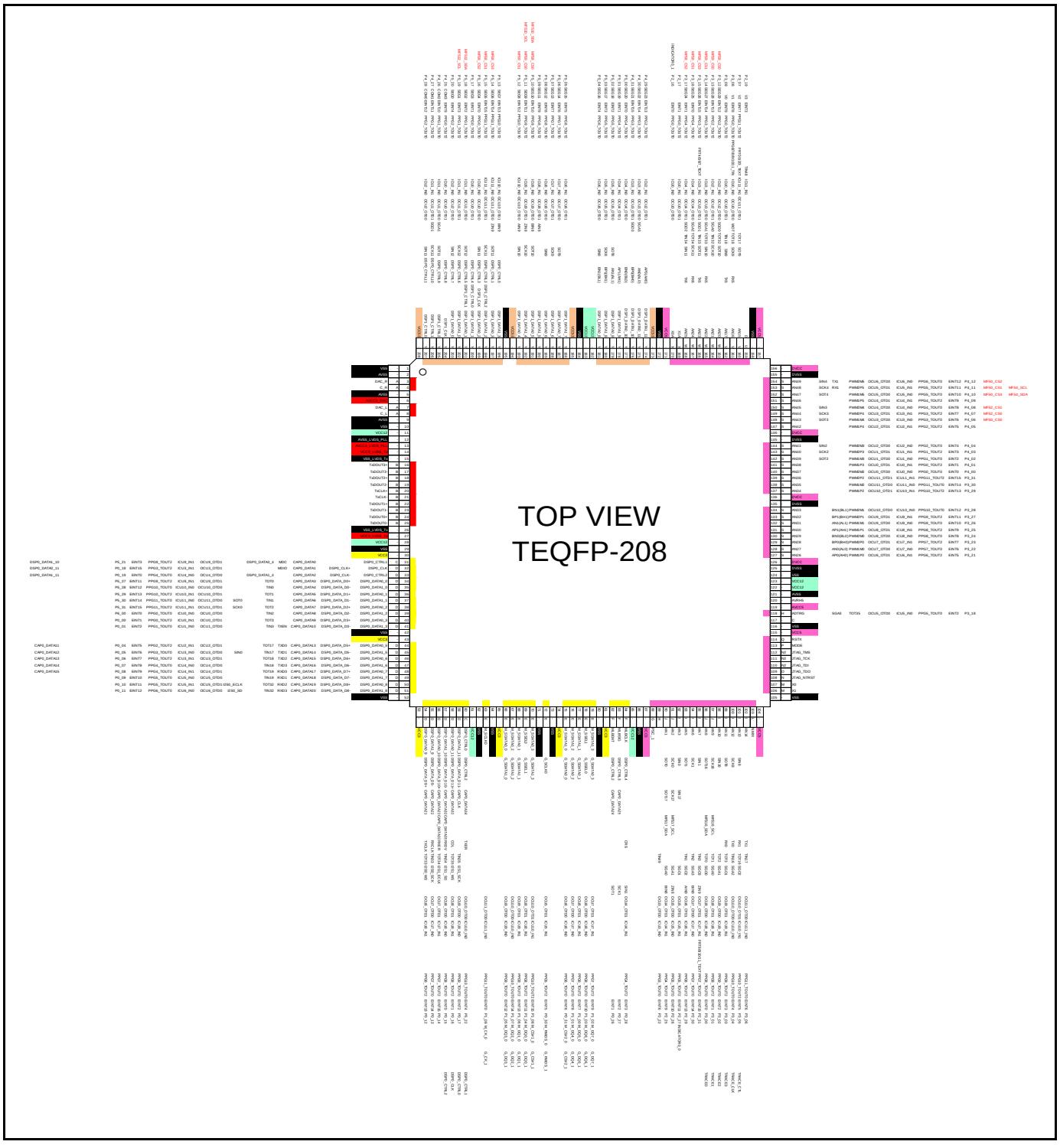


Notes:

- *The pins highlighted in "red" character are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
12 to 27	Set to ground

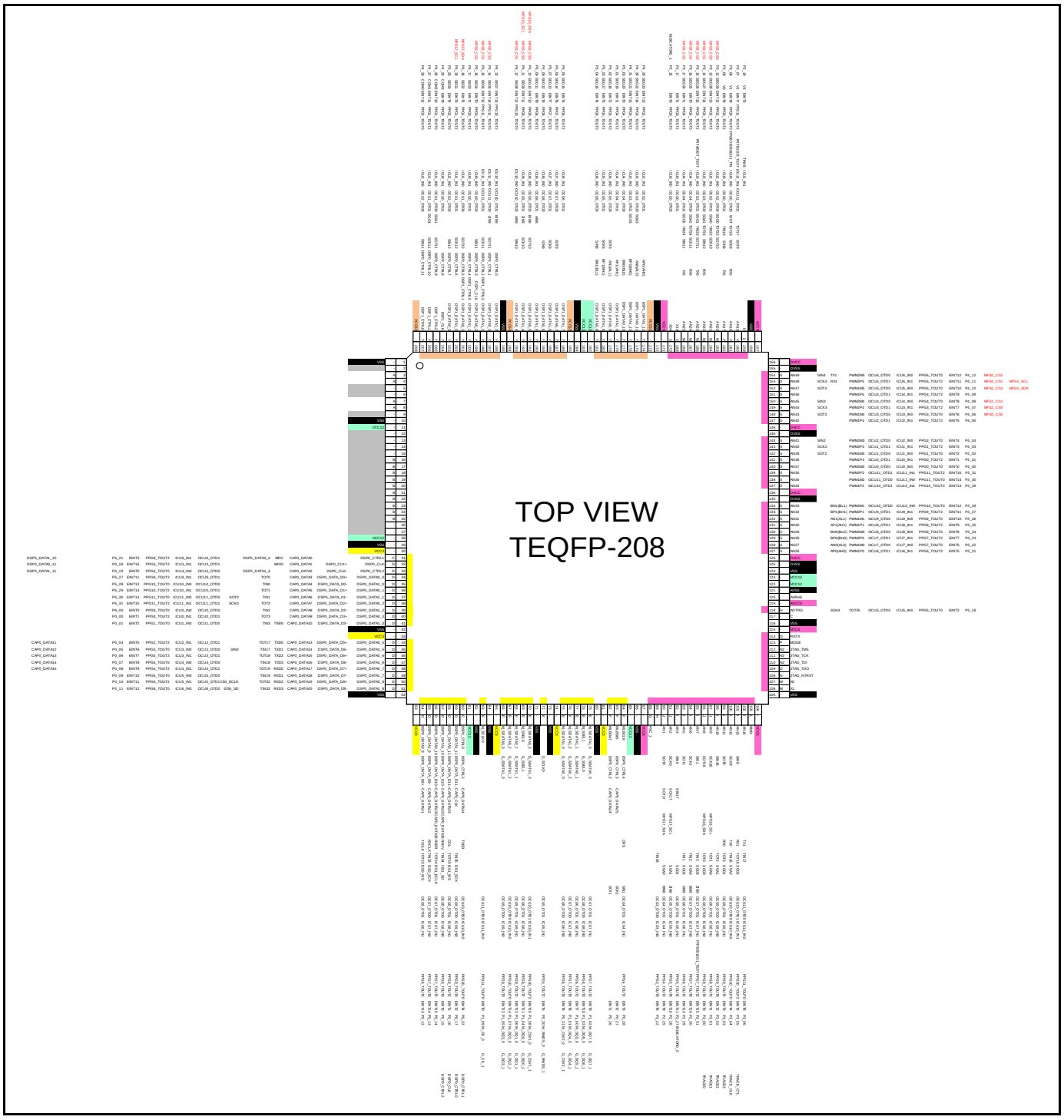
Figure 4-11: TEQFP-208 (S6J326CKxx, S6J32LEKxx)



Note:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*

Figure 4-12: TEQFP-208 (S6J325CKxx, S6J32NEKxx)

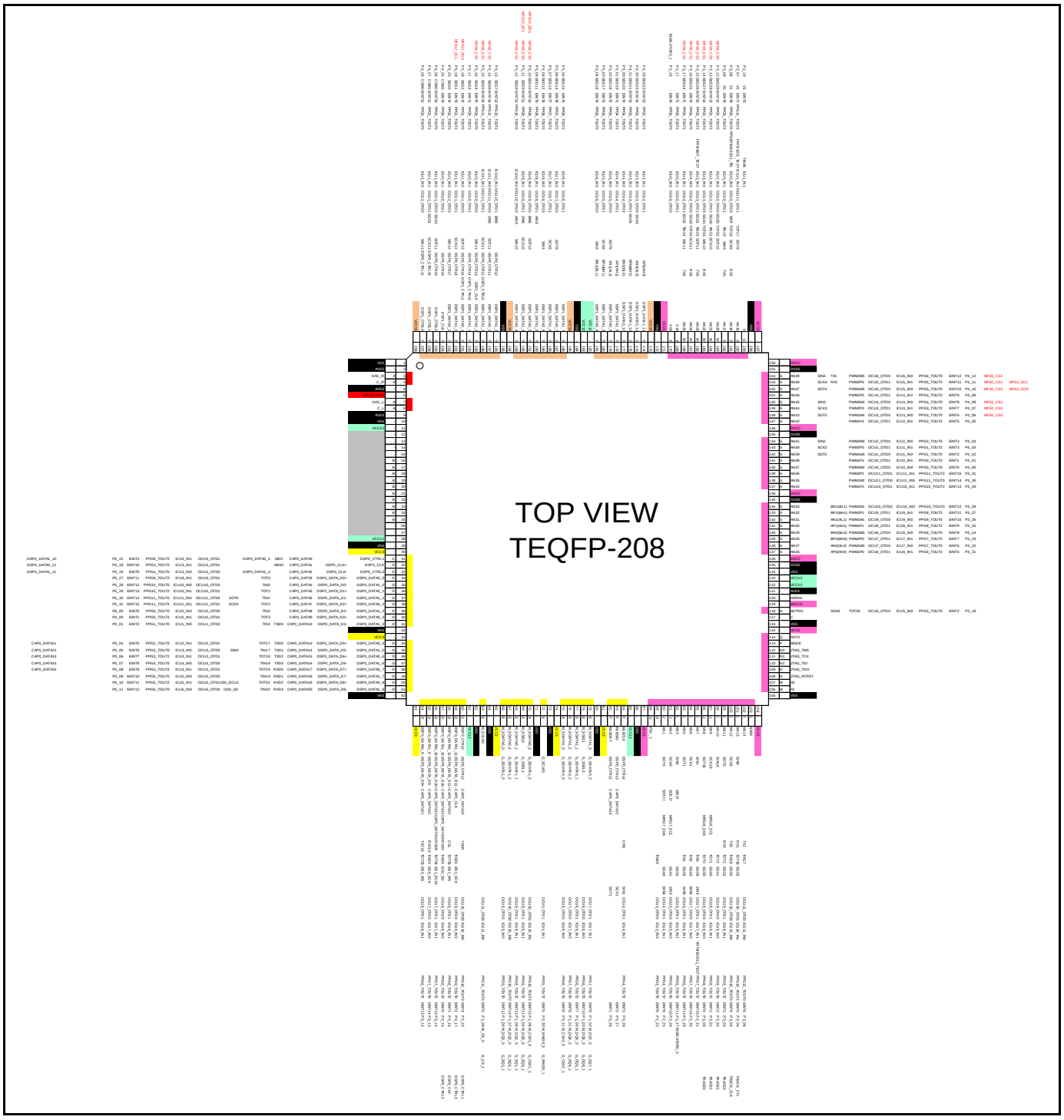


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9, and 12 to 27	Set to ground
3, 4, 7, 8	Open

Figure 4-13: TEQFP-208 (S6J324CKxx)

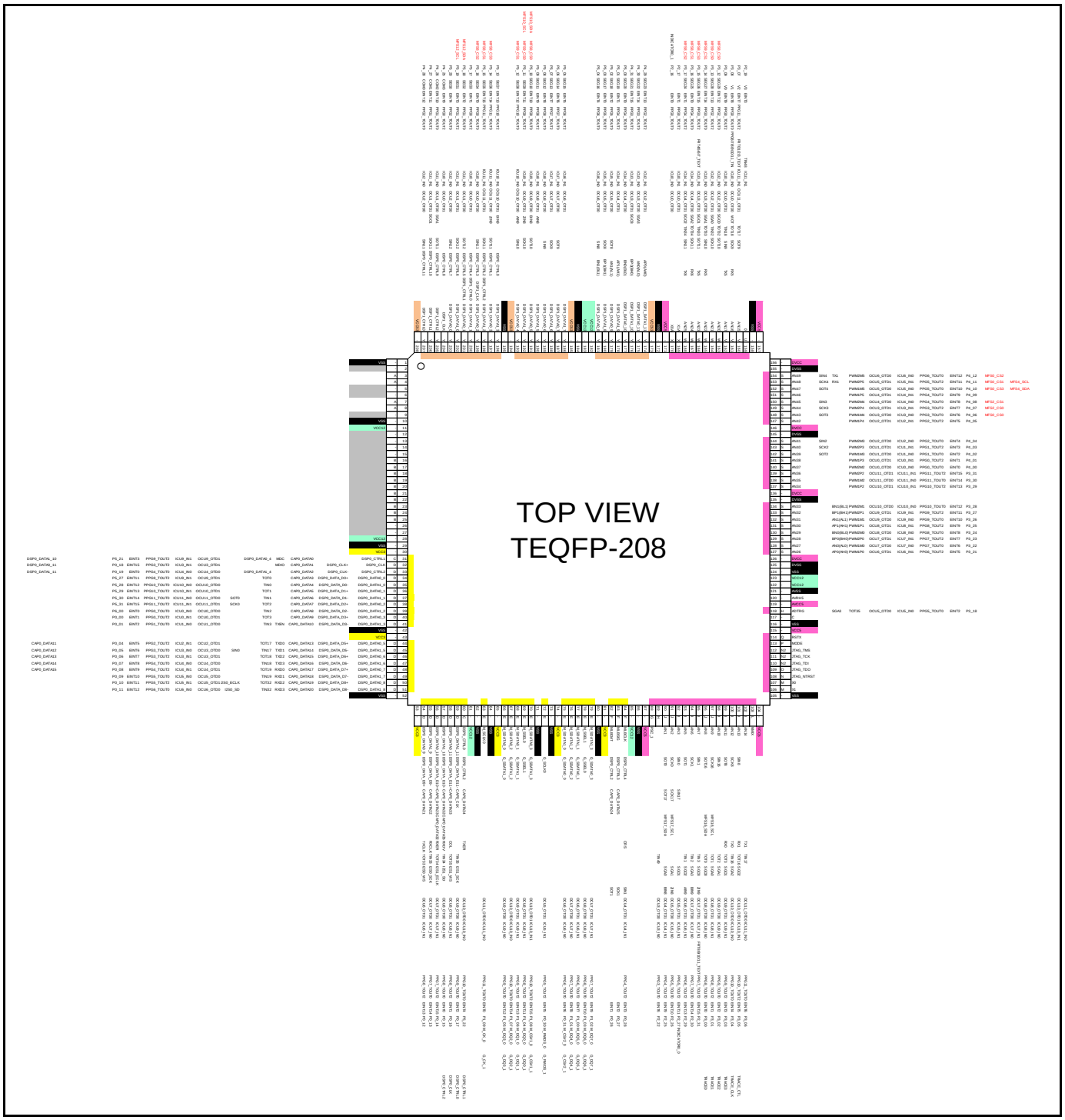


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
12 to 27	Set to ground

Figure 4-14: TEQFP-208 (S6J323CKxx)

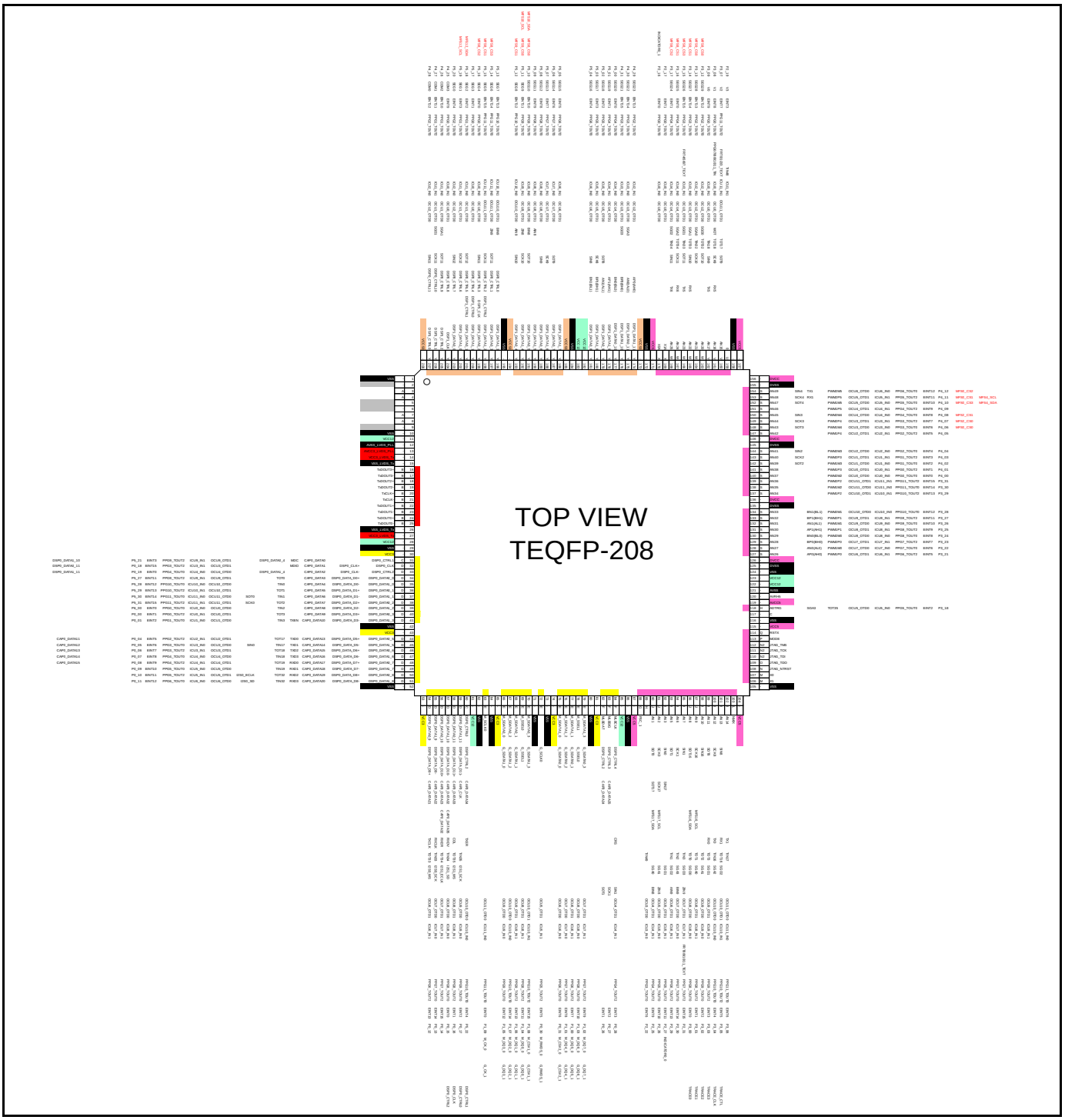


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

Package Pin Number	Condition on PCB
2, 5, 6, 9, and 12 to 27	Set to ground
3, 4, 7, 8	Open

Figure 4-15: TEQFP-208 (S6J32KEKxx)

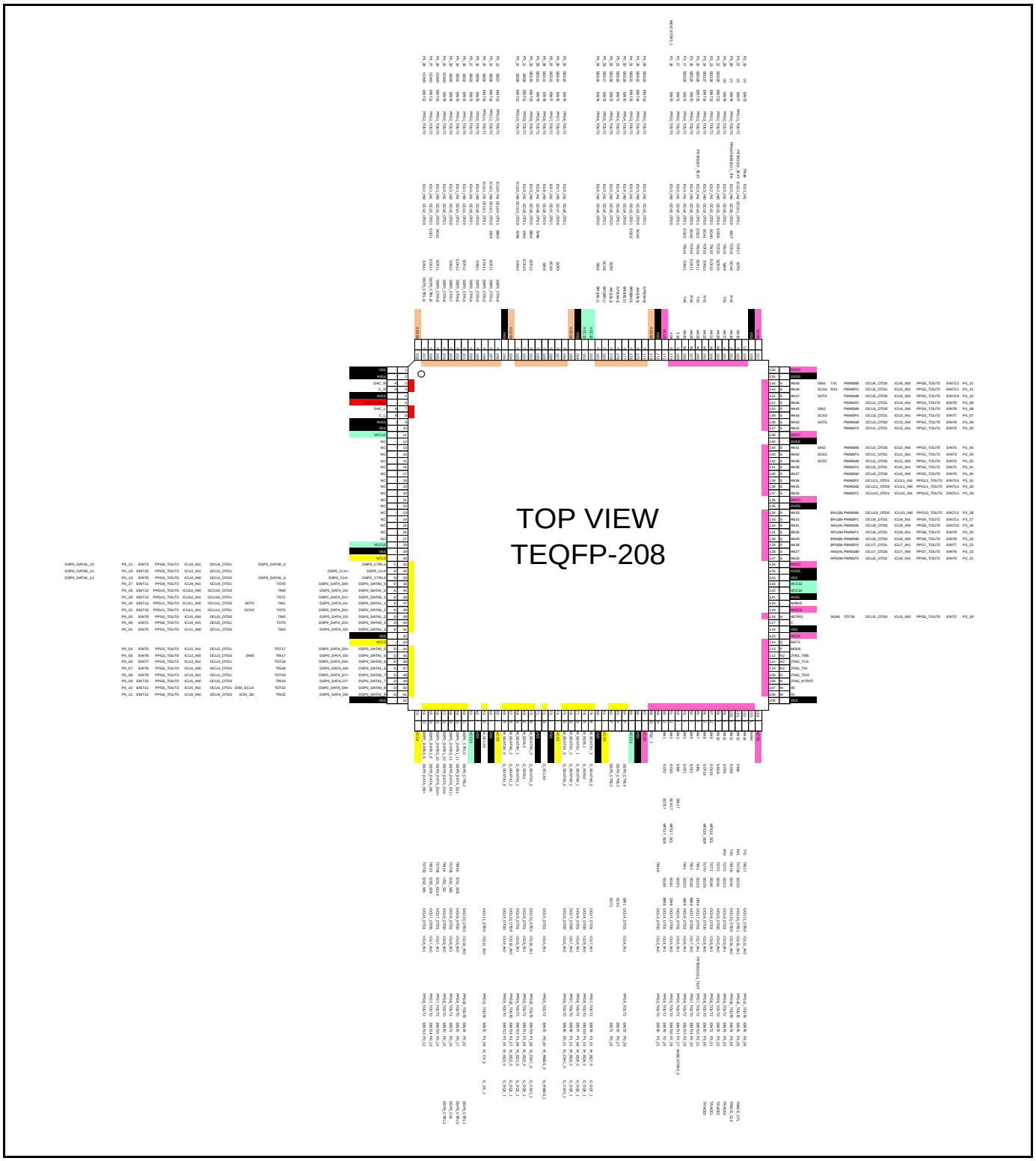


Notes:

- *The pins highlighted in "red" font are not supported for products with revision A and C.*
- *Any function at the following pins is not supported.*

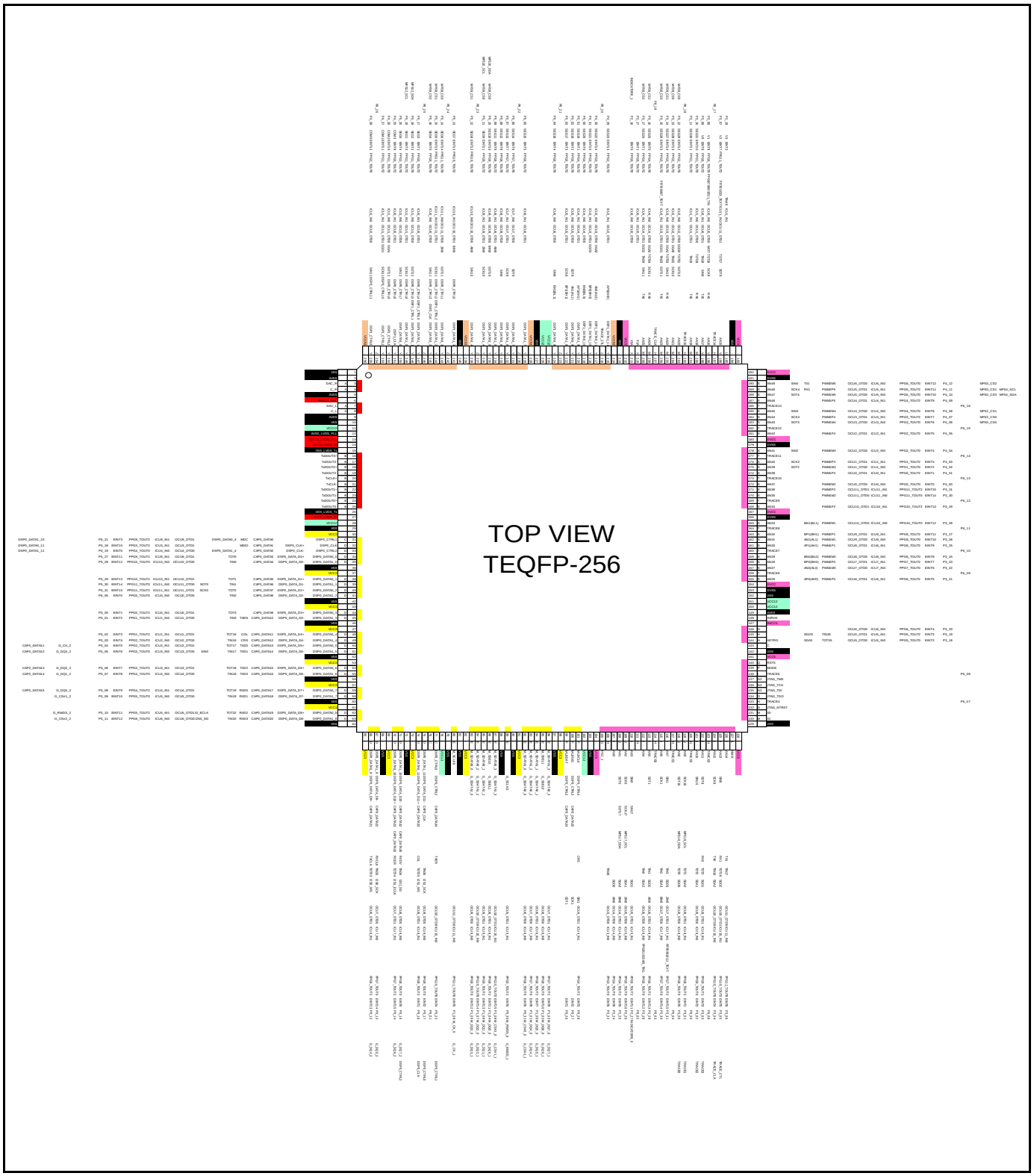
Package Pin Number	Condition on PCB
2, 5, 6, 9	Set to ground
3, 4, 7, 8	Open

Figure 4-16: TEQFP-208 (S6J32xAKxx)



4.1.3 TEQPF-256 Pin Assignment

Figure 4-17: TEQFP-256



4.2 Package Dimensions

Function Digit	TEQFP-216	TEQFP-208	TEQFO-256
3, 4, 5, 6, 7, 8, 9, K, L, M, N	Figure 4-18	Figure 4-19	Figure 4-21
B		Figure 4-20	-

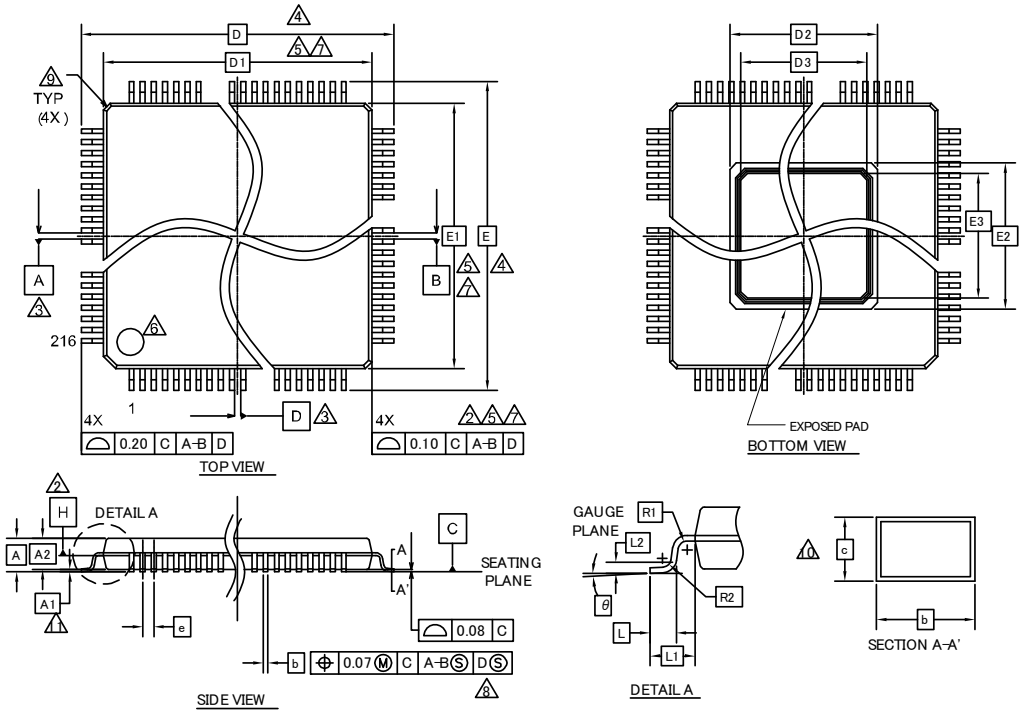
Note:

− *Same size is specified for MIN, NOM, MAX, then it should be regarded as maximum size.*

4.2.1 TEQFP216

Figure 4-18 LEQ216

Package Type	Package Code
TEQFP216	LEQ216



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A 1	0.05	——	0.15
A 2	1.35	1.40	1.45
D		26.00 BSC	
D 1		24.00 BSC	
D 2		9.90 REF	
D 3		8.70 REF	
E		26.00 BSC	
E 1		24.00 BSC	
E 2		9.90 REF	
E 3		8.70 REF	
R 1	0.08	——	——
R 2	0.08	——	0.20
θ	0°	4°	8°
c	0.09	——	0.20
b	0.13	0.18	0.23
L	0.45	0.60	0.75
L 1		1.00 REF	
L 2		0.25	
e		0.40 BSC	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

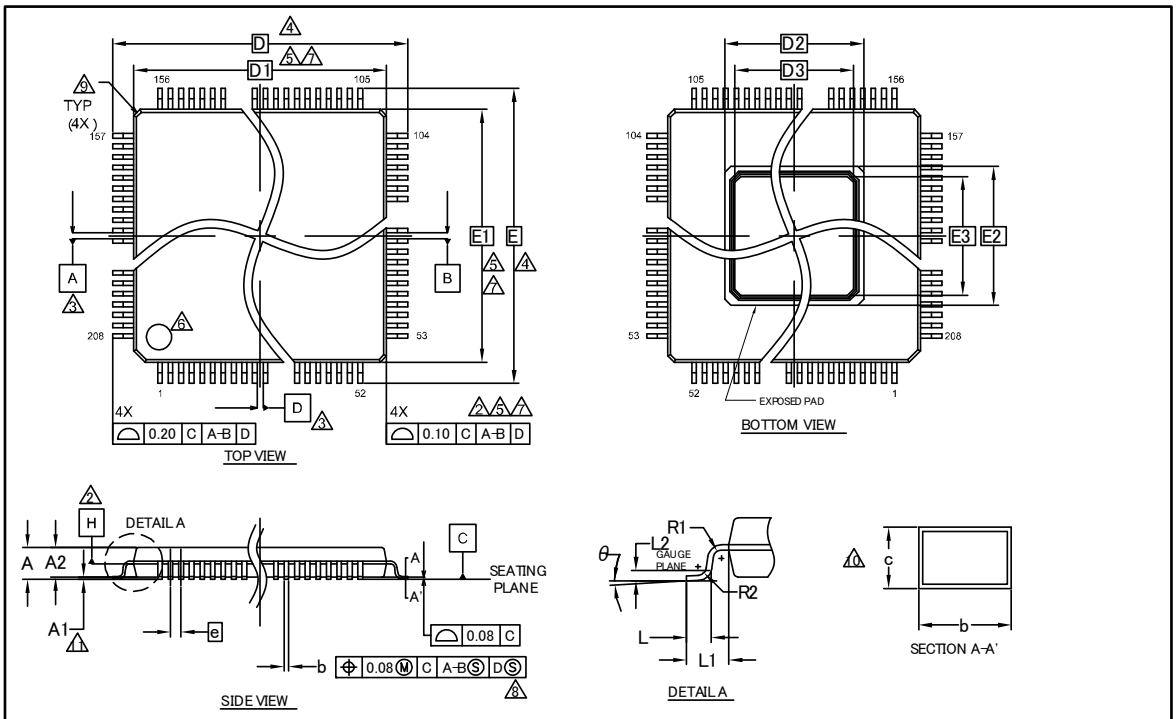
002-10860 *B

PACKAGE OUTLINE, 216 LEAD TEQFP
24.0X24.0X1.7 MM LEQ216 REV*B

4.2.2 TEQFP208

Figure 4-19: LET208

Package Type	Package Code
TEQFP208	LET208



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		30.00 BSC	
D1		28.00 BSC	
D2		9.90 REF	
D3		8.71 REF	
E		30.00 BSC	
E1		28.00 BSC	
E2		9.90 REF	
E3		8.71 REF	
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	4°	8°
c	0.12	—	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.50 BSC	

NOTES

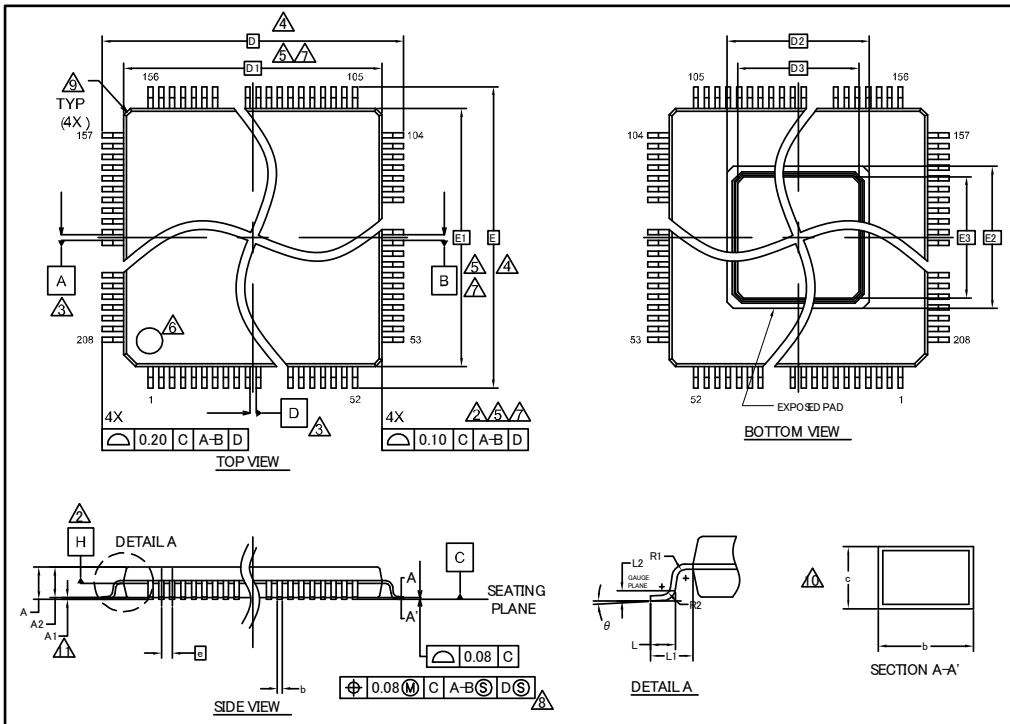
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13651 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LET208 REV*A

Figure 4-20:LER208

Package Type	Package Code
TEQFP208	LER208



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D		30.00 BSC	
D1		28.00 BSC	
D2		9.26 REF	
D3		8.06 REF	
E		30.00 BSC	
E1		28.00 BSC	
E2		9.26 REF	
E3		8.06 REF	
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.50 BSC	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

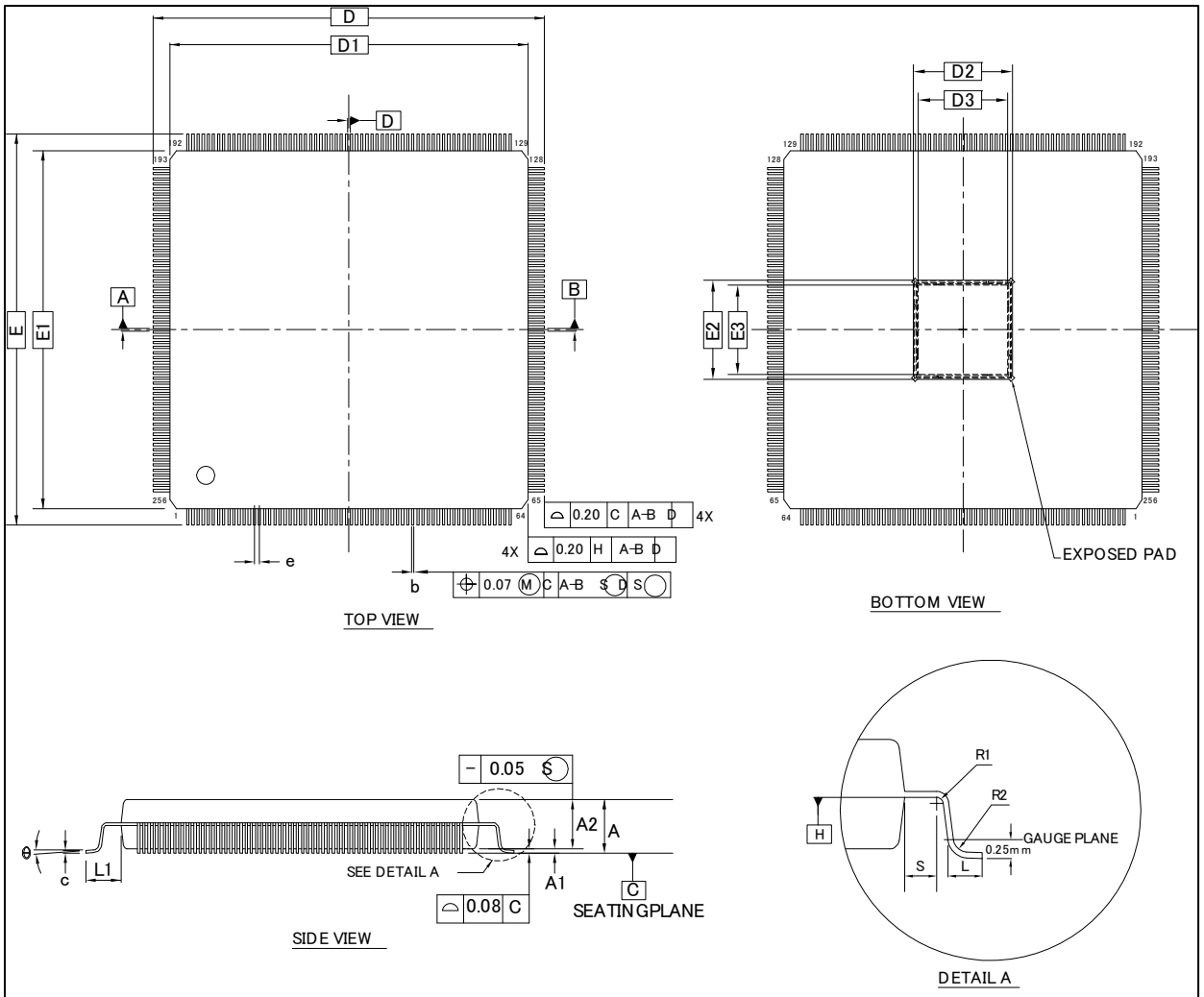
002-13654 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LER208 REV*A

4.2.3 TEQFP256

Figure 4-21:LEL256

Package Type	Package Code
TEQFP256	LEL256



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.70
A1	0.05	–	0.15
A2	1.35	1.40	1.45
D		30.00 BSC.	
D1		28.00 BSC.	
D2		9.90 REF.	
D3		8.70 REF.	
E		30.00 BSC.	
E1		28.00 BSC.	
E2		9.90 REF.	
E3		8.70 REF.	

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
b	0.13	0.18	0.23
e		0.40 BSC.	
R2	0.08	–	0.20
R1	0.08	–	–
θ	0°	3.5°	7°
c	0.09	–	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
S	0.20	–	–

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE.

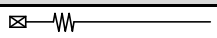
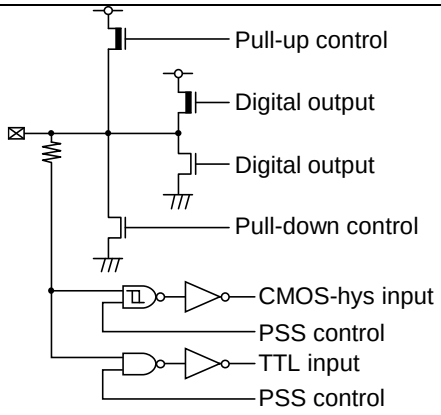
002-10752 *A

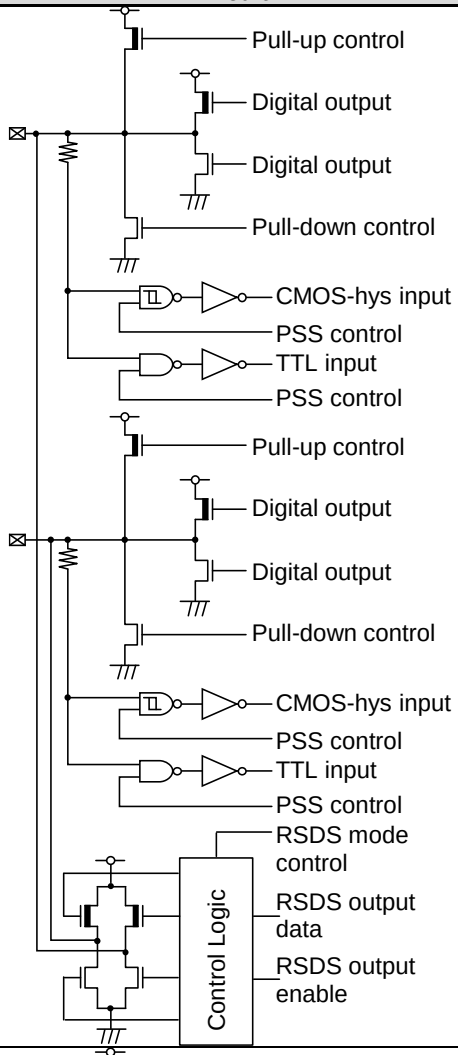
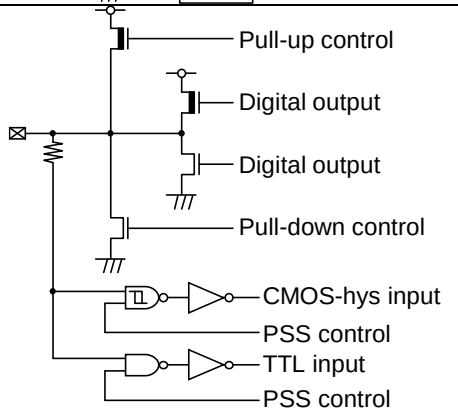
PACKAGE OUTLINE, 256 LEAD TEQFP
28.0X28.0X1.7 MM LEL256 REV*A

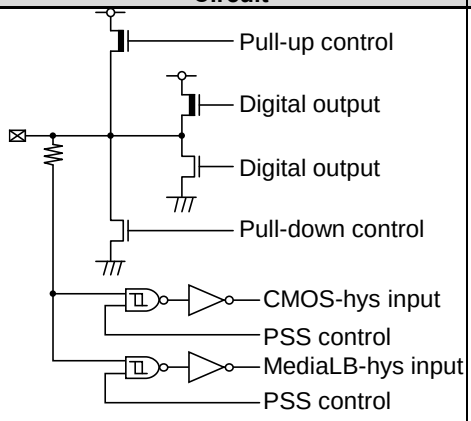
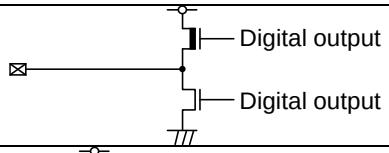
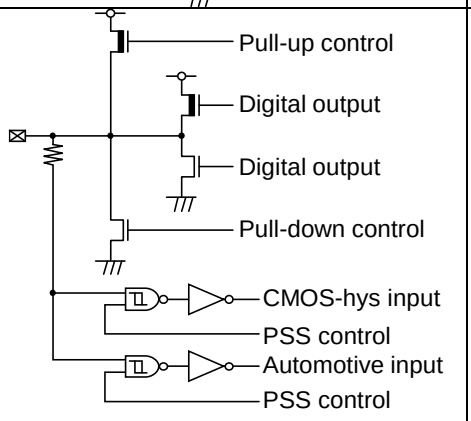
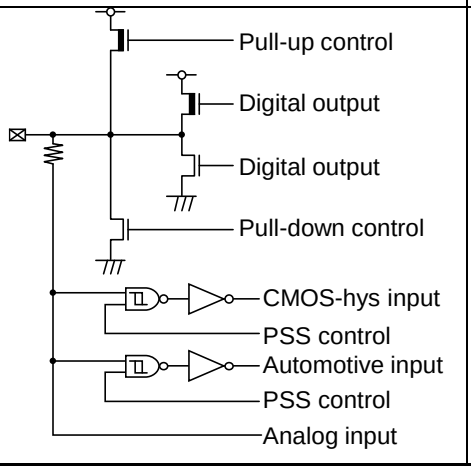
5. I/O Circuit Type

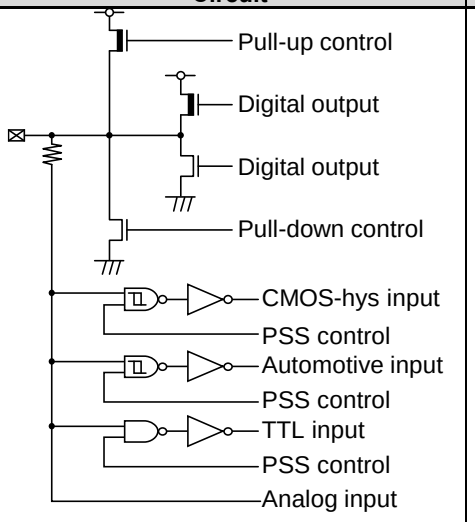
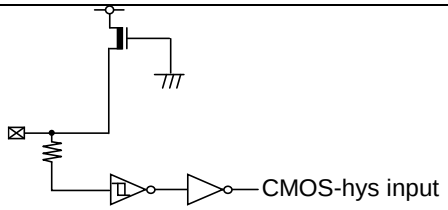
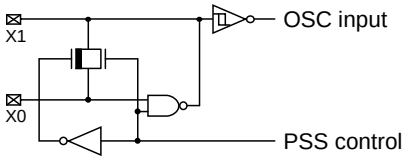
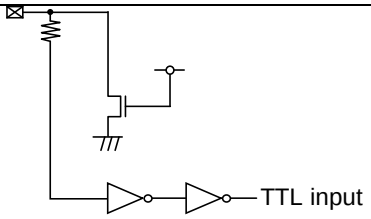
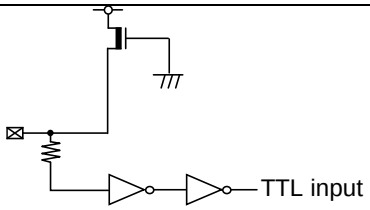
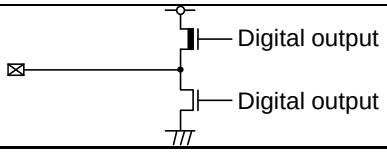
5.1 I/O Circuit Type

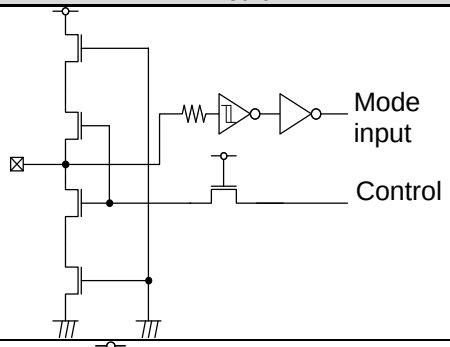
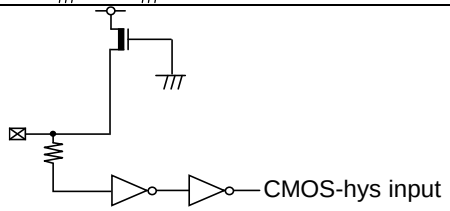
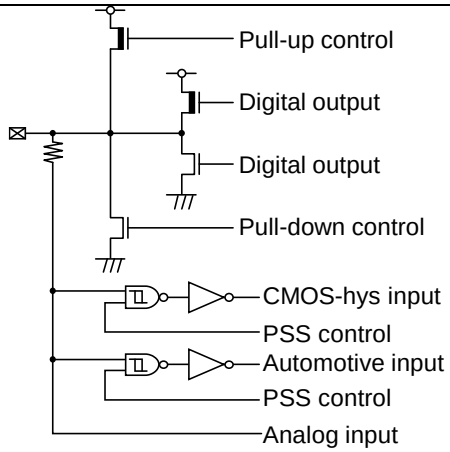
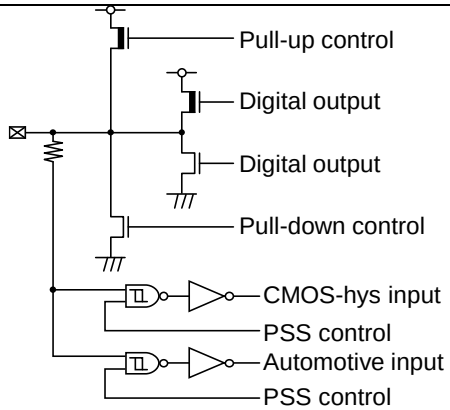
This section explains I/O circuit types.

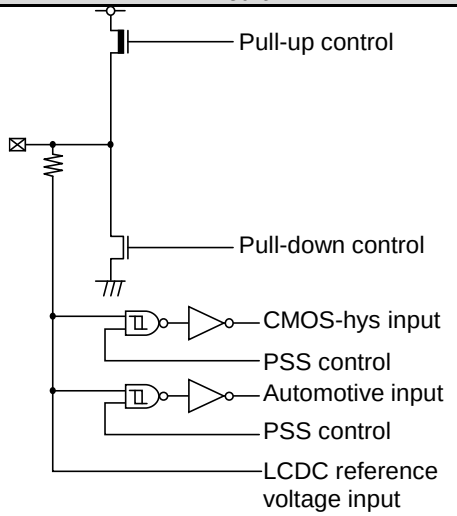
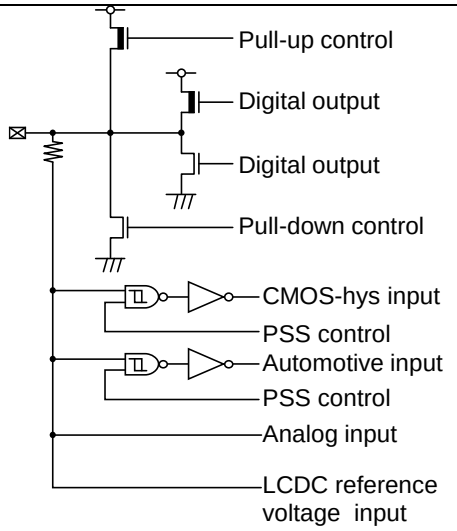
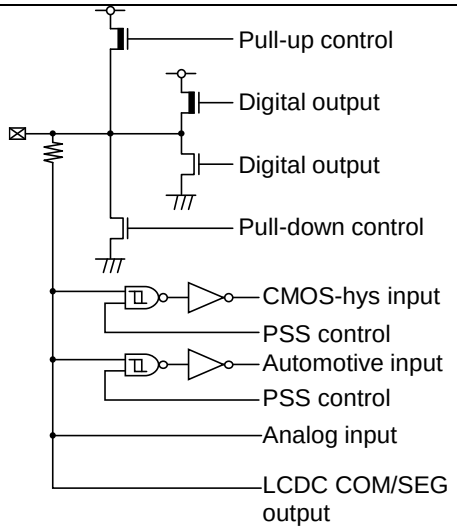
Type	Circuit	Remark
A		– Analog output (3 V) – Audio DAC output
B		– Analog output (3 V) – LVDS output
C		– General-purpose I/O port – Output 2 mA, 5 mA, 10 mA or 20 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – TTL input

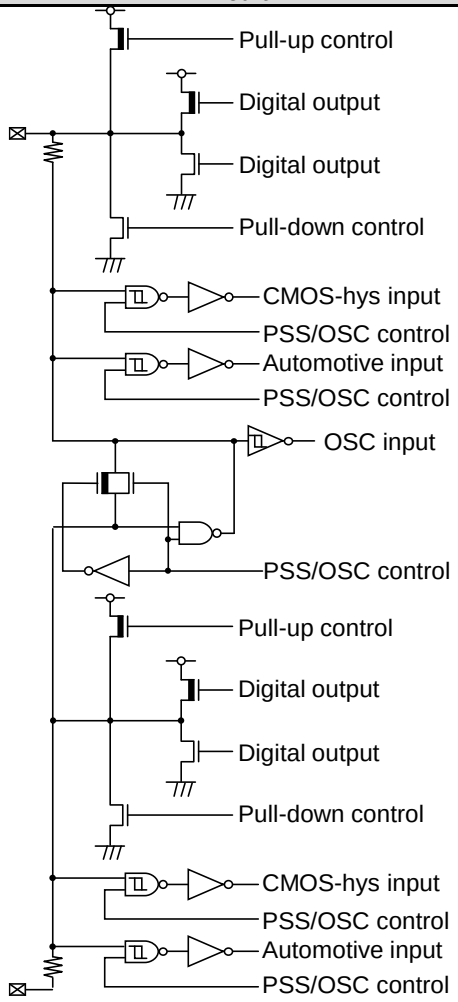
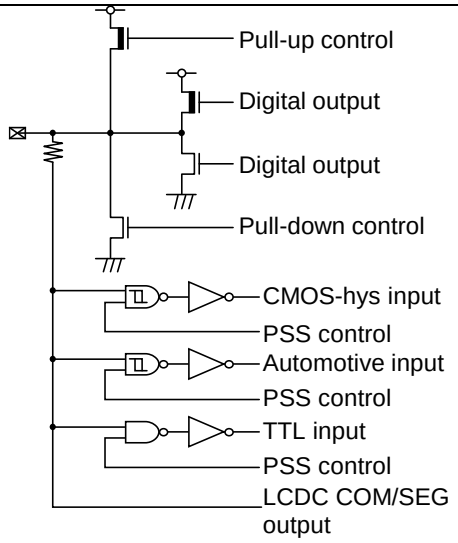
Type	Circuit	Remark
D		– General-purpose I/O port – Output 2 mA, 5 mA, 10 mA or 20 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – TTL input – RSDS differential output data
E		– General-purpose I/O port – Output 2 mA, 5 mA or 10 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – TTL input

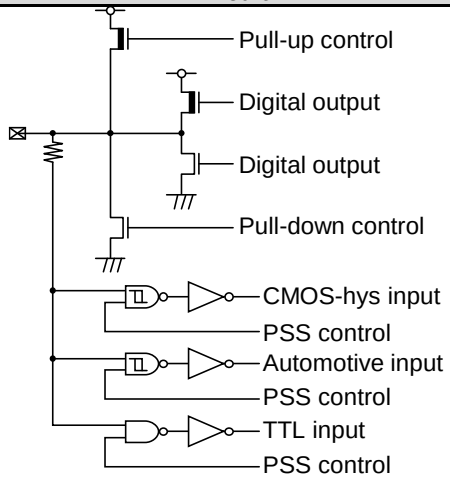
Type	Circuit	Remark
F		– General-purpose I/O port – Output 2 mA, 5 mA, 6 mA or 10 mA selectable – 33 kΩ with pull-up resistor control – 33 kΩ with pull-down resistor control – CMOS hysteresis input – MediaLB level hysteresis input
G		– External 1.2 V regulator control – Output 2 mA
H		– General-purpose I/O port – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
I		– General-purpose I/O port with analog input – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input

Type	Circuit	Remark
J		– General-purpose I/O port with analog input – Output 1 mA, 2 mA, 3 mA(I^2C) or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input – TTL input
L		– 50 kΩ with pull-up – CMOS hysteresis input
M		– Main oscillation I/O
N		– JTAG_NTRST – 50 kΩ with pull-down – TTL input
N2		– JTAG_TDI/TMS/TCK – 50 kΩ with pull-up – TTL input
O		– JTAG_TDO – Output 5 mA

Type	Circuit	Remark
P		– Mode input – CMOS hysteresis input
Q		– CMOS hysteresis input – 50 kΩ with pull-up
S		– General-purpose I/O port with analog input – Output 1 mA, 2 mA, 5 mA or 30 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
T		– General-purpose I/O port – Output 1 mA, 2 mA, 5 mA or 30 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input

Type	Circuit	Remark
U		– General-purpose input port with LCDC reference voltage input – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
V		– General-purpose I/O port with analog input and LCDC reference voltage input – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
W		– General-purpose I/O port with analog input and LCDC COM/SEG output – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input

Type	Circuit	Remark
X		– Sub oscillation I/O shared General-purpose I/O port – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
Y		– General-purpose I/O port with LCDC COM/SEG output – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input – TTL input

Type	Circuit	Remark
Z		– General-purpose I/O port – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input – TTL input

5.2 Note

Alphabets, which show the I/O circuit type, are described with the corresponding pin number in the pin assignment figure.

6. Port Description

6.1 Port Description List

The table shows the port function of description which is supported. The port function which is not described in the table is not supported for the product.

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
VCC12	+1.2-V power supply pin	11, 28, 61, 85, 122, 123, 182, 183	11, 28, 63, 87, 128, 129, 190, 191	
VCC5	+5.0-V power supply pin	87, 104, 115, 157, 171	89, 108, 119, 163, 179	
VCC3	+3.3-V power supply pin	30, 43, 53, 65, 74, 81	30, 43, 55, 67, 76, 83	
VCC53	+3.3 V/+5.0 V selection power supply pin	173, 185, 194, 208	181, 193, 202, 216	
VCC3_LVDS_Tx	LVDS Tx power supply pin	14, 27	14, 27	
VSS	GND	1, 10, 29, 42, 52, 62, 64, 71, 73, 80, 86, 105, 116, 124, 158, 172, 184, 195	1, 10, 29, 42, 54, 64, 66, 73, 75, 82, 88, 109, 120, 130, 164, 180, 192, 203	
VSS_LVDS_Tx	LVDS Tx GND	15, 26	15, 26	
AVCC3_DAC	Audio DAC power supply pin	6	6	
AVCC3_LVDS_PLL	LVDS PLL power supply pin	13	13	
AVSS_LVDS_PLL	LVDS PLL GND	12	12	
AVCC5	A/D converter analog power supply pin	119	125	
AVRH5	A/D converter upper limit reference voltage pin	120	126	
AVSS	A/D converter GND	2, 5, 9, 121	2, 5, 9, 127	
DVCC	SMC large current port power supply pin	126, 136, 146,156	132, 142, 152,162	
DVSS	SMC large current port GND	125, 135, 145,155	131, 141, 151, 161	
X1	Main clock oscillator output pin	106	110	
X0	Main clock oscillator input pin	107	111	
X1A	Sub-clock oscillator output	169	177	
X0A	Sub-clock oscillator input	170	178	
NMIX	Non-maskable interrupt input pin	103	107	
RSTX	External reset input pin	114	118	
PSC_1	External Power Supply Control pin	88	90	
MODE	Mode Pin	113	117	
C	External capacity connection output pin	117	121	
JTAG_NTRST	JTAG test reset input pin	108	112	
JTAG_TDO	JTAG test data output pin	109	113	
JTAG_TDI	JTAG test data input pin	110	114	
JTAG_TCK	JTAG test clock input pin	111	115	
JTAG_TMS	JTAG test mode state input pin	112	116	
TRACE0	Trace data 0 output pin	96	100	
TRACE1	Trace data 1 output pin	97	101	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
TRACE2	Trace data 2 output pin	98	102	
TRACE3	Trace data 3 output pin	99	103	
TRACE_CLK	Trace clock	100	104	
TRACE_CTL	Trace control	101	105	
ADTRG	A/D converter external trigger input pin	118	122	
AN0	ADC Analog 0 input pin	-	92	
AN1	ADC Analog 1 input pin	90	93	
AN2	ADC Analog 2 input pin	91	94	
AN3	ADC Analog 3 input pin	92	95	
AN4	ADC Analog 4 input pin	-	96	
AN5	ADC Analog 5 input pin	93	97	
AN6	ADC Analog 6 input pin	94	98	
AN7	ADC Analog 7 input pin	95	99	
AN8	ADC Analog 8 input pin	96	100	
AN9	ADC Analog 9 input pin	97	101	
AN10	ADC Analog 10 input pin	98	102	
AN11	ADC Analog 11 input pin	99	103	
AN12	ADC Analog 12 input pin	100	104	
AN13	ADC Analog 13 input pin	101	105	
AN14	ADC Analog 14 input pin	102	106	
AN15	ADC Analog 15 input pin	160	166	
AN16	ADC Analog 16 input pin	161	167	
AN17	ADC Analog 17 input pin	162	168	
AN18	ADC Analog 18 input pin	-	169	
AN19	ADC Analog 19 input pin	-	170	
AN20	ADC Analog 20 input pin	163	171	
AN21	ADC Analog 21 input pin	164	172	
AN22	ADC Analog 22 input pin	165	173	
AN23	ADC Analog 23 input pin	166	174	
AN24	ADC Analog 24 input pin	167	175	
AN25	ADC Analog 25 input pin	168	176	
AN26	ADC Analog 26 input pin	127	133	
AN27	ADC Analog 27 input pin	128	134	
AN28	ADC Analog 28 input pin	129	135	
AN29	ADC Analog 29 input pin	130	136	
AN30	ADC Analog 30 input pin	131	137	
AN31	ADC Analog 31 input pin	132	138	
AN32	ADC Analog 32 input pin	133	139	
AN33	ADC Analog 33 input pin	134	140	
AN34	ADC Analog 34 input pin	137	143	
AN35	ADC Analog 35 input pin	138	144	
AN36	ADC Analog 36 input pin	139	145	
AN37	ADC Analog 37 input pin	140	146	
AN38	ADC Analog 38 input pin	141	147	
AN39	ADC Analog 39 input pin	142	148	
AN40	ADC Analog 40 input pin	143	149	
AN41	ADC Analog 41 input pin	144	150	
AN42	ADC Analog 42 input pin	147	153	
AN43	ADC Analog 43 input pin	148	154	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
AN44	ADC Analog 44 input pin	149	155	
AN45	ADC Analog 45 input pin	150	156	
AN46	ADC Analog 46 input pin	151	157	
AN47	ADC Analog 47 input pin	152	158	
AN48	ADC Analog 48 input pin	153	159	
AN49	ADC Analog 49 input pin	154	160	
TX0	CAN transmission data 0 output pin	100	104	
TX1	CAN transmission data 1 output pin	102, 154	106, 160	
TX5	CAN transmission data 5 output pin	162, 166	168, 174	
TX6	CAN transmission data 6 output pin	168	170, 176	
RX0	CAN reception data 0 input pin	99	103	
RX1	CAN reception data 1 input pin	101, 153	105, 159	
RX5	CAN reception data 5 input pin	161, 165	167, 173	
RX6	CAN reception data 6 input pin	167	169. 175	
EINT0	External interrupt input pin	33, 39, 57, 63, 96, 140, 167, 170, 177,199	33, 39, 59, 65, 100, 146, 175, 178, 185, 207	
EINT1	External interrupt input pin	40, 58, 82, 97, 141, 168, 169, 178, 200	40, 60, 84, 101, 147, 176, 177, 186,208,	
EINT2	External interrupt input pin	41, 59, 83, 98, 118, 142, 179, 201,	41, 61, 85, 102, 122, 148, 187, 209	
EINT3	External interrupt input pin	31, 84, 99, 143, 159, 180, 202	31, 44, 86, 103, 123, 149, 165, 188, 210	
EINT4	External interrupt input pin	60, 100, 144, 181, 203	45, 62, 104, 124, 150, 189, 211	
EINT5	External interrupt input pin	44, 72, 101, 127, 147, 186	46, 74, 105, 133, 153, 194,	
EINT6	External interrupt input pin	45, 75, 89, 102, 128, 148, 187,	47, 77, 91, 106, 134, 154, 195	
EINT7	External interrupt input pin	46, 77, 129, 149, 160, 188	48, 79, 135, 155, 166, 196	
EINT8	External interrupt input pin	47, 76, 130, 150, 161, 189	49, 78, 92, 136, 156, 167, 197	
EINT9	External interrupt input pin	48, 79, 90, 131, 151, 162, 190 204	50, 81, 93, 137, 157, 168, 198, 212,	
EINT10	External interrupt input pin	49, 78, 91, 132, 152, 191,205	51, 80, 94, 138, 158, 169, 199, 213	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
EINT11	External interrupt input pin	34, 50, 69, 92, 133, 153, 192, 206	34,52,71, 95,139,159, 170, 200, 214	
EINT12	External interrupt input pin	35, 51, 66, 134, 154, 163, 193, 207	35, 53, 68, 96, 140, 160, 171, 201, 215	
EINT13	External interrupt input pin	36, 54, 68, 93, 137, 164, 174, 196	36, 56, 70, 97, 143, 172, 182, 204	
EINT14	External interrupt input pin	37, 55, 67, 94, 138, 165, 175, 197	37, 57, 69, 98, 144, 173, 183, 205	
EINT15	External interrupt input pin	32, 38, 56, 70, 95, 139, 166, 176, 198	32, 38, 58, 72, 99, 145, 174, 184, 206	
MFS0_CS0	Multi-function serial ch.0 chip select 0 pin	148	154	
MFS0_CS1	Multi-function serial ch.0 chip select 1 pin	153	159	
MFS0_CS2	Multi-function serial ch.0 chip select 2 pin	154	160	
MFS0_CS3	Multi-function serial ch.0 chip select 3 pin	152	158	
MFS2_CS0	Multi-function serial ch.2 chip select 0 pin	149	155	
MFS2_CS1	Multi-function serial ch.2 chip select 1 pin	150	156	
MFS8_CS0	Multi-function serial ch.8 chip select 0 pin	163, 191	171, 199	
MFS8_CS1	Multi-function serial ch.8 chip select 1 pin	167, 198	175, 206	
MFS8_CS2	Multi-function serial ch.8 chip select 2 pin	168, 199	176, 207	
MFS8_CS3	Multi-function serial ch.8 chip select 3 pin	166, 197	174, 205	
MFS9_CS0	Multi-function serial ch.9 chip select 0 pin	164, 192	172, 200	
MFS9_CS1	Multi-function serial ch.9 chip select 1 pin	165, 193	173, 201	
SCK0	Multi-function serial ch.0 clock I/O pin	38, 91	38, 94	
SCK1	Multi-function serial ch.1 clock I/O pin	83, 94	85, 98	
SCK2	Multi-function serial ch.2 clock I/O pin	143	149	
SCK3	Multi-function serial ch.3 clock I/O pin	149	155	
SCK4	Multi-function serial ch.4 clock I/O pin	153	159	
SCK8	Multi-function serial ch.8 clock I/O pin	100, 180	104, 188	
SCK9	Multi-function serial ch.9 clock I/O pin	161, 188	167, 196	
SCK10	Multi-function serial ch.10 clock I/O pin	164, 192	172, 200	
SCK11	Multi-function serial ch.11 clock I/O pin	167, 198, 206	175, 206, 214	
SCK12	Multi-function serial ch.12 clock I/O pin	202	210	
SCK16	Multi-function serial ch.16 clock I/O pin	97	101	
SCK17	Multi-function serial ch.17 clock I/O pin	91	94	
SIN0	Multi-function serial ch.0 serial data input pin	45, 92	47, 95	
SIN1	Multi-function serial ch.1 serial data input pin	84, 95	86, 99	
SIN2	Multi-function serial ch.2 serial data input pin	144	150	
SIN3	Multi-function serial ch.3 serial data input pin	150	156	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
SIN4	Multi-function serial ch.4 serial data input pin	154	160	
SIN8	Multi-function serial ch.8 serial data input pin	101, 181	105, 189	
SIN9	Multi-function serial ch.9 serial data input pin	162, 189	168, 197	
SIN10	Multi-function serial ch.10 serial data input pin	165, 193	173, 201	
SIN11	Multi-function serial ch.11 serial data input pin	168, 199, 207	176, 207, 215	
SIN12	Multi-function serial ch.12 serial data input pin	203	211	
SIN16	Multi-function serial ch.16 serial data input pin	98	102	
SIN17	Multi-function serial ch.17 serial data input pin	92	95	
SOT0	Multi-function serial ch.0 serial data output pin	37, 90	37, 93	
SOT1	Multi-function serial ch.1 serial data output pin	82, 93	84, 97	
SOT2	Multi-function serial ch.2 serial data output pin	142	148	
SOT3	Multi-function serial ch.3 serial data output pin	148	154	
SOT4	Multi-function serial ch.4 serial data output pin	152	158	
SOT8	Multi-function serial ch.8 serial data output pin	99, 179	103, 187	
SOT9	Multi-function serial ch.9 serial data output pin	160, 187	166, 195	
SOT10	Multi-function serial ch.10 serial data output pin	163, 191	171, 199	
SOT11	Multi-function serial ch.11 serial data output pin	166, 197, 205	174, 205, 213	
SOT12	Multi-function serial ch.12 serial data output pin	201	209	
SOT16	Multi-function serial ch.16 serial data output pin	96	100	
SOT17	Multi-function serial ch.17 serial data output pin	90	93	
SCL4 (MFS4_SCL)	I^2C ch.4 clock I/O pin	153	159	
SCL10 (MFS10_SCL)	I^2C ch.10 clock I/O pin	192	200	
SCL12 (MFS12_SCL)	I^2C ch.12 clock I/O pin	202	210	
SCL16 (MFS16_SCL)	I^2C ch.16 clock I/O pin	97	101	
SCL17 (MFS17_SCL)	I^2C ch.17 clock I/O pin	91	94	
SDA4 (MFS4_SDA)	I^2C ch.4 serial data I/O pin	152	158	
SDA10 (MFS10_SDA)	I^2C ch.10 serial data I/O pin	191	199	
SDA12 (MFS12_SDA)	I^2C ch.12 serial data I/O pin	201	209	
SDA16 (MFS16_SDA)	I^2C ch.16 serial data I/O pin	96	100	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
SDA17 (MFS17_SDA)	I²C ch.17 serial data I/O pin	90	93	
PPG0_TOUT0	Base timer 0 output pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
PPG0_TOUT2	Base timer 1 output pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
PPG1_TOUT0	Base timer 2 output pin	41,142,201, 205	41,148,169, 209,213	
PPG1_TOUT2	Base timer 3 output pin	143, 202, 206	44, 149, 170, 210, 214	
PPG2_TOUT0	Base timer 4 output pin	144, 163, 203, 207	45, 150, 171, 211, 215	
PPG2_TOUT2	Base timer 5 output pin	44, 147, 164, 174	46, 153, 172, 182	
PPG3_TOUT0	Base timer 6 output pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
PPG3_TOUT2	Base timer 7 output pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
PPG4_TOUT0	Base timer 8 output pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
PPG4_TOUT2	Base timer 9 output pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
PPG5_TOUT0	Base timer 10 output pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	
PPG5_TOUT2	Base timer 11 output pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
PPG6_TOUT0	Base timer 12 output pin	51, 75, 154, 181	53, 77, 96, 124, 160,189	
PPG6_TOUT2	Base timer 13 output pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
PPG7_TOUT0	Base timer 14 output pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
PPG7_TOUT2	Base timer 15 output pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
PPG8_TOUT0	Base timer 16 output pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
PPG8_TOUT2	Base timer 17 output pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
PPG9_TOUT0	Base timer 18 output pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
PPG9_TOUT2	Base timer 19 output pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
PPG10_TOUT0	Base timer 20 output pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
PPG10_TOUT2	Base timer 21 output pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
PPG11_TOUT0	Base timer 22 output pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
PPG11_TOUT2	Base timer 23 output pin	38, 139, 160, 198	38, 145, 166, 206	
PPG0/1/2/3/4/5_TIN1	Base timer 0/2/4/6/8/10 input pin	-	96	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
PPG6/7/8/9/10/11_TIN1	Base timer 12/14/16/18/20/22 input pin	161	167	
WOT	RTC overflow output pin	161	167	
PWM1M0	SMC ch.0 output pin	128	134	
PWM1M1	SMC ch.1 output pin	132	138	
PWM1M2	SMC ch.2 output pin	138	144	
PWM1M3	SMC ch.3 output pin	142	148	
PWM1M4	SMC ch.4 output pin	148	154	
PWM1M5	SMC ch.5 output pin	152	158	
PWM1P0	SMC ch.0 output pin	127	133	
PWM1P1	SMC ch.1 output pin	131	137	
PWM1P2	SMC ch.2 output pin	137	143	
PWM1P3	SMC ch.3 output pin	141	147	
PWM1P4	SMC ch.4 output pin	147	153	
PWM1P5	SMC ch.5 output pin	151	157	
PWM2M0	SMC ch.0 output pin	130	136	
PWM2M1	SMC ch.1 output pin	134	140	
PWM2M2	SMC ch.2 output pin	140	146	
PWM2M3	SMC ch.3 output pin	144	150	
PWM2M4	SMC ch.4 output pin	150	156	
PWM2M5	SMC ch.5 output pin	154	160	
PWM2P0	SMC ch.0 output pin	129	135	
PWM2P1	SMC ch.1 output pin	133	139	
PWM2P2	SMC ch.2 output pin	139	145	
PWM2P3	SMC ch.3 output pin	143	149	
PWM2P4	SMC ch.4 output pin	149	155	
PWM2P5	SMC ch.5 output pin	153	159	
OCU0_OTD0	Output compare 0 ch.0 output pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
OCU0_OTD1	Output compare 0 ch.1 output pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
OCU1_OTD0	Output compare 1 ch.0 output pin	41, 142, 201, 205	41, 148, 169, 209, 213	
OCU1_OTD1	Output compare 1 ch.1 output pin	143, 202, 206	44, 149, 170, 210, 214	
OCU2_OTD0	Output compare 2 ch.0 output pin	144, 163, 203, 207	45, 150, 171, 211, 215	
OCU2_OTD1	Output compare 2 ch.1 output pin	44, 147, 164, 174	46, 153, 172, 182	
OCU3_OTD0	Output compare 3 ch.0 output pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
OCU3_OTD1	Output compare 3 ch.1 output pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
OCU4_OTD0	Output compare 4 ch.0 output pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
OCU4_OTD1	Output compare 4 ch.1 output pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
OCU5_OTD0	Output compare 5 ch.0 output pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
OCU5_OTD1	Output compare 5 ch.1 output pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
OCU6_OTD0	Output compare 6 ch.0 output pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
OCU6_OTD1	Output compare 6 ch.1 output pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
OCU7_OTD0	Output compare 7 ch.0 output pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
OCU7_OTD1	Output compare 7 ch.1 output pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
OCU8_OTD0	Output compare 8 ch.0 output pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
OCU8_OTD1	Output compare 8 ch.1 output pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
OCU9_OTD0	Output compare 9 ch.0 output pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
OCU9_OTD1	Output compare 9 ch.1 output pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
OCU10_OTD0	Output compare 10 ch.0 output pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
OCU10_OTD1	Output compare 10 ch.1 output pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
OCU11_OTD0	Output compare 11 ch.0 output pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
OCU11_OTD1	Output compare 11 ch.1 output pin	38, 139, 160, 198	38, 145, 166, 206	
ICU0_IN0	Input Capture 0 ch.0 input pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
ICU0_IN1	Input Capture 0 ch.1 input pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
ICU1_IN0	Input Capture 1 ch.0 input pin	41, 142, 201, 205	41, 148, 169, 209, 213	
ICU1_IN1	Input Capture 1 ch.1 input pin	143, 159, 202, 206	44, 149, 165, 170, 210, 214	
ICU2_IN0	Input Capture 2 ch.0 input pin	144, 163, 203, 207	45, 150, 171, 211, 215	
ICU2_IN1	Input Capture 2 ch.1 input pin	44, 147, 164, 174	46, 153, 172, 182	
ICU3_IN0	Input Capture 3 ch.0 input pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
ICU3_IN1	Input Capture 3 ch.1 input pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
ICU4_IN0	Input Capture 4 ch.0 input pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
ICU4_IN1	Input Capture 4 ch.1 input pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
ICU5_IN0	Input Capture 5 ch.0 input pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
ICU5_IN1	Input Capture 5 ch.1 input pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
ICU6_IN0	Input Capture 6 ch.0 input pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
ICU6_IN1	Input Capture 6 ch.1 input pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
ICU7_IN0	Input Capture 7 ch.0 input pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
ICU7_IN1	Input Capture 7 ch.1 input pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
ICU8_IN0	Input Capture 8 ch.0 input pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
ICU8_IN1	Input Capture 8 ch.1 input pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
ICU9_IN0	Input Capture 9 ch.0 input pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
ICU9_IN1	Input Capture 9 ch.1 input pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
ICU10_IN0	Input Capture 10 ch.0 input pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
ICU10_IN1	Input Capture 10 ch.1 input pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
ICU11_IN0	Input Capture 11 ch.0 input pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
ICU11_IN1	Input Capture 11 ch.1 input pin	38, 139, 160, 198	38, 145, 166, 206	
SGA0	Sound generator ch.0 SGA output pin	90, 97, 164	93, 101, 172	
SGA1	Sound generator ch.1 SGA output pin	91, 98, 165, 205	94, 102, 173, 213	
SGA2	Sound generator ch.2 SGA output pin	100, 167	96, 104, 175	
SGA3	Sound generator ch.3 SGA output pin	94, 118, 175	98, 122, 183	
SGO0	Sound generator ch.0 SGO output pin	96, 163	92, 100, 171	
SGO1	Sound generator ch.1 SGO output pin	92,99,166,206	95,103,174,214	
SGO2	Sound generator ch.2 SGO output pin	93, 101, 168	97, 105, 176	
SGO3	Sound generator ch.3 SGO output pin	95, 176	99, 123, 184	
AN0(AL0)	PCM PWM ch.0 output pin	128, 175	134, 183	
AN1(AL1)	PCM PWM ch.1 output pin	132, 179	138, 187	
AP0(AH0)	PCM PWM ch.0 output pin	127, 174	133, 182	
AP1(AH1)	PCM PWM ch.1 output pin	131, 178	137, 186	
BN0(BL0)	PCM PWM ch.0 output pin	130, 177	136, 185	
BN1(BL1)	PCM PWM ch.1 output pin	134, 181	140, 189	
BP0(BH0)	PCM PWM ch.0 output pin	129, 176	135, 184	
BP1(BH1)	PCM PWM ch.1 output pin	133, 180	139, 188	
I2S0_ECLK	I2S external clock ch.0 input pin	50	52	
I2S1_ECLK	I2S external clock ch.1 input pin	56	58	
I2S0_SCK	I2S continuous serial clock ch.0 pin	55	57	
I2S1_SCK	I2S continuous serial clock ch.1 pin	59	61	
I2S0_SD	I2S serial data ch.0 pin	51	53	
I2S1_SD	I2S serial data ch.1 pin	57	59	
I2S0_WS	I2S word select ch.0 pin	54	56	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
I2S1_WS	I2S word select ch.1 pin	58	60	
C_L	Audio DAC external capacity connection output pin (L)	8	8	
C_R	Audio DAC external capacity connection output pin (R)	4	4	
DAC_L	Audio DAC output pin (L)	7	7	
DAC_R	Audio DAC output pin (R)	3	3	
FRT0/1/2/3_TEXT	Free-run timer ch.0/1/2/3 clock input pin	160	166	
FRT4/5/6/7_TEXT	Free-run timer ch.4/5/6/7 clock input pin	166	174	
FRT8/9/10/11_TEXT	Free-run timer ch.4/5/6/7 clock input pin	95	99	
TIN0	Reload timer ch.0 event input pin	35	35, 96	
TIN1	Reload timer ch.1 event input pin	37, 93	37, 97	
TIN2	Reload timer ch.2 event input pin	39, 94	39, 98	
TIN3	Reload timer ch.3 event input pin	41, 95	41, 99	
TIN16	Reload timer ch.16 event input pin	100	45, 104	
TIN17	Reload timer ch.17 event input pin	45, 102	47, 106	
TIN18	Reload timer ch.18 event input pin	47, 162	49, 168	
TIN19	Reload timer ch.19 event input pin	49	51, 170	
TIN32	Reload timer ch.32 event input pin	51, 164	53, 172	
TIN33	Reload timer ch.33 event input pin	55, 166	57, 174	
TIN34	Reload timer ch.34 event input pin	57, 168	59, 176	
TIN35	Reload timer ch.35 event input pin	59	61, 123	
TIN48	Reload timer ch.48 event input pin	159	165	
TIN49	Reload timer ch.49 event input pin	89	91	
TOT0	Reload timer ch.0 output pin	34, 96	34, 100	
TOT1	Reload timer ch.1 output pin	36, 97	36, 101	
TOT2	Reload timer ch.2 output pin	38, 98	38, 102	
TOT3	Reload timer ch.3 output pin	40, 99	40, 103	
TOT16	Reload timer ch.16 output pin	101	44, 105	
TOT17	Reload timer ch.17 output pin	44, 160	46, 166	
TOT18	Reload timer ch.18 output pin	46, 161	48, 167	
TOT19	Reload timer ch.19 output pin	48	50, 169	
TOT32	Reload timer ch.32 output pin	50, 163	52, 171	
TOT33	Reload timer ch.33 output pin	54, 165	56, 173	
TOT34	Reload timer ch.34 output pin	56,167	58, 175	
TOT35	Reload timer ch.35 output pin	58, 118	60, 122	
AIN8	Up/Down counter AIN input pin ch.8	190	92, 198	
AIN9	Up/Down counter AIN input pin ch.9	93, 193	97, 201	
BIN8	Up/Down counter BIN input pin ch.8	90, 191	93, 199	
BIN9	Up/Down counter BIN input pin ch.9	94, 196	98, 204	
ZIN8	Up/Down counter ZIN input pin ch.8	91, 192	94, 200	
ZIN9	Up/Down counter ZIN input pin ch.9	95, 197	99, 205	
RXD0	Ethernet pin	48	50	
RXD1	Ethernet pin	49	51	
RXD2	Ethernet pin	50	52	
RXD3	Ethernet pin	51	53	
TXD0	Ethernet pin	44	46	
TXD1	Ethernet pin	45	47	
TXD2	Ethernet pin	46	48	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
TXD3	Ethernet pin	47	49	
COL	Ethernet pin	58	44, 60	
CRS	Ethernet pin	84	45, 86	
RXER	Ethernet pin	56	58	
RXDV	Ethernet pin	57	59	
RXCLK	Ethernet pin	55	57	
TXER	Ethernet pin	60	62	
TXEN	Ethernet pin	41	41	
TXCLK	Ethernet pin	54	56	
MDC	Ethernet pin	31	31	
MDIO	Ethernet pin	32	32	
MLBCLK	MediaLB pin	84	86	
MLBDAT	MediaLB pin	82	84	
MLBSIG	MediaLB pin	83	85	
TxCLK-	LVDS clock output pin	21	21	Described as TXOUT4M in FPD-Link Converter
TxCLK+	LVDS clock output pin	20	20	Described as TXOUT4P in FPD-Link Converter
TxDOUT0-	LVDS data output pin	25	25	Described as TXOUT0M in FPD-Link Converter
TxDOUT0+	LVDS data output pin	24	24	Described as TXOUT0P in FPD-Link Converter
TxDOUT1-	LVDS data output pin	23	23	Described as TXOUT1M in FPD-Link Converter
TxDOUT1+	LVDS data output pin	22	22	Described as TXOUT1P in FPD-Link Converter
TxDOUT2-	LVDS data output pin	19	19	Described as TXOUT2M in FPD-Link Converter
TxDOUT2+	LVDS data output pin	18	18	Described as TXOUT2P in FPD-Link Converter
TxDOUT3-	LVDS data output pin	17	17	Described as TXOUT3M in FPD-Link Converter
TxDOUT3+	LVDS data output pin	16	16	Described as TXOUT3P in FPD-Link Converter
G_SCLK0	Graphic HS-SPI clock output pin	72	74	
G_SDATA0_0	Graphic HS-SPI0 data 0 pin	75	77	
G_SDATA0_1	Graphic HS-SPI0 data 1 pin	77	79	
G_SDATA0_2	Graphic HS-SPI0 data 2 pin	76	78	
G_SDATA0_3	Graphic HS-SPI0 data 3 pin	79	81	
G_SDATA1_0	Graphic HS-SPI1 data 0 pin	66	68	
G_SDATA1_1	Graphic HS-SPI1 data 1 pin	68	70	
G_SDATA1_2	Graphic HS-SPI1 data 2 pin	67	69	
G_SDATA1_3	Graphic HS-SPI1 data 3 pin	70	72	
G_SSEL0	Graphic HS-SPI select 0 output pin	78	80	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
G_SSEL1	Graphic HS-SPI select 1 output pin	69	71	
G_CK_1	Hyper Bus 1 clock output pin	63	65	
G_CS#1_1	Hyper Bus 1 select 1 output pin	70	72	
G_CS#2_1	Hyper Bus 1 select 2 output pin	75	77	
G_DQ0_1	Hyper Bus 1 Data 0 pin	69	71	
G_DQ1_1	Hyper Bus 1 Data 1 pin	68	70	
G_DQ2_1	Hyper Bus 1 Data 2 pin	67	69	
G_DQ3_1	Hyper Bus 1 Data 3 pin	66	68	
G_DQ4_1	Hyper Bus 1 Data 4 pin	76	78	
G_DQ5_1	Hyper Bus 1 Data 5 pin	77	79	
G_DQ6_1	Hyper Bus 1 Data 6 pin	78	80	
G_DQ7_1	Hyper Bus 1 Data 7 pin	79	81	
G_RWDS_1	Hyper Bus 1 RWDS pin #699	72	74	
G_CK_2	Hyper Bus 2 clock output pin	44	46	
G_CS#1_2	Hyper Bus 2 select 1 output pin	49	51	
G_CS#2_2	Hyper Bus 2 select 2 output pin	51	53	
G_DQ0_2	Hyper Bus 2 Data 0 pin	48	50	
G_DQ1_2	Hyper Bus 2 Data 1 pin	47	49	
G_DQ2_2	Hyper Bus 2 Data 2 pin	46	48	
G_DQ3_2	Hyper Bus 2 Data 3 pin	45	47	
G_DQ4_2	Hyper Bus 2 Data 4 pin	54	56	
G_DQ5_2	Hyper Bus 2 Data 5 pin	55	57	
G_DQ6_2	Hyper Bus 2 Data 6 pin	56	58	
G_DQ7_2	Hyper Bus 2 Data 7 pin	57	59	
G_RWDS_2	Hyper Bus 2 RWDS pin	50	52	
M_SCLK0	MCU HS-SPI clock output pin	63	65	
M_SDATA0_0	MCU HS-SPI0 data 0 pin	66	68	
M_SDATA0_1	MCU HS-SPI0 data 1 pin	68	70	
M_SDATA0_2	MCU HS-SPI0 data 2 pin	67	69	
M_SDATA0_3	MCU HS-SPI0 data 3 pin	70	72	
M_SDATA1_0	MCU HS-SPI1 data 0 pin	75	77	
M_SDATA1_1	MCU HS-SPI1 data 1 pin	77	79	
M_SDATA1_2	MCU HS-SPI1 data 2 pin	76	78	
M_SDATA1_3	MCU HS-SPI1 data 3 pin	79	81	
M_SSEL0	MCU HS-SPI select 0 output pin	69	71	
M_SSEL1	MCU HS-SPI select 1 output pin	78	80	
M_CK_0	MCU Hyper Bus clock output pin	63	65	
M_CS#1_0	MCU Hyper Bus select 1 output pin	70	72	
M_CS#2_0	MCU Hyper Bus select 2 output pin	75	77	
M_DQ0_0	MCU Hyper Bus Data 0 pin	69	71	
M_DQ1_0	MCU Hyper Bus Data 1 pin	68	70	
M_DQ2_0	MCU Hyper Bus Data 2 pin	67	69	
M_DQ3_0	MCU Hyper Bus Data 3 pin	66	68	
M_DQ4_0	MCU Hyper Bus Data 4 pin	76	78	
M_DQ5_0	MCU Hyper Bus Data 5 pin	77	79	
M_DQ6_0	MCU Hyper Bus Data 6 pin	78	80	
M_DQ7_0	MCU Hyper Bus Data 7 pin	79	81	
M_RWDS_0	MCU Hyper Bus RWDS pin #699	72	74	
COM0	LCDC Segment(Duty) Common Output Pin	207	215	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
COM1	LCDC Segment(Duty) Common Output Pin	206	214	
COM2	LCDC Segment(Duty) Common Output Pin	205	213	
COM3	LCDC Segment(Duty) Common Output Pin	204	212	
SEG0	LCDC Segment(Duty) Output Pin	203	211	
SEG1	LCDC Segment(Duty) Output Pin	202	210	
SEG2	LCDC Segment(Duty) Output Pin	201	209	
SEG3	LCDC Segment(Duty) Output Pin	200	208	
SEG4	LCDC Segment(Duty) Output Pin	199	207	
SEG5	LCDC Segment(Duty) Output Pin	198	206	
SEG6	LCDC Segment(Duty) Output Pin	197	205	
SEG7	LCDC Segment(Duty) Output Pin	196	204	
SEG8	LCDC Segment(Duty) Output Pin	193	201	
SEG9	LCDC Segment(Duty) Output Pin	192	200	
SEG10	LCDC Segment(Duty) Output Pin	191	199	
SEG11	LCDC Segment(Duty) Output Pin	190	198	
SEG12	LCDC Segment(Duty) Output Pin	189	197	
SEG13	LCDC Segment(Duty) Output Pin	188	196	
SEG14	LCDC Segment(Duty) Output Pin	187	195	
SEG15	LCDC Segment(Duty) Output Pin	186	194	
SEG16	LCDC Segment(Duty) Output Pin	181	189	
SEG17	LCDC Segment(Duty) Output Pin	180	188	
SEG18	LCDC Segment(Duty) Output Pin	179	187	
SEG19	LCDC Segment(Duty) Output Pin	178	186	
SEG20	LCDC Segment(Duty) Output Pin	177	185	
SEG21	LCDC Segment(Duty) Output Pin	176	184	
SEG22	LCDC Segment(Duty) Output Pin	175	183	
SEG23	LCDC Segment(Duty/Static) Output Pin	174	182	
SEG24	LCDC Segment(Duty/Static) Output Pin	168	176	
SEG25	LCDC Segment(Duty/Static) Output Pin	167	175	
SEG26	LCDC Segment(Duty/Static) Output Pin	166	174	
SEG27	LCDC Segment(Duty/Static) Output Pin	165	173	
SEG28	LCDC Segment(Duty/Static) Output Pin	164	172	
SEG29	LCDC Segment(Duty/Static) Output Pin	163	171	
SEG30	LCDC Segment(Duty/Static) Output Pin	-	170	
SEG31	LCDC Segment(Duty/Static) Output Pin	-	169	
V0	LCDC Reference Voltage V0 Input Pin	162	168	
V1	LCDC Reference Voltage V1 Input Pin	161	167	
V2	LCDC Reference Voltage V2 Input Pin	160	166	
V3	LCDC Reference Voltage V3 Input Pin	159	165	
DSP0_CLK	Display 0 Clock output pin	32, 58	32, 60	
DSP0_CLK-	Display 0 RSDS Clock output pin	33	33	
DSP0_CLK+	Display 0 RSDS Clock output pin	32	32	
DSP0_CTRL0	Display 0 Control output pin	59, 60, 196	61, 62, 204	
DSP0_CTRL1	Display 0 Control output pin	31, 60, 197	31, 62, 205	
DSP0_CTRL2	Display 0 Control output pin	33, 57, 60, 82, 198	33, 59, 62, 84, 206	
DSP0_CTRL3	Display 0 Control output pin	83, 199	85, 207	
DSP0_CTRL4	Display 0 Control output pin	84, 200	86, 208	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
DSP0_CTRL5	Display 0 Control output pin	201	209	
DSP0_CTRL6	Display 0 Control output pin	202	210	
DSP0_CTRL7	Display 0 Control output pin	203	211	
DSP0_CTRL8	Display 0 Control output pin	204	212	
DSP0_CTRL9	Display 0 Control output pin	205	213	
DSP0_CTRL10	Display 0 Control output pin	206	214	
DSP0_CTRL11	Display 0 Control output pin	207	215	
DSP0_DATA0_0	Display 0 Data output pin	34	34	
DSP0_DATA0_1	Display 0 Data output pin	36	36	
DSP0_DATA0_2	Display 0 Data output pin	38	38	
DSP0_DATA0_3	Display 0 Data output pin	40	40	
DSP0_DATA0_4	Display 0 Data output pin	31	31, 44	
DSP0_DATA0_5	Display 0 Data output pin	44	46	
DSP0_DATA0_6	Display 0 Data output pin	46	48	
DSP0_DATA0_7	Display 0 Data output pin	48	50	
DSP0_DATA0_8	Display 0 Data output pin	50	52	
DSP0_DATA0_9	Display 0 Data output pin	54	56	
DSP0_DATA0_10	Display 0 Data output pin	56	58	
DSP0_DATA0_11	Display 0 Data output pin	32, 58	32, 60	
DSP0_DATA1_0	Display 0 Data output pin	35	35	
DSP0_DATA1_1	Display 0 Data output pin	37	37	
DSP0_DATA1_2	Display 0 Data output pin	39	39	
DSP0_DATA1_3	Display 0 Data output pin	41	41	
DSP0_DATA1_4	Display 0 Data output pin	33	33, 45	
DSP0_DATA1_5	Display 0 Data output pin	45	47	
DSP0_DATA1_6	Display 0 Data output pin	47	49	
DSP0_DATA1_7	Display 0 Data output pin	49	51	
DSP0_DATA1_8	Display 0 Data output pin	51	53	
DSP0_DATA1_9	Display 0 Data output pin	55	57	
DSP0_DATA1_10	Display 0 Data output pin	31, 57	31, 59	
DSP0_DATA1_11	Display 0 Data output pin	33, 59	33, 61	
DSP0_DATA_D0-	Display 0 RSDS Data output pin	35	35	
DSP0_DATA_D0+	Display 0 RSDS Data output pin	34	34	
DSP0_DATA_D1-	Display 0 RSDS Data output pin	37	37	
DSP0_DATA_D1+	Display 0 RSDS Data output pin	36	36	
DSP0_DATA_D2-	Display 0 RSDS Data output pin	39	39	
DSP0_DATA_D2+	Display 0 RSDS Data output pin	38	38	
DSP0_DATA_D3-	Display 0 RSDS Data output pin	41	41	
DSP0_DATA_D3+	Display 0 RSDS Data output pin	40	40	
DSP0_DATA_D4-	Display 0 RSDS Data output pin	-	45	
DSP0_DATA_D4+	Display 0 RSDS Data output pin	-	44	
DSP0_DATA_D5-	Display 0 RSDS Data output pin	45	47	
DSP0_DATA_D5+	Display 0 RSDS Data output pin	44	46	
DSP0_DATA_D6-	Display 0 RSDS Data output pin	47	49	
DSP0_DATA_D6+	Display 0 RSDS Data output pin	46	48	
DSP0_DATA_D7-	Display 0 RSDS Data output pin	49	51	
DSP0_DATA_D7+	Display 0 RSDS Data output pin	48	50	
DSP0_DATA_D8-	Display 0 RSDS Data output pin	51	53	
DSP0_DATA_D8+	Display 0 RSDS Data output pin	50	52	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
DSP0_DATA_D9-	Display 0 RSDS Data output pin	55	57	
DSP0_DATA_D9+	Display 0 RSDS Data output pin	54	56	
DSP0_DATA_D10-	Display 0 RSDS Data output pin	57	59	
DSP0_DATA_D10+	Display 0 RSDS Data output pin	56	58	
DSP0_DATA_D11-	Display 0 RSDS Data output pin	59	61	
DSP0_DATA_D11+	Display 0 RSDS Data output pin	58	60	
DSP1_CLK	Display 1 Clock output pin	199, 204	207, 212	
DSP1_CTRL0	Display 1 Control output pin	200, 207	208, 215	
DSP1_CTRL1	Display 1 Control output pin	201, 206	209, 214	
DSP1_CTRL2	Display 1 Control output pin	198, 205	206, 213	
DSP1_DATA0_0	Display 1 Data output pin	203	211	
DSP1_DATA0_1	Display 1 Data output pin	201	209	
DSP1_DATA0_2	Display 1 Data output pin	199	207	
DSP1_DATA0_3	Display 1 Data output pin	197	205	
DSP1_DATA0_4	Display 1 Data output pin	193	201	
DSP1_DATA0_5	Display 1 Data output pin	191	199	
DSP1_DATA0_6	Display 1 Data output pin	189	197	
DSP1_DATA0_7	Display 1 Data output pin	187	195	
DSP1_DATA0_8	Display 1 Data output pin	181	189	
DSP1_DATA0_9	Display 1 Data output pin	179	187	
DSP1_DATA0_10	Display 1 Data output pin	177	185	
DSP1_DATA0_11	Display 1 Data output pin	175	183	
DSP1_DATA1_0	Display 1 Data output pin	202	210	
DSP1_DATA1_1	Display 1 Data output pin	200	208	
DSP1_DATA1_2	Display 1 Data output pin	198	206	
DSP1_DATA1_3	Display 1 Data output pin	196	204	
DSP1_DATA1_4	Display 1 Data output pin	192	200	
DSP1_DATA1_5	Display 1 Data output pin	190	198	
DSP1_DATA1_6	Display 1 Data output pin	188	196	
DSP1_DATA1_7	Display 1 Data output pin	186	194	
DSP1_DATA1_8	Display 1 Data output pin	180	188	
DSP1_DATA1_9	Display 1 Data output pin	178	186	
DSP1_DATA1_10	Display 1 Data output pin	176	184	
DSP1_DATA1_11	Display 1 Data output pin	174	182	
CAP0_CLK	Video Capture 0 Clock input pin	59	61	
CAP0_DATA0	Video Capture 0 Data input pin	31	31	
CAP0_DATA1	Video Capture 0 Data input pin	32	32	
CAP0_DATA2	Video Capture 0 Data input pin	33	33	
CAP0_DATA3	Video Capture 0 Data input pin	34	34	
CAP0_DATA4	Video Capture 0 Data input pin	35	35	
CAP0_DATA5	Video Capture 0 Data input pin	36	36	
CAP0_DATA6	Video Capture 0 Data input pin	37	37	
CAP0_DATA7	Video Capture 0 Data input pin	38	38	
CAP0_DATA8	Video Capture 0 Data input pin	39	39	
CAP0_DATA9	Video Capture 0 Data input pin	40	40	
CAP0_DATA10	Video Capture 0 Data input pin	41	41	
CAP0_DATA11	Video Capture 0 Data input pin	44	44, 46	
CAP0_DATA12	Video Capture 0 Data input pin	45	45, 47	
CAP0_DATA13	Video Capture 0 Data input pin	44, 46	46, 48	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
CAP0_DATA14	Video Capture 0 Data input pin	45, 47	47, 49	
CAP0_DATA15	Video Capture 0 Data input pin	46, 48	48, 50	
CAP0_DATA16	Video Capture 0 Data input pin	47	49	
CAP0_DATA17	Video Capture 0 Data input pin	48	50	
CAP0_DATA18	Video Capture 0 Data input pin	49	51	
CAP0_DATA19	Video Capture 0 Data input pin	50	52	
CAP0_DATA20	Video Capture 0 Data input pin	51	53	
CAP0_DATA21	Video Capture 0 Data input pin	54	56	
CAP0_DATA22	Video Capture 0 Data input pin	55	57	
CAP0_DATA23	Video Capture 0 Data input pin	56	58	
CAP0_DATA24	Video Capture 0 Data input pin	82	84	
CAP0_DATA25	Video Capture 0 Data input pin	83	85	
CAP0_DATA32	Video Capture 0 Data input pin	56, 57	58, 59	
CAP0_DATA33	Video Capture 0 Data input pin	58	60	
CAP0_DATA34	Video Capture 0 Data input pin	60	62	
CAP0_DATA35	Video Capture 0 Data input pin	57	59	
INDICATOR0_0	Indicator PWM output pin 0 It can also obtained from INDICATOR0_1)	92	95	
INDICATOR0_1	Indicator PWM output pin (It can also obtained from INDICATOR0_0)	170	178	
P0_00	General-Purpose I/O port	40	40	
P0_01	General-Purpose I/O port	41	41	
P0_02	General-Purpose I/O port	-	44	
P0_03	General-Purpose I/O port	-	45	
P0_04	General-Purpose I/O port	44	46	
P0_05	General-Purpose I/O port	45	47	
P0_06	General-Purpose I/O port	46	48	
P0_07	General-Purpose I/O port	47	49	
P0_08	General-Purpose I/O port	48	50	
P0_09	General-Purpose I/O port	49	51	
P0_10	General-Purpose I/O port	50	52	
P0_11	General-Purpose I/O port	51	53	
P0_12	General-Purpose I/O port	54	56	
P0_13	General-Purpose I/O port	55	57	
P0_14	General-Purpose I/O port	56	58	
P0_15	General-Purpose I/O port	57	59	
P0_16	General-Purpose I/O port	58	60	
P0_17	General-Purpose I/O port	59	61	
P0_18	General-Purpose I/O port	32	32	
P0_19	General-Purpose I/O port	33	33	
P0_26	General-Purpose I/O port	82	84	
P0_27	General-Purpose I/O port	83	85	
P0_28	General-Purpose I/O port	84	86	
P0_30	General-Purpose I/O port	72	74	
P0_31	General-Purpose I/O port	75	77	
P1_00	General-Purpose I/O port	77	79	
P1_01	General-Purpose I/O port	76	78	
P1_02	General-Purpose I/O port	79	81	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
P1_03	General-Purpose I/O port	78	80	
P1_04	General-Purpose I/O port	69	71	
P1_05	General-Purpose I/O port	66	68	
P1_06	General-Purpose I/O port	68	70	
P1_07	General-Purpose I/O port	67	69	
P1_08	General-Purpose I/O port	70	72	
P1_09	General-Purpose I/O port	63	65	
P2_16	General-Purpose I/O port	170	178	
P2_17	General-Purpose I/O port	169	177	
P2_19	General-Purpose I/O port	159	165	
P2_22	General-Purpose I/O port	89	91	
P2_24	General-Purpose I/O port	-	92	
P2_25	General-Purpose I/O port	90	93	
P2_26	General-Purpose I/O port	91	94	
P2_27	General-Purpose I/O port	92	95	
P2_28	General-Purpose I/O port	-	96	
P2_29	General-Purpose I/O port	93	97	
P2_30	General-Purpose I/O port	94	98	
P2_31	General-Purpose I/O port	95	99	
P3_00	General-Purpose I/O port	96	100	
P3_01	General-Purpose I/O port	97	101	
P3_02	General-Purpose I/O port	98	102	
P3_03	General-Purpose I/O port	99	103	
P3_04	General-Purpose I/O port	100	104	
P3_05	General-Purpose I/O port	101	105	
P3_06	General-Purpose I/O port	102	106	
P3_07	General-Purpose I/O port	160	166	
P3_08	General-Purpose I/O port	161	167	
P3_09	General-Purpose I/O port	162	168	
P3_10	General-Purpose I/O port	-	169	
P3_11	General-Purpose I/O port	-	170	
P3_12	General-Purpose I/O port	163	171	
P3_13	General-Purpose I/O port	164	172	
P3_14	General-Purpose I/O port	165	173	
P3_15	General-Purpose I/O port	166	174	
P3_16	General-Purpose I/O port	167	175	
P3_17	General-Purpose I/O port	168	176	
P3_18	General-Purpose I/O port	118	122	
P3_19	General-Purpose I/O port	-	123	
P3_20	General-Purpose I/O port	-	124	
P3_21	General-Purpose I/O port	127	133	
P3_22	General-Purpose I/O port	128	134	
P3_23	General-Purpose I/O port	129	135	
P3_24	General-Purpose I/O port	130	136	
P3_25	General-Purpose I/O port	131	137	
P3_26	General-Purpose I/O port	132	138	
P3_27	General-Purpose I/O port	133	139	
P3_28	General-Purpose I/O port	134	140	
P3_29	General-Purpose I/O port	137	143	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
P3_30	General-Purpose I/O port	138	144	
P3_31	General-Purpose I/O port	139	145	
P4_00	General-Purpose I/O port	140	146	
P4_01	General-Purpose I/O port	141	147	
P4_02	General-Purpose I/O port	142	148	
P4_03	General-Purpose I/O port	143	149	
P4_04	General-Purpose I/O port	144	150	
P4_05	General-Purpose I/O port	147	153	
P4_06	General-Purpose I/O port	148	154	
P4_07	General-Purpose I/O port	149	155	
P4_08	General-Purpose I/O port	150	156	
P4_09	General-Purpose I/O port	151	157	
P4_10	General-Purpose I/O port	152	158	
P4_11	General-Purpose I/O port	153	159	
P4_12	General-Purpose I/O port	154	160	
P4_25	General-Purpose I/O port	204	212	
P4_26	General-Purpose I/O port	205	213	
P4_27	General-Purpose I/O port	206	214	
P4_28	General-Purpose I/O port	207	215	
P4_29	General-Purpose I/O port	174	182	
P4_30	General-Purpose I/O port	175	183	
P4_31	General-Purpose I/O port	176	184	
P5_00	General-Purpose I/O port	177	185	
P5_01	General-Purpose I/O port	178	186	
P5_02	General-Purpose I/O port	179	187	
P5_03	General-Purpose I/O port	180	188	
P5_04	General-Purpose I/O port	181	189	
P5_05	General-Purpose I/O port	186	194	
P5_06	General-Purpose I/O port	187	195	
P5_07	General-Purpose I/O port	188	196	
P5_08	General-Purpose I/O port	189	197	
P5_09	General-Purpose I/O port	190	198	
P5_10	General-Purpose I/O port	191	199	
P5_11	General-Purpose I/O port	192	200	
P5_12	General-Purpose I/O port	193	201	
P5_13	General-Purpose I/O port	196	204	
P5_14	General-Purpose I/O port	197	205	
P5_15	General-Purpose I/O port	198	206	
P5_16	General-Purpose I/O port	199	207	
P5_17	General-Purpose I/O port	200	208	
P5_18	General-Purpose I/O port	201	209	
P5_19	General-Purpose I/O port	202	210	
P5_20	General-Purpose I/O port	203	211	
P5_21	General-Purpose I/O port	31	31	
P5_22	General-Purpose I/O port	60	62	
P5_27	General-Purpose I/O port	34	34	
P5_28	General-Purpose I/O port	35	35	
P5_29	General-Purpose I/O port	36	36	
P5_30	General-Purpose I/O port	37	37	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
P5_31	General-Purpose I/O port	38	38	
P6_00	General-Purpose I/O port	39	39	
EP	Exposed Pad	-	-	Connect the exposed pad to ground. The exposed pad is isolated with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

6.2 Remark

Notes:

- *The port description list shows the port function of description, which is mounted and supported on the product. The function, which is not described in this table, is not supported and assured.*
- *See the function list of the product as well.*

7. Precautions and Handling Devices

7.1 Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

7.1.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

7.1.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 ˚C and 30 ˚C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 ˚C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.1.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7.2 Handling Devices

For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

About Handling Unused Pins

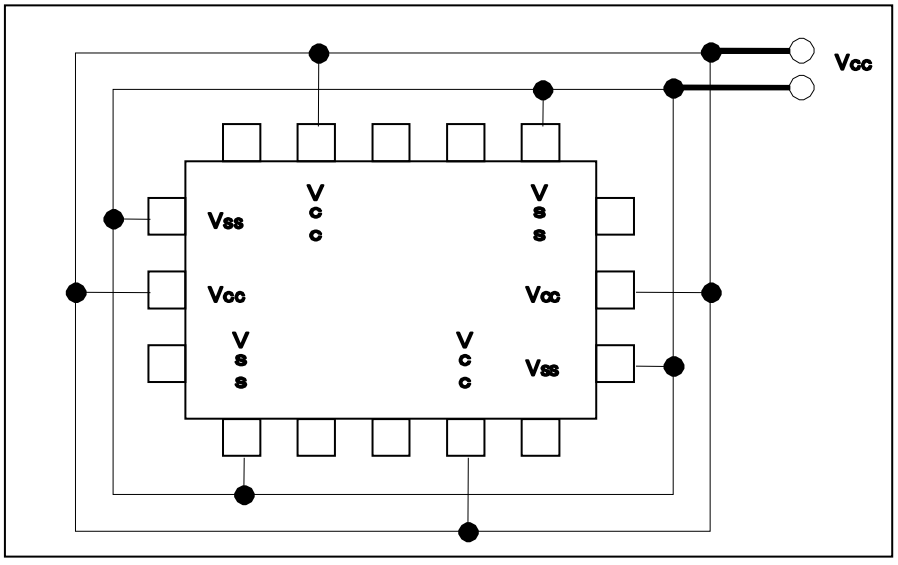
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kΩ or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 7-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device.

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

About the Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

Point to Note during PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that AVCC=AVRH=VCC and AVSS=VSS.

Points to Note about Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AVCC, AVRH, and AVSS) and analog inputs (AN0 to AN63) of an A/D converter.
At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AVCC. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

Method to Switch off VCC12 during Power-off Sequence

□ For revision M, P

During power-off sequence, it is necessary to switch off VCC12 by driving PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, RSTX needs to be asserted before switching off VCC12 to inactivate the operation of VCC12 supplied domain below the operation assurance range.

□ For except revision M, P

During power-off sequence, it is necessary to switch off VCC12 by driving PSC1 pin low by entering PSS mode (power domain 2 off). If VCC12 needs to be switched off by other means, VCC5 needs ramping down to occur LVDH1 reset before switching off VCC12 to inactivate the operation of VCC12 supplied domain below the operation assurance range.

About C Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (refer to the pin assignment) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet.

Precautions on Designing a Mounting Substrate

Measures against heat generation from the package must be taken for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad.

Notes on Writing to a Register Containing a Status Flag

In writing to a register containing a status flag (particularly an interrupt request flag, etc.) to control a function, it is important to take care not to accidentally clear the status flag.
Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.
Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

8. Electric Characteristics

8.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	$V_{CC}5$	V_{SS}-0.3	V_{SS}+6.0	V	
	$V_{CC}53$	V_{SS}-0.3	V_{SS}+6.0	V	$V_{CC}53 \leq V_{CC}5$
	$V_{CC}3$	V_{SS}-0.3	V_{SS}+4.0	V	$V_{CC}3 \leq V_{CC}5$
	DV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	$DV_{CC} \leq V_{CC}5$
	$V_{CC}12$	V_{SS}-0.3	V_{SS}+1.8	V	$V_{CC}12 \leq V_{CC}53$ $V_{CC}12 \leq V_{CC}3$ $V_{CC}12 \leq DV_{CC}$ $V_{CC}12 \leq AV_{CC}5$
Analog supply voltage*1, *2	$AV_{CC}5$	V_{SS}-0.3	V_{SS}+6.0	V	$AV_{CC}5 \leq V_{CC}5$
	$AV_{CC}3$_DAC	V_{SS}-0.3	V_{SS}+4.0	V	for DAC
	$V_{CC}3$_LVDS_Tx	V_{SS}-0.3	V_{SS}+4.0	V	for LVDS
	$AV_{CC}3$_LVDS_PLL	V_{SS}-0.3	V_{SS}+4.0	V	for LVDS PLL
Analog reference voltage*1	AVRH5	V_{SS}-0.3	V_{SS}+6.0	V	$AVRH5 \leq AV_{CC5}$
Input voltage*1	V_{I1}	V_{SS}-0.3	V_{CC5}+0.3	V	5-V pins not shared SMC
	V_{I2}	V_{SS}-0.3	DV_{CC}+0.3	V	5-V pins shared SMC
	V_{I3}	V_{SS}-0.3	V_{CC3}+0.3	V	3-V pins
	V_{IE}	V_{SS}-0.3	V_{CC53}+0.3	V	5-V/3-V pins
Input voltage for shared ADC*1	V_{IA1}	V_{SS}-0.3	V_{CC5}+0.3 AV_{CC5}+0.3	V	5-V pins not shared SMC
	V_{IA2}	V_{SS}-0.3	DV_{CC}+0.3 AV_{CC5}+0.3	V	5-V pins shared SMC
Output voltage*1	V_{O1}	V_{SS}-0.3	V_{CC5}+0.3	V	5-V pins not shared SMC*13
	V_{O2}	V_{SS}-0.3	DV_{CC}+0.3	V	5-V pins shared SMC*13
	V_{O3}	V_{SS}-0.3	V_{CC3}+0.3	V	3-V pins
	V_{O4}	V_{SS}-0.3	V_{CC53}+0.3	V	5-V/3-V pins
Maximum clamp current	$\|I_{CLAMP}\|$	-	4	mA	*12, *A
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*12, *A
"L"-level maximum output current*3	I_{OL1}	-	3.5	mA	When setting is 1 mA*6, *7, *8
	I_{OL2}	-	7	mA	When setting is 2 mA*6, *7, *8, *9
	I_{OL3}	-	10	mA	When setting is 5 mA*6, *7, *8, *9
	I_{OL4}	-	16	mA	When setting is 10 mA*9
	I_{OL5}	-	30	mA	When setting is 20 mA*9
	I_{OL6}	-	40	mA	When setting is 30 mA*7
	I_{OL7}	-	8	mA	When setting is 3 mA *10
	I_{OL8}	-	11	mA	When setting is 6 mA *11

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"L"-level average output current*4	I_{OLAV1}	-	1	mA	When setting is 1 mA*6, *7, *8
	I_{OLAV2}	-	2	mA	When setting is 2 mA*6, *7, *8, *9
	I_{OLAV3}	-	5	mA	When setting is 5 mA*6, *7, *8, *9
	I_{OLAV4}	-	10	mA	When setting is 10 mA*9
	I_{OLAV5}	-	20	mA	When setting is 20 mA*9
	I_{OLAV6}	-	30	mA	When setting is 30 mA*7
	I_{OLAV7}	-	3	mA	When setting is 3 mA *10
	I_{OLAV8}	-	6	mA	When setting is 6 mA *11
"L"-level total output current*5	ΣI_{OL1}	-	50	mA	*6, *10
	ΣI_{OL2}	-	250	mA	*7
	ΣI_{OL3}	-	50	mA	*8
	ΣI_{OL4}	-	50	mA	*9, *11
"H"-level maximum output current*3	I_{OH1}	-	-3.5	mA	When setting is 1 mA*6, *7, *8
	I_{OH2}	-	-7	mA	When setting is 2 mA*6, *7, *8, *9
	I_{OH3}	-	-10	mA	When setting is 5 mA*6, *7, *8, *9
	I_{OH4}	-	-16	mA	When setting is 10 mA*9
	I_{OH5}	-	-30	mA	When setting is 20 mA*9
	I_{OH6}	-	-40	mA	When setting is 30 mA*7
	I_{OH8}	-	-11	mA	When setting is 6 mA *11
"H"-level average output current*4	I_{OHAV1}	-	-1	mA	When setting is 1 mA*6, *7, *8
	I_{OHAV2}	-	-2	mA	When setting is 2 mA*6, *7, *8, *9
	I_{OHAV3}	-	-5	mA	When setting is 5 mA*6, *7, *8, *9
	I_{OHAV4}	-	-10	mA	When setting is 10 mA*9
	I_{OHAV5}	-	-20	mA	When setting is 20 mA*9
	I_{OHAV6}	-	-30	mA	When setting is 30 mA*7
	I_{OHAV8}	-	-6	mA	When setting is 6 mA *11
"H"-level total output current*5	ΣI_{OH1}	-	-50	mA	*6, *10
	ΣI_{OH2}	-	-250	mA	*7
	ΣI_{OH3}	-	-50	mA	*8
	ΣI_{OH4}	-	-50	mA	*9, *11
Power dissipation and Operation temperature Case 1	P_D	-	3300	mW	-
	T_A	-40	+97	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and Operation temperature Case 2	P_D	-	3150	mW	-
	T_A	-40	+100	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and Operation temperature Case 3	P_D	-	3000	mW	-
	T_A	-40	+102	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and Operation temperature Case 4	P_D	-	2900	mW	-
	T_A	-40	+105	°C	Both should be satisfied.
	T_C	-40	+144	°C	
Power dissipation and Operation temperature Case 5	P_D	-	2800	mW	-
	T_A	-40	+105	°C	Both should be satisfied.
	T_C	-40	+144	°C	

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
System Thermal Resistance	Theta j-a	-	16	°C/W	The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at Operation Assurance Condition.
Package Thermal Resistance	Theta j-c	-	7.5	°C/W	-
Storage temperature	Tstg	-55	+150	°C	-

*1: These parameters are based on the condition that VSS=AVSS=DVSS=0.0 V.

*2: Take care that DVCC, AVCC5 do not exceed VCC5 at, for example, the power-on time.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Output of 5-V pins.

*7: Output of SMC pins.

*8: Output of 5-V/3-V pins.

*9: Output of 3-V pins.

*10: Output of I^2C.

*11: Output of Media LB pins

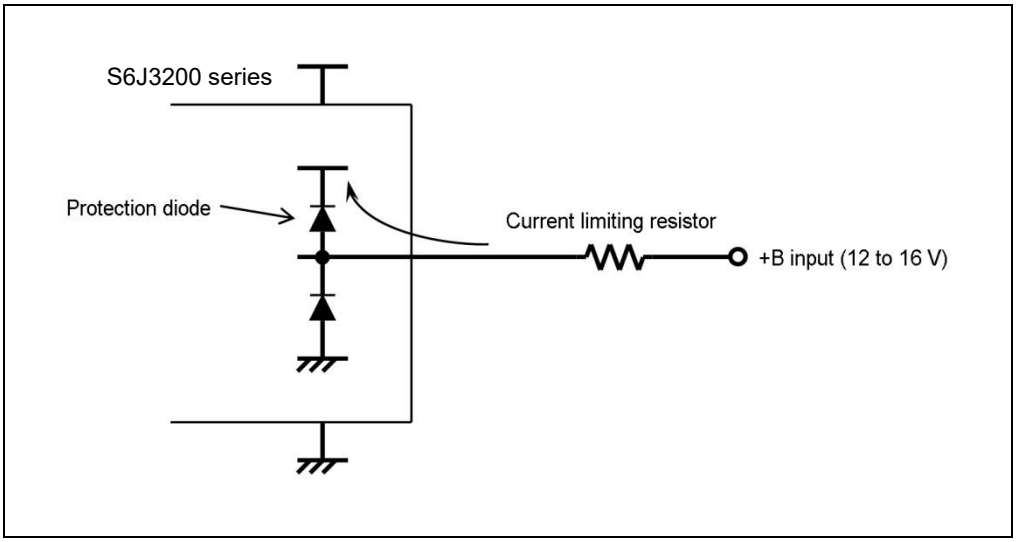
*12: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.

*13: Take care that the output voltage does not exceed AVCC5 + 0.3 V because ADC Analog input pins (AN0-49) are internally connected to the analog elements.

*A: Relevant pins: All general-purpose ports and analog input pins

- Corresponding pins: all general-purpose ports
- Use within the operation assurance condition (See 8.2. Operation Assurance Condition).
- Use at DC voltage (current).
- The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Example of a recommended circuit



WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

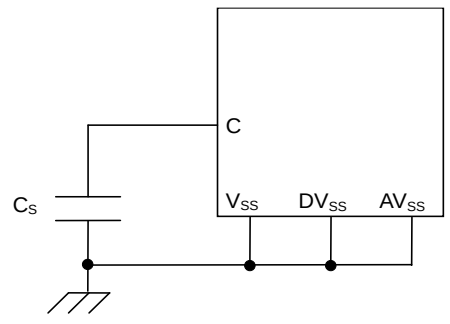
8.2 Operation Assurance Condition

Parameter	Symbol		Value		Unit	Remarks
	Power Supply	Corresponding Ground	Min	Max		
Supply voltage	V_{CC5}	V_{SS}	4.5	5.5	V	Specified electric characteristics are assured in this range.
	V_{CC53}*1	V_{SS}	4.5	5.5	V	
			3.0	3.6	V	
	DV_{CC}	DV_{SS}	4.5	5.5	V	
	AV_{CC5}	AV_{SS}	4.5	5.5	V	
	V_{CC3}	V_{SS}	3.0	3.6	V	
	V_{CC12}	V_{SS}	1.15*2	1.3	V	
			1.1	1.3	V	
	AV_{CC3}_DAC	AV_{SS3}_DAC	3.0	3.6	V	
	V_{CC3}_LVDS_Tx	V_{SS3}_LVDS_Tx	3.0	3.6	V	
	AV_{CC3}_LVDS_PLL	AV_{SS3}_LVDS_PLL	3.0	3.6	V	
	V_{CC5}	V_{SS}	3.5	5.5	V	Specified electric characteristics are NOT assured in this range.
	V_{CC53}*1	V_{SS}	2.7	5.5	V	
	DV_{CC}	DV_{SS}	3.5	5.5	V	
	AV_{CC5}	AV_{SS}	3.5	5.5	V	
	V_{CC3}	V_{SS}	2.7	3.6	V	
	AV_{CC3}_DAC	AV_{SS3}_DAC	2.7	3.6	V	
	V_{CC3}_LVDS_Tx	V_{SS3}_LVDS_Tx	2.7	3.6	V	
	AV_{CC3}_LVDS_PLL	AV_{SS3}_LVDS_PLL	2.7	3.6	V	
Smoothing capacitor*3	C_S	-	4.7		µF	Tolerance of up to ±40%
Operating temperature	T_A	-	-40	+105	°C	See the notes below.
	T_C	-	-40	+144	°C	

Notes:

- **1. $V_{CC}53$ should be connected with either $V_{CC}5$ or $V_{CC}3$ on your system board because LVD does not support $V_{CC}53$ itself.*
- **2. The value is only applied to the product series with revision digit A.*
- **3. For the connections of smoothing capacitor C_S, see the following diagram.*
- *Power supply sequence is recommended as*
  VCC5 ➔ [DVCC or AVCC5 or VCC3 or AVCC3] ➔ VCC12 ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
  VCC5 ➔ [AVCC5 or DVCC] ➔ [VCC12 or VCC3 or AVCC3_DAC] ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
  VCC5 ➔ AVCC5 ➔ [DVCC or VCC12 or VCC3 or AVCC3_DAC] ➔ [AVCC3_LVDS_PLL or VCC3_LVDS_TX]
- *Note that power supplies inside "[ ]" can be turned on in arbitrary order.*

C Pin Connection Diagram



WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this datasheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

Notes:

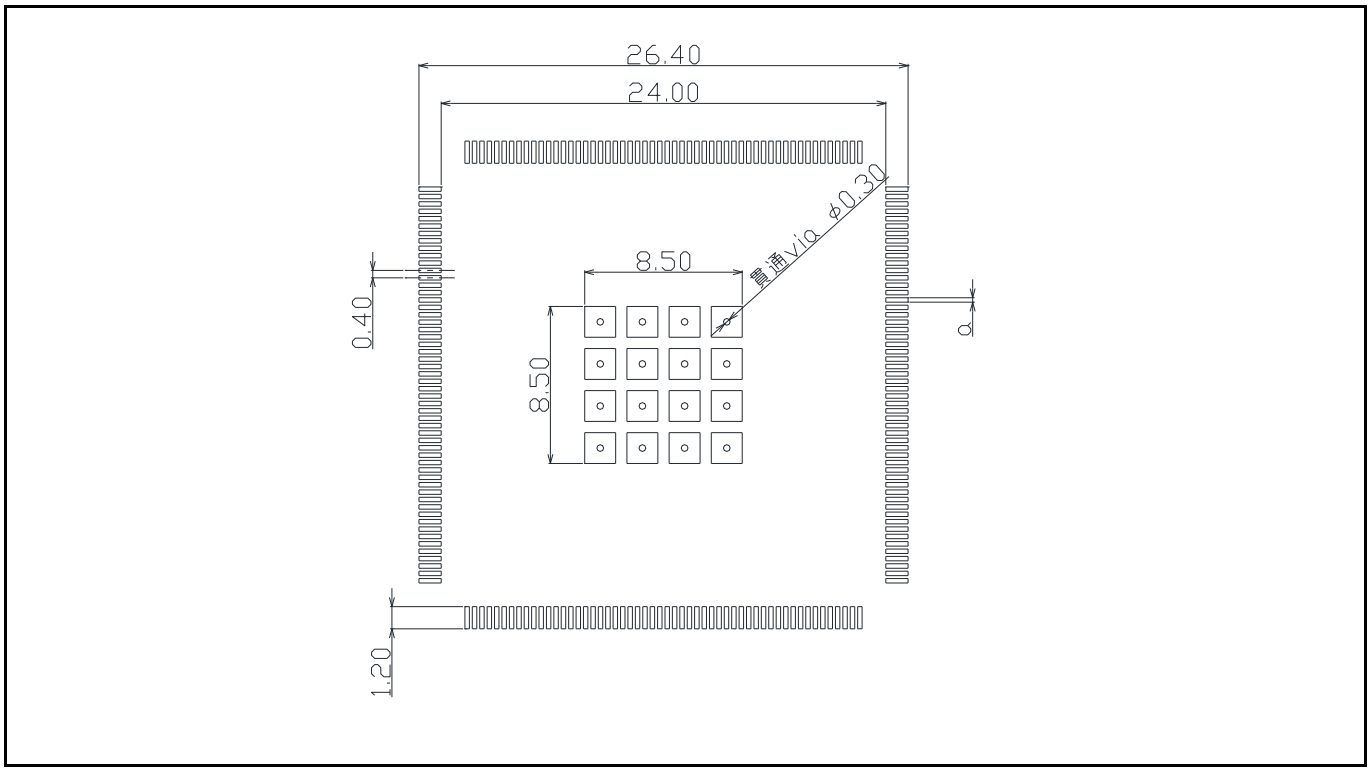
- *T_A: Ambient temperature (JEDEC)*
- *T_C: Case temperature (JEDEC), the maximum measured temperature of package case top.*
- *Both rating of T_A and T_C should simultaneously be satisfied as maximum operation temperature.*
- *The following condition should be satisfied in order to facilitate heat dissipation.*
    1. *Four or more layers PCB should be used.*
    2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
    3. *One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.*
    4. *35% or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
    5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Figure 8-1: Example Thermal Via Holes on PCB

Notes:

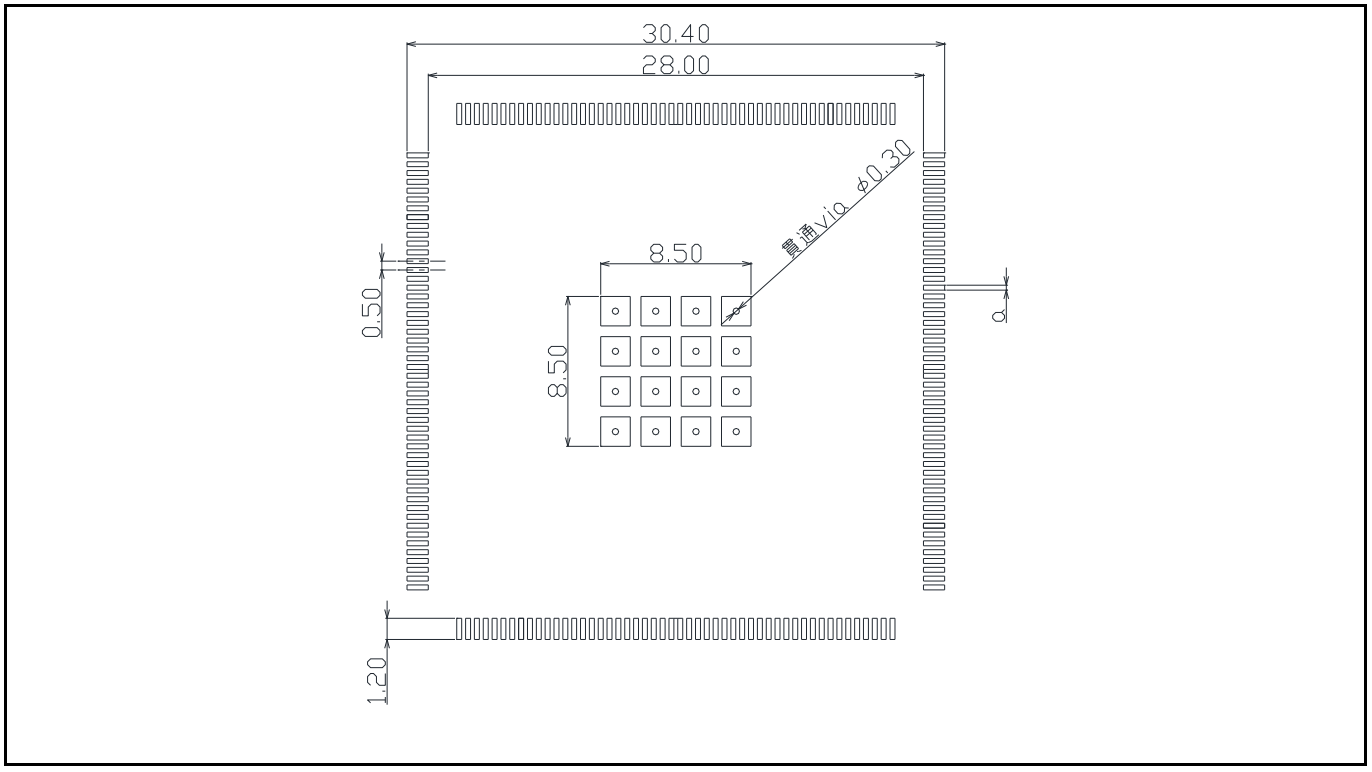
- *Figure 8-1 is a schematic diagram showing PCB in section.*
- *Figure 8-2, Figure 8-3, and Figure 8-4 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.*
- *When thermal via holes cannot be with lands, the followings are recommended as represented by Figure 8-5 which is an example for LEQ216.*
- *(1). Increase pattern area size as much as possible inside the package outline.*
- *(2). Place thermal via holes to be with lands as close as possible.*
- *0.25 mm $\leq a \leq$ 0.30 mm in Figure 8-1, Figure 8-2, Figure 8-3, and Figure 8-4*
- *It is recommended to connect the land pattern to the VSS-ground level (GND plan of inner layer bellow the MCU) as thermal heat sink.*

Figure 8-2: Land Pattern and Thermal Via LEQ216



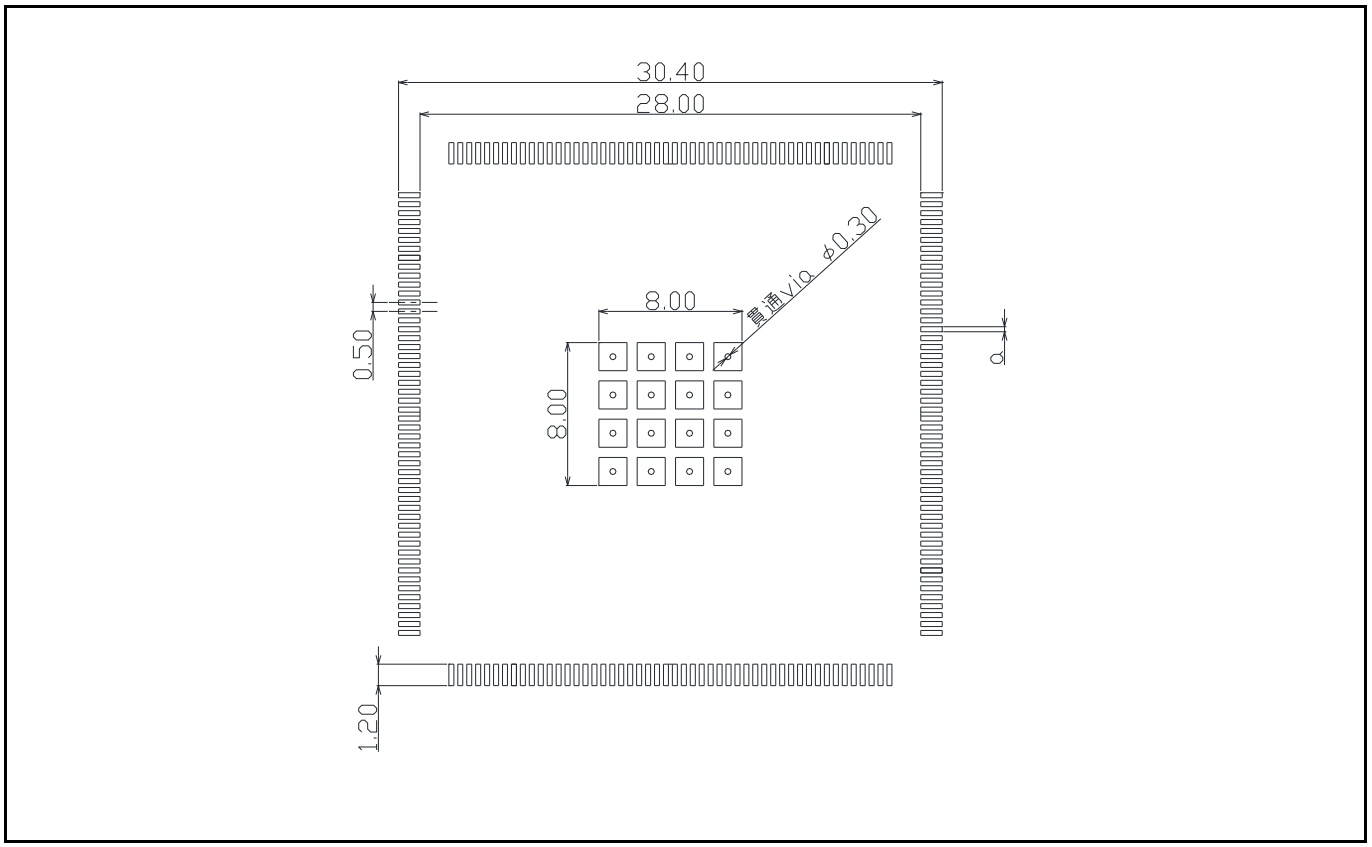
0.25 mm ≤ a ≤ 0.30 mm

Figure 8-3: Land Pattern and Thermal Via LET208



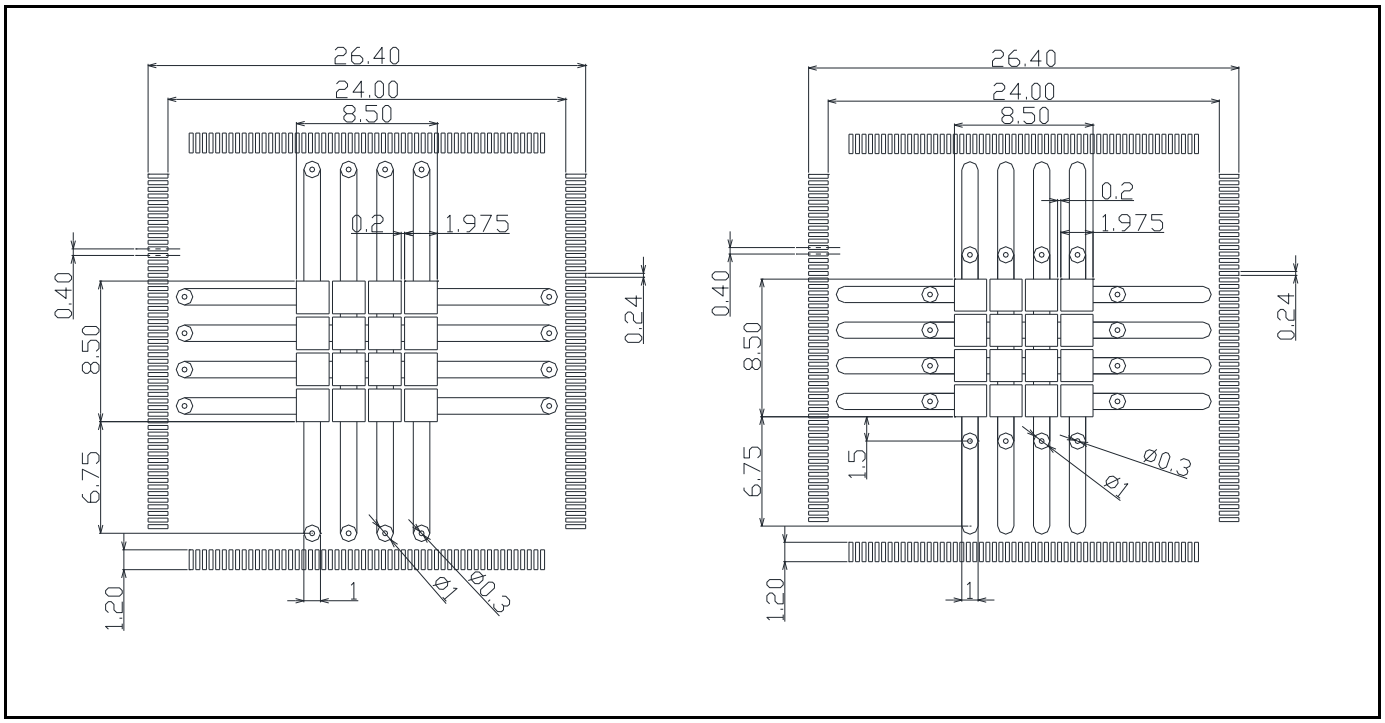
0.25 mm ≤ a ≤ 0.30 mm

Figure 8-4: Land Pattern and Thermal Via LER208



0.25 mm ≤ a ≤ 0.30 mm

Figure 8-5: Optional Land Pattern



0.25 mm ≤ a ≤ 0.30 mm

8.3 DC Characteristics

8.3.1 Port Function Characteristics

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level Input voltage	V_{IH1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	CMOS hysteresis input level is selected	$0.7 \times V_{C53}$	-	$V_{CC53}+0.3$	V	
	V_{IH2}		Automotive input level is selected	$0.8 \times V_{C53}$	-	$V_{CC53}+0.3$	V	
	V_{IH3}		TTL input level is selected	2.0	-	$V_{CC53}+0.3$	V	
	V_{IH4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 19	CMOS hysteresis input level is selected	$0.7 \times V_{C5}$	-	$V_{CC5}+0.3$	V	*1
	V_{IH5}		Automotive input level is selected	$0.8 \times V_{C5}$	-	$V_{CC5}+0.3$	V	*1
	V_{IH6}	P2_25, 26, P3_00, 01	TTL input level is selected	2.0	-	$V_{CC5}+0.3$	V	
	V_{IH7}	RSTX NMIX	-	$0.7 \times V_{C5}$	-	$V_{CC5}+0.3$	V	
	V_{IH8}	MD	-	$0.7 \times V_{C5}$	-	$V_{CC5}+0.3$	V	
	V_{IH9}	JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS	-	2.3	-	$V_{CC5}+0.3$	V	
	V_{IH10}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	CMOS hysteresis input level is selected	$0.7 \times V_{C3}$	-	$V_{CC3}+0.3$	V	
	V_{IH11}	P0_00 to 19, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	TTL input level is selected	2.0	-	$V_{CC3}+0.3$	V	
	V_{IH12}	P0_26 to 28	-	1.8	-	$V_{CC3}+0.3$	V	MediaLB

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level Input voltage	V_{IL1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3× V_{CC53}	V	
	V_{IL2}		Automotive input level is selected	V_{SS}-0.3	-	0.5× V_{CC53}	V	
	V_{IL3}		TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 19	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3× V_{CC5}	V	*1
	V_{IL5}		Automotive input level is selected	V_{SS}-0.3	-	0.5× V_{CC5}	V	*1
	V_{IL6}	P2_25, 26, P3_00, 01	TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL7}	RSTX NMIX	-	V_{SS}-0.3	-	0.3× V_{CC5}	V	
	V_{IL8}	MD	-	V_{SS}-0.3	-	0.3× V_{CC5}	V	
	V_{IL9}	JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS	-	V_{SS}-0.3	-	0.8	V	
	V_{IL10}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	CMOS hysteresis input level is selected	V_{SS}-0.3	-	0.3× V_{CC3}	V	
	V_{IL11}	P0_00 to 19, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	TTL input level is selected	V_{SS}-0.3	-	0.8	V	
	V_{IL12}	P0_26 to 28	-	V_{SS}-0.3	-	0.7	V	MediaLB

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Hysteresis voltage	V_{HYS1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	CMOS hysteresis input level is selected	-	0.158× V_{CC53}	-	V	
	V_{HYS2}		Automotive input level is selected	-	0.104× V_{CC53}	-	V	
	V_{HYS3}		TTL input level is selected	-	0.032× V_{CC53}	-	V	
	V_{HYS4}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 19	CMOS hysteresis input level is selected	-	0.158× V_{CC5}	-	V	
	V_{HYS5}		Automotive input level is selected	-	0.104× V_{CC5}	-	V	
	V_{HYS6}	P2_25, 26, P3_00, 01	TTL input level is selected	-	0.032× V_{CC5}	-	V	
	V_{HYS7}	RSTX NMIX	-	-	0.158× V_{CC5}	-	V	
	V_{HYS8}	MD	-	-	0.158× V_{CC5}	-	V	
	V_{HYS9}	JTAG_NTRST JTAG_TCK JTAG_TDI JTAG_TMS	-	-	0.032× V_{CC5}	-	V	
	V_{HYS10}	P0_26 to 28, 30, 31, P1_00 to 09, P5_21, 22 P6_01	CMOS hysteresis input level is selected	-	0.188× V_{CC3}	-	V	
	V_{HYS11}	P0_30, 31, P1_00 to 09, P5_21, 22, P6_01	TTL input level is selected	-	0.164× V_{CC3}	-	V	
	V_{HYS12}	P0_26 to 28	-	-	0.124× V_{CC3}	-	V	MediaLB

*1: P3_21 to P3_31, P4_00 to P4_12 and P6_9 to P6-16 are supplied with power by DVCC.

(Condition: See 8.2. Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	$V_{CC}53$=3.0 V I_{OH}=-0.5 mA	$V_{CC}53$ - 0.5	-	$V_{CC}53$	V	
	V_{OH2}		$V_{CC}53$=3.0 V I_{OH}=-1.0 mA	$V_{CC}53$ - 0.5	-	$V_{CC}53$	V	
	V_{OH3}		V_{CC53}=3.0 V I_{OH}=-2.0 mA	$V_{CC}53$ - 0.5	-	$V_{CC}53$	V	
	V_{OH4}	P2_16, 17, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 19	$V_{CC}5$=4.5 V I_{OH}=-1.0 mA	$V_{CC}5$ - 0.5	-	$V_{CC}5$	V	*1
	V_{OH5}		$V_{CC}5$=4.5 V I_{OH}=-2.0 mA	$V_{CC}5$ - 0.5	-	$V_{CC}5$	V	*1
	V_{OH6}		V_{CC5}=4.5 V I_{OH}=-5.0 mA	$V_{CC}5$ - 0.5	-	$V_{CC}5$	V	*1
	V_{OH7}	PSC_1	V_{CC5}=4.5 V I_{OH}=-2.0 mA	V_{CC5} - 0.5	-	$V_{CC}5$	V	
	V_{OH8}	JTAG_TDO	$V_{CC}5$=4.5 V I_{OH}=-5.0 mA	V_{CC5} - 0.5	-	$V_{CC}5$	V	
	V_{OH10}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC}=4.5 V I_{OH}=-30.0 mA	DV_{CC} - 0.5	-	DV_{CC}	V	SMC
	V_{OH11}		DV_{CC}=4.5 V I_{OH}=-40.0 mA	DV_{CC} - 0.5	-	DV_{CC}	V	SMC Tj=-40°C
	V_{OH12}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	$V_{CC}3$=3.0 V I_{OH}=-2.0 mA	V_{CC3} - 0.5	-	$V_{CC}3$	V	
	V_{OH13}		$V_{CC}3$=3.0 V I_{OH}=-5.0 mA	V_{CC3} - 0.5	-	$V_{CC}3$	V	
	V_{OH14}		V_{CC3}=3.0 V I_{OH}=-10.0 mA	V_{CC3} - 0.5	-	$V_{CC}3$	V	
	V_{OH15}	P0_00 to 19, P5_21, 22, 27 to 31, P6_00, 01	V_{CC3}=3.0 V I_{OH}=-20.0 mA	V_{CC3} - 0.5	-	$V_{CC}3$	V	
	V_{OH16}	P0_26 to 28	$V_{CC}3$=3.0 V I_{OH}=-6.0 mA	2.0	-	$V_{CC}3$	V	MediaLB

(Condition: See 8.2. Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P4_25 to 31, P5_00 to 20, P6_20 to 26	V_{CC}53=3.0 V I_{OL}=0.5 mA	0	-	0.4	V	
	V_{OL2}		V_{CC}53=3.0 V I_{OL}=1.0 mA	0	-	0.4	V	
	V_{OL3}		VCC53=3.0 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL4}	P2_16, 17, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 19	V_{CC}5=4.5 V I_{OL}=1.0 mA	0	-	0.4	V	*1
	V_{OL5}		V_{CC}5=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	*1
	V_{OL6}		VCC5=4.5 V I_{OL}=5.0 mA	0	-	0.4	V	*1
	V_{OL7}	PSC_1	VCC5=4.5 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL8}	JTAG_TDO	V_{CC}5=4.5 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL9}	P2_25, 26, P3_00, 01	V_{CC}5=4.5 V I_{OL}=3.0 mA	0	-	0.4	V	I^2C
	V_{OL10}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC}=4.5 V I_{OL}=30.0 mA	0	-	0.55	V	SMC
	V_{OL11}		DV_{CC}=4.5 V I_{OL}=40.0 mA	0	-	0.55	V	SMC Tj=-40 °C
	V_{OL12}	P0_00 to 19, 26 to 28, 30, 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	V_{CC}3=3.0 V I_{OL}=2.0 mA	0	-	0.4	V	
	V_{OL13}		V_{CC}3=3.0 V I_{OL}=5.0 mA	0	-	0.4	V	
	V_{OL14}		VCC3=3.0 V I_{OL}=10.0 mA	0	-	0.4	V	
	V_{OL15}	P0_00 to 19, P5_21, 22, 27 to 31, P6_00, 01	VCC3=3.0 V I_{OL}=20.0 mA	0	-	0.4	V	
	V_{OL16}	P0_26 to 28	V_{CC}3=3.0 V I_{OL}=6.0 mA	0	-	0.4	V	MediaLB

*1: P3_21 to P3_31, P4_00 to P4_12 and P6_9 to P6-16 are supplied with power by DVCC.

(Condition: See 8.2. Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31	$V_{CC}5=V_{CC}53=DV_{CC}=AV_{CC}=5.5$ V $V_{SS} < VI < V_{CC}$	-5	-	+5	µA	5-V pins 5-V/3-V pins
		P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	$V_{CC}3=3.6$ V $V_{SS} < VI < V_{CC3}$	-10	-	+10	µA	3-V pins
Pull-up resistor	R_{UP1}	RSTX, NMIX	-	25	50	100	kΩ	
	R_{UP2}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31	Pull-up resistor Selected Vcc53 = 4.5 V to 5.5 V	25	50	100	kΩ	5-V pins 5-V/3-V pins
		P4_25 to 31, P5_00 to 20	Pull-up resistor Selected Vcc53 = 3.0 V to 3.6 V	40	100	200	kΩ	5-V/3-V pins
	R_{UP3}	P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	Pull-up resistor selected	17	33	66	kΩ	3-V pins
	R_{UP4}	JTAG_TDI, JTAG_TMS, JTAG_TCK	-	25	50	100	kΩ	
Pull-down resistor	R_{down1}	P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31,P5_00 to 20, P6_02 to 31	Pull-down resistor Selected Vcc53 = 4.5 V to 5.5 V	25	50	100	kΩ	5-V pins 5-V/3-V pins
		P4_25 to 31,P5_00 to 20	Pull-down resistor Selected Vcc53 = 3.0 V to 3.6 V	40	100	200	kΩ	5-V/3-V pins
	R_{down2}	P0_00 to 31, P1_00 to 09, P5_21, 22, 27 to 31, P6_00, 01	Pull-down resistor selected	17	33	66	kΩ	3-V pins
	R_{down3}	JTAG_NTRST	-	25	50	100	kΩ	
Input capacitance	C_{IN1}	P0_00 to 31, P1_00 to 09, P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P4_25 to 31, P5_00 to 20, P5_21 22, 27 to 31, P6_00 to 08, 17 to 26	-	-	5	15	pF	
	C_{IN2}	P3_21 to 31, P4_00 to 12, P6_09 to 16	-	-	15	45	pF	When using SMC

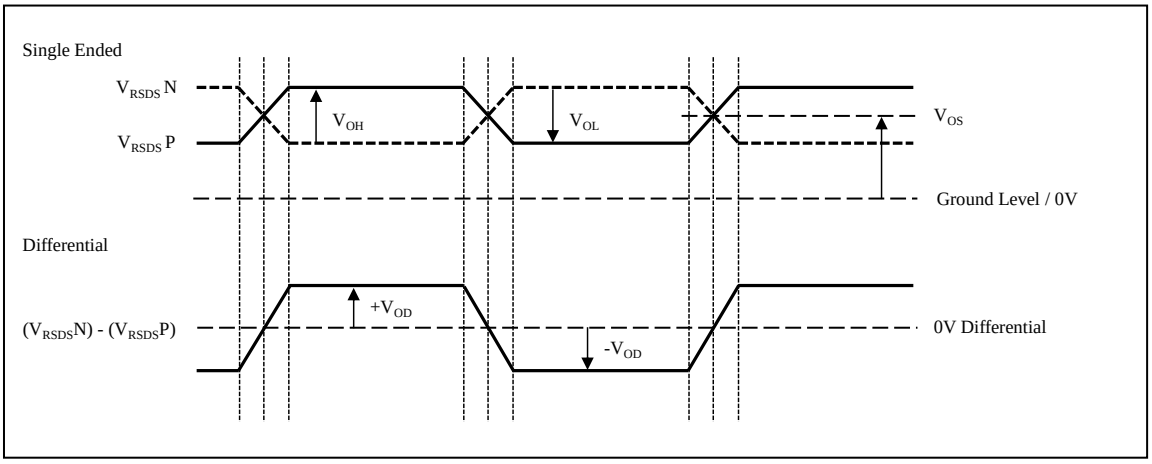
(Condition: See 8.2. Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	Delta-V_{OH8}	P3_21 to 31, P4_00 to 12, P6_09 to 16	DV_{CC}=4.5 V I_{OH}=-30.0 mA Maximum deviation of V_{OH8}	-	-	90	mV	*
High current output drive capacity Phase-to-phase deviation2	Delta-V_{OL8}		DV_{CC}=4.5 V I_{OL}= 30.0 mA Maximum deviation of V_{OL84}	-	-	90	mV	*
LCD divider resistor	R_{LCD}	V0 to V1, V1 to V2, V2 to V3	-	6.25	12.5	25	kΩ	
COM0 to COM3 output impedance	R_{VCOM}	COMm (m=0 to 3)	-	-	-	4.5	kΩ	
COM0 to COM3 output impedance	R_{VSEG}	SEGn (n=00 to 31)	-	-	-	17	kΩ	
LCDC leak current	I_{LCDC}	V0 to V3, COMm (m=0 to 3), SEGn (n=00 to 31)	T_A= + 25 °C	-0.5	-	+0.5	µA	

*: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH4} / V_{OL4} for each pin is defined. Same for other channels.

(Condition: See 8.2. Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output Differential Voltage	$\lvert V_{OD} \rvert$	DSP0_DATAn+, DSP0_DATAn- n=0 to 11	BOOST=0 (Drivability 2mA) R_L = 100 Ω	100	200	600	mV	
			BOOST=1 (Drivability 4mA) R_L = 50 Ω					
Output Offset Voltage	V_{OS}		BOOST=0 (Drivability 2mA) R_L = 100 Ω	0.5	1.2	1.5	V	
			BOOST=1 (Drivability 4mA) R_L = 50 Ω					



8.3.2 Power Supply Current

8.3.2.1 Run Mode

■This characteristic is specified for the series with the function digit 3, 4, 5, 6, 7, 8 and 9.

(Condition: See 8.2. Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
$I_{CC}5$	$V_{CC}5$	Normal Operation	45	-	mA	25	-
			-	70	mA	105	
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-
$I_{CC}12$	$V_{CC}12$	CPU:240 MHz, HPM:120 MHz, GDC 2D and 3D engine:200 MHz	820	-	mA	25	-
			-	1600	mA	105	
		CPU:240 MHz, HPM:120 MHz, GDC 2D engine only:200 MHz	700	-	mA	25	-
			-	1480	mA	105	
		CPU:120 MHz, HPM:60 MHz, GDC: 0 MHz For TC FLASH Programming or Erasing	-	1120	mA	105	-
		CPU:80 MHz, HPM:40 MHz, GDC: 0 MHz For TC FLASH Programming or Erasing	-	1040	mA	105	-
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-
ILVDS	$V_{CC}3$_ LVDS_Tx	50 MHz	-	56	mA	105	*1
	$AV_{CC}3$_ LVDS_PLL	50 MHz	-	7	mA	105	For revision F, J
			-	9	mA	105	For revision M, P

Notes:

- *The output port current is not included in the specified value *1.*

  A few mA which depends on usage for FPD-Link data transfer should be estimated for each port in an actual application, and then it should be added to the current consumption at Vcc3_LVDS_Tx.
- *The current consumption at Vcc3_LVDS_Tx is specified under R_L=100 Ω, C_L=5 pF, f=50 MHz, and 0/1 alternation pattern output.*

■This characteristic is specified for the series with the function digit B.

(Condition: See 8.2. Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
$I_{CC}5$	$V_{CC}5$	Normal Operation	45	-	mA	25	-
			-	70	mA	105	
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-
$I_{CC}12$	$V_{CC}12$	CPU:160 MHz, HPM:160 MHz, GDC 2D and 3D engine:160 MHz	880	-	mA	25	-
			-	1410	mA	105	
		CPU:120 MHz, HPM:60 MHz, GDC: 0 MHz For TC FLASH Programming or Erasing	-	1120	mA	105	-
		CPU:80 MHz, HPM:40 MHz, GDC: 0 MHz For TC FLASH Programming or Erasing	-	1040	mA	105	-
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-

■This characteristic is specified for the series with the function digit K, L, M, and N.

(Condition: See 8.2. Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
$I_{CC}5$	$V_{CC}5$	Normal Operation	45	-	mA	25	-
			-	70	mA	105	
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-
$I_{CC}12$	$V_{CC}12$	CPU:240 MHz, HPM:120 MHz, GDC 2D and 3D engine:200 MHz	822	-	mA	25	-
			-	1635	mA	105	
		CPU:240 MHz, HPM:120 MHz, GDC 2D engine only:200 MHz	702	-	mA	25	-
			-	1515	mA	105	
		CPU:120 MHz, HPM:60 MHz, GDC:0 MHz For TC FLASH Programming or Erasing	-	1155	mA	105	-
		CPU:80 MHz, HPM:40 MHz, GDC:0 MHz For TC FLASH Programming or Erasing	-	1075	mA	105	-
		Adder for Work Flash Programming or Erasing.	-	20	mA	105	-
ILVDS	$V_{CC}3$_ LVDS_Tx	50 MHz	-	56	mA	105	*1
	$AV_{CC}3$_ LVDS_PLL	50 MHz	-	9	mA	105	

Notes:

- *The output port current is not included in the specified value *1.*

  A few mA which depends on usage for FPD-Link data transfer should be estimated for each port in an actual application, and then it should be added to the current consumption at Vcc3_LVDS_Tx.

- *The current consumption at Vcc3_LVDS_Tx is specified under R_L=100 Ω, C_L=5 pF, f=50 MHz, and 0/1 alternation pattern output.*

8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF)

■This characteristic is specified for the series with the function digit 3, 4, 5, 6, 7, 8, 9, K, L, M, and N.

(Condition: See 8.2. Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCT5}	$V_{CC}5$	4 MHz Crystal for Main Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	350	600	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)
		4 MHz Crystal for Main Oscillator PD1=ON, PD4_0 or PD4_1=ON	345	575	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)
		4 MHz Crystal for Main Oscillator PD1=ON	340	550	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)
		8 MHz Crystal for Main Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	450	730	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)
		8 MHz Crystal for Main Oscillator PD1=ON, PD4_0 or PD4_1=ON	445	705	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)
		8 MHz Crystal for Main Oscillator PD1=ON	440	680	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)
		4 MHz External clock PD1=ON, PD4_0=ON, PD4_1=ON	180	400	µA	25	-
		4 MHz External Clock PD1=ON, PD4_0 or PD4_1=ON	175	375	µA	25	-
		4 MHz External Clock PD1=ON	170	350	µA	25	-
		8 MHz External clock PD1=ON, PD4_0=ON, PD4_1=ON	190	420	µA	25	-
		8 MHz External Clock PD1=ON, PD4_0 or PD4_1=ON	185	395	µA	25	-
		8 MHz External Clock PD1=ON	180	370	µA	25	-
		32 kHz Crystal for Sub Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	85	300	µA	25	-
		32 kHz Crystal for Sub Oscillator PD1=ON, PD4_0 or PD4_1=ON	80	275	µA	25	-
		32 kHz Crystal for Sub Oscillator PD1=ON	75	250	µA	25	-

Notes:

- *The values will be evaluated after engineering samples release.*
- *The values have been standardized with regulator standby mode (RMSEL=1).*

■This characteristic is specified for the series with the function digit B.

(Condition: See 8.2.Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCT5}	$V_{CC}5$	4 MHz Crystal for Main Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	350	650	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)
		4 MHz Crystal for Main Oscillator PD1=ON, PD4_0 or PD4_1=ON	345	615	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)
		4 MHz Crystal for Main Oscillator PD1=ON	340	590	µA	25	C_L=10 pF MCGAIN=0b00(4 MHz)-
		8 MHz Crystal for Main Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	450	775	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)
		8 MHz Crystal for Main Oscillator PD1=ON, PD4_0 or PD4_1=ON	445	750	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)-
		8 MHz Crystal for Main Oscillator PD1=ON	440	725	µA	25	C_L=10 pF MCGAIN=0b01(8 MHz)-
		32 kHz Crystal for Sub Oscillator PD1=ON, PD4_0=ON, PD4_1=ON	85	345	µA	25	-
		32 kHz Crystal for Sub Oscillator PD1=ON, PD4_0 or PD4_1=ON	80	320	µA	25	-
		32 kHz Crystal for Sub Oscillator PD1=ON	75	295	µA	25	-

Notes:

- *The values will be evaluated after engineering samples release.*
- *The values have been standardized with regulator standby mode (RMSEL=1).*

8.3.2.3 PSS Stop Mode Shutdown

■This characteristic is specified for the series with the function digits 3, 4, 5, 6, 7, 8, 9, K, L, M, and N.

(Condition: See 8.2.Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCH5}	$V_{CC}5$	PD1=ON, PD4_0=ON, PD4_1=ON	65	270	µA	25	-
		PD1=ON, PD4_0 or PD4_1=ON	60	245	µA	25	-
		PD1=ON	55	220	µA	25	-

■This characteristic is specified for the series with the function digits B.

(Condition: See 8.2.Operation Assurance Condition)

Symbol	Pin Name	Conditions	Value		Unit	T_A (°C)	Remark
			Typ	Max			
I_{CCH5}	$V_{CC}5$	PD1=ON, PD4_0=ON, PD4_1=ON	65	315	µA	25	-
		PD1=ON, PD4_0 or PD4_1=ON	60	290	µA	25	-
		PD1=ON	55	265	µA	25	-

Notes:

- *The values will be evaluated after engineering samples release.*
- *The values have been standardized with regulator standby mode (RMSEL=1).*

8.4 AC Characteristics

8.4.1 Source Clock Timing

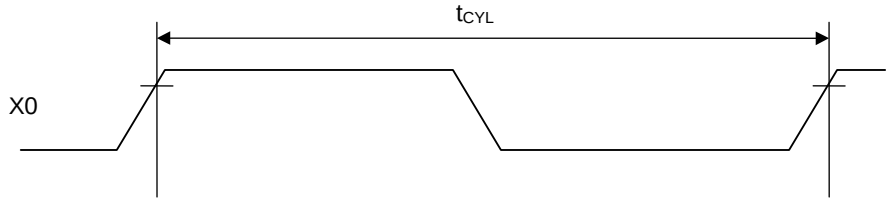
(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	3.6	-	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	62.5	-	277.8	ns	
CAN PLL jitter (when locked)	t_{PJ}	-	-	-1.5	-	1.5	ns	
Internal Slow CR oscillation frequency	F_{CRS}	-	-	50	100	150	kHz	
Internal Fast CR oscillation frequency	F_{CRF}	-	-	2.40	4.00	5.61	MHz	Before trim
				3.20	4.00	4.81	MHz	After trim

Notes:

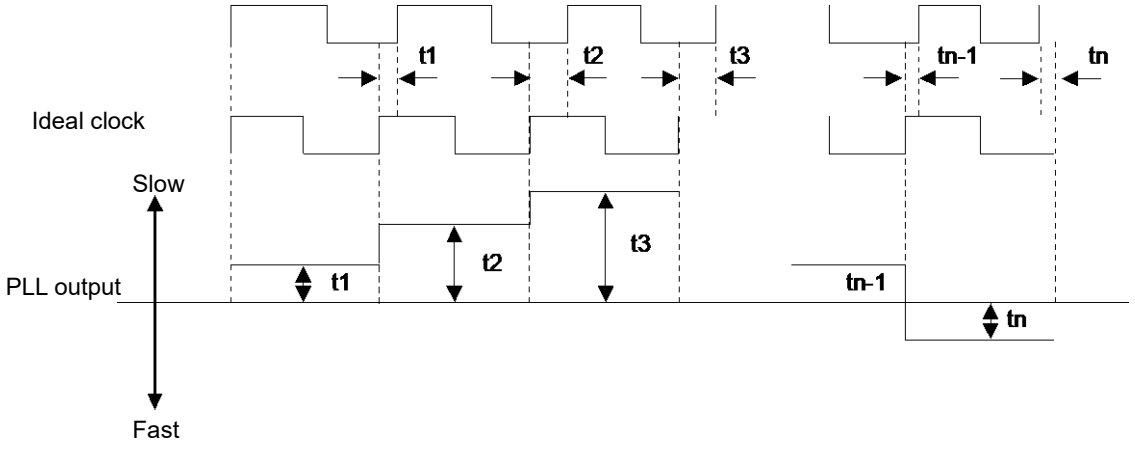
- *The maximum/minimum values have been standardized with the main clock and PLL clock in use.*
- *The error of source oscillator frequency must be smaller than 3000 ppm.*
- *Enough evaluation and adjustment are recommended using oscillator on your system board.*

- X0 and X1 clock timing



CAN PLL jitter

A time difference from the ideal clock is guaranteed for each cycle period within 20,000 cycles.

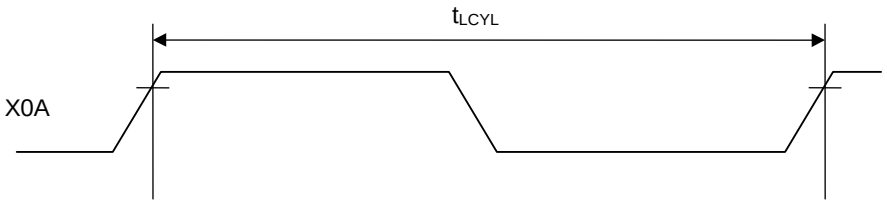


8.4.2 Sub Clock Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	-	-	30.52	-	µs	

- X0A and X1A clock timing



8.4.3 Internal Clock Timing

- This chapter shows the characteristics for internal clock timing at the current stage.
- In the column symbol, same clock names as described in CHAPTER 5: CLOCK SYSTEM of Platform hardware manual are used.
- Corresponding functions for these clocks are described in CHAPTER 5: CLOCK CONFIGURATION of S6J3200 series hardware manual.

(Condition: See 8.2.Operation Assurance Condition)

Table 8-1: Assured Combination of Clock Frequency

Symbol	Max Value Combination				Unit	Remarks
	Function digit 3, 4, 5, 6, 7, 8, 9, K, L, M, N			Function digit B		
	Max *1	Max *2	Max *3	Max *4		
F_{SSCG0}	232 (464)	200 (800)	160 (640)	160 (640)	MHz	SSCG0 output clock
F_{SSCG1}	200 (800)	200 (800)	200 (800)	200 (800)	MHz	SSCG1 output clock
F_{SSCG2}	200 (800)	200 (800)	200 (800)	160 (640)	MHz	SSCG2 output clock
F_{SSCG3}	400 (800)	400 (800)	400 (800)	400 (800)	MHz	SSCG3 output clock
F_{PLL0}	240 (480)	200 (800)	200 (800)	160 (640)	MHz	PLL0 output clock
F_{PLL1}	400 (800)	400 (800)	400 (800)	320 (640)	MHz	PLL1 output clock
F_{PLL2}	200 (800)	200 (800)	200 (800)	200 (800)	MHz	PLL2 output clock
F_{PLL3}	240 (480)	240 (480)	240 (480)	240 (480)	MHz	PLL3 output clock
F_{CLK_CPU0}	240	200	160	160	MHz	
F_{CLK_SHE}	240	200	160	160	MHz	
F_{CLK_FCLK}	80	66.7	80	80	MHz	
F_{CLK_ATB}	120	100	80	80	MHz	
F_{CLK_DBG}	120	100	80	80	MHz	
F_{CLK_HPM}	120	200	160	160	MHz	
F_{CLK_HPM2}	60	100	80	80	MHz	
F_{CLK_DMA}	120	200	160	160	MHz	
F_{CLK_MEMC}	120	200	160	160	MHz	
F_{CLK_EXTBUS}	40	40	40	40	MHz	Unused
F_{CLK_SYSC1}	40	40	40	40	MHz	
$F_{CLK_HAPP0A0}$	40	40	40	40	MHz	Unused
$F_{CLK_HAPP0A1}$	40	40	40	40	MHz	Unused
$F_{CLK_HAPP1B0}$	60	50	80	80	MHz	
$F_{CLK_HAPP1B1}$	40	40	40	40	MHz	Unused
F_{CLK_LLPBM}	240	200	160	160	MHz	
F_{CLK_LLPBM2}	120	100	80	80	MHz	
F_{CLK_LCP}	60	50	80	80	MHz	
F_{CLK_LCP0}	40	40	40	40	MHz	
F_{CLK_LCP0A}	60	66.7	80	80	MHz	
F_{CLK_LCP1}	40	40	40	40	MHz	Unused
F_{CLK_LCP1A}	60	66.7	80	80	MHz	
F_{CLK_LAPP0}	40	40	40	40	MHz	Unused
F_{CLK_LAPP0A}	40	40	40	40	MHz	Unused
F_{CLK_LAPP1}	40	40	40	40	MHz	Unused
F_{CLK_LAPP1A}	40	40	40	40	MHz	Unused
F_{CLK_TRC}	100	100	100	100	MHz	
F_{CLK_CD1}	400	400	400	400	MHz	
F_{CLK_CD1A0}	100	100	100	100	MHz	Unused
F_{CLK_CD1A1}	100	100	100	100	MHz	Unused

Symbol	Max Value Combination				Unit	Remarks
	Function digit 3, 4, 5, 6, 7, 8, 9, K, L, M, N			Function digit B		
	Max *1	Max *2	Max *3	Max *4		
F_{CLK_CD1B0}	100	100	100	100	MHz	Unused
F_{CLK_CD1B1}	100	100	100	100	MHz	Unused
F_{CLK_CD2}	400	400	400	320	MHz	Unused
F_{CLK_CD2A0}	400	400	400	320	MHz	
F_{CLK_CD2A1}	400	400	400	320	MHz	Unused
F_{CLK_CD2B0}	400	400	400	320	MHz	Unused
F_{CLK_CD2B1}	400	400	400	320	MHz	Unused
F_{CLK_CD3}	200	200	200	160	MHz	Unused
F_{CLK_CD3A0}	200	200	200	160	MHz	
F_{CLK_CD3A1}	200	200	200	160	MHz	Unused
F_{CLK_CD3B0}	200	200	200	160	MHz	Unused
F_{CLK_CD3B1}	200	200	200	160	MHz	Unused
F_{CLK_CD4}	200	200	200	200	MHz	
F_{CLK_CD4A0}	200	200	200	200	MHz	Unused
F_{CLK_CD4A1}	200	200	200	200	MHz	Unused
F_{CLK_CD4B0}	200	200	200	200	MHz	Unused
F_{CLK_CD4B1}	200	200	200	200	MHz	Unused
F_{CLK_CD5}	240	240	240	240	MHz	
F_{CLK_CD5A0}	120	120	120	120	MHz	
F_{CLK_CD5A1}	120	120	120	120	MHz	Unused
F_{CLK_CD5B0}	60	60	60	60	MHz	
F_{CLK_CD5B1}	60	60	60	60	MHz	Unused
F_{CLK_HSSPI}	200	200	200	200	MHz	
F_{CLK_SYSC0H}	60	66.7	80	80	MHz	
F_{CLK_COMH}	60	66.7	80	80	MHz	
F_{CLK_RAM0H}	60	66.7	80	80	MHz	
F_{CLK_RAM1H}	60	66.7	80	80	MHz	
F_{CLK_SYSC0P}	60	66.7	80	80	MHz	
F_{CLK_COMP}	60	66.7	80	80	MHz	
F_{CLK_CAN}	40	40	40	40	MHz	

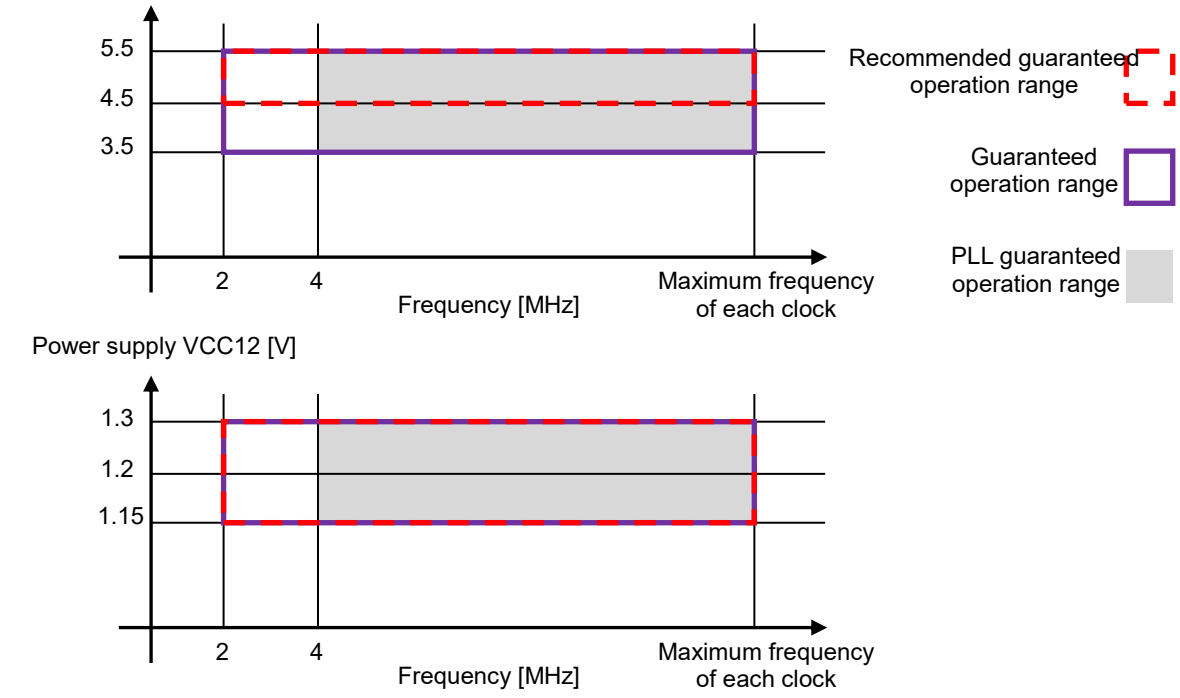
Notes:

- **1: Maximum clock frequencies when CPU clock = 240 MHz.*
- *For SSCG, down spread and center spread modes are supported with following conditions:*
  - *For down spread mode, clock frequency setting can be up to max SSCG frequency defined in above table.*
  - *For center spread mode, an appropriate clock frequency setting has to be chosen so that the modulated clock does not exceed the max SSCG frequency defined in above table.*
- *240 MHz or less is available for PLL.*
- **2: Maximum clock frequencies when CPU clock = 200 MHz.*
- **3: Maximum clock frequencies when CPU clock = 160 MHz. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.*
- *From *1 to *3, they are applied to the product series with function digit 3, 4, 5, 6, 7, 8, 9, K, L, M, and N.*
- **4: Maximum clock frequencies when CPU clock = 160 MHz for the product series with the function digit B. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.*
- *Even if a combination of clock frequency is able to be configured by software, the frequency should be configured under maximum frequency described in Table 8-1. For example, 80 MHz of CLK_LCP0A seems to be configurable from both divided 240 MHz and 160 MHz of CLK_CPU. But each duty ratio of configured 80 MHz as an internal signal is different from one another. In this series, the 80 MHz from the 160 MHz divided by 2 can only be assured, but the 240 MHz divided by 3 cannot be assured from the internal timing design point of view.*
- *F_{CLK_TRC}/2 (half frequency of F_{CLK_TRC}) comes out of the trace clock port of package external pin.*
- *The frequency described in () is maximum output frequency of SSCG PLL / PLL multiplier circuit.*
- *The configurable minimum frequency of PLLn and SSCGn output is 400 MHz.*

- *"Unused" means a clock source which doesn't have any supply destinations. Configure these clocks to a lower clock frequency than the described maximum.*

- Operation assurance range

Relationship between the internal clock frequency and supply voltage

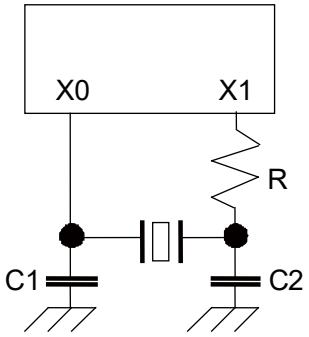


Note: CPU will be reset, when the power supply voltage is equal to or less than LVD setting voltage.

- Relationship between the oscillation clock frequency and internal clock frequency

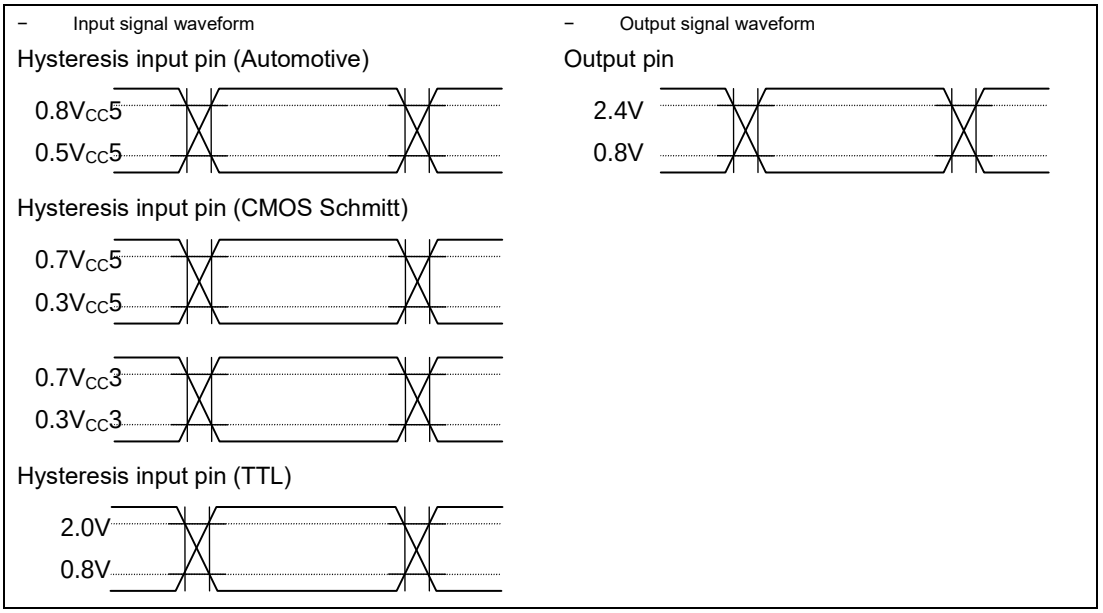
		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4		Multiplied by 40	Multiplied by 60
Oscillation clock frequency [MHz]	4	2	4	8	12	16	…	160	240

- Oscillation circuit example

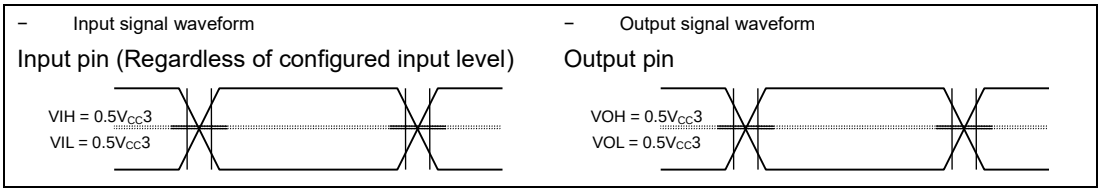


Note:
For the configuration of an oscillation circuit, request the oscillator manufacturer to perform a circuit matching evaluation before starting design.

AC characteristics are specified by the following measurement reference voltage values.



DDR-HSSPI and HyperBus AC characteristics are specified with the following reference voltage regardless of input level configuration automotive, CMOS Schmitt, and TTL.

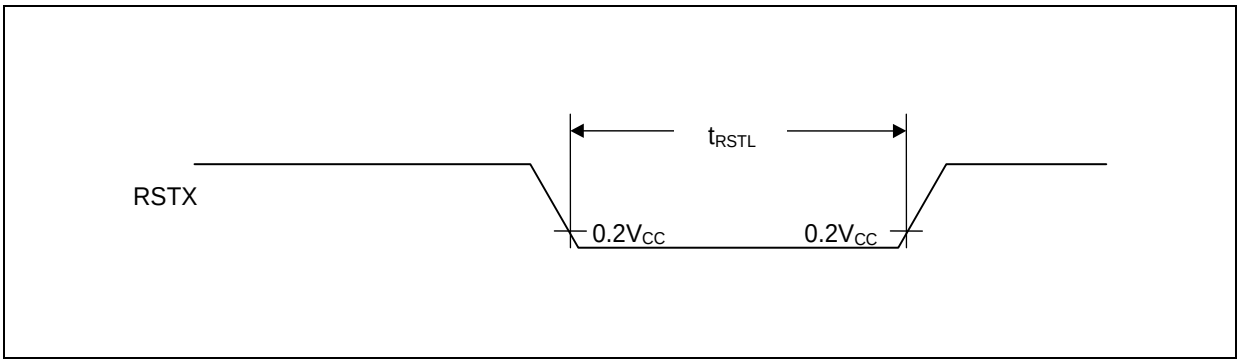


8.4.4 Reset

8.4.4.1 Reset Input

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	
Reset input pulse filtered				-	1	µs	

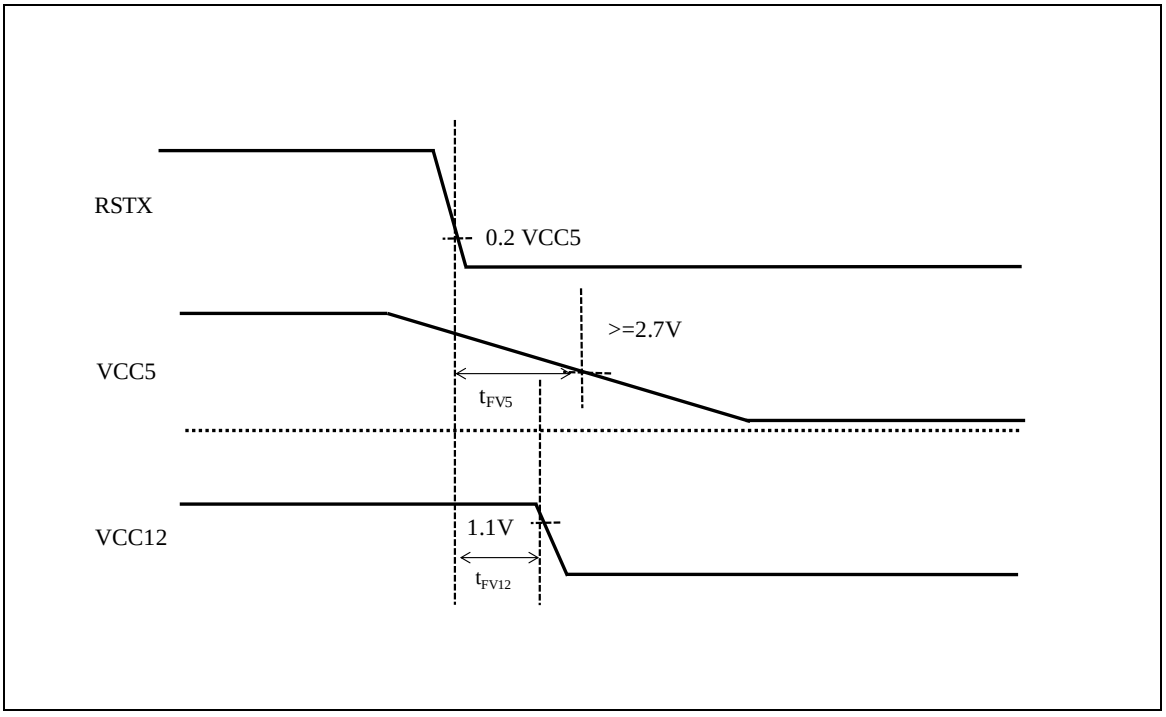


8.4.4.2 Power Supply Voltage Stability Conditions

□ For revision M, P

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC5 stability time after RSTX assertion	t_{FV5}	VCC5	-	35	-	µs	VCC5>=2.7 V
VCC12 stability time after RSTX assertion	t_{FV12}	VCC12		35	-	µs	VCC12>=1.1 V



Note:

This AC specification isn't applied except revision M, P.

8.4.5 Power-On Conditions

8.4.5.1 Power-On Conditions

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.15	2.35	2.55	V	
Reset release voltage	-	VCC5	-	2.25	2.45	2.65	V	
Level detection time	-	-	-	-	-	540	µs	*1
Power off time	t_{OFF}	VCC5	-	1	-	-	ms	*2
Power ramp rate	dV/dt	VCC5	VCC5: Between 0.2 V to 2.55 V	-	-	6	mV/µs	*3
Maximum ramp rate guaranteed to not generate power-on reset	|dV/dt|	VCC5	VCC5: Between 2.6 V and 4.5 V	-	-	50	mV/µs	*4

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: If Vcc is held below 0.2 V for a minimum period of t_{OFF}, power-on reset will occur. If t_{OFF} is not satisfied, power-on reset will still occur if the power ramp rate is kept below 6 mV/µs.

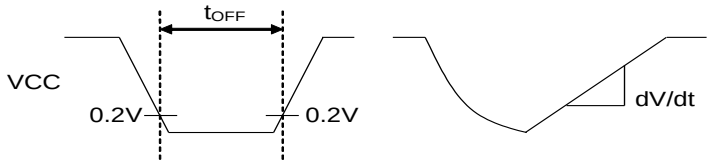
*3: This is the power ramp rate with which power-on reset will always occur regardless of power-off time, as mentioned in *2.

*4: When VCC5 is within 2.6 V - 4.5 V, and VCC5 fluctuation is below 50mV/us, the power-on reset is suppressed. Between 4.5 V - 5.5 V, the power-on reset does not occur with any VCC5 fluctuation.

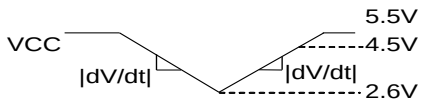
Note:

− *When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.*

Power off time, Power ramp rate at Power-on



Maximum ramp rate guaranteed to not generate power-on reset



8.4.5.2 VCC12 Stabilization Time during Power-On / PSS to RUN Transition

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
					Min	Typ	Max		
VCC12 stabilization time during power-on		VCC12	-		-	-	14.2	ms	*5
VCC12 stabilization time during PSS (PD2 off) to RUN transition (Fast-CR untrimmed)	-	VCC12	SYSC0_ SPECFGR: EX12VRSTCNT	0000	-	-	0.7	ms	*5
				0001	-	-	1.4		
				0010	-	-	2.1		
				0011	-	-	2.8		
				0100	-	-	3.5		
				0101	-	-	4.2		
				0110	-	-	4.9		
				0111	-	-	5.7		
				1000	-	-	6.4		
				1001	-	-	7.1		
				1010	-	-	8.5		
				1011	-	-	9.9		
				1100	-	-	11.4		
				1101	-	-	12.8		
				1110 (default)	-	-	14.2		
				1111	-	-	21.3		
VCC12 stabilization time during PSS (PD2 off) to RUN transition (Fast-CR trimmed)	-	VCC12	SYSC0_ SPECFGR: EX12VRSTCNT	0000	-	-	0.8	ms	*5
				0001	-	-	1.6		
				0010	-	-	2.4		
				0011	-	-	3.3		
				0100	-	-	4.1		
				0101	-	-	4.9		
				0110	-	-	5.8		
				0111	-	-	6.6		
				1000	-	-	7.4		
				1001	-	-	8.3		
				1010	-	-	9.9		
				1011	-	-	11.6		
				1100	-	-	13.3		
				1101	-	-	14.9		
				1110 (default)	-	-	16.6		
				1111	-	-	24.9		

*5: After LVDL2 reset release during power-on sequence and PSS (PD2 off) to RUN transition, VCC12 has to rise above operation assurance range within this time.

8.4.6 Multi-Function Serial

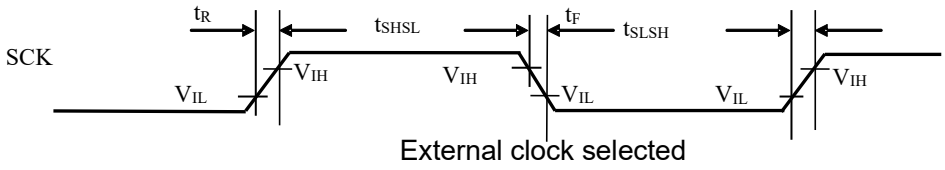
8.4.6.1 UART (Asynchronous Serial Interface) Timing (SMR: MD2-0=0b000, 0b001)

(1) External Clock Selected (BGR: EXT=1)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(C_L = 50 pF, I_{OL}=-2 mA, I_{OH}=2 mA), (C_L=20 pF, I_{OL}=-1 mA, I_{OH}=1 mA)	t_{CLK_LCPnA}*1 +10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12		t_{CLK_LCPnA}*1 +10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	
SCK rising time	t_R			-	5	ns	

*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12



External clock selected

External clock selected

8.4.6.2 CSIO Timing (SMR: MD2-0=0b010)

(1) Normal Synchronous Transfer (SCR: SPI=0) and Mark Level "H" of Serial Clock Output (SMR: SCINV=0)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
				$3t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$3t_{CLK_COMP}$	-		
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12		0	30	ns	
				0	20*3		
		SCK16 to SCK17 SOT16 to SOT17		0	15		
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12		26.5	-	ns	
				20*3			
		SCK16 to CK17 SIN16 to SIN17		20			
SCK ↑→ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17		0	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2			
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		
SCK ↓→ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		-	28.5	ns	function digit 3 to 9 K to N
					25*3		
					30		function digit B
		SCK16 to SCK17 SOT16 to SOT17			25		
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		10	-	ns	function digit 3 to 9 K to N
				11.5			function digit B
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17		1	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	

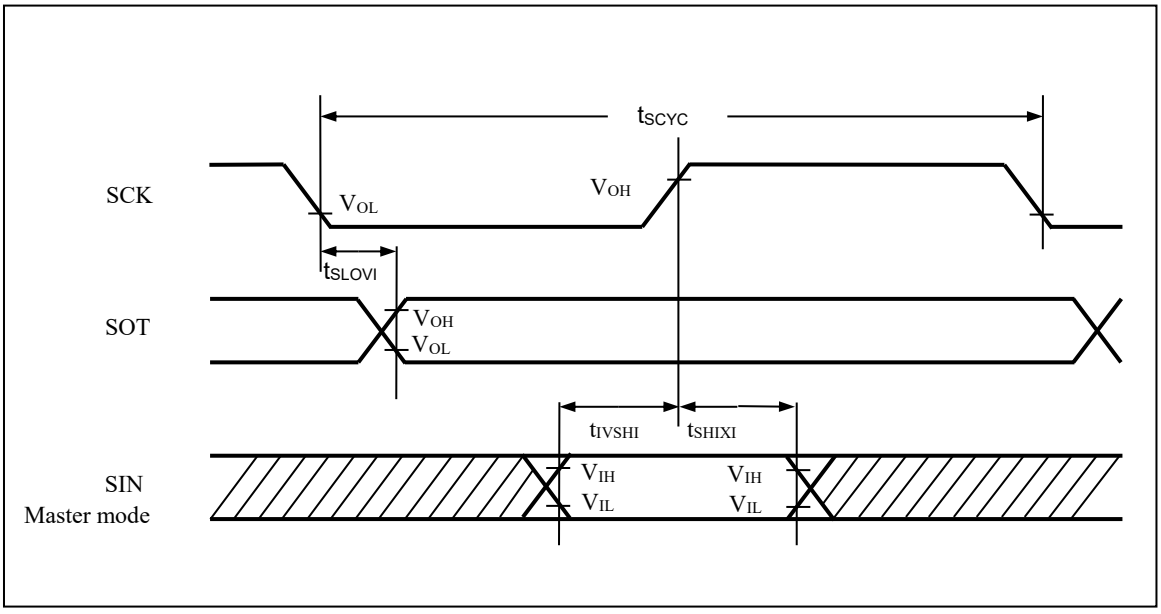
*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12

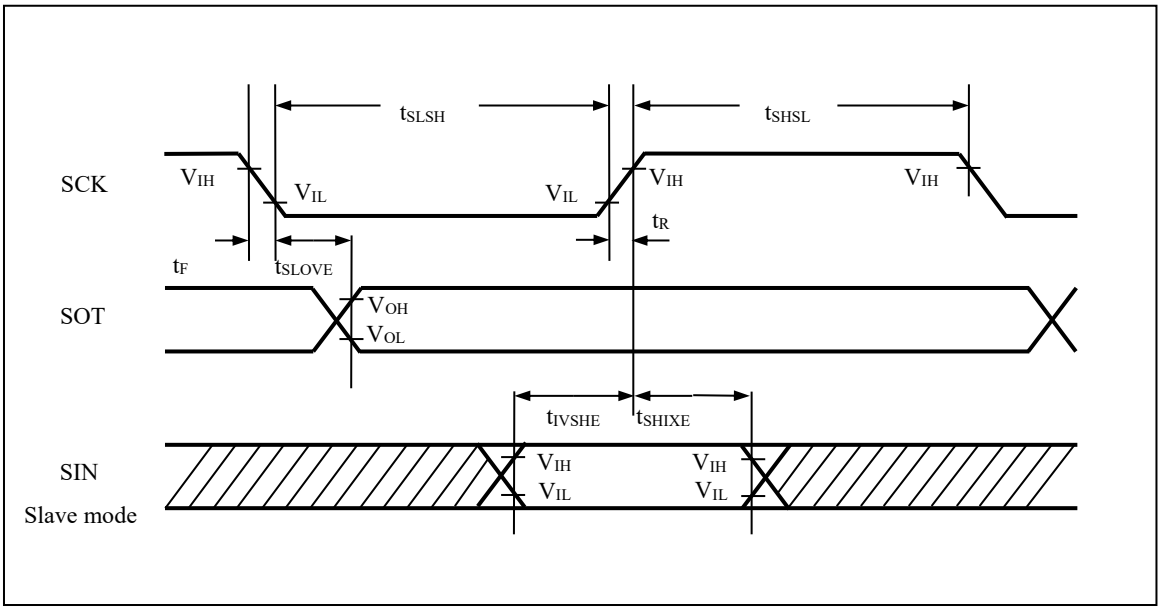
*2: n=0: Group2 of ch.0 /ch1, n=1: Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

*3: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *CL is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*




tSLSH
tSHSL
SCK
VIH
VIL
VIL
VIH
VIH
tR
tF
tSLOVE
SOT
VOH
VOL
tIVSHE
tSHIXE
SIN
Slave mode
VIH
VIL
VIH
VIL

(2) Normal Synchronous Transfer (SCR: SPI=0) and Mark Level "L" of Serial Clock Output (SMR: SCINV=1)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$3t_{CLK_LCPnA}$ *1	-	ns	
				$3t_{CLK_LCPnA}$ *2	-		
		SCK16 to SCK17		$3t_{CLK_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK8 to SCK12 SOT0 to SOT4, SOT8 to SOT12		0	30	ns	
				0	20*3		
		SCK16 to SCK17 SOT16 to SOT17		0	15		
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12,		26.5	-	ns	
				20*3	-		
		SCK16 to SCK17 SIN16 to SIN17		20	-		
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SOT0 to SOT4, SOT8 to SOT12, SOT16 to SOT17		0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK_LCPnA}$ *1	-	ns	
				$2t_{CLK_LCPnA}$ *2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$ *1	-	ns	
				$2t_{CLK_LCPnA}$ *2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	-	28.5	ns	function digit 3 to 9 K to N
					25*3		
					30		function digit B
		SCK16 to SCK17 SOT16 to SOT17			25		
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17		10	-	ns	function digit 3 to 9 K to N
				11.5			function digit B
SCK ↓ → Valid SIN hold time	t_{SLIXE}			1	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	

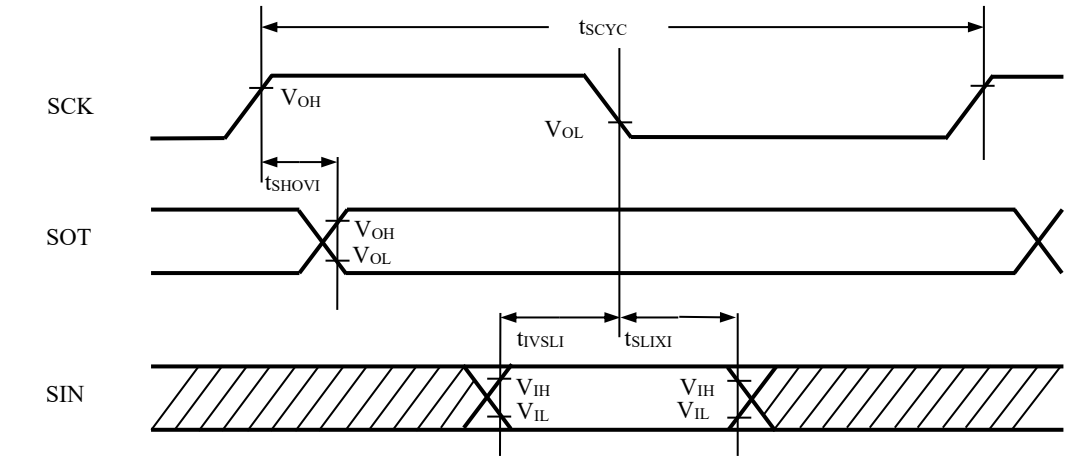
*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12

*2: n=0: Group2 of ch.0 /ch1, n=1: Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

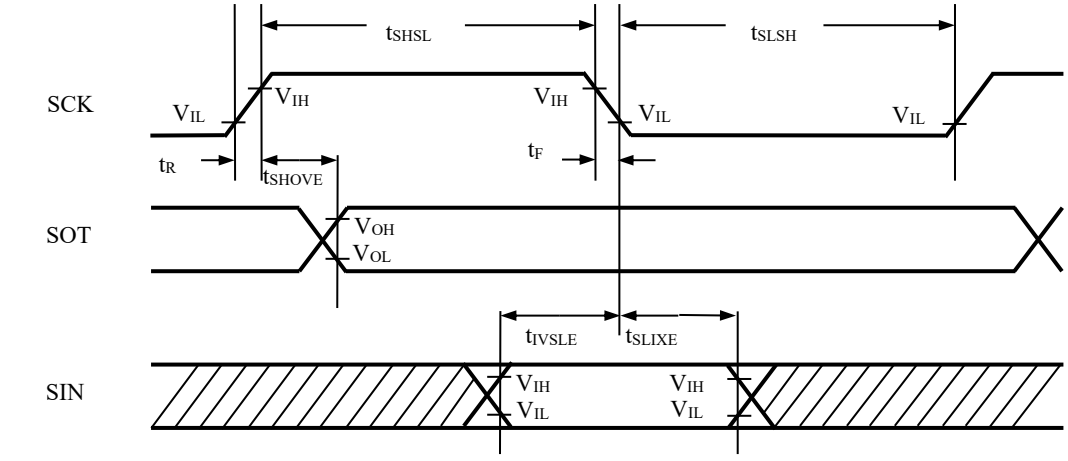
*3: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *C_L is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



Master mode



Slave mode

(3) SPI Supported (SCR: SPI=1), and Mark Level "H" of Serial Clock Output (SMR: SCINV=0)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master Mode (CL=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
				$3t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$3t_{CLK_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	30	ns	
				0	20*3		
		SCK16 to SCK17 SOT16 to SOT17		0	15		
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12,		26.5	-	ns	
				20*3	-		
		SCK16 to SCK17 SIN16 to SIN17		20	-		
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17		0	-	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK4, SCK8 to SCK12 SOT0 to SOT4, SOT8 to SOT12		$2t_{CLK_LCPnA}$*1 - 30	-	ns	
				$2t_{CLK_LCPnA}$*2 - 20	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$*1 - 15	-		

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-		
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		-	28.5	ns	function digit 3 to 9 K to N
					25*3		
					30		function digit B
		SCK16 to SCK17 SOT16 to SOT17			25		

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	10	-	ns	function digit 3 to 9 K to N
				11.5			function digit B
SCK ↓ → Valid SIN hold time	t_{SLIXE}			1	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17		-	5	ns	

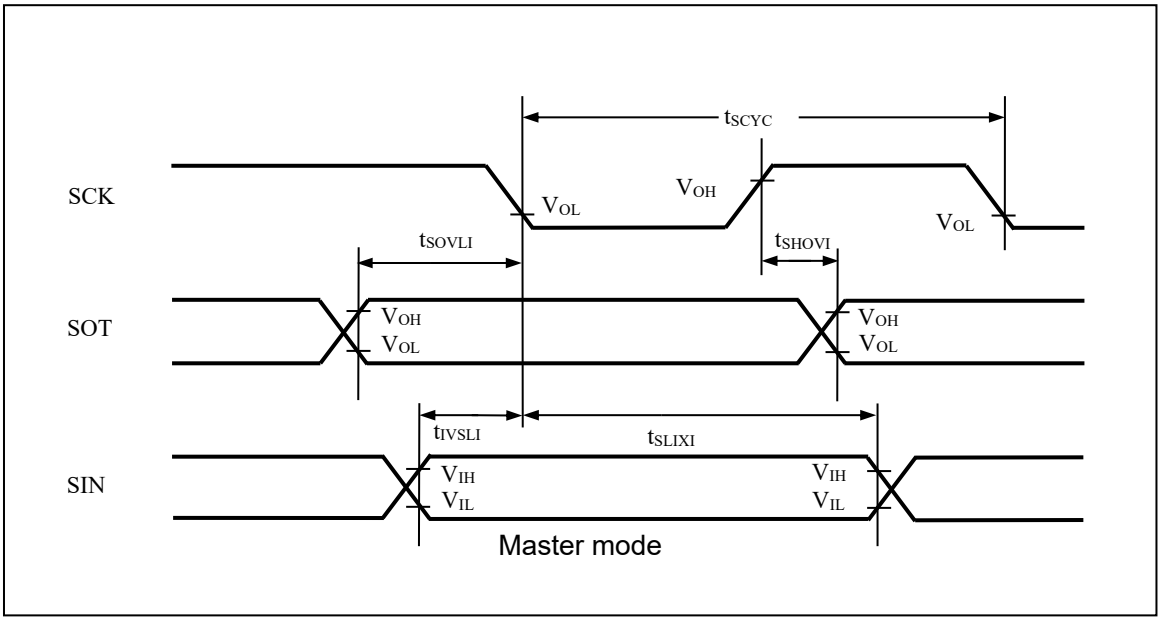
*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12

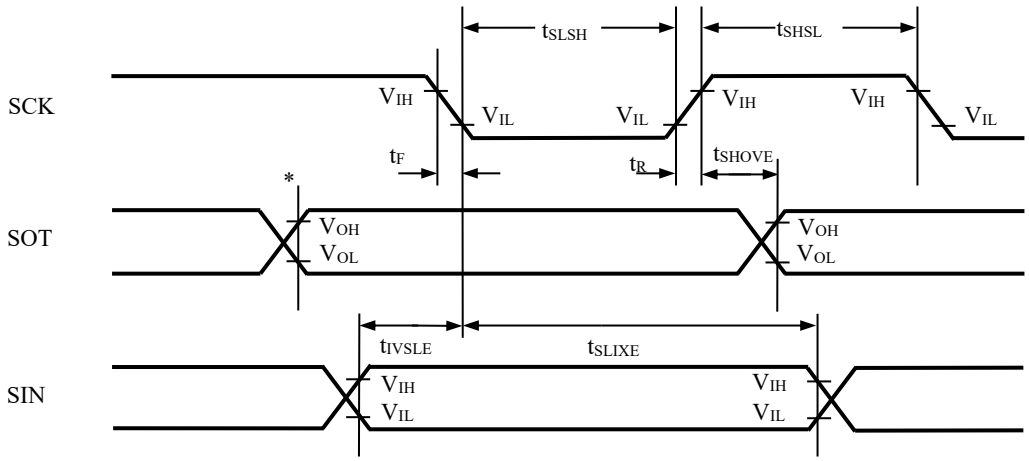
*2: n=0: Group2 of ch.0 /ch1, n=1: Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

*3: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *C_L is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*





* Changes when writing to the TDR register

Slave mode

(4) SPI Supported (SCR: SPI=1), and Mark Level "L" of Serial Clock Output (SMR: SCINV=1)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK8 to SCK12	Master Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$3t_{CLK_LCPnA}$*1	-	ns	
				$3t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$3t_{CLK_COMP}$	-		
SCK ↓ -> SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		0	30	ns	
				0	20*3		
		SCK16 to SCK17 SOT16 to SOT17		0	15		
Valid SIN -> SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK8 to SCK12, SIN0 to SIN4, SIN8 to SIN12,		26.5	-	ns	
				20*3	-		
		SCK16 to SCK17 SOT16 to SOT17		20	-		
SCK ↑ -> Valid SIN hold time	t_{SHIXI}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17		0	-	ns	
SOT -> SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK4, SCK8 to SCK12 SOT0 to SOT4, SOT8 to SOT12		$2t_{CLK_LCPnA}$*1 - 30	-	ns	
				$2t_{CLK_LCPnA}$*2 - 20	-		
		SCK16 to SCK17 SOT16 to SOT17		$2t_{CLK_COMP}$ - 15	-	ns	

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2			
		SCK16 to SCK17		$2t_{CLK_COMP}$	-	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12		$2t_{CLK_LCPnA}$*1	-	ns	
				$2t_{CLK_LCPnA}$*2	-		
		SCK16 to SCK17		$2t_{CLK_COMP}$	-	ns	
SCK ↓ -> SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK8 to SCK12, SOT0 to SOT4, SOT8 to SOT12,		-	28.5	ns	function digit 3 to 9 K to N
					25*3		
					30		function digit B
		SCK16 to SCK17 SOT16 to SOT17			25		
Valid SIN -> SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17 SIN0 to SIN4, SIN8 to SIN12, SIN16 to SIN17	Slave Mode (C_L=20 pF, I_{OL}=-5 mA, I_{OH}=5 mA)	10	-	ns	function digit 3 to 9 K to N
				11.5			function digit B
SCK ↑ -> Valid SIN hold time	t_{SHIXE}			1		ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17		-	5	ns	
SCK rising time	t_R	SCK0 to SCK4, SCK8 to SCK12 SCK16 to SCK17		-	5	ns	

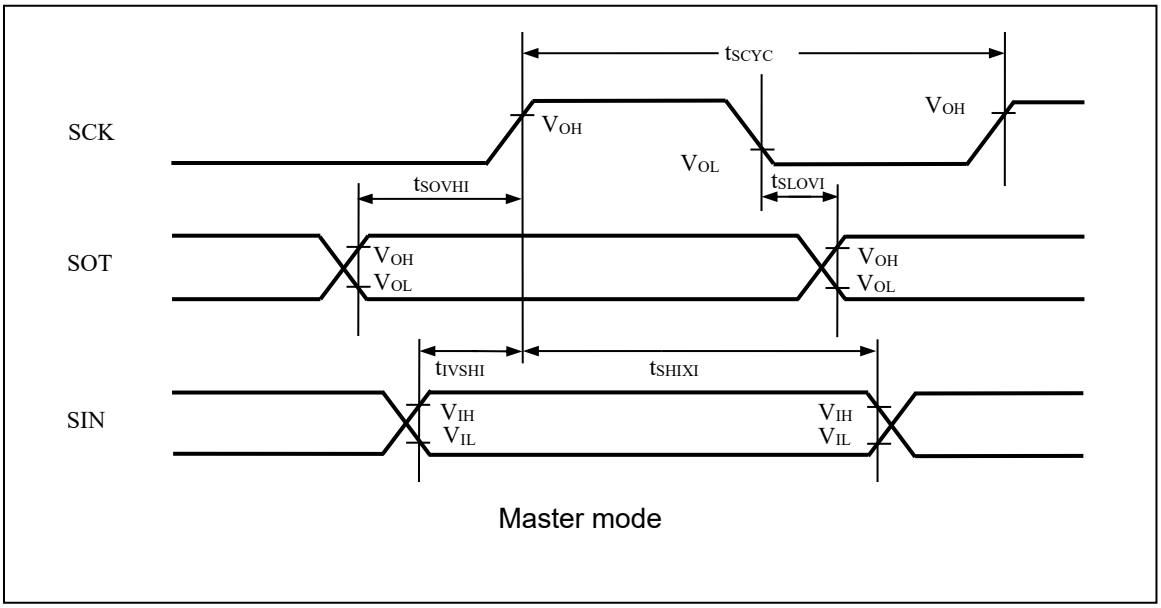
*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12

*2: n=0: Group2 of ch.0 /ch1, n=1: Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

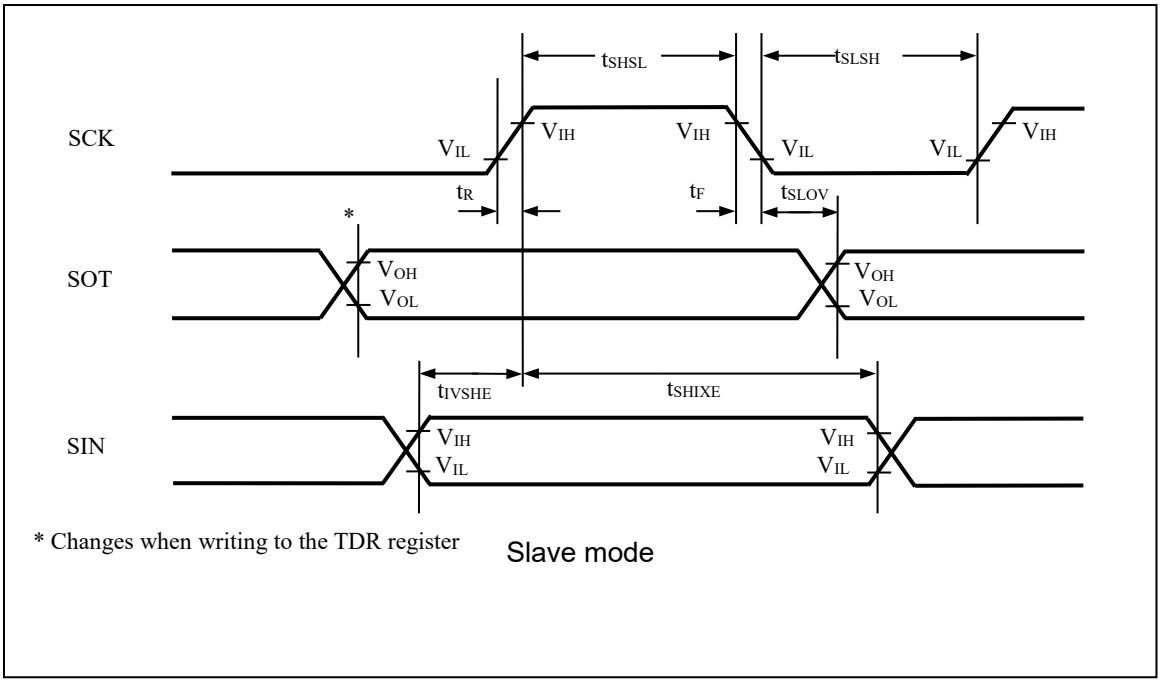
*3: Group2 of ch.0, ch1, Group1 of ch.8 (refer to CHAPTER 11: Port Configuration in HWM)

Notes:

- *This table provides the alternate current standard for CLK synchronous mode.*
- *C_L is the load capability value connected to the pin at the test time.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



Master mode



* Changes when writing to the TDR register

Slave mode

(5) Mark Level "H" of Serial Clock Output (SMR: SCINV=0) and Mark Level "H" of Serial Chip Select (SCSCR: CSLVL=1)

(Condition: See 8.2.Operation Assurance Condition)

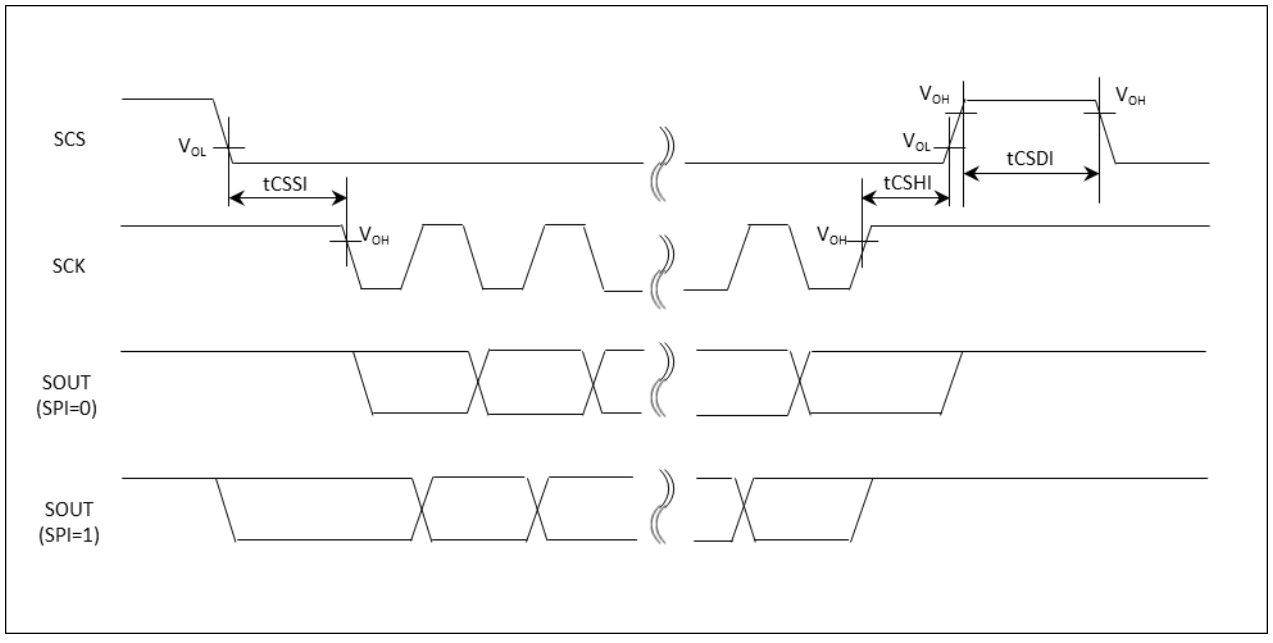
Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↓ →SCK ↓ setup time	t_{CSSI}	Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↑ →SCS ↑ hold time	t_{CSHI}		0*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↓ →SCS ↓ clock change time	t_{SCC}	Round Function Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	3tcp+0	3tcp+20	ns	

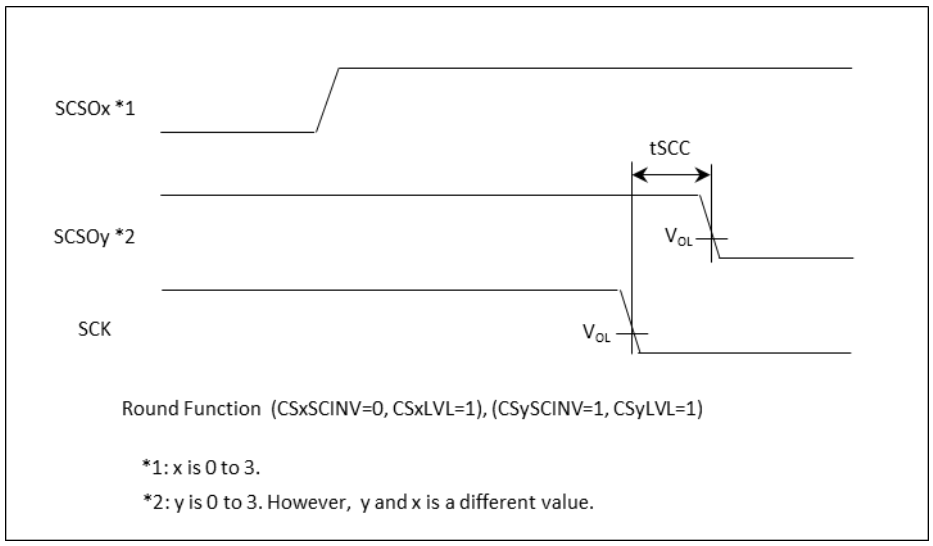
*1) SCSTR1.CSSU=0. t_{CSSI} can be configured.

*2) SCSTR0.CSHD=0. t_{CSHI} can be configured.

*3) SCSTR3/2.CSDS=0. t_{CSDI} can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=0, CSxLVL=1), (CSySCINV=1, CSyLVL=1)

*1: x is 0 to 3.

*2: y is 0 to 3. However, y and x is a different value.

(6) Mark Level "L" of Serial Clock Output (SMR: SCINV=1) and Mark Level "H" of Serial Chip Select (SCSCR: CSLVL=1)

(Condition: See 8.2.Operation Assurance Condition)

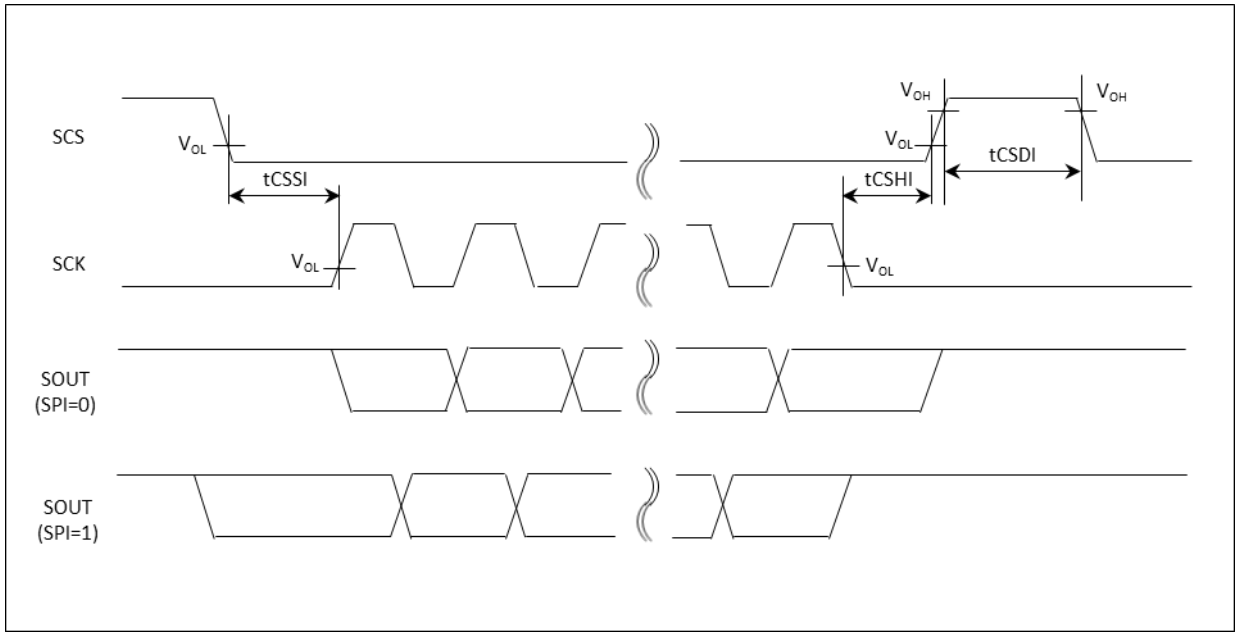
Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↓ →SCK ↑ setup time	t_{CSSI}	Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↓ →SCS ↑ hold time	t_{CSHI}		0*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↑ →SCS ↓ clock change time	t_{SCC}	Round Function Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	3tcp+0	3tcp+20	ns	

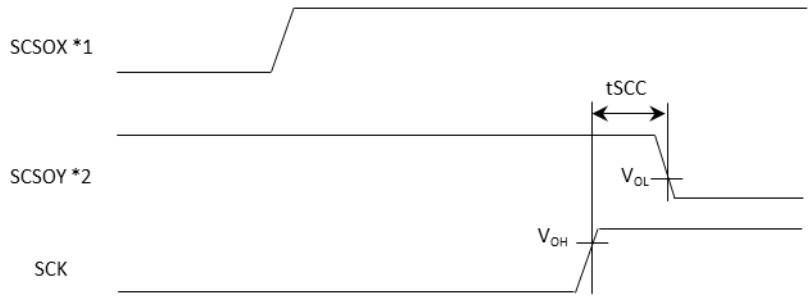
*1) SCSTR1.CSSU=0. t_{CSSI} can be configured.

*2) SCSTR0.CSHD=0. t_{CSHI} can be configured.

*3) SCSTR3/2.CSDS=0. t_{CSDI} can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=1, CSxLVL=1), (CSySCINV=0, CSyLVL=1)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

(7) Mark Level "H" of Serial Clock Output (SMR: SCINV=0) and Mark Level "L" of Serial Chip Select (SCSCR: CSLVL=0)

(Condition: See 8.2.Operation Assurance Condition)

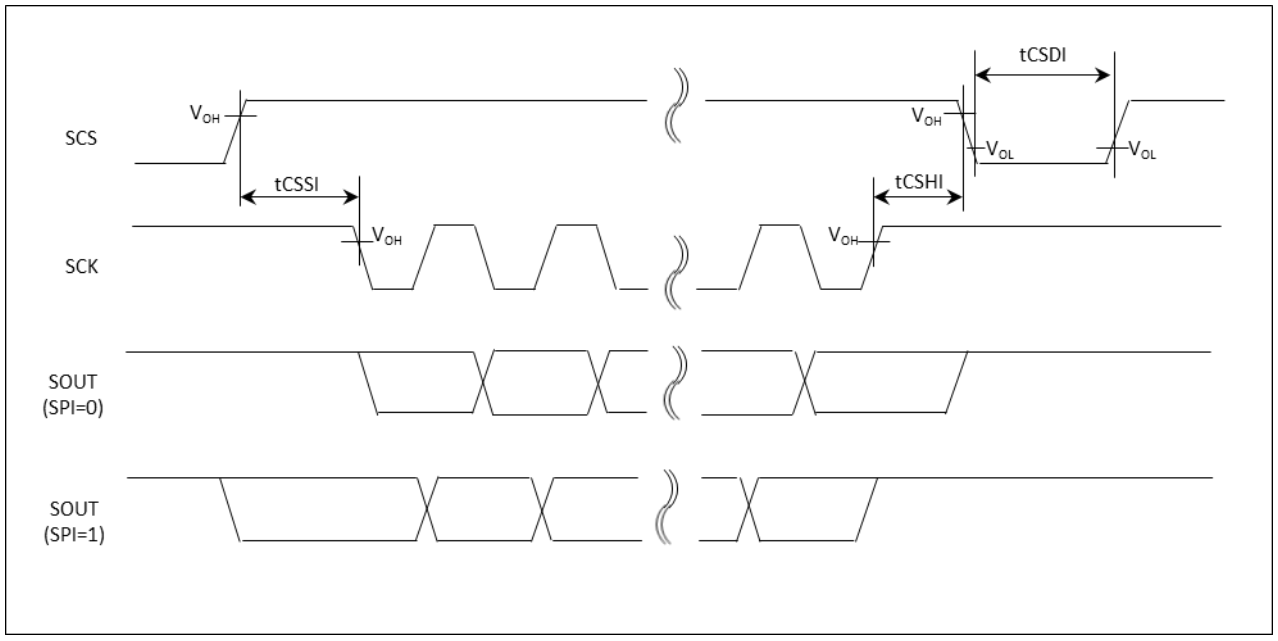
Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↑ →SCK ↓ setup time	t_{CSSI}	Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↑ →SCS ↓ hold time	t_{CSHI}		0*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↓ →SCS ↑ clock change time	t_{SCC}	Round Function Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	3tcp+0	3tcp+20	ns	

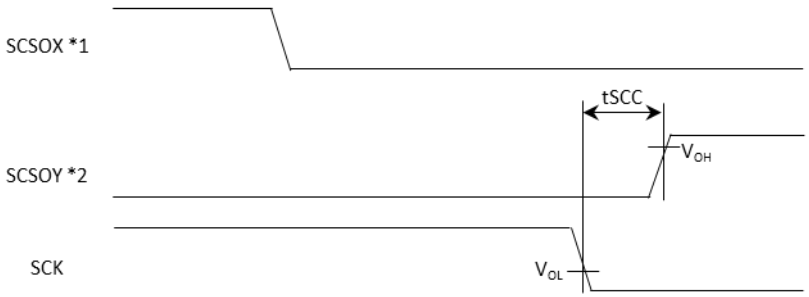
*1) SCSTR1.CSSU=0. t_{CSSI} can be configured.

*2) SCSTR0.CSHD=0. t_{CSHI} can be configured.

*3) SCSTR3/2.CSDS=0. t_{CSDI} can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=0, CSxLVL=0), (CSySCINV=1, CSyLVL=0)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

(8) Mark Level "L" of Serial Clock Output (SMR: SCINV=1) and Mark Level "L" of Serial Chip Select (SCSCR: CSLVL=0)

(Condition: See 8.2.Operation Assurance Condition)

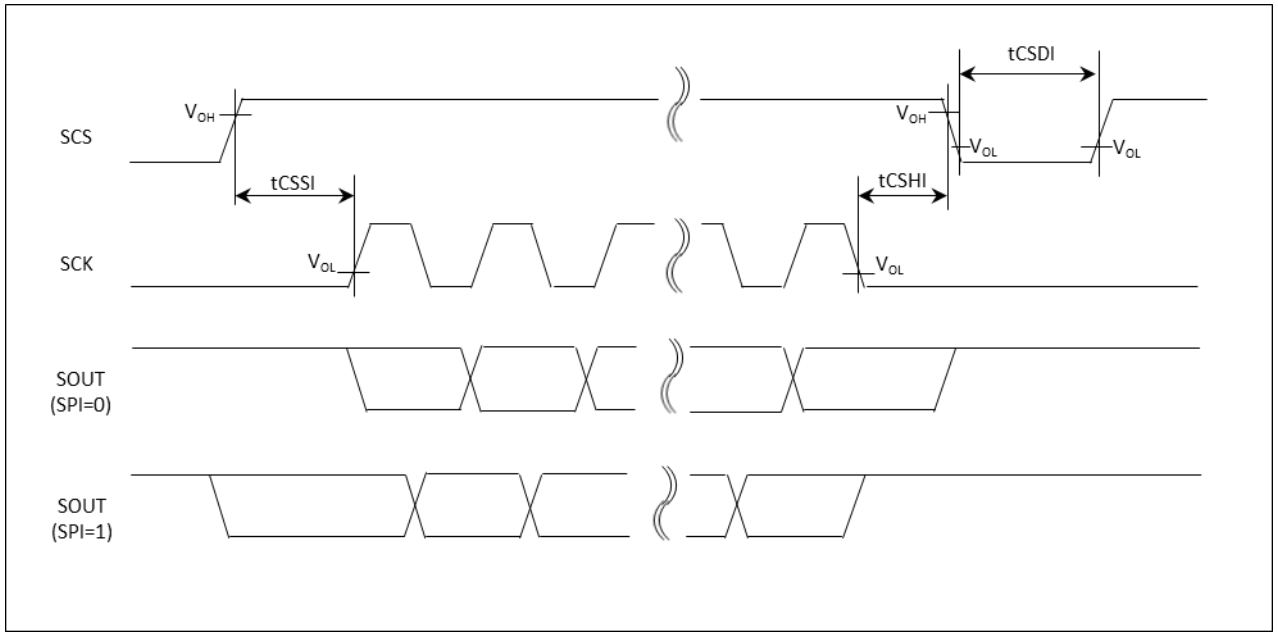
Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
SCS ↑ →SCK ↑ setup time	t_{CSSI}	Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	-20*1	-	ns	
SCK ↓ →SCS ↓ hold time	t_{CSHI}		0*2	-	ns	
SCS deselect time	t_{CSDI}		-20+5tcp*3	-	ns	
SCK ↑ →SCS ↑ clock change time	t_{SCC}	Round Function Master mode (C_L = 20 pF I_{OL}=-5 mA, I_{OH}=5 mA)	3tcp+0	3tcp+20	ns	

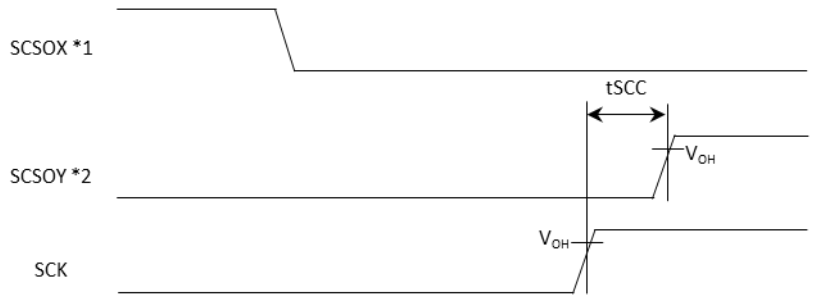
*1) SCSTR1.CSSU=0. t_{CSSI} can be configured.

*2) SCSTR0.CSHD=0. t_{CSHI} can be configured.

*3) SCSTR3/2.CSDS=0. t_{CSDI} can be configured.

tcp is bus clock. Ch0-4 is CLK_LCP0A. Ch8-12 is CLK_LCP1A. Ch16-17 is CLK_COMP.





Round Function (CSxSCINV=1, CSxLVL=0), (CSySCINV=0, CSyLVL=0)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.

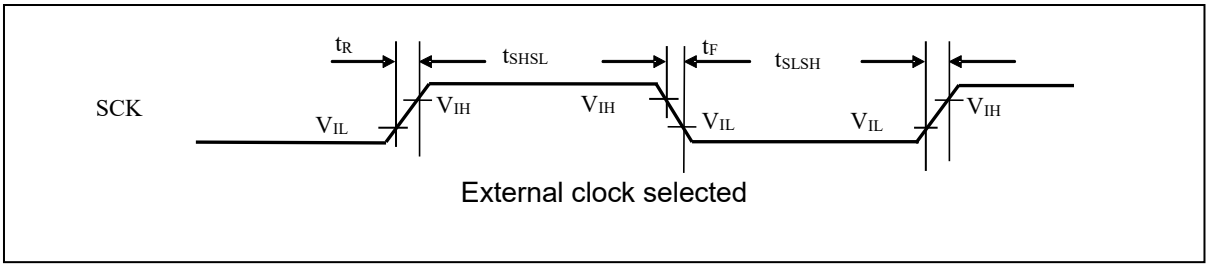
8.4.6.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR: MD2-0=0b011)

(1) External Clock Selected (BGR: EXT=1)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK8 to SCK12	(C_L = 50 pF, I_{OL}=-2 mA, I_{OH}=2 mA), (C_L=20 pF, I_{OL}=-1 mA, I_{OH}=1 mA)	t_{CLK_LCPnA}*1+10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK8 to SCK12		t_{CLK_LCPnA}*1+10	-	ns	
		SCK16 to SCK17		t_{CLK_COMP} +10	-	ns	
SCK falling time	t_F	SCK0 to SCK4, SCK8 to SCK12, SCK16 to SCK17		-	5	ns	
SCK rising time	t_R			-	5	ns	

*1: n=0: ch.0 to ch.4, n=1: ch.8 to ch.12



External clock selected

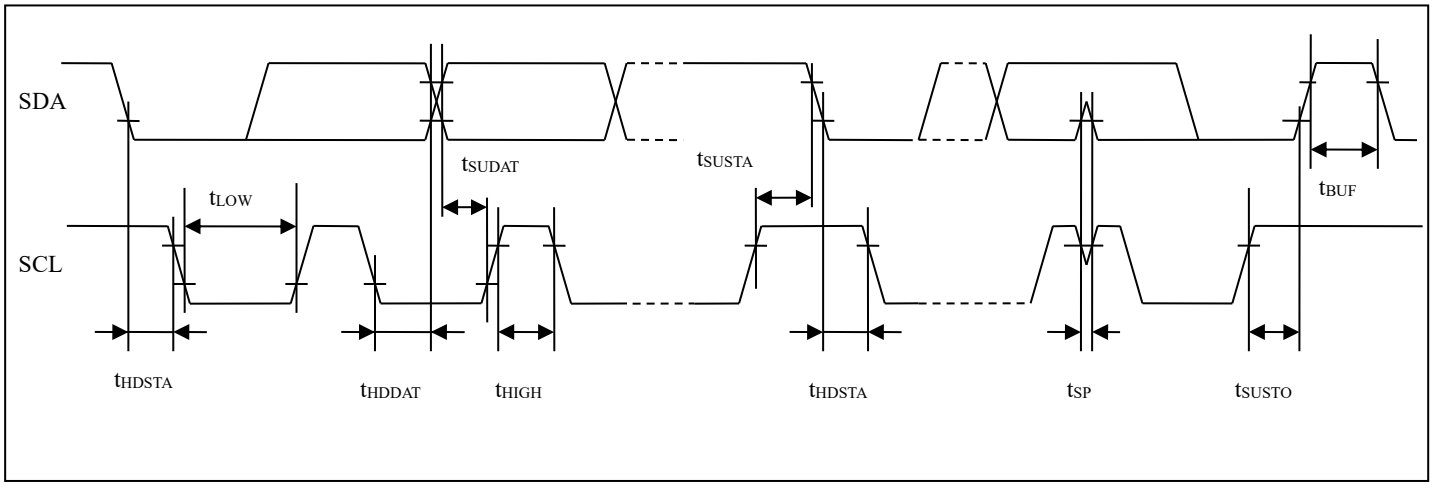
8.4.6.4 I^2C Timing (SMR: MD2-0=0b100)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		Fast Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCL4, 10, 12, 16, and 17	(C_L = 50 pF, I_{OL}=-2 mA, I_{OH}=2 mA), (C_L=20 pF, I_{OL}=-1 mA, I_{OH}=1 mA)	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		4.0	-	0.6	-	µs	
Period of "L" for SCL clock	t_{LOW}	SCL4, 10, 12, 16, and 17		4.7	-	1.3	-	µs	
Period of "H" for SCL clock	t_{HIGH}	SCL4, 10, 12, 16, and 17		4.0	-	0.6	-	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		0	3.45*1	0	0.9*2	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16, and 17		250	-	100	-	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SDA4, 10, 12, 16, and 17 SCL4, 10, 12, 16 and 17		4.0	-	0.6	-	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	-		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-		$2t_{CLK_COMP}$	-	$2t_{CLK_COMP}$	-	ns	

Notes:

- **1: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.*
- **2: A fast mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".*
- *SCL4, 10, 12 and SDA4, 10, 12 only support the standard mode.*



8.4.7 Timer Input

(Condition: See 8.2.Operation Assurance Condition)

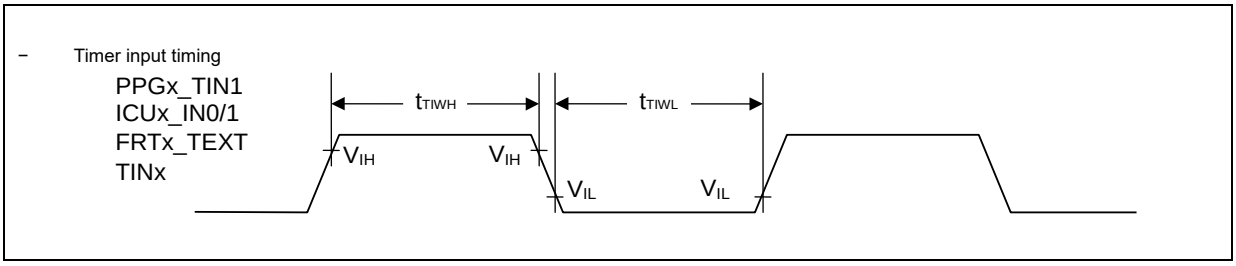
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TWH}, t_{TWL}	PPG0_TIN1 to PPG11_TIN1	-	$4t_{CLK_LCPnA}$*1	-	ns	$4t_{CLK_LCPnA}$*1 ≥100 ns
				100			$4t_{CLK_LCPnA}$*1 <100 ns
		ICU0_IN0 to ICU11_IN0, ICU0_IN1 to ICU11_IN1	-	$4t_{CLK_LCPnA}$*2	-	ns	$4t_{CLK_LCPnA}$*2 ≥100 ns
				100			$4t_{CLK_LCPnA}$*2 <100 ns
		FRT0_TEXT to FRT11_TEXT	-	$4t_{CLK_LCPnA}$*2	-	ns	$4t_{CLK_LCPnA}$*2 ≥100 ns
				100			$4t_{CLK_LCPnA}$*2 <100 ns
		TIN0 to TIN3, TIN16 to TIN19	-	$4t_{CLK_LCPnA}$*3	-	ns	$4t_{CLK_LCPnA}$*3 ≥100 ns
				100			$4t_{CLK_LCPnA}$*3 <100 ns
		TIN32 to TIN35	-	$4t_{CLK_LLPBM2}$	-	ns	$4t_{CLK_LLPBM2}$ ≥100 ns
				100			$4t_{CLK_LLPBM2}$ <100 ns
		TIN48 to TIN49	-	$4t_{CLK_COMP}$	-	ns	$4t_{CLK_COMP}$ ≥100 ns
				100			$4t_{CLK_COMP}$ <100 ns

*1: n=0: ch.0 to ch.5, n=1: ch.6 to ch.11

*2: n=0: ch.0 to ch.7, n=1: ch.8 to ch.11

*3: n=0: ch.0 to ch.3, n=1: ch.16 to ch.19

- Timer input timing

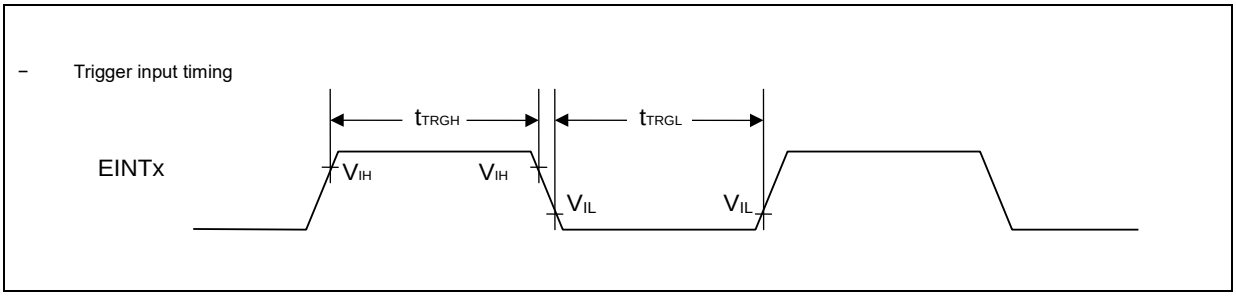


8.4.8 *Trigger Input*

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	EINT0 to EINT15	-	100	-	ns	

- Trigger input timing

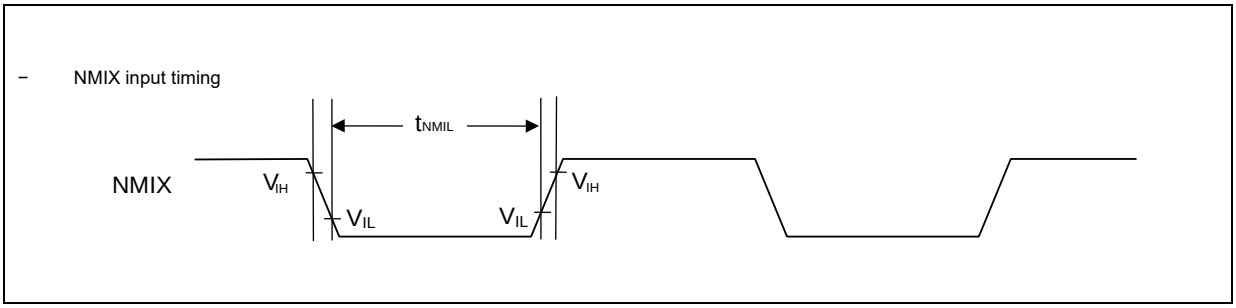


8.4.9 NMI Input

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	300	-	ns	

- NMIX input timing



8.4.10 Low-Voltage Detection

8.4.10.1 LVDL0

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Pin Name	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detection Voltage	-	-	0.9	0.95	1.0	V	*1
Release Voltage	-	-	0.925	1.025	1.125	V	
Level Detection Time	-	-	-	-	30	µs	*2

Notes:

- *1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
- *2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

8.4.10.2 LVDH0

Note:

- LVDH0 is only used to generate power-on reset. Refer to chapter Power-On Conditions for related parameters.

8.4.10.3 LVDL1

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Detection Voltage	-	LVDL1V=10 (Default)	0.92	0.97	1.02	V	No	*1
Release Voltage	-		0.945	1.045	1.145	V		
Detection Voltage	-	LVDL1V=11	1.02	1.07	1.12	V		
Release Voltage	-		1.095	1.145	1.195	V		
Detection Time	-	-	-	-	30	µs	-	*2

Notes:

- *1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
- *2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

8.4.10.4 LVDH1

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}5$	-	4.5	-	5.5	V		-
Detection Voltage	$V_{CC}5$	LVDH1V=0000	2.20	2.35	2.50	V	No	*1
Release Voltage	$V_{CC}5$		2.30	2.45	2.60	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0001	2.60	2.75	2.90	V		
Release Voltage	$V_{CC}5$		2.70	2.85	3.00	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0010	2.70	2.85	3.00	V		
Release Voltage	$V_{CC}5$		2.80	2.95	3.10	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0011	3.40	3.60	3.80	V		
Release Voltage	$V_{CC}5$		3.50	3.70	3.90	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0100	3.60	3.80	4.00	V	Yes	-
Release Voltage	$V_{CC}5$		3.70	3.90	4.10	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0101	3.80	4.00	4.20	V		
Release Voltage	$V_{CC}5$		3.90	4.10	4.30	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0110 (Default)	4.00	4.20	4.40	V		
Release Voltage	$V_{CC}5$		4.10	4.30	4.50	V		
Detection Voltage	$V_{CC}5$	LVDH1V=0111	4.20	4.40	4.60	V		
Release Voltage	$V_{CC}5$		4.30	4.50	4.70	V		
Detection Voltage	$V_{CC}5$	LVDH1V=Other	4.40	4.65	4.90	V		
Release Voltage	$V_{CC}5$		4.50	4.75	5.00	V		
Detection Time	-	-	-	-	30	µs		*2
Power supply voltage regulation	$V_{CC}5$	-	-2	-	2	V/ms		*3

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (3.5 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*
- **3: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.*

– *Following power supply voltage stability conditions need to be ensured. Moreover, the EXVRSTCNT bit in the SYSC0_SPECFGR register has to be "0" for Revision other than M, P.*

For Revision M, P

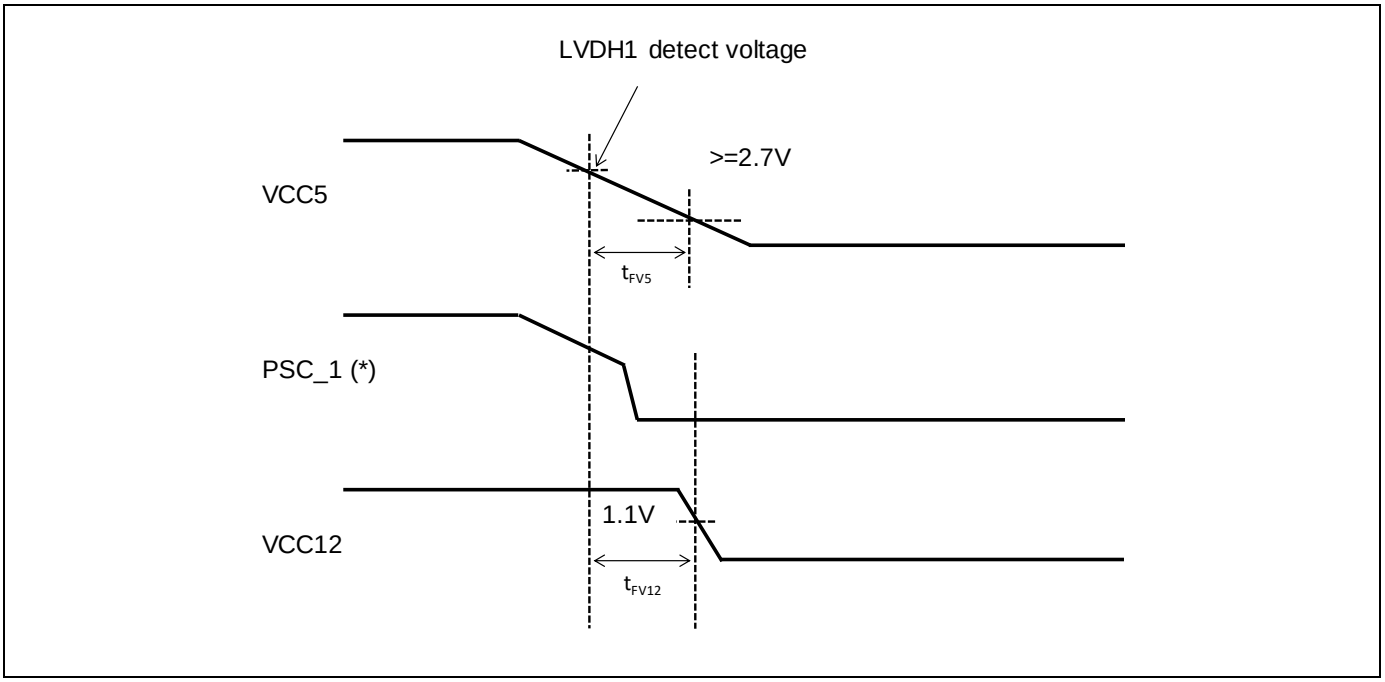
(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC5 stability time after LVDH1 low voltage detection	t_{FV5}	VCC5	-	55	-	µs	VCC5>=2.7 V
VCC12 stability time after LVDH1 low voltage detection	t_{FV12}	VCC12		55	-	µs	VCC12>=1.1 V

For except Revision M, P

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
VCC12 stability time after LVDH1 low voltage detection	t_{FV12}	VCC12		588	-	µs	VCC12>=1.1 V



**: The behavior of PSC_1 depends on the EXVRSTCNT bit regardless of revision. If the bit is set to "1", PSC_1 keeps 'H' level.*

8.4.10.5 LVDL2

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}12$	-	1.1	-	1.3	V	-	-
Detection Voltage	$V_{CC}12$	LVDL2V=00 (Default)	0.72	0.77	0.82	V	No	*1
Release Voltage	$V_{CC}12$		0.795	0.845	0.895	V		
Detection Voltage	$V_{CC}12$	LVDL2V=01	0.82	0.87	0.92	V		
Release Voltage	$V_{CC}12$		0.895	0.945	0.995	V		
Detection Voltage	$V_{CC}12$	LVDL2V=10	0.92	0.97	1.02	V		
Release Voltage	$V_{CC}12$		0.995	1.045	1.095	V		
Detection Voltage	$V_{CC}12$	LVDL2V=11	1.02	1.07	1.12	V		
Release Voltage	$V_{CC}12$		1.095	1.145	1.195	V		
Detection Time	-	-	-	-	30	µs	-	*2

Notes:

- **1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (1.1 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*

8.4.10.6 LVDH2

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Pin Name	Conditions	Value			Unit	Guaranteed MCU Operation Range	Remarks
			Min	Typ	Max			
Supply Voltage Range	$V_{CC}3$	-	3.0	-	3.6	V	-	-
Detection Voltage	$V_{CC}3$	LVDH2V=0000 (Default)	2.2	2.35	2.5	V	No	*1
Release Voltage	$V_{CC}3$		2.3	2.45	2.6	V		
Detection Voltage	$V_{CC}3$	LVDH2V=0001	2.6	2.75	2.9	V		
Release Voltage	$V_{CC}3$		2.7	2.85	3.0	V		
Detection Voltage	$V_{CC}3$	LVDH2V=0010	2.7	2.85	3.0	V	Yes	-
Release Voltage	$V_{CC}3$		2.8	2.95	3.1	V		
Detection Time	-	-	-	-	30	µs	-	*2
Power supply voltage regulation	$V_{CC}5$	-	-2	-	2	V/ms	-	*3

Notes:

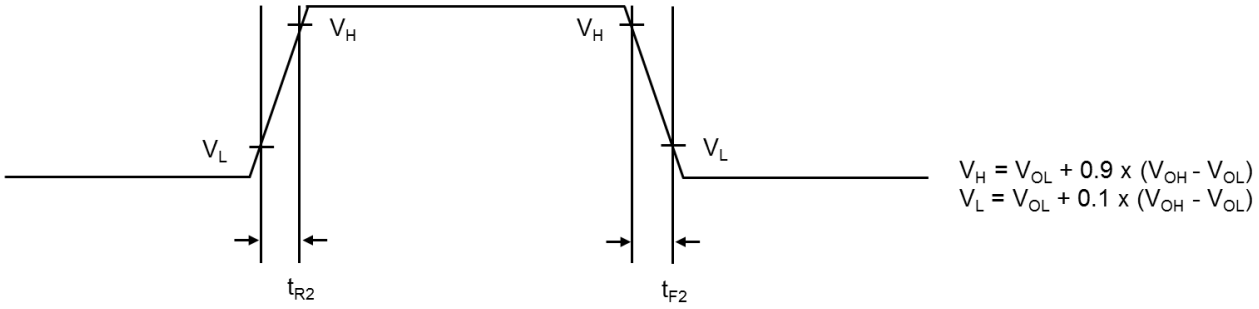
- **1: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7 V).*
- **2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.*
- **3: Suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.*

8.4.11 High Current Output Slew Rate

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise / fall time	t_{R2}, t_{F2}	P3_21 to 31, P4_00 to 12	-	15	-	100	ns	Load capacitance 85 pF

・Slew rate output timing



8.4.12 Display Controller

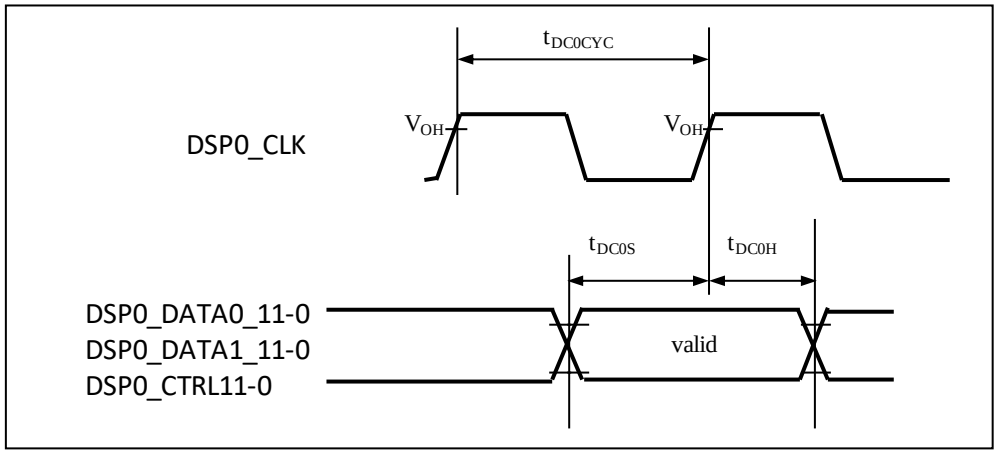
8.4.12.1 Display Controller0 Timing (TTL Mode)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks	
				Min	Max			
Clock Cycle	t_{DC0CYC}	DSP0_CLK	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA)	15.625	-	ns	*1	
				20	-	ns	*2	
Data/Control output to DSP0_CLK time	t_{DC0S}	DSP0_DATA0_11-0 DSP0_DATA1_11-0 DSP0_CTRL4-0		t_{DCOCYC} – 7.3	-	ns	*3	Pins in VCC3 domain
				t_{DCOCYC} – 5.6			*4	
				t_{DCOCYC} – 6.4			*5	
				t_{DCOCYC} – 5.0			*6	
DSP0_CLK to Data/Control valid time	t_{DC0H}			0.8	-	ns	*3	
				-1.3			*4	
				0.6			*5	
				-5.1			*6	
Data/Control output to DSP0_CLK time	t_{DC0S}	DSP0_CTRL11-0	(C_L = 20 pF, IOL=-5 mA, IOH=5 mA)	t_{DCOCYC} – 8.7	-	ns	*3	If any of DSP0_CTRL11-0 in VCC53 domain is used
				t_{DCOCYC} – 8.4			*4	
				t_{DCOCYC} – 8.2			*5	
				t_{DCOCYC} – 5.0			*6	
DSP0_CLK to Data/Control valid time	t_{DC0H}			0.8	-	ns	*3	
				-1.5			*4	
				0.6			*5	
				-5.1			*6	

Notes:

- *For *1, when used with DSP0_DATA* and DSP0_CTRL4-0 in VCC3 area.*
- *For *2, when used with DSP0_CTRL11-0 in VCC53 area.*
- *For *3, it is targeted by the product series with function digit 3 to 9 and revision digit F.*
- *For *4, it is targeted by the product series with function digit 3 to 9 and revision digit M, P.*
- *For *5, it is targeted by the product series with function digit K to N.*
- *For *6, it is targeted by the product series with function digit B.*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*
- *The clock output delay can be adjusted. See Chapter "Graphic Subsystem" of TRM for details.*



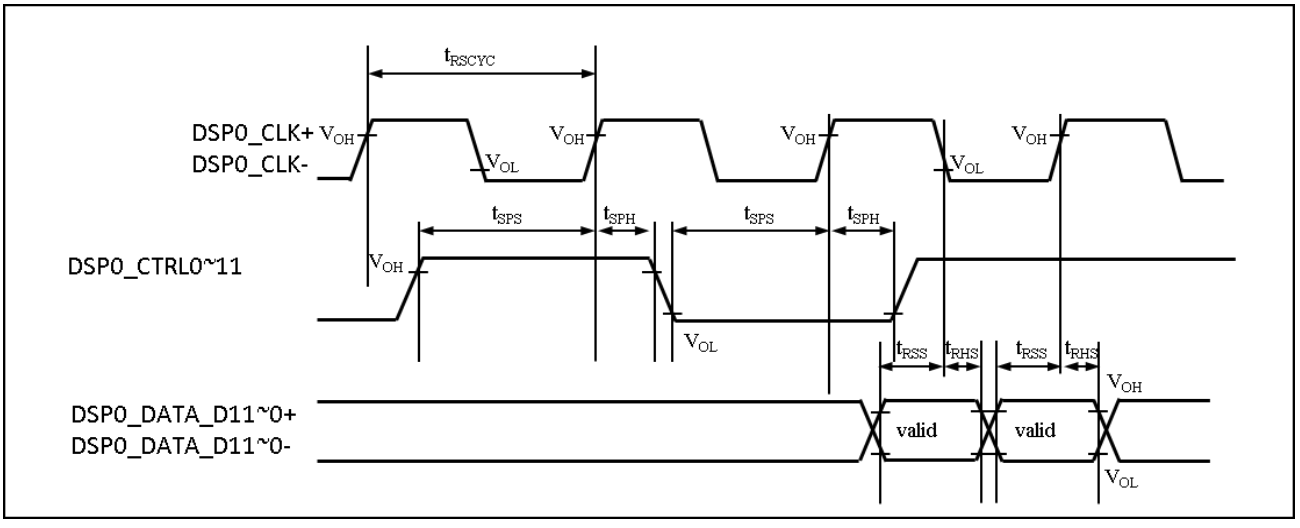
8.4.12.2 Display Controller0 Timing (RSDS)

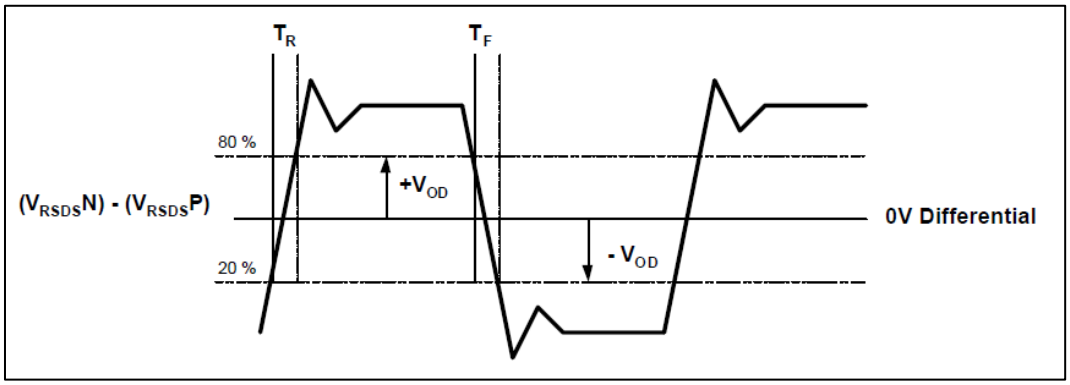
(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	t_{RSCYC}	DSP0_CLK+ DSP0_CLK-	(C_L = 20 pF, I_{OL}=-4 mA, I_{OH}=4 mA)	15.625	-	ns	
Data output to DSP0_CLK time	t_{RSS}	DSP0_DATA_D11~0+ DSP0_DATA_D11~0-		t_{RSCYC}/2 – 5.0	-	ns	*1
				t_{RSCYC}/2 – 5.3			*2
				t_{RSCYC}/2 – 5.0			*3
				t_{RSCYC}/2 – 6.1			*4
DSP0_CLK to Data valid time	t_{RSH}			-0.1	-	ns	*1
				-0.1			*2
				-0.1			*3
				0.5			*4
Control output to DSP0_CLK time	t_{SPS}	DSP0_CTRL11~0		t_{RSCYC} – 9.1	-	ns	*1
				t_{RSCYC} – 10.1			*2
				t_{RSCYC} – 9.0			*3
				t_{RSCYC} – 11.4			*4
DSP0_CLK to Control valid time	t_{SPH}			1.1	-	ns	*1
				1			*2
				1			*3
				2.1			*4

Notes:

- *For *1, it is targeted by the product series with function digit 3 to 9 and revision digit F.*
- *For *2, it is targeted by the product series with function digit 3 to 9 and revision digit M, P.*
- *For *3, it is targeted by the product series with function digit K to N.*
- *For *4, it is targeted by the product series with function digit B.*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*
- *The clock output delay can be adjusted. See the "Graphic Subsystem" chapter in the TRM for details.*




T_R
T_F
80 %
20 %
$+V_{OD}$
$-V_{OD}$
$(V_{RSDS}N) - (V_{RSDS}P)$
0V Differential

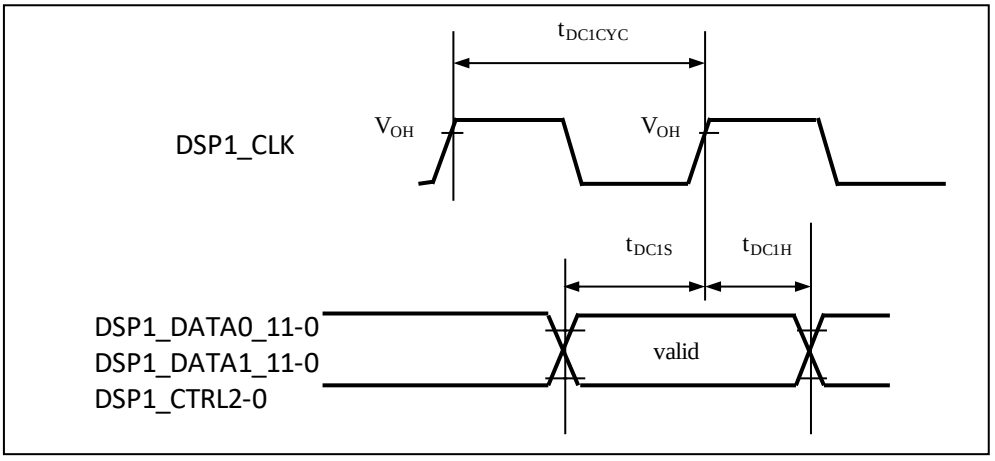
8.4.12.3 Display Controller1 Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	t_{DC1CYC}	DSP1_CLK	(C_L = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA),	20.0	-	ns	
Data/Control output to DSP1_CLK time	t_{DC1S}	DSP1_DATA0_11-0 DSP1_DATA1_11-0 DSP1_CTRL2-0		t_{DC1CYC} – 4.3	-	ns	*1
				t_{DC1CYC} – 4.2			*2
				t_{DC1CYC} – 4.1			*3
DSP1_CLK to Data/Control valid time	t_{DC1H}			-4.7	-	ns	*1
				-2.4			*2
				-2.3			*3

Notes:

- *For *1, it is targeted by the product series with function digit 3 to 9 and revision digit F.*
- *For *2, it is targeted by the product series with function digit 3 to 9 and revision digit M, P.*
- *For *3, it is targeted by the product series with function digit K to N.*
- *Values valid for unshifted display clock (dsp_ClockInvert=0, dsp_ClockShift=0).*
- *The clock output delay can be adjusted. See the "Graphic Subsystem" chapter in the TRM for details.*

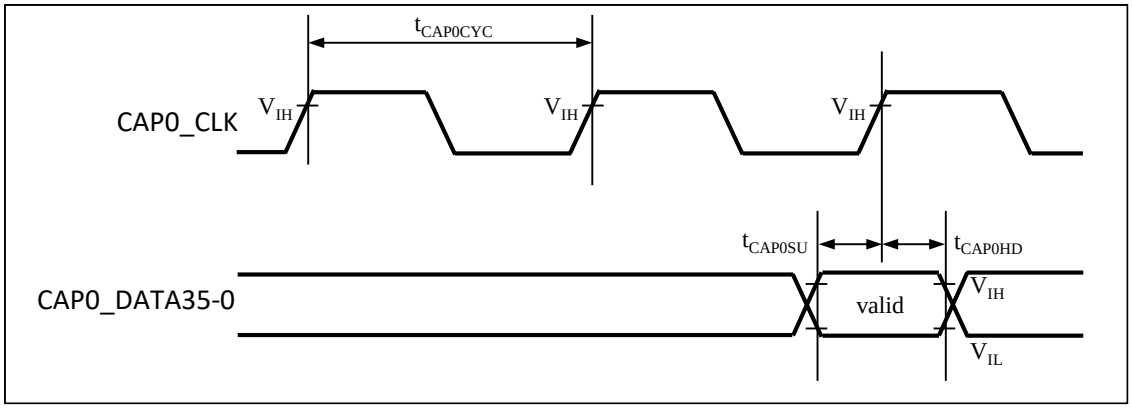


8.4.13 Video Capture

8.4.13.1 Video Capture Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Clock Cycle	$t_{CAP0CYC}$	CAP0_CLK	-	12.5	-	ns	
Capture data setup time	t_{CAP0SU}	CAP0_DATA35~0		4.0	-	ns	
Capture data hold time	t_{CAP0HD}	CAP0_DATA35~0		1.0	-	ns	



8.4.14 FPD-Link (LVDS)

8.4.14.1 For Revision M, P

(See Figure 2-1: Option and Part Number for S6J320C.)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output clock frequency	f	-	5	-	50	MHz	
Differential output voltage	V_{OD}	R_L = 100 Ω C_L = 5 pF (differential)	210	300	390	mV	One of three is selectable
			250	350	450	mV	
			295	400	505	mV	
Variation of V_{OD}	delta V_{OD}		-	-	25	mV	
Common mode voltage	V_{CM}		1.075	1.200	1.325	V	One of two is selectable
			1.125	1.250	1.375	V	
Variation of V_{CM}	delta V_{CM}		-	-	25	mV	
Cycle time of TXCLKP/M	T_{CIP}	-	20	T	200	ns	Equals 1/f
Duty of TXCLKP/M	T_{CDT}	-	-	4 / 7 x T	-	ns	
Internal PLL lockup time	T_{PLLL}	-	-	-	10	ms	
Cycle to cycle jitter	T_{C2C}	-	-	-	0.11 x T / 7	ns	
Channel to Channel skew of TXOUTxP/M	T_{CSK}	-	-	-	200	ps	
Skew of TXOUTxP and TXOUTxM	T_{DSK}	-	-	-	50	ps	
Output pulse position for bit 0	T_0	f = 50 MHz	-0.235	0	+0.235	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.235	1 / 7 x T	1 / 7 x T +0.235	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.235	2 / 7 x T	2 / 7 x T +0.235	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.235	3 / 7 x T	3 / 7 x T +0.235	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.235	4 / 7 x T	4 / 7 x T +0.235	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.235	5 / 7 x T	5 / 7 x T +0.235	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.235	6 / 7 x T	6 / 7 x T +0.235	ns	
Output pulse position for bit 0	T_0	f = 40 MHz	-0.25	0	+0.25	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.25	1 / 7 x T	1 / 7 x T +0.25	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.25	2 / 7 x T	2 / 7 x T +0.25	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.25	3 / 7 x T	3 / 7 x T +0.25	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.25	4 / 7 x T	4 / 7 x T +0.25	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.25	5 / 7 x T	5 / 7 x T +0.25	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.25	6 / 7 x T	6 / 7 x T +0.25	ns	

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output pulse position for bit 0	T_0	f = 25 MHz	-0.45	0	+0.45	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.45	1 / 7 x T	1 / 7 x T +0.45	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.45	2 / 7 x T	2 / 7 x T +0.45	ns	
Output pulse position for bit 3	T_3		3 / 7 x T - 0.45	3 / 7 x T	3 / 7 x T +0.45	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.45	4 / 7 x T	4 / 7 x T +0.45	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.45	5 / 7 x T	5 / 7 x T +0.45	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.45	6 / 7 x T	6 / 7 x T +0.45	ns	
Output pulse position for bit 0	T_0	f = 5 MHz	-2.00	0	+2.00	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -2.00	1 / 7 x T	1 / 7 x T +2.00	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -2.00	2 / 7 x T	2 / 7 x T +2.00	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -2.00	3 / 7 x T	3 / 7 x T +2.00	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -2.00	4 / 7 x T	4 / 7 x T +2.00	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -2.00	5 / 7 x T	5 / 7 x T +2.00	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -2.00	6 / 7 x T	6 / 7 x T +2.00	ns	

Notes:

- *All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.*
- *Channel to Channel skew of TXOUTxP/M is included in output pulse position.*

8.4.14.2 For Revision F

(See Figure 2-1: Option and Part Number for S6J320C.)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Output clock frequency	f	-	10	-	50	MHz	
Differential output voltage	V_{OD}	R_L = 100 Ω C_L = 5 pF (differential)	210	300	390	mV	One of three is selectable
			250	350	450	mV	
			295	400	505	mV	
Variation of V_{OD}	delta V_{OD}		-	-	25	mV	
Common mode voltage	V_{CM}		1.075	1.200	1.325	V	One of two is selectable
			1.125	1.250	1.375	V	
Variation of V_{CM}	delta V_{CM}		-	-	25	mV	
Cycle time of TXCLKP/M	T_{CIP}	-	20	T	100	ns	Equals 1/f
Duty of TXCLKP/M	T_{CDT}	-	-	4 / 7 x T	-	ns	
Channel to Channel skew of TXOUTxP/M	T_{CSK}	-	-	-	200	ps	
Skew of TXOUTxP and TXOUTxM	T_{DSK}	-	-	-	50	ps	
Output pulse position for bit 0	T_0	f = 50 MHz	-0.25	0	+0.25	ns	
Output pulse position for bit 1	T_1		1 / 7 x T -0.25	1 / 7 x T	1 / 7 x T +0.25	ns	
Output pulse position for bit 2	T_2		2 / 7 x T -0.25	2 / 7 x T	2 / 7 x T +0.25	ns	
Output pulse position for bit 3	T_3		3 / 7 x T -0.25	3 / 7 x T	3 / 7 x T +0.25	ns	
Output pulse position for bit 4	T_4		4 / 7 x T -0.25	4 / 7 x T	4 / 7 x T +0.25	ns	
Output pulse position for bit 5	T_5		5 / 7 x T -0.25	5 / 7 x T	5 / 7 x T +0.25	ns	
Output pulse position for bit 6	T_6		6 / 7 x T -0.25	6 / 7 x T	6 / 7 x T +0.25	ns	

Notes:

- *All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.*
- *Channel to Channel skew of TXOUTxP/M is included in output pulse position.*

Figure 8-6: LVDS AC Timing Chart

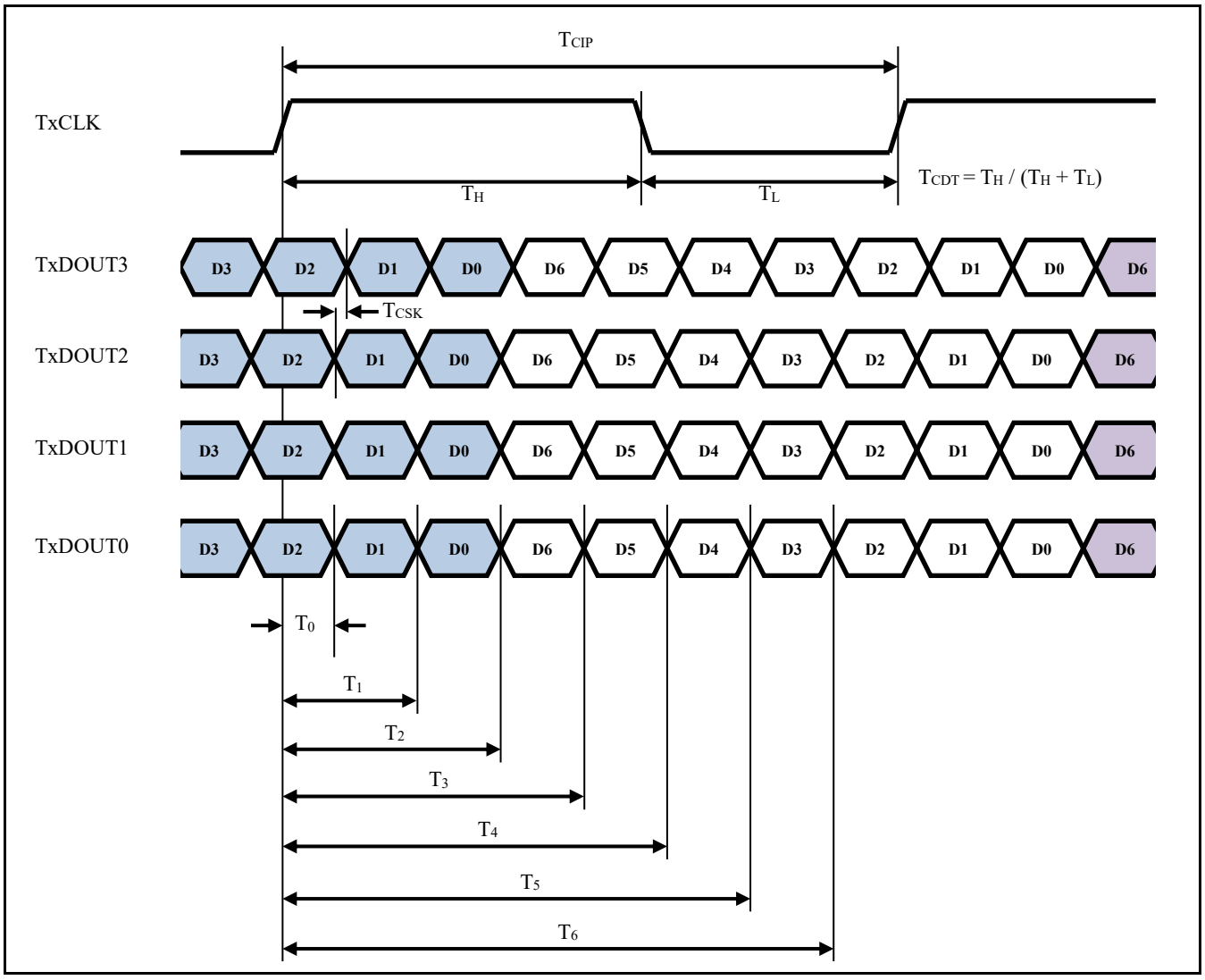
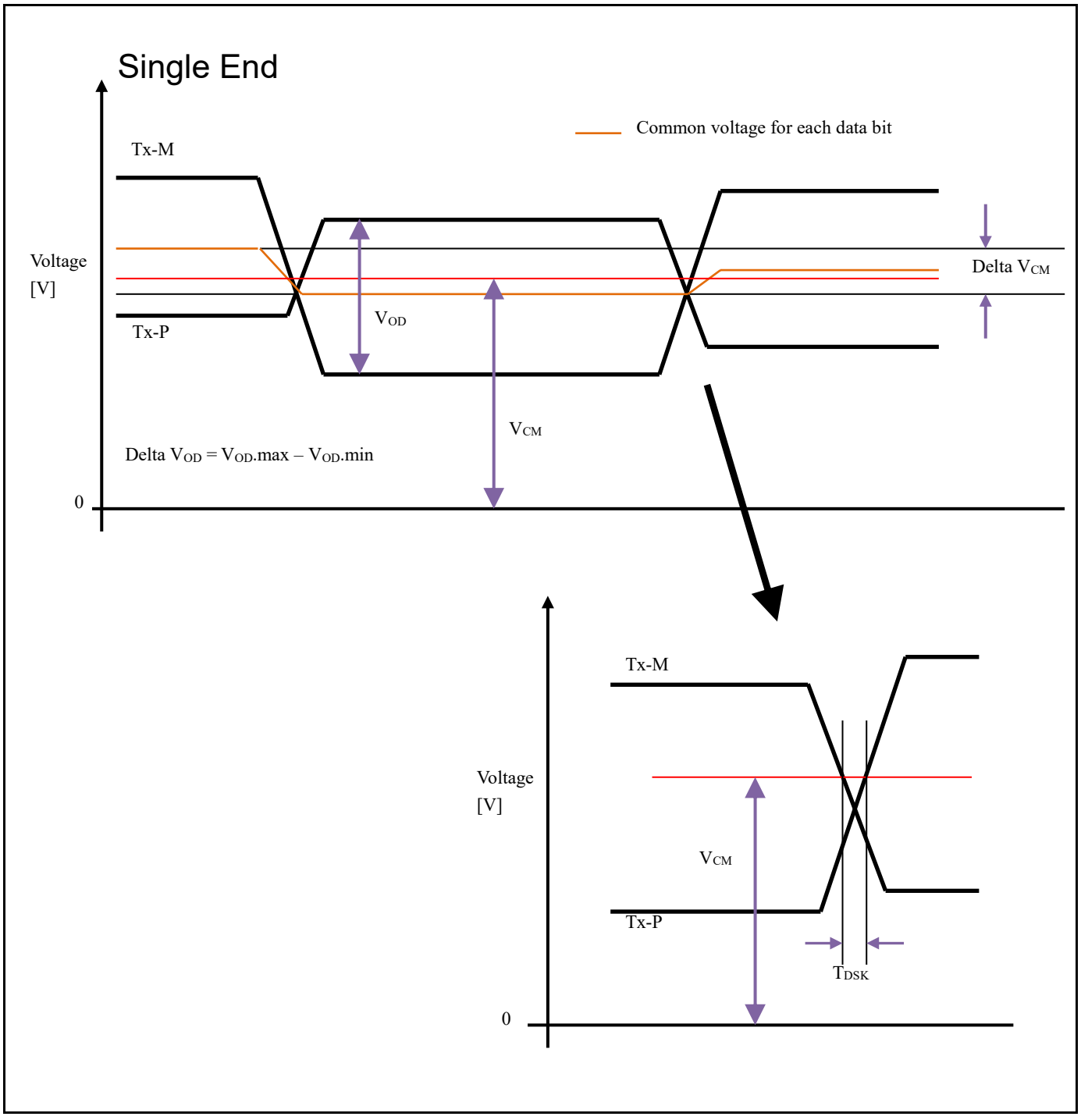


Figure 8-7: LVDS AC Timing Chart



8.4.15 DDR-HSSPI

DDR-HSSPI AC characteristics are specified with the specific reference voltage of VIL, VIH, VOL, VOH = 0.5 Vcc3 as mentioned in Section 8.4.3, regardless of automotive input-level configuration, CMOS Schmitt, and TTL.

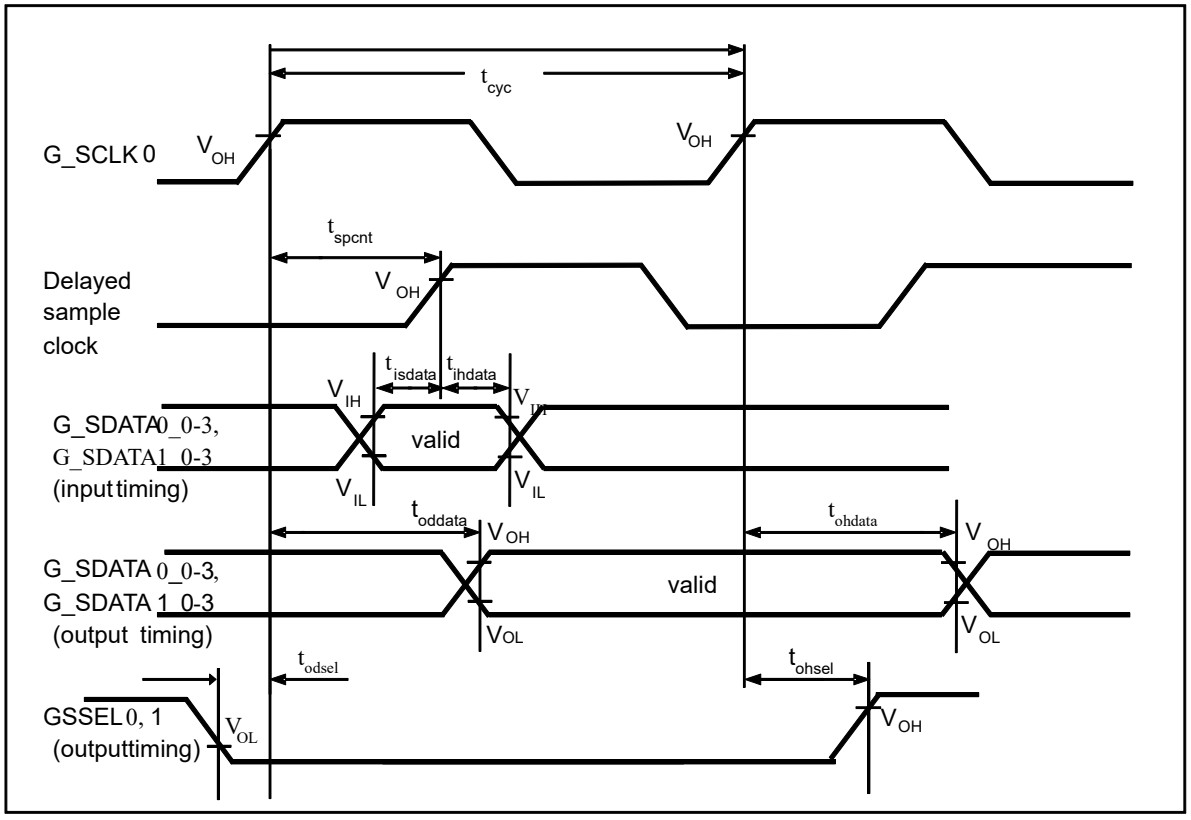
8.4.15.1 DDR-HSSPI Interface Timing (SDR Mode)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HSSPI clock cycle	t_{cyc}	G_SCLK0 M_SCLK0	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	10	-	ns	
				20	-		when Quad Page Program
G_SCLK↑ -> delayed sample clock↑	t_{spcnt}	-		0	31.5	ns	
GSDATA -> G_SCLK↑ Input setup time	t_{isdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ -> GSDATA Input hold time	t_{ihdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑ -> GSDATA Output delay time	t_{oddata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		-	tcyc/2 + 2	ns	
G_SCLK↑ -> GSDATA Output hold time	t_{ohdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		tcyc/2 - 3	-	ns	
GSSEL↓ -> G_SCLK Output delay time	t_{odsel}	G_SSEL0, 1 M_SSEL0, 1		- 12.00+(SS 2CD+0.5)*t cyc	-	ns	
G_SCLK↑ -> GSSEL Output hold time	t_{ohsel}	G_SSEL0, 1 M_SSEL0, 1		tcyc - 2	-	ns	

Notes:

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*


t cyc
G_SCLK 0
V OH
V OH
t spcnt
Delayed
sample
clock
V OH
t isdata
t ihdata
V IH
V IH
G_SDATA0_0-3,
G_SDATA1_0-3
(input timing)
valid
V IL
V IL
t oddata
t ohdata
V OH
V OH
G_SDATA 0_0-3,
G_SDATA 1_0-3
(output timing)
valid
VOL
V OL
t odsel
t ohsel
GSSEL 0, 1
(outputtiming)
V OL
V OH

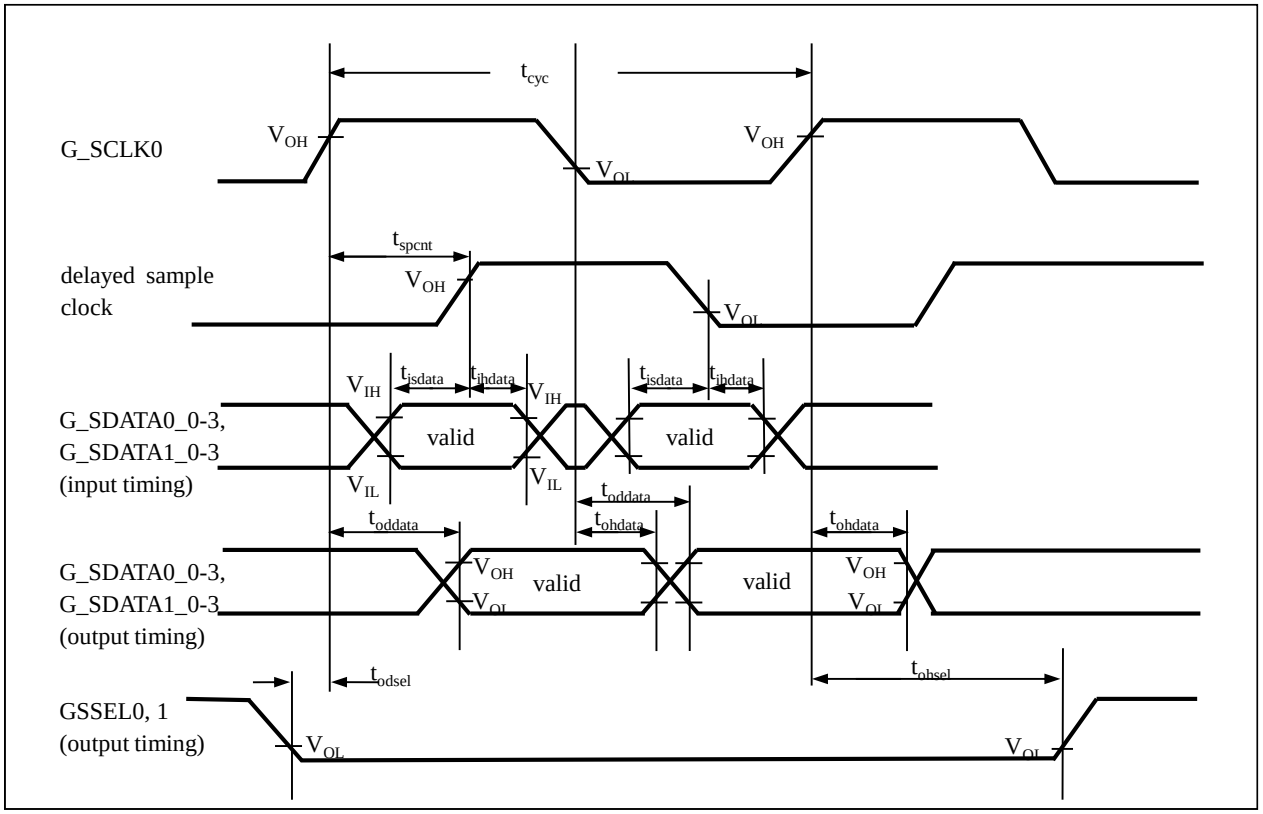
8.4.15.2 DDR-HSSPI Interface Timing (DDR Mode)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
HSSPI clock cycle	t_{cyc}	G_SCLK0 M_SCLK0	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	
G_SCLK↑↓ -> delayed sample clock↑	t_{spcnt}	-		0	31.5	ns	
GSDATA -> G_SCLK↑↓ Input setup time	t_{isdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑↓ -> GSDATA Input hold time	t_{ihdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		*1	-	ns	
G_SCLK↑↓ -> GSDATA Output delay time	t_{oddata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		-	tcyc/4 + 1.5	ns	
G_SCLK↑↓ -> GSDATA Output hold time	t_{ohdata}	G_SDATA0_0-3 G_SDATA1_0-3 M_SDATA0_0-3 M_SDATA1_0-3		Tcyc/4 - 1.0	-	ns	
GSSEL ↓ -> G_SCLK Output delay time	t_{odsel}	G_SSEL0, 1 M_SSEL0, 1		- 15.75+(SS 2CD+0.5)*t cyc	-	ns	
G_SCLK↑ -> GSSEL Output hold time	t_{ohsel}	G_SSEL0, 1 M_SSEL0, 1		0.75*tcyc - 2.0	-	ns	

Notes:

- *SS2CD [1:0] should be configured as 01, 10, or 11.*
- *For *1, the delay of the delay sample clock can be configured (DLP function).*


t_{cyc}
G_SCLK0
V_{OH}
V_{OL}
t_{spcnt}
delayed sample clock
V_{IH}
V_{IL}
t_{isdata}
t_{ihdata}
G_SDATA0_0-3, G_SDATA1_0-3 (input timing)
valid
t_{oddata}
t_{ohdata}
G_SDATA0_0-3, G_SDATA1_0-3 (output timing)
t_{odsel}
t_{ohsel}
GSSEL0, 1 (output timing)

8.4.16 HyperBus

HyperBus AC characteristics are specified with the specific reference voltage of VIL, VIH, VOL, VOH = 0.5Vcc3 as 8.4.3 regardless of input level configuration automotive, CMOS Schmitt, and TTL.

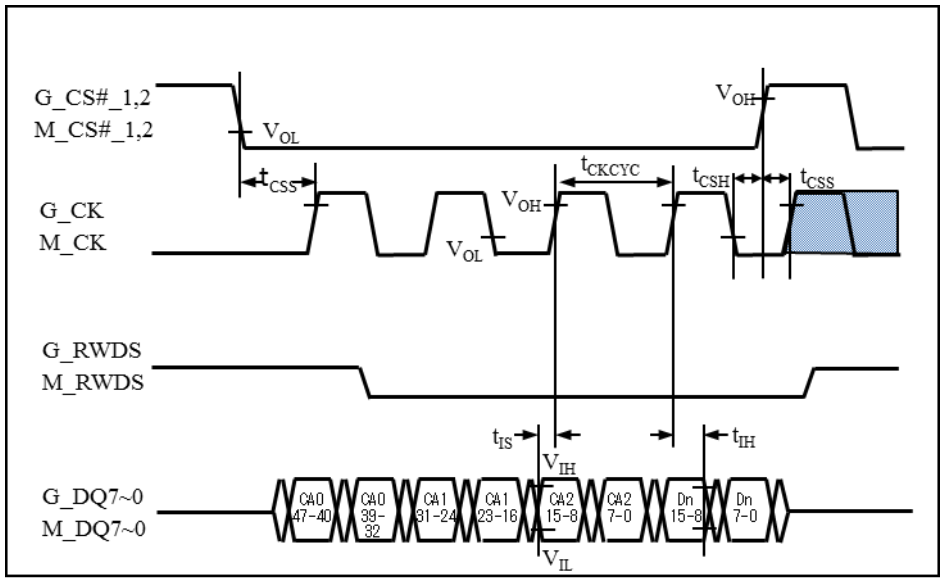
8.4.16.1 HyperBus Write Timing (HyperFlash)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{CKCYC}	G_CK M_CK	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	(A)
				10	-	ns	(B)
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC} - 3.25	-	ns	(A)
				t_{CKCYC} -2.0	-	ns	(B)
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC}/2	-	ns	

Notes:

- *(A): The value will be targeted by the product series with revision digit A.*
- *(B): The value will be targeted by the product series with after revision digit B.*
- *Hyper Bus clock cycle is always (1/F_{CLK_CD1})*4.*



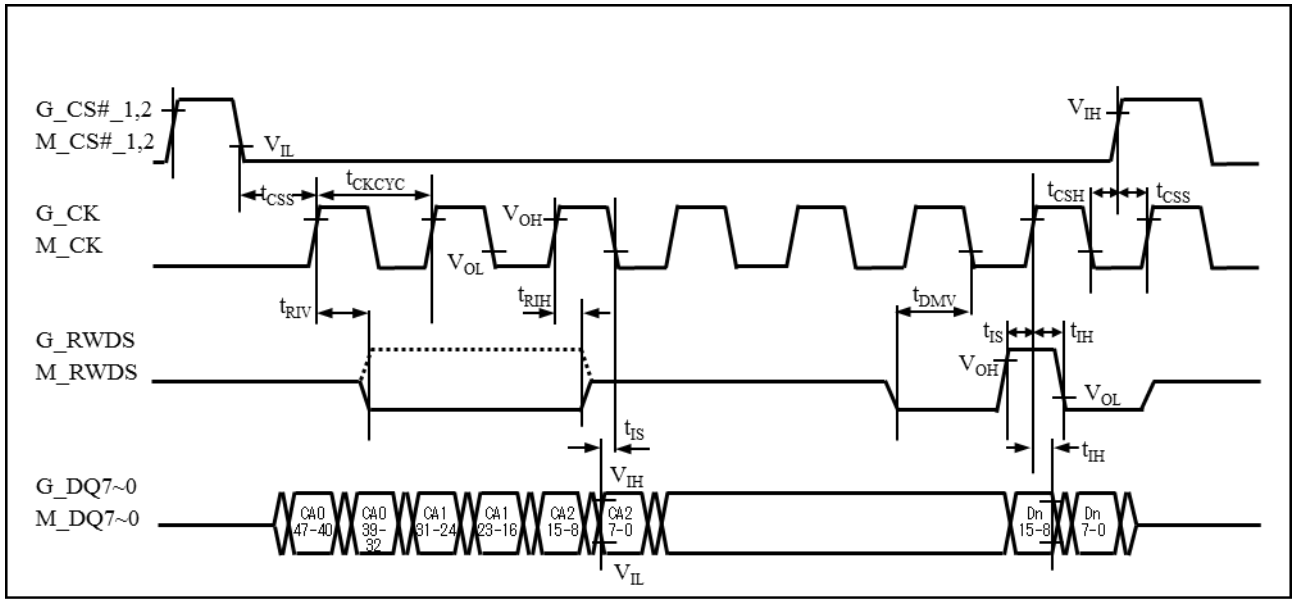
8.4.16.2 Hyper Bus Write Timing (HyperRAM)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{CKCYC}	G_CK M_CK	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	(A)
				10	-	ns	(B)
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC} - 3.25	-	ns	(A)
				t_{CKCYC} - 2.0	-	ns	(B)
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{CKCYC}/2	-	ns	
RWDS↓-> CK↓ Data Mask Valid	t_{DMV}	G_RWDS M_RWDS		1	-	ns	
CK↑ -> RWDS↑↓ Refresh Indicator Valid	t_{RIV}	G_RWDS M_RWDS		-	6	ns	
CK↑ -> RWDS(Hi-z) Refresh Indicator Hold	t_{RIH}	G_RWDS M_RWDS		0	-	ns	

Notes:

- *(A): The value is targeted by the product series with revision digit A.*
- *(B): The value is targeted by the product series with after revision digit B.*
- *Hyper Bus clock cycle is always (1/F_{CLK_CD1})*4.*
- *When configuring the HyperBus clock cycle, take into account the HyperRAM refresh interval.*

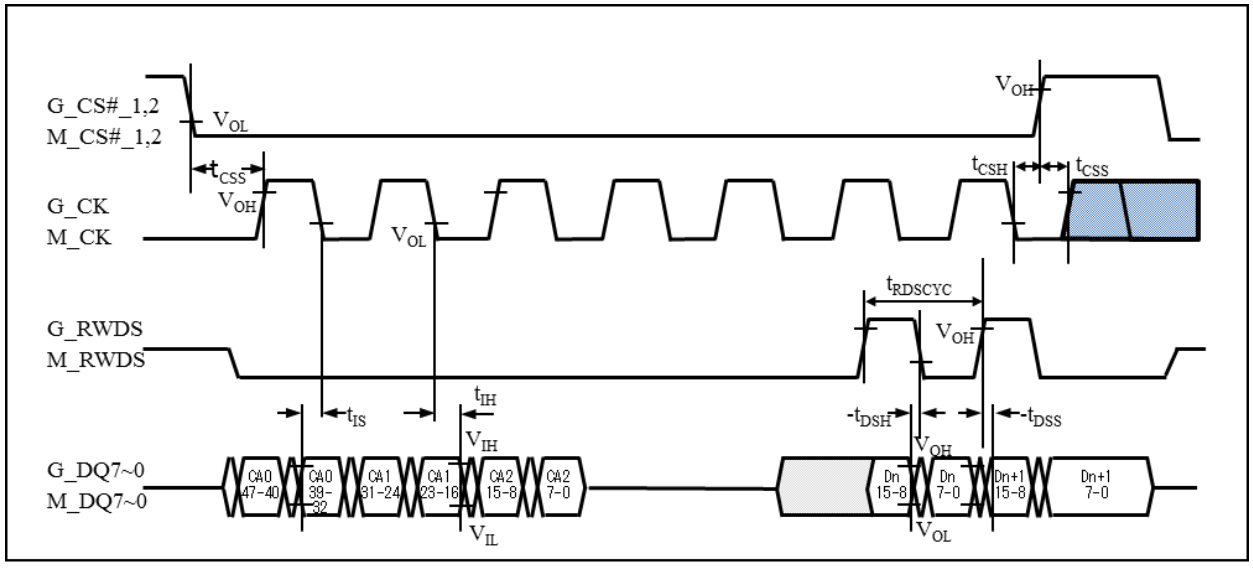


8.4.16.3 Hyper Bus Read Timing (HyperFlash)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{RDSCYC}	G_CK, G_RWDS M_CK, M_RWDS	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	(A)
				10	-	ns	(B)
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} - 3.25	-	ns	(A)
				t_{RDSCYC} -2.0		ns	(B)
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} / 2	-	ns	
DQ-> RDS↑↓ Setup time	t_{DSS}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.85	-		(C)
RDS↑↓-> DQ Hold time	t_{DSH}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.9	-		(C)

- *(A): The value is targeted by the product series with revision digit A.*
- *(B): The value is targeted by the product series with after revision digit B.*
- *(C): The value is targeted by the product series with function digit 3 to 9 and revision digit H, M, P.*
- *Hyper Bus clock cycle is always ($1/F_{CLK_CD1}$)*4.*



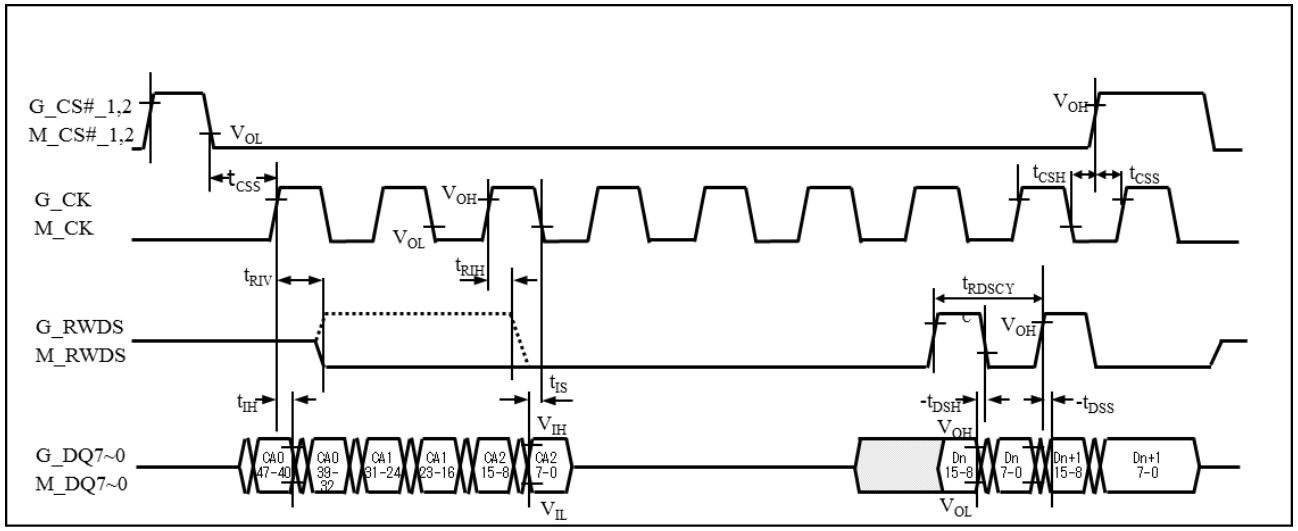
8.4.16.4 Hyper Bus Read Timing (HyperRAM)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Hyper Bus clock cycle	t_{RDSCYC}	G_CK, G_RWDS M_CK, M_RWDS	(C_L = 20 pF, I_{OL}=-10 mA, I_{OH}=10 mA),	12.5	-	ns	(A)
				10	-	ns	(B)
CS↑↓ -> CK↑ Chip Select setup time	t_{CSS}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} -3.25	-	ns	(A)
				t_{RDSCYC} -2.0	-	ns	(B)
DQ -> CK↑↓ Setup time	t_{IS}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↑↓ -> DQ Hold time	t_{IH}	G_DQ7-0 M_DQ7-0		1.25	-	ns	
CK↓ -> CS↑ Chip select hold time	t_{CSH}	G_CS#_1,2 M_CS#_1,2		t_{RDSCYC} /2	-	ns	
DQ-> RWDS↑↓ (valid) Setup time	t_{DSS}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.85	-		(C)
RWDS↑↓-> DQ (invalid) Hold time	t_{DSH}	G_DQ7-0 M_DQ7-0		-0.8	-	ns	
				-0.9	-		(C)
CK↑ -> RWDS↑↓ Refresh Indicator Valid	t_{RIV}	G_RWDS M_RWDS		-	6	ns	
CK↑ -> RWDS(Hi-z) Refresh Indicator Hold	t_{RIH}	G_RWDS M_RWDS		0	-	ns	

Notes:

- *(A): The value is targeted by the product series with revision digit A.*
- *(B): The value is targeted by the product series with after revision digit B.*
- *(C): The value is targeted by the product series with function digit 3 to 9 and revision digit H, M, P.*
- *Hyper Bus clock cycle is always (1/F_{CLK_CD1})*4.*
- *When configuring the HyperBus clock cycle, take into account the HyperRAM refresh interval.*

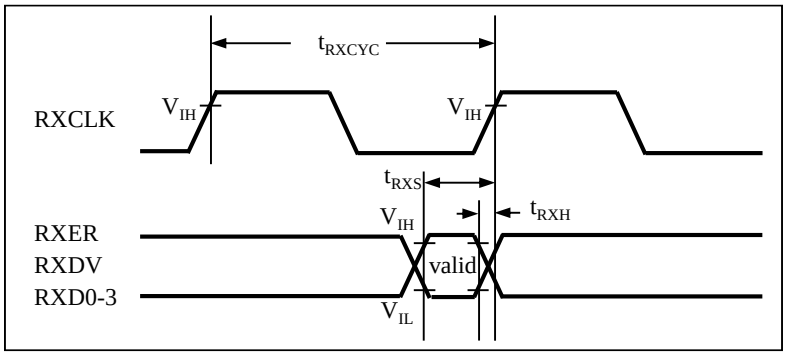


8.4.17 Ethernet AVB

8.4.17.1 Ethernet Receive Timing

(Condition: See 8.2.Operation Assurance Condition)

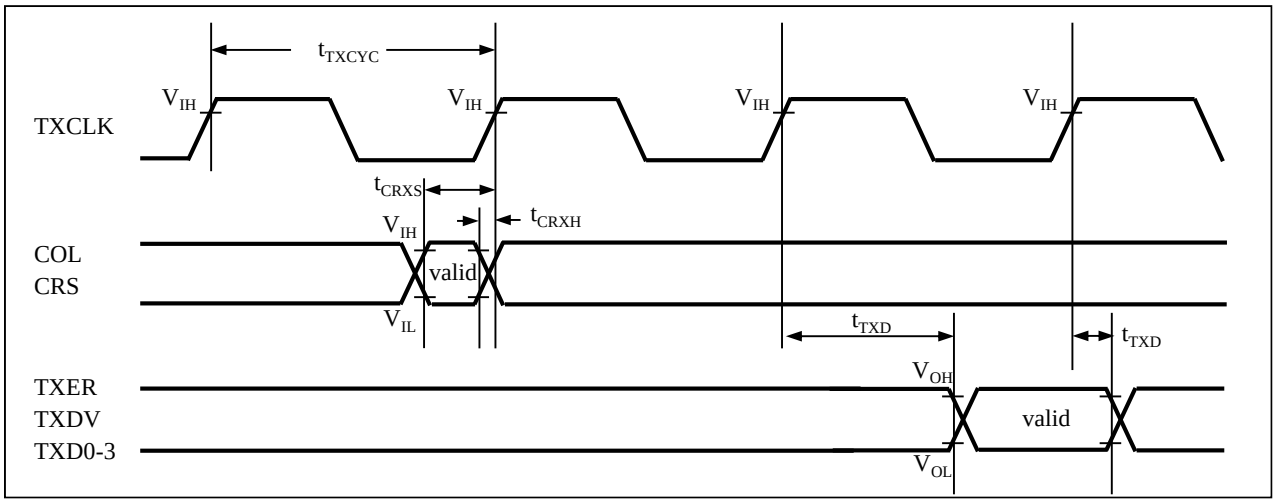
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
RXCLK cycle	t_{RXCYC}	RXCLK	-	40.0	-	ns	
RX setup time	t_{RXS}	RXER RXDV RXD0-3		10.0	-	ns	t_{RXCYC} -30ns
RX hold time	t_{RXH}	RXER RXDV RXD0-3		0	-	ns	



8.4.17.2 Ethernet Transmit Timing

(Condition: See 8.2.Operation Assurance Condition)

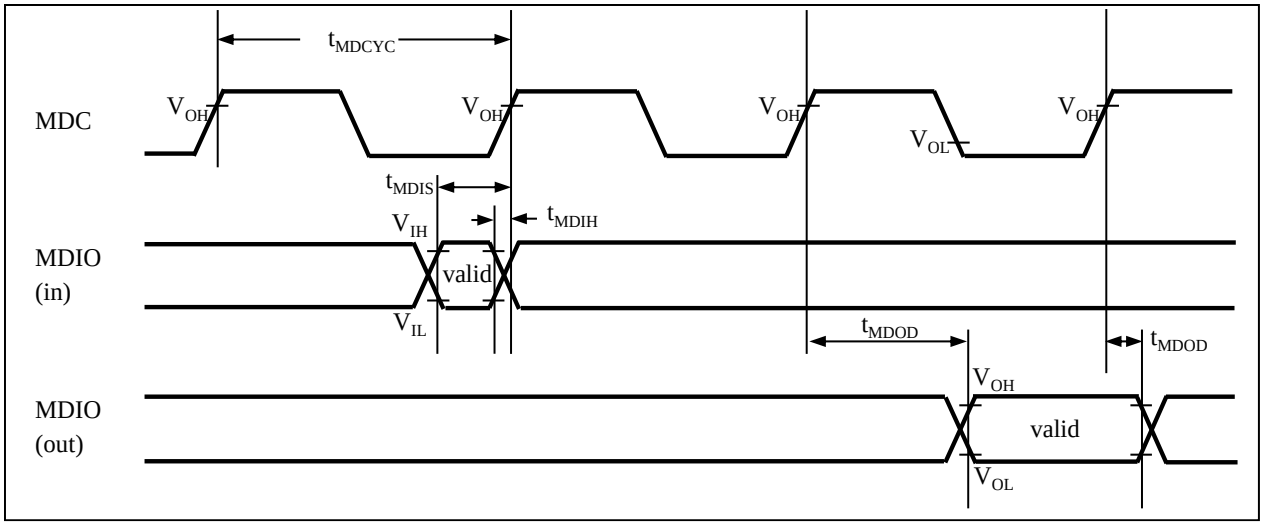
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TXCLK cycle	t_{TXCYC}	RXCLK	(C_L = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA),	40.0	-	ns	
COL/CRS input setup time	t_{CRXS}	COL CRS		12.0	-	ns	
COL/CRS input hold time	t_{CRXH}	COL CRS		0.5	-	ns	
Tx delay time	t_{TXD}	TXER TXDV TXD0-3		0.5	25	ns	



8.4.17.3 MDIO Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MDC cycle	t_{MDCYC}	MDC	(C_L = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA),	400.0	-	ns	
MDIO input setup time	t_{MDIS}	MDIO		100.0	-	ns	
MDIO input hold time	t_{MDIH}	MDIO		0.0	-	ns	
MDIO output delay time	t_{MDOD}	MDIO		10.0	190.0	ns	



8.4.18 MediaLB

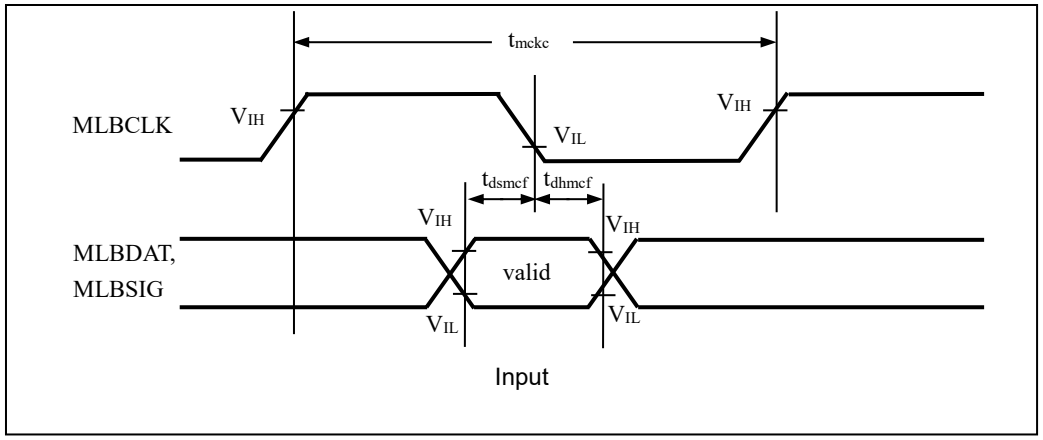
8.4.18.1 MediaLB Input Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	-	40	-	ns	
MLBSIG, MLBDAT Input setup	t_{dsmcf}	MLBSIG MLBDAT		1.0	-	ns	
MLBSIG, MLBDAT Input hold	t_{dhmcf}	MLBSIG MLBDAT		4.0	-	ns	

Note:

- *CLK_HAPP1B0 (internal) frequency > MLBCLK (external) frequency*



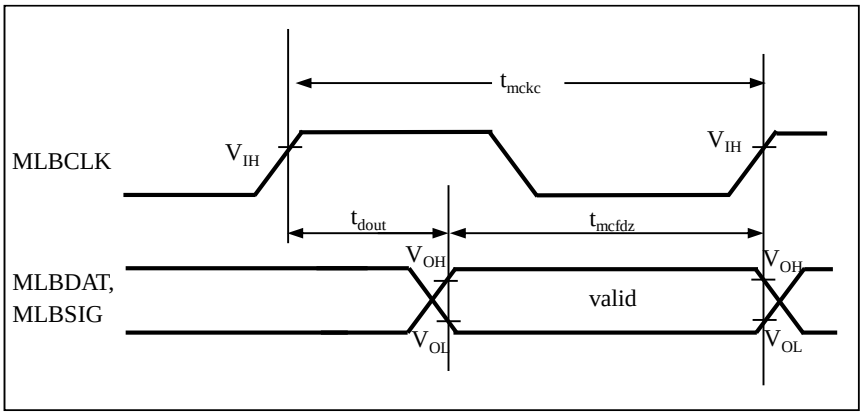
8.4.18.2 MediaLB Output Timing

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MLBCLK cycle	t_{mckc}	MLBCLK	(C_L = 20 pF, I_{OL}=-6 mA, I_{OH}=6 mA),	40	-	ns	
MLBSIG, MLBDAT output stop	t_{mcfdz}	MLBSIG MLBDAT		26.5	-	ns	t_{mckc} - t_{dout}
MLBSIG, MLBDAT output delay	t_{dout}	MLBSIG MLBDAT		0	13.5	ns	

Note:

- *CLK_HAPP1B0 (internal) frequency > MLBCLK (external) frequency*



8.4.19 Port Noise Filter

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse filtered	-	ALL GPIO	-	67	-	ns	
Input pulse filtered	-	EINT0-15 or TIN0-3, 16-19, 32-35, 48, 49	-	67	-	ns	
Input pulse filtered	-	SCL4, 10, 12, 16, 17 Or SDA4, 10, 12, 16, 17	-	240	-	ns	

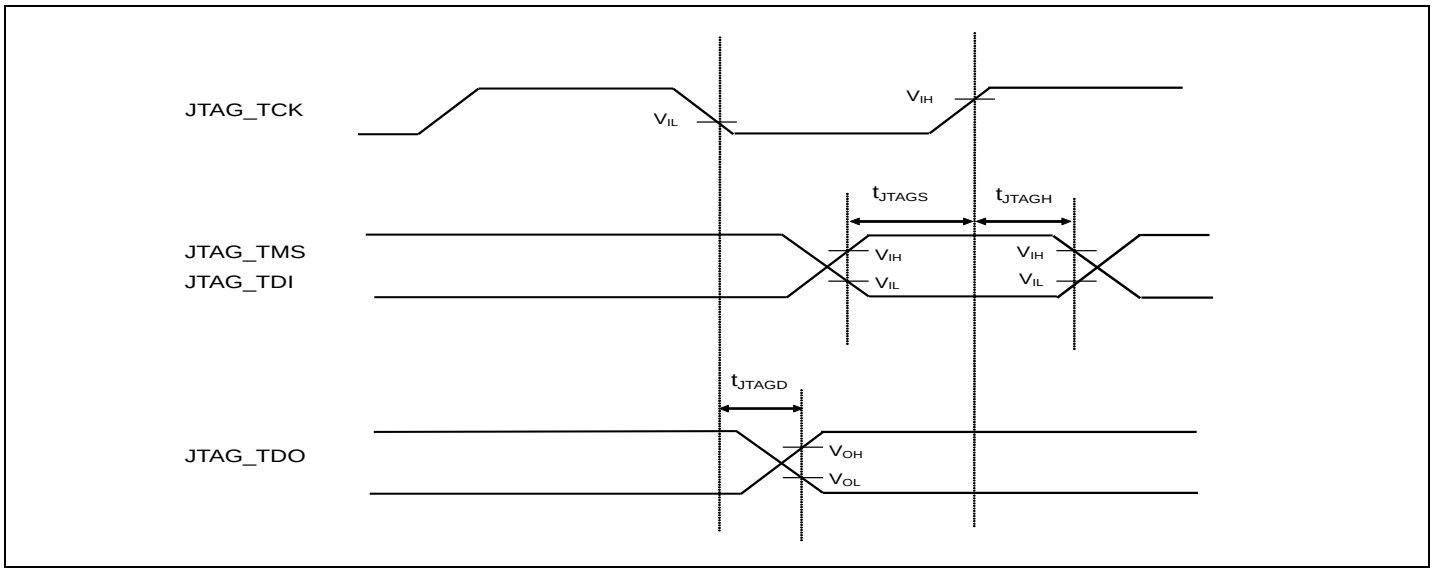
Note:

- *The spec guarantees that the rectangular pulse wider than min value is never removed.*

8.4.20 JTAG

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	JTAG_TCK, JTAG_TMS, JTAG_TDI	C_L = 20 pF	16	-	ns	
TMS, TDI hold time	t_{JTAGH}	JTAG_TCK, JTAG_TMS, TDI	C_L = 20 pF	10	-	ns	
TDO delay time	t_{JTAGD}	JTAG_TCK, JTAG_TDO	C_L = 20 pF	-	25	ns	



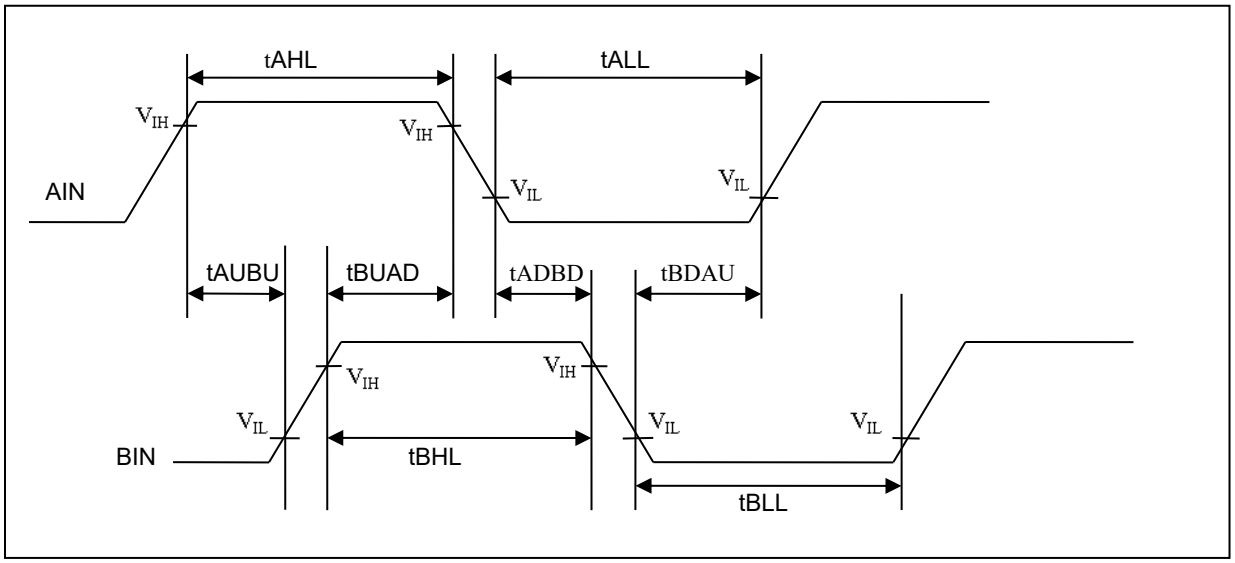
8.4.21 QPRC

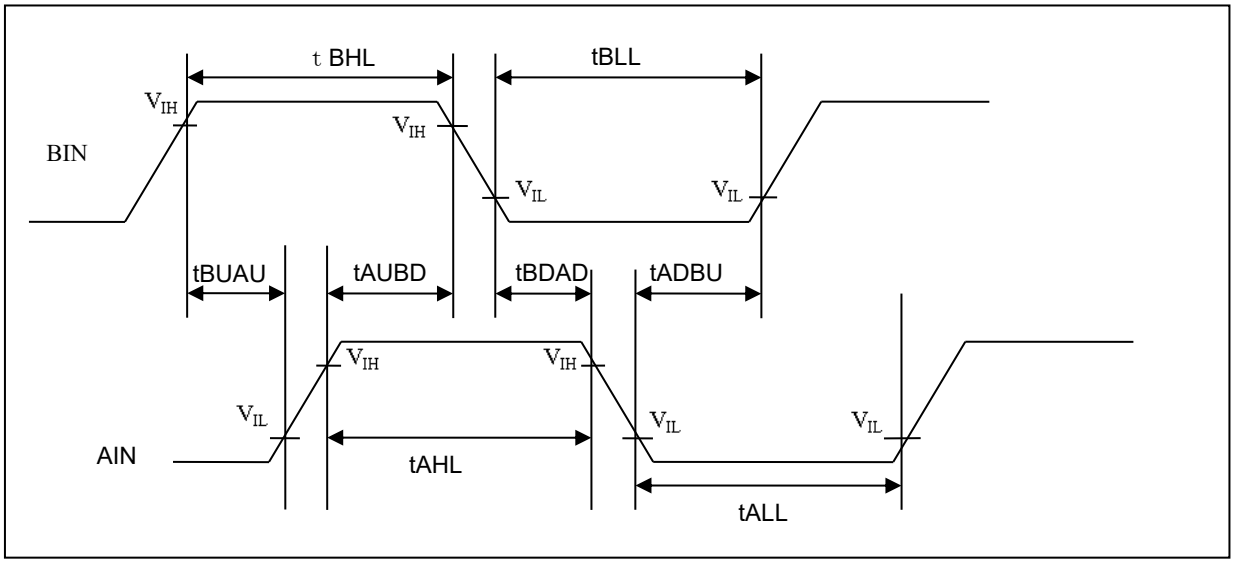
(Condition: See 8.2.Operation Assurance Condition)

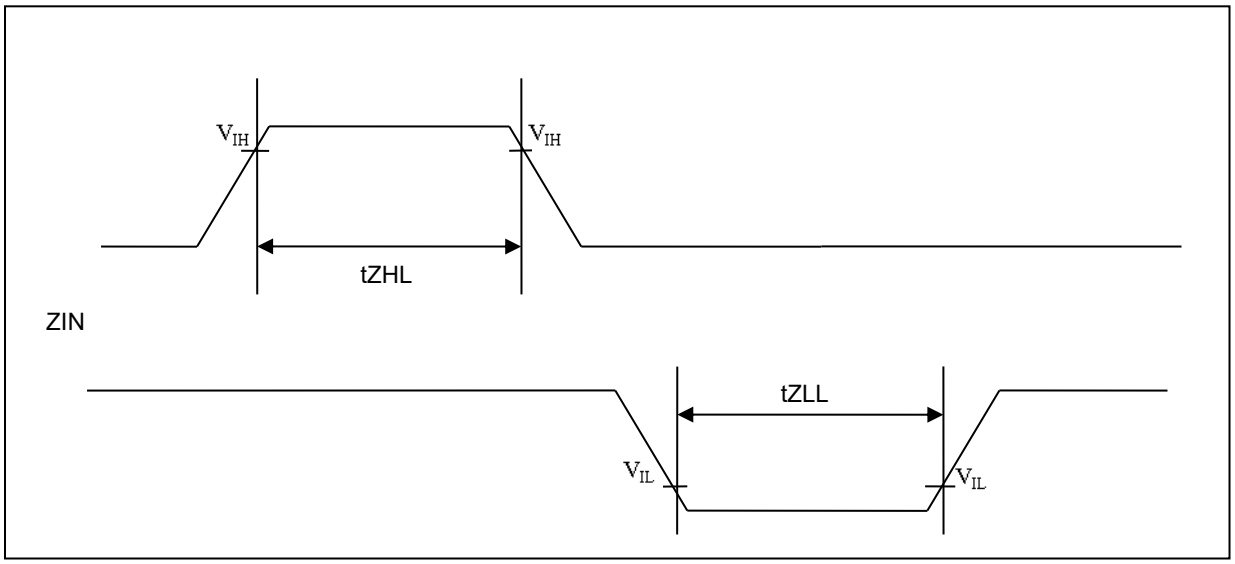
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
"H" width of AIN	tAHL	AIN	—	4tCLK_LCP1A	—	ns	
"L" width of AIN	tALL	AIN	—	4tCLK_LCP1A	—		
"H" width of BIN	tBHL	BIN	—	4tCLK_LCP1A	—	ns	
"L" width of BIN	tBLL	BIN	—	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "H" level of AIN	tAUBU	BIN	PC_Mode2 or PC_mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "H" level of BIN	tBUAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "L" level of AIN	tADBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "L" level of BIN	tBDAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "H" level of BIN	tBUAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "H" level of AIN	tAUBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "L" level of BIN	tBDAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "L" level of AIN	tADBU	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
"H" width of ZIN	tZHL	ZIN	QCR:CGSC="0"	4tCLK_LCP1A	—	ns	
"L" width of ZIN	tZLL	ZIN	QCR:CGSC="0"	4tCLK_LCP1A	—	ns	
Rising or falling timing of AIN/BIN from level valid timing of ZIN	tZABE	AIN/BIN	QCR:CGSC="1"	4tCLK_LCP1A	—	ns	
Level valid timing of ZIN from falling or rising timing of AIN/BIN	tABEZ	ZIN	QCR:CGSC="1"	4tCLK_LCP1A	—	ns	

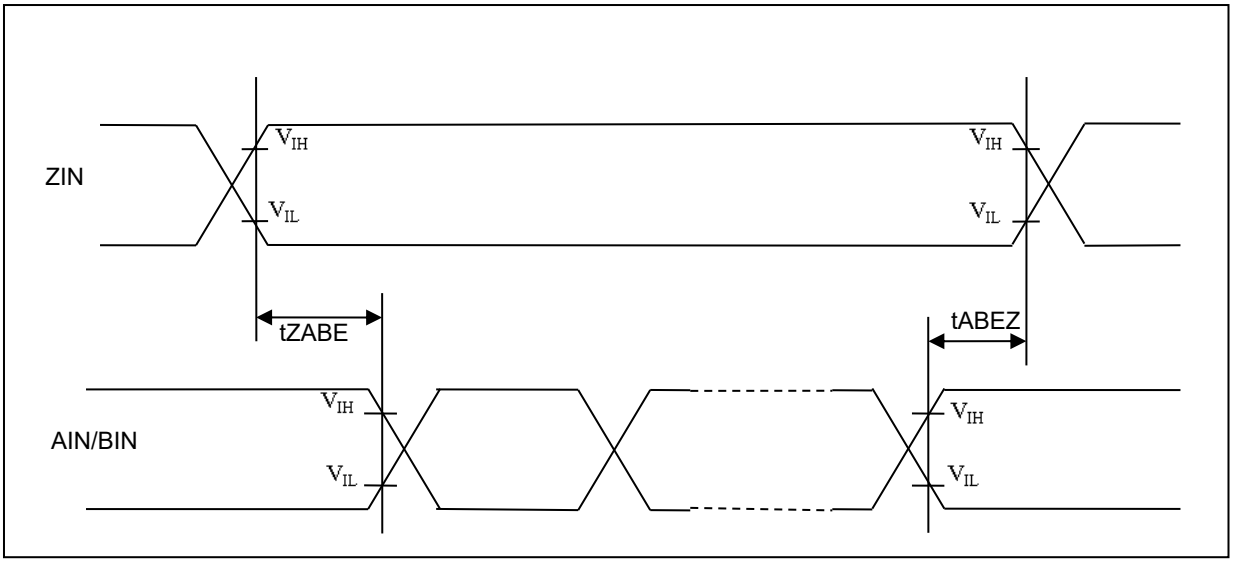
Note:

- *t is the period of peripheral clock (CLK)*


tAHL
tALL
VIH
VIH
AIN
VIL
VIL
tAUBU
tBUAD
tADBD
tBDAU
VIH
VIH
VIL
VIL
VIL
BIN
tBHL
tBLL


t BHL
tBLL
VIH
VIH
BIN
VIL
VIL
tBUAU
tAUBD
tBDAD
tADBU
VIH
VIH
VIL
VIL
VIL
AIN
tAHL
tALL


VIH
VIH
tZHL
ZIN
tZLL
VIL
VIL


ZIN
V_{IH}
V_{IL}
V_{IH}
V_{IL}
tZABE
tABEZ
AIN/BIN
V_{IH}
V_{IL}
V_{IH}
V_{IL}

8.4.22 I2S

8.4.22.1 I2S Timing – Master mode (MSMD=1)

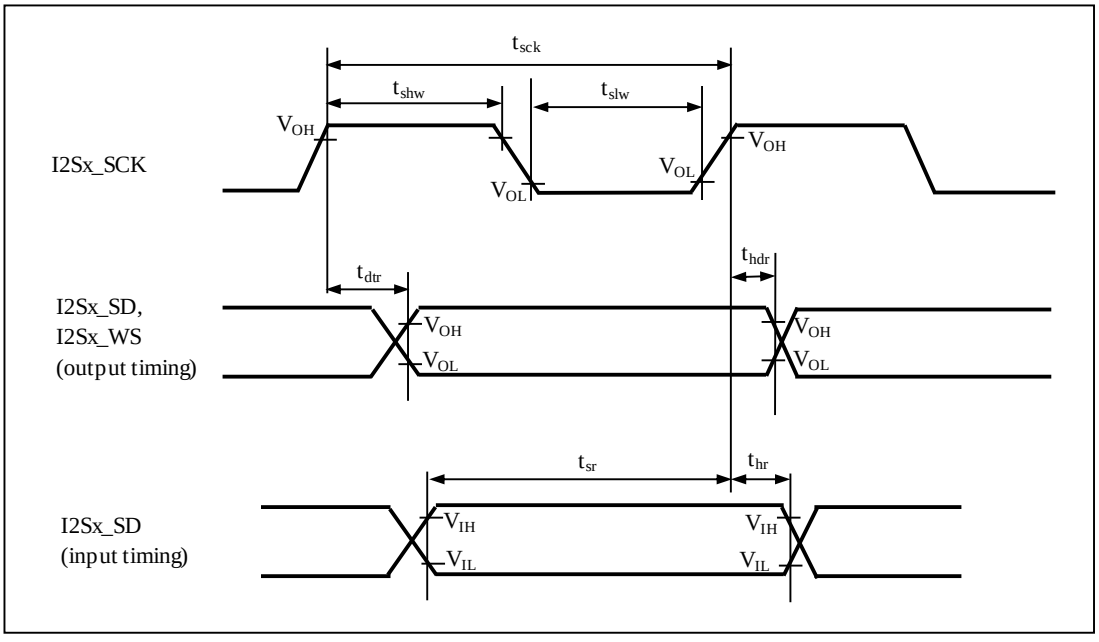
(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
ECLK0/ECLK1 clock cycle	t_{eck}	ECLK0, ECLK1	(C_L = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA) CPOL=0, SMPL=1	20	-	ns	Only relevant if external ECLK input is selected. *1
ECLK0/ECLK1 clock "H" pulse width	t_{ehw}			0.40* t_{eck}	0.60* t_{eck}	ns	
ECLK0/ECLK1 clock "L" pulse width	t_{elw}			0.40* t_{eck}	0.60* t_{eck}	ns	
I2S clock cycle (output SCK)	t_{sck}	I2S0_SCK, I2S1_SCK		66.66	-	ns	
I2S clock "H" pulse width	t_{shw}			0.35* t_{sck}	0.65* t_{sck}	ns	
I2S clock "L" pulse width	t_{slw}			0.35* t_{sck}	0.65* t_{sck}	ns	
Sender delay time SCK↑ -> SD/WS valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD, I2S0_WS, I2S1_WS		-	26	ns	*2
Sender hold time SCK↑ -> SD/WS invalid	t_{htr}			-10	-	ns	*2
Receiver setup time SD valid -> SCK↑	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		21	-	ns	*2
Receiver hold time SCK↑ -> SD valid	t_{hr}			10	-	ns	*2

Notes:

*1: ECKM = 1. Refer to the Resource Input Configuration chapter in TRM for required RESSEL register settings.

*2: See the I2S register description chapter in TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values as per above table will remain the same.



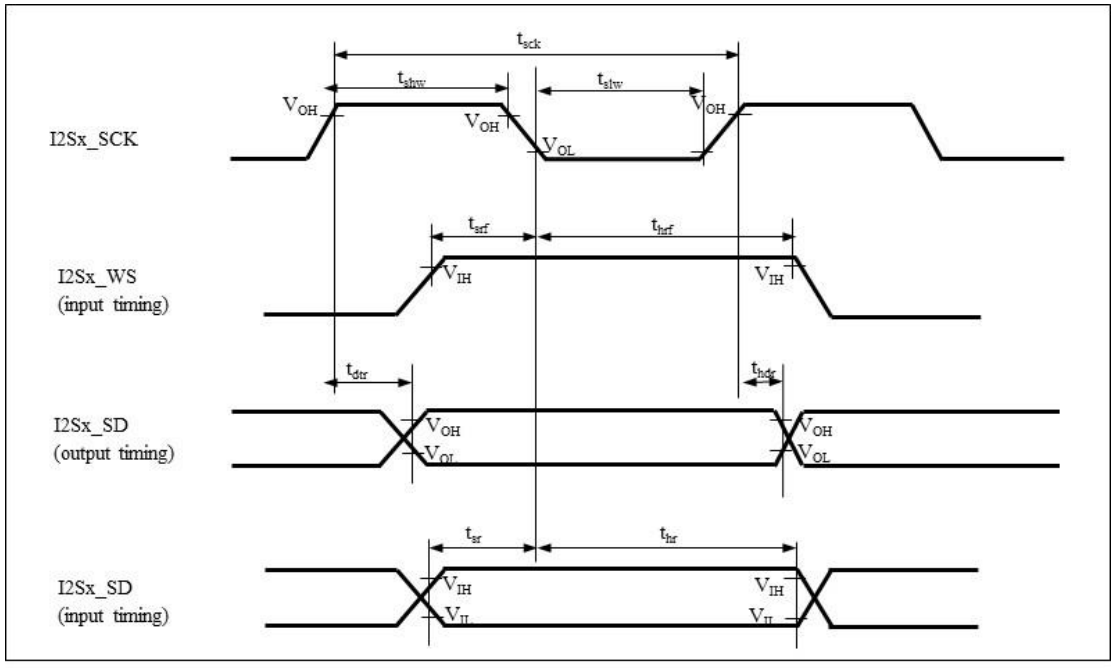
8.4.22.2 I2S Timing – Slave mode (MSMD=0)

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
I2S clock cycle (input SCK)	t_{sck}	I2S0_SCK, I2S1_SCK	(C_L = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA) CPOL=0, SMPL=0	66.66	-	ns	
I2S clock “H” pulse width	t_{shw}	I2S0_SCK, I2S1_SCK		0.40* t_{sck}	0.60* t_{sck}	ns	
I2S clock “L” pulse width	t_{slw}			0.40* t_{sck}	0.60* t_{sck}	ns	
Setup time WS transition -> SCK↓	t_{srf}	I2S0_SCK, I2S1_SCK, I2S0_WS, I2S1_WS		40	-	ns	*1
Hold time SCK↓ -> WS transition	t_{hrf}			10	-	ns	*1
Sender delay time SCK↑ -> SD valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		-	26	ns	*1
Sender hold time SCK↑ -> SD invalid	t_{htr}			-10	-	ns	*1
Receiver setup time SD valid -> SCK↓	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		21	-	ns	*1
Receiver hold time SCK↓ -> SD valid	t_{hr}			10	-	ns	*1

Note:

*1: See the I2S register description chapter in the TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values based on the table above will remain the same.



8.5 A/D Converter

8.5.1 Electrical Characteristics

(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Total Error	-	-	-	-	±12	LSB	*3
Integral Non linearity	-	-	-	-	±4.0	LSB	*4
Differential Non linearity	-	-	-	-	±1.9	LSB	*4
Zero transition voltage	V_{ZT}	AN0 to AN49	AVRL -11.5LSB	-	AVRL +12.5LSB	V	*5
Full-scale transition voltage	V_{FST}	AN0 to AN49	AVRH -13.5LSB	-	AVRH +10.5LSB	V	
Sampling time	t_{SMP}	-	0.3	-	-	µs	*1
Compare time	t_{CMP}	-	0.8	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.1	-	-	µs	*1
A/D trigger input time		ADTRG	$4t_{CLK_LCP1A}$	-	-	ns	$4t_{CLK_LCP1A} \geq$ 100ns
			100				$4t_{CLK_LCP1A} <$ 100ns
Resumption time	-	-	-	-	1	us	-
Analog port input current	I_{AIN}	AN0 to AN17	-1.0	-	1.0	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
		AN18 to AN25	-2.0	-	2.0	µA	
		AN26 to AN49	-3.0	-	3.0	µA	
Analog input voltage	V_{AIN}	AN0 to AN49	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVRH5	4.5	-	5.5	V	$AV_{CC} \geq$ AVRH
	AVRL	AVSS	-	0.0	-	V	
Power supply current	I_A	AVCC	-	500	900	µA	
	I_{AH}		-	1.0	100	µA	*2
	I_R	AVRH	-	1.0	2.0	mA	
	I_{RH}		-	-	5.0	µA	*2
Variation between channels	-	AN0 to AN49	-	-	4.0	LSB	

*1: Time per channel

*2: Definition of the power supply current (when V_{CC}=AV_{CC}=5.0 V) while the A/D converter is not operating and in stop mode

*3: Total Error is a comprehensive static error that includes the linearity after trimming by software.
1LSB= (AVRH-AVRL)/4096

*4: 1LSB= (VFST-VZT)/4094

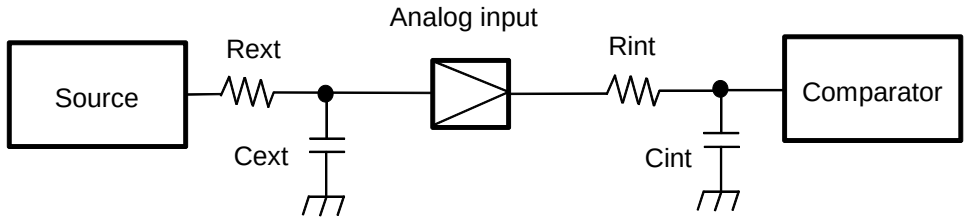
*5: 1LSB= (AVRH-AVRL)/4096

8.5.2 Notes on A/D Converters

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model



Rint : Analog input impedance
3.9 kΩ (max) (4.5 V≤AV_{CC}≤5.5 V)
Cint : Capacitance of MCU input pin
11.0pF (max) (4.5 V≤AV_{CC}≤5.5 V)
Rext : External driving impedance
Cext : Capacitance of PCB at A/D converter input

The following approximation formula for the replacement model above can be used:
sampling time (minimum) = 9 x ((Rin + Rext) x Cin + Rext x Cext)

Note: Use the numerical values provided here simply as a guide.

8.5.3 Glossary

Resolution: Analog change that can be identified by an A/D converter

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics

Includes zero transition error, full-scale transition error, and non-linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB
Total error: Difference between the actual value and the theoretical value.

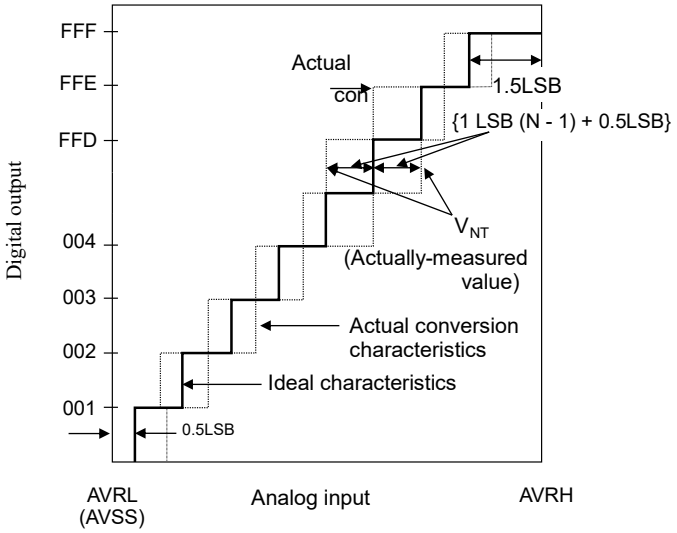
8.5.4 Calibration Condition

Calibration Condition should be the followings.

- AVCC=5.0 V
- AVRH=5.0 V
- T_A=25°C
- system clock frequency (CLK_LCP1A) = 10 MHz

See A/D Converter Calibration in the S6J3200 hardware manual.

Total error



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\text{LSB}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{4096}\ [\text{V}]$$

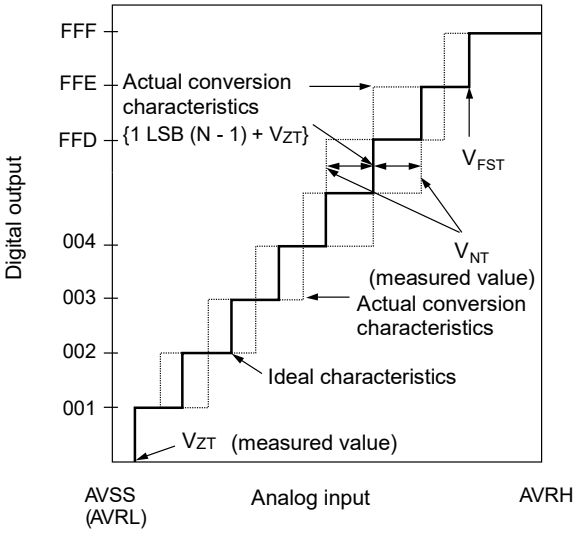
N: A/D converter digital output value.

V_{ZT}(Ideal value) = AVRL + 0.5LSB[V]

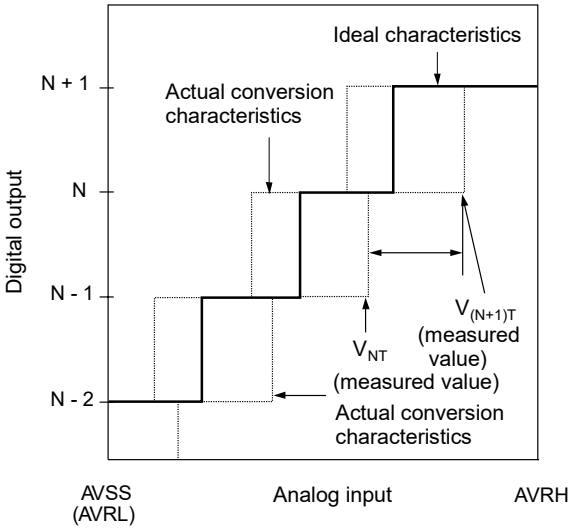
V_{FST}(Ideal value) = AVRH - 1.5LSB[V]

V_{NT}: Voltage at which the digital output changes from "(N – 1)" to "N".

Integral linearity error



Differential linearity error



$$\text{Integral linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{ZT}\}}{1\text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1\text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}\ [\text{V}]$$

V_{ZT}: Voltage for which digital output changes from "0x000" to "0x001"

V_{FST}: Voltage for which digital output changes from "0xFFE" to "0xFFF".

8.6 Audio DAC

8.6.1 Electrical Characteristics

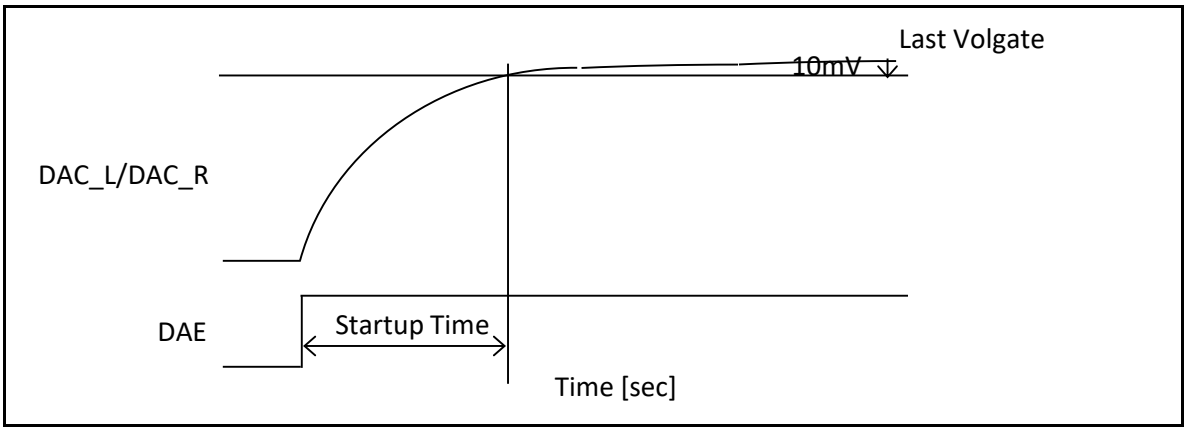
(Condition: See 8.2.Operation Assurance Condition)

Parameter	Symbol	Pin Name	Conditions *1	Value			Unit	Remarks
				Min	Typ	Max		
system clock frequency	F_{CLKDA0}	-	-	2.048	-	18.432	MHz	
sampling clock	fs	-	-	8	-	48	kHz	
Analog output load resistance *2	R_L	DAC_L DAC_R	-	20	-	-	kΩ	
Analog output load capacitance *2	C_L		-	-	-	100	pF	
capacitance	-	C_L C_R	-	5	10	20	µF	
Analog output single-end output range (±full scale)	-	DAC_L DAC_R	R_L=20 kΩ C_L=100 pF	-	0.673 AVCC3_DAC	-	V_{P-P}	
Analog output voltage (zero)	-		-	-	0.5 AVCC3_DAC	-	V	
THD+N *3	-	-	signal frequency: 1 kHz LPF(fc: 20 kHz)	-	-82	-72	dB	
SNR *3	-	-	signal frequency: 1 kHz LPF(fc: 20 kHz)— – A-weighting filter	85	89	-	dB	
Dynamic range *3	-	-		83	86	-	dB	
Out-of-Band Energy	-	-	20 kHz to 64 fs	-	-	-33	dB	
Channel Separation	-	-	-	-	80	-	dB	
Output impedance	-	-	-	150	200	250	Ω	
PSRR	-	-	digital input: zero — noise 50 Hz	-	-35	-	dB	
			digital input: zero — noise 1 kHz	-	-50	-	dB	
			digital input: zero — noise 20 kHz	-	-40	-	dB	
			digital input: full scale sine	-	-13	-	dB	
Supply current normal operation	-	AVCC3 _DAC	-	-	2.2	3.2	mA	
Supply current power-down	-	AVCC3 _DAC	-	-	-	100	µA	
Startup Time *4	-	-	DAE↑	-	650 *5	-	ms	

Notes:

- **1: All parameters specified fs=44.1 kHz, system clock 256 fs and 16-bit data, R_L-20 kΩ, C_L=100 pF, unless otherwise noted.*
- **2: Refer to bellow note on R_L load connection.*
- **3: These values do not include the noise caused by the analog power supply. (Refer to 7. Use examples)*
- **4: 10µF is connected to C_L, C_R.*
- **5: Startup time (Figure 8-8)*

Figure 8-8: Startup Time



Startup time can be calculated as follows.

1. Startup time (TYP) = 650 [ms] (Table 5.2)

2. CCOM=10uF×(1±α/100)

CCOM is a capacitor connected to Terminal C_L/C_R including capacitance variance.

α=Capacitance variance [%]

3. Startup time = Start up time (TYP)×(1±α) [ms]

For example, CCOM=11μF then α= (11μF-10μF)/10μF=10[%]

So, Startup time = 650ms × （1+10/100） = 715 [ms]

Notes:

- *Two usages of R_L load connection.*
- *Case1: R_L is connected to AVCC3_DAC /2 (Figure 8-9)*
- *Case2: The coupling capacitance must be inserted as shown in (Figure 8-10).*

Figure 8-9: R_L is Connected to AVCC_DAC/2 (Example)

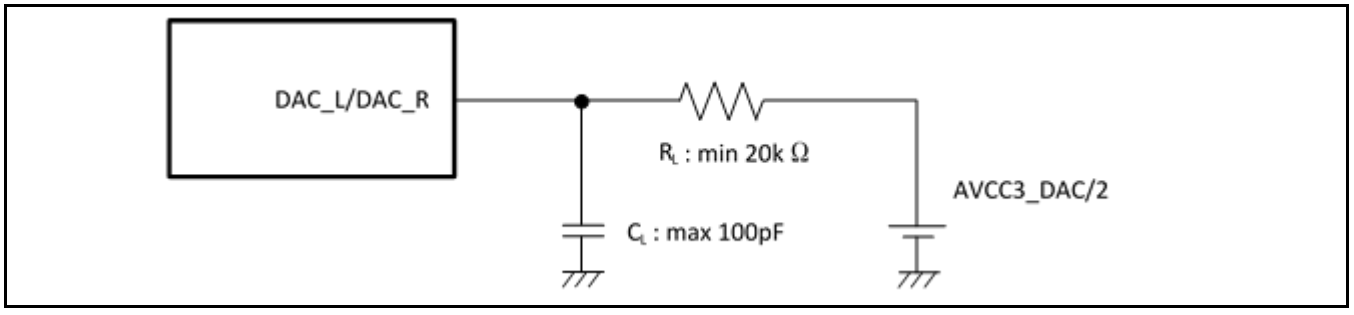
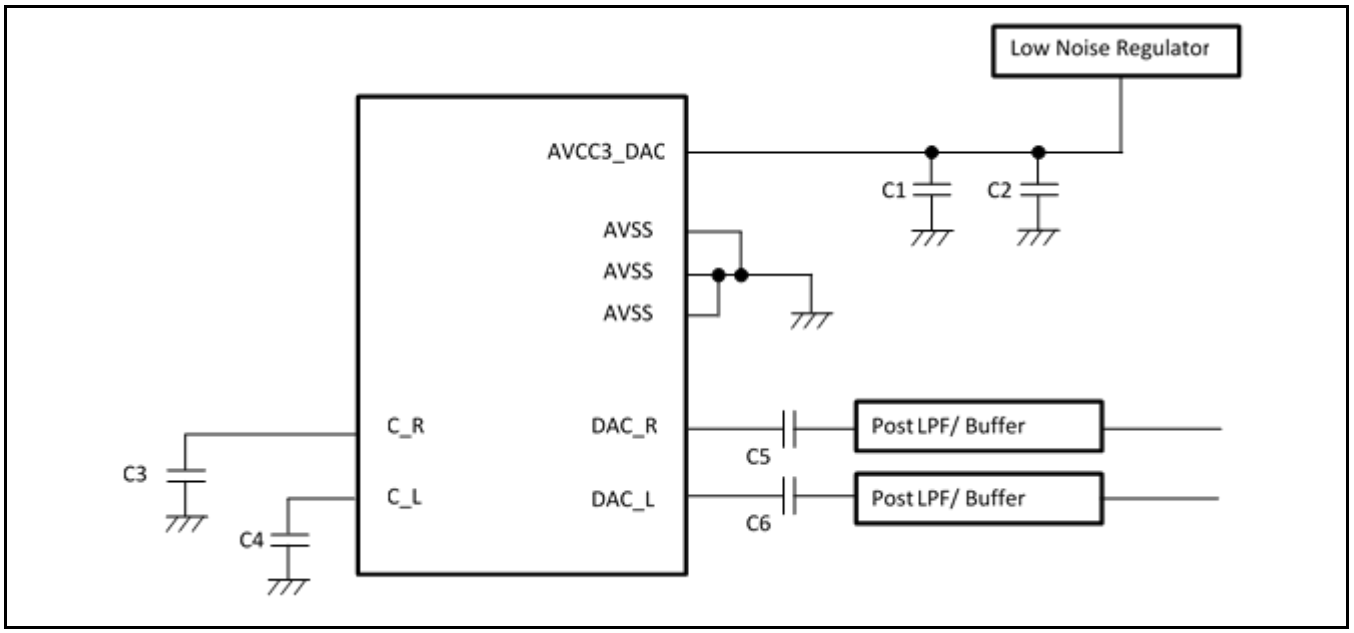


Figure 8-10: Coupling Capacitance (Example)



Notes:

- *C1: more than 10 µF low ESR capacitors*
- *C2: 0.1 µF ceramic capacitors*
- *C3, C4, C5, C6: 10 µF low ESR capacitors*
- *Impedance of each power line must be as low as possible.*

Notes:

- *When DAC is not used in your system, the related pins should be*
- *AVCC3_DAC=GND and AVSS=GND*
- *C_L=OPEN and C_R=OPEN*
- *DAC_L=OPEN and DAC_R=OPEN*

8.7 Flash Memory

8.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max*3		
Sector erase time	-	300	1100	ms	8 kB sector*1 Internal preprogramming time included
	-	800	3700	ms	64 kB sector*1 Internal preprogramming time included
8 bit write time	-	15	288	µs	System-level overhead time excluded*1
16 bit write time	-	19	384	µs	System-level overhead time excluded*1
32 bit write time	-	27	567	µs	System-level overhead time excluded*1
64 bit write time	-	45	945	µs	System-level overhead time excluded*1
8 bit (with ECC) write time	-	19	384	µs	System-level overhead time excluded*1
16 bit (with ECC) write time	-	23	483	µs	System-level overhead time excluded*1
32 bit (with ECC) write time	-	31	651	µs	System-level overhead time excluded*1
64 bit (with ECC) write time	-	49	1029	µs	System-level overhead time excluded*1
Erase count*2 / Data retention time	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T_A=+85 degrees Celsius

Notes:

- **1: Guaranteed value for up to 100,000 erases*
- **2: Number of erases for each sector*

8.7.2 Notes

□ For revision M, P

While the Flash memory is written or erased, shutdown of the external power (Vcc5 and Vcc12) is prohibited.

In the application system, where Vcc5 and Vcc12 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function or external reset (RSTX).

For external power supply voltage stability conditions please see chapter 8.4.4.2 and 8.4.10.4.

□ For except revision M, P

While the Flash memory is written or erased, shutdown of the external power (V_{CC}5 and Vcc12) is prohibited.

In the application system where V_{CC}5 and Vcc12 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC}5 at 2.7 V or more and Vcc12 at 1.1 V or more within the duration calculated by the following expression:

Td*1 [µs] + (1 / F_{CRF}*2[MHz]) x 1029 + 25 [µs]

*1: See "8.4.10 Low-Voltage Detection"

*2: See "8.4.1 Source Clock "

9. Abbreviation

Abbreviation	Definition	Remark
A/D converter	Analog to Digital Converter	
ADC	Analog to Digital Converter	
AHB	Advanced High performance Bus	
AMBATM	Advanced Microcontroller Bus Architecture	
APB	Advanced Peripheral Bus	
ATCM	TCM-A port	
AXI	Advanced eXtensible Interface	
B0TCM	TCM B0 port	
B1TCM	TCM B1 port	
BBU	Bit Banding Unit	
BDR	Boot Description Record	
BT	Base Timer	
BTL	Bridge-Tied Load	
CAN	Control Area Network	
CD	Clock Domain	
CPU	Central Processing Unit	
CR	CR Oscillator	
CRC	Cyclic Redundancy Check	
CSV	Clock SuperVisor	
DAC	Digital Analog Converter	
DAP	Debug Access Port	
DED	Dual Error Detection	
DMA	Direct Memory Access	
DMAC	DMA Controller	
EAM	Exclusive Access Memory	
ECC	Error Correction Code	
ETM	Embedded Trace Macro	
EXT-IRC	External InteRrupt Controller	
FIQ	Fast Interrupt Request	
FPU	Floating Point Unit	
FRT	Free-Run Timer	
GPIO	General Purpose I/O	
HPM	High Performance Matrix	
HW-WDT	Hardware Watchdog Timer	
I/O	Input or Output	
I2S	Inter-IC Sound	
ICU	Input Capture Unit	
IPCU	Inter-Processor Communication Unit	
IRC	InteRrupt Controller	
IRQ	InteRrupt Request	
ISR	Interrupt Service Routine	
JTAG	Joint Test Action Group	
LLPP	Low Latency Peripheral Port	
LVD	Low Voltage Detector	
MCU	MicroController Unit	
MFS	Multi-Function Serial interface	
MLB	Media LB	

Abbreviation	Definition	Remark
NF	Noise Filter	
NMI	Non Maskable Interrupt	
OCU	Output Compare Unit	
OSC	OSCillator	
PCB	Printed Circuit Board	
PCBA	Printed Circuit Board Assembly	
PCM	Pulse Coded Module	
PD	Power Domain	
PLL	Phase Locked Loop	
PONR	Power ON Reset	
PPC	Port Pin Configuration	
PSC	Power Supply Control	
PSS	Power Saving State	
PWM	Pulse Width Modulation	
QPRC	Quad Position & Revolution Counter	
RAM	Random Access Memory	
RIC	Resource Input Configuration	
RLT	Reload Timer	
ROM	Read Only Memory	
RSDS	Reduced Swing Differential Signal	
RTC	Real Time Clock	
RVD	Low Voltage Detection and Reset for RAM Retention	
SCT	Source Clock Timer	
SEC	Single Error Correction	
SECDED	Single Error Correction and Dual Error Detection	
SG	Sound Generator	
SHE	Secure Hardware Extension	
SMC	Stepper Motor Controller	
SMIX	Sound Mixer	
SPI	Serial Peripheral Interface	
SRAM	Static RAM	
SSCG	Spread Spectrum Clock Generation	
SWFG	Sound Waveform Generator	
SW-WDT	Software Watchdog Timer	
SYSC	System Controller	
TCFLASH	FLASH connected to TCM	
TCM	Tightly Coupled Memory	
TCRAM	RAM connected to TCM	
TPU	Timing Protection Unit	
TSU	Time Stamp Unit	
UDC	Up-down Counter	
VIC	Vectored Interrupt Controller	
VRAM	Video RAM	
WDR	Watchdog Description Record	
WDT	Watchdog Timer	
WFG	Waveform Generator	
WorkFLASH	Work FLASH Memory	

10. Ordering Information

Table 10-1: Order Part Number Table

Part Number	Package
S6J32BAKSESE2000A	LER208 (208-pin plastic TEQFP)
S6J323CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J323CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J323CLUPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J324CKSMSE2000A	LET208 (208-pin plastic TEQFP)
S6J324CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J324CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J325CKSFSE2000A	LET208 (208-pin plastic TEQFP)
S6J325CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J325CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J325CLUPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J326CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J326CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J327CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J327CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J327CLUPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J328CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J328CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J328CLSPSC2D000	LEQ216 (216-pin plastic TEQFP)
S6J329CKSPSE20000	LET208 (208-pin plastic TEQFP)
S6J329CKUPSE20000	LET208 (208-pin plastic TEQFP)
S6J329CLSPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J329CLSPSC2D000	LEQ216 (216-pin plastic TEQFP)
S6J329CLUPSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32KEKSMSE20000	LET208 (208-pin plastic TEQFP)
S6J32KELSMSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32LEKSMSE20000	LET208 (208-pin plastic TEQFP)
S6J32LELSMSC20000	LEQ216 (216-pin plastic TEQFP)

Part Number	Package
S6J32MEKSMSE20000	LET208 (208-pin plastic TEQFP)
S6J32MELSMSC20000	LEQ216 (216-pin plastic TEQFP)
S6J32NEKSMSE20000	LET208 (208-pin plastic TEQFP)
S6J32NELSMSC20000	LEQ216 (216-pin plastic TEQFP)

*1 TEQFP-256 is for trace.

11. Errata

This section describes the errata for the S6J3200 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number
S6J32BAxSE S6J323CxxM/P S6J324CxSM/P S6J325CxxF/M/P S6J326CxSM/P S6J327CxxM/P S6J328CxSM/P S6J329CxxM/P S6J32KExSM S6J32LExSM S6J32MExSM S6J32NExSM

S6J32B/3/4/5/6/7/8/9/K/L/M/N Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3200 Series devices.

Items	Part Number	Fix Status
1. MCAN wrong message transmission	S6J32BAxSE S6J323CxxM/P S6J324CxSM/P S6J325CxxF/M/P S6J326CxSM/P S6J327CxxM/P S6J328CxSM/P S6J329CxxM/P S6J32KExSM S6J32LExSM S6J32MExSM S6J32NExSM	No silicon fix planned.
2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID		
3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID		

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control filed information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

■ **Fix Status**

Not be planned.

2. **CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID**

■ **Problem Definition**

CAN FD controller message order inversion when multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

■ **Configuration**

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

■ **Expected behavior**

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

■ **Observed behavior**

It may happen, depending on the delay between the individual Tx requests, that multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

■ **Workaround**

First, write the group of Tx messages with the same Message ID to the Message RAM and then request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID, ensure that no message with this Message ID has a pending Tx request.

Applications not able to use the above workaround can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

■ **Fix Status**

Not be planned

3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

■ **Problem Definition**

There was an incomplete description related to transmission from multiple buffers configured with the same Message ID in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual.

■ **Detailed explanation**

The following is the updated description in Section 3.5.2 Dedicated Tx Buffers and Section 3.5.4 Tx Queue of the Hardware Manual.

Section 3.5.2 Dedicated Tx Buffers:

- Original content in the Hardware Manual:

In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

- Enhancement:

These Tx buffers shall be requested in ascending order with the lowest buffer number first. Alternatively, all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to TXBAR.

Section 3.5.4 Tx Queue:

- Original content in the Hardware Manual:

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

- Replacement:

In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on the numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

- Original content in the Hardware Manual:

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

- Replacement:

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

■ **Workaround**

In case a defined order of transmission is required, the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with the same Message ID shall be requested in ascending order with the lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

■ **Fix Status**

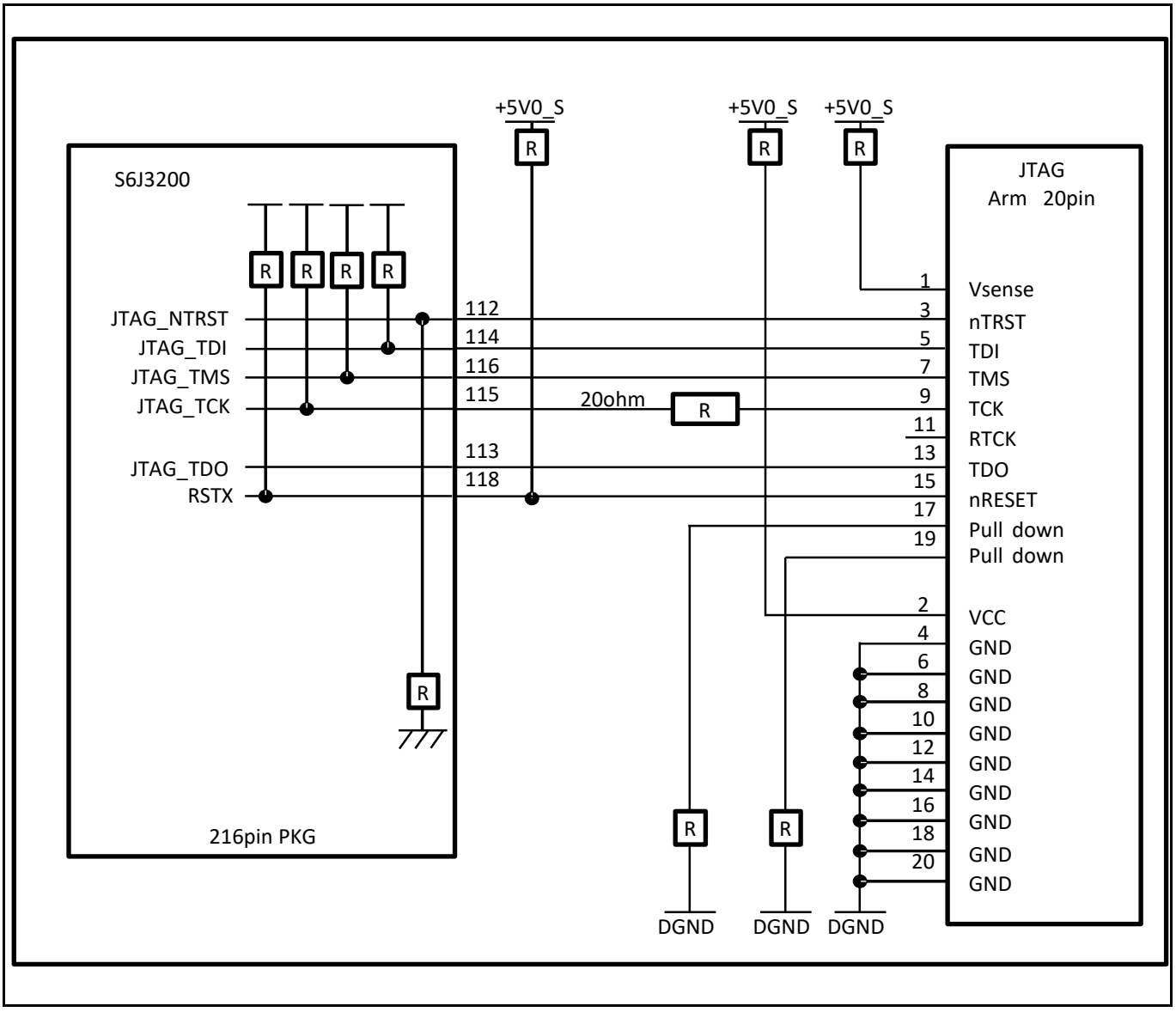
No silicon fix planned. Use workaround.

Hardware Manual will be updated accordingly.

12. Appendix

12.1 Application 1: JTAG tool Connection

This is an application example of JTAG tool connection. See the relevant application note 002-09861 in detail.



13. Major Changes

Spansion Publication Number: S6J3200_DS708-00003

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
-	-	See 11.1 Supplementary Information as described in "1.Overview 1.2. Document Definition”
Revision 0.3		
-	-	See 11.1 Supplementary Information as described in "1.Overview 1.2. Document Definition”
Revision 0.4		
-	-	See 11.1 Supplementary Information as described in "1.Overview 1.2. Document Definition”
Revision 1.0		
-	-	See 11.1 Supplementary Information as described in "1.Overview 1.2. Document Definition”
Revision *O		
185,187, 188	11. Errata	Added about CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID
Revision *Q		
185,187, 188,189	11. Errata	Added about CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID

NOTE: Please see “Document History” about later revised information.

13.1 Supplementary Information

All the changes between previous and current document edition are described in this sheet.

Following "ID" is a number which is owned by every change. A change which is applied to other documents of same family should have a same ID.

Summary	Error Page	Error	Correct Page	Correct	ID
Original document code: DS708-00003-0v02-E, Previous document code: DS708-00003-0v01-E					
Rev. 1.0 December 26, 2014					
Pin assignment	22, 23	(Relation on pin assignment) ||Function||PORT || ||MFS8_CS0||P3_08|| ||MFS9_CS0||P3_09|| ||MFS9_CS1||P3_10|| ||MFS8_CS3||P3_11|| ||MFS8_CS1||P3_12|| ||MFS8_CS2||P3_13||	22, 23	(Relation on pin assignment) ||Function||PORT || ||MFS8_CS0||P3_12|| ||MFS9_CS0||P3_13|| ||MFS9_CS1||P3_14|| ||MFS8_CS3||P3_15|| ||MFS8_CS1||P3_16|| ||MFS8_CS2||P3_17||	#150

Summary	Error Page	Error	Correct Page	Correct	ID
I2S port name	22,23	I2S1_WS1 I2S1_SCK1	22,23	I2S1_WS I2S1_SCK	#190
Ethernet port name	22,23	RDX0, RDX1, RDX2, RDX3	22,23	RXD0, RXD1, RXD2, RXD3	#191
Vcc12 power supply	62	Vss12: 1.15(min), 1.3(max)	62	Vss12: 1.15(min), 1.3(max) 1.1(min)*1, 1.3(max) ― *1. The value will be for the product series with revision digit B.	#169
Current consumption	69	ICC12: -(typ), 1900(max) ICCT5: -(typ), 2620(max) ICCH5: -(typ), 2620(max)	68	ICC12: 950(typ),1900(max) ICCT5: 350(typ),700(max) ICCH5: 150(typ),450(max)	#170
Vcc5 current consumption	69	ICC5 Normal operation 60mA(max)	68	ICC5 Normal operation 45mA(typ), 75mA(max)	#181
Current consumption of FPD link	69	-	68	ILVDS: VCC3_LVDS_Tx,AVCC3_LVDS_PLL: 70mA (FPD-Link)	#204
Source clock error	72	Note: - ,,,, - Jitter of source oscillator must be smaller than 300ppm.	71	Note: - ,,,, - The error of source oscillator frequency must be smaller than 300ppm.	#178
Trace clock	74, 75	FCLK_TRC: 50MHz	73, 74	FCLK_TRC: 100MHzNote;- FCLK_TRC/2 (half frequency of FCLK_TRC) comes out of the trace clock port of package external pin.	#182
Internal clock frequency	75	Notes; -,,,	74	Notes; -,,, - Even if a combination of clock frequency is able to be configured by software, the frequency should be configured under maximum frequency described in Table. For example, 80MHz of CLK_LCP0A seems to be configurable from both divided 240MHz and 160MHz of CLK_CPU. But each duty ratio of configured 80MHz as an internal signal is different from one another. In this series, the 80MHz from the 160MHz divided by 2 can only be assured, but the 240MHz divided by 3 cannot be assured from the internal timing design point of view.	#180

Summary	Error Page	Error	Correct Page	Correct	ID
Power On condition	79	Level detection voltage: 2.25(min) 2.45(typ) 2.65(max)	78	Level detection voltage: 2.15(min) 2.35(typ) 2.55(max) Reset release voltage: 2.25(min) 2.45(typ) 2.65(max)	#138
Display controller AC specification	101	Display controller0 Timing (TTL mode)tDC0CYC:12.5ns (min)|tDC0D|:- (Remarks)tDC0V:- (Remarks)Notes:- ,,,,Display controller0 Timing (RSDS)|tRSD|:- (Remarks)tSPV:- (Remarks)Notes:- ,,,,	100	Display controller0 Timing (TTL mode)tDC0CYC:12.5ns (min) *120ns(min) *2|tDC0D|:*3 (Remarks)tDC0V:*1, *4 (Remarks)Notes:- ,,,,— For *1, when used with DSP0_DATA* and DSP0_CTRL4-0 in VCC3 area.— For *2, when used with DSP0_DATA* and DSP0_CTRL4-0 in VCC53 area.— For *3, the value can be configured and adjusted.— For *4, the value is defined as tDC0CYC - |tDC0D| and depends on adjustment of *3.Display controller0 Timing (RSDS)|tRSD|:*1 (Remarks)tSPV:*2 (Remarks)Notes:- ,,,,— For *1, the value can be configured and adjusted.— For *2, the value is defined as tDC0CYC - |tDC0D| and depends on adjustment of *1.	#187
Video Capture	104	TCAP0CYC: 11.11ns (min) tCAP0SU: 2ns (min)	103	TCAP0CYC: 12.5ns (min) tCAP0SU: 4ns (min)	#188

Summary	Error Page	Error	Correct Page	Correct	ID
Note of NC pins, LVDS pins, and other no-used pin	105	-	104	Note:— All the corresponding ports of products which don't support FPD-Link should be connected to GND.AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-.	#143
FPD-Link timing chart	105	-	105, 106	Figure: LVDS AC characteristics (Timing chart)	#183

Summary	Error Page	Error	Correct Page	Correct	ID
HyperBus AC specification	108-112	16-1 (3 items) CS ↓ -> RDS ↓ Chip select active to RDS valid (Low): CS ↑ -> RDS(Hi-z) Chip select Inactive to RDS High-Z: CS ↑ -> CS ↓ Chip select HIGH between operation: 16-2 (4 items) CS ↑ -> CS ↓ Chip select HIGH between transaction: CS ↓ -> CS ↑ Chip select maximum LOW time: Read-Writer recovery time : CK ↓ -> CK ↓ (4th) Page open time : 16-3 (7 items) Read Initial Access Time : CS ↑ ↓ -> CK ↑ Chip select active to RDS valid (Low): CS ↑ -> RDS(Hi-Z) Chip select Inactive to RDS High-Z: CK ↑ ↓ -> DQ (Low Z) Clock to DQs Low Z: CS ↑ -> DQ (Hi-Z) Chip select Inactive to DQs High-Z: CK ↑ ↓ -> RDS ↑ ↓ CK transition to RDS transition: CS ↑ -> CS ↓ Chip select HIGH between Operation: 16-4 (8 items) CK ↓ -> CK ↓ (4th) Page open time: CS ↑ -> RWDS(Hi-Z) Chip select Inactive to RWDS High-Z: CK ↑ ↓ -> DQ (Low Z) Clock to DQs Low Z: CS ↑ -> DQ (Hi-Z) Chip select Inactive to DQs High-Z: CK ↑ ↓ -> RWDS ↑ ↓ CK transition to RWDS transition: CS ↑ -> CS ↓ Chip select HIGH between Transition: CS ↓ -> CS ↑ Chip select maximum LOW time: Read-Writer recovery time	109-112	(Removed)	#173

Summary	Error Page	Error	Correct Page	Correct	ID
HyperBus AC specification	108, 109	tCKCYC: 12.5ns(min)tCSS:3ns (min)tIS:1.25ns (min)tCSH:1.25ns (min)Notes;- ,,,,	109,110	tCKCYC: 12.5ns(min) (A)10ns(min) (B)tCSS:3.25ns (max) (A)2ns (max) (B)tIS:5.25ns (max) (A)4ns (max) (B)tCSH:1ns (min)Notes;- ,,,,- (A): The value will be targeted by the product series with revision digit A. - (B): The value will be targeted by the product series with revision digit B.	#184
HyperBus AC specification	109	tDMV: 0ns (min) Notes; - ,,,,	110	tDMV: 5.25ns (max) (A) 4ns (max) (B) Notes; - ,,,, - (A): The value will be targeted by the product series with revision digit A. - (B): The value will be targeted by the product series with revision digit B.	#185
HyperBus AC specification	110,111	tRDSCYC:12.5ns (min)tDSS:-0.8ns (min)0.8ns (max)tDSH:-0.8ns (min)0.8ns (max)Notes;- ,,,,	111,112	tRDSCYC:12.5ns (min) (A)10ns (min) (B)tDSS:-0.8ns (min)- (max)tDSH:-4.2ns (min)- (max)Notes;- ,,,,- (A): The value will be targeted by the product series with revision digit A. - (B): The value will be targeted by the product series with revision digit B.	#186

Summary	Error Page	Error	Correct Page	Correct	ID
Original document code: DS708-00003-0v02-E, Previous document code: DS708-00003-0v01-E					
Rev. 2.0 May 20, 2015					
Note for Basic Option	11	Notes; - ,,,	11	Notes; - ,,, − The CLK_CPU is assigned for CPU clock. The CLK_CD3A0 is assigned for Graphic clock. They are defined at the chapter of Clock Configuration.	#194
Power domain reset	15	-	15	Power domain (PD): ---- See the platform manual and chapter STATE TRANSITION in detail. The product series supports the power off control of PD1, PD2 (including PD3 and 5), and PD6. The power domain resets of PD3 and PD5 included in PD2 are not supported in the product series, and "0" is always read from the reset factor flags of them.	#175
Original document code: DS708-00003-0v03-E, Previous document code: DS708-00003-0v02-E					
Rev. 1.0 May 20, 2015					
Display output	10	Number of display outputs: 2 outputs simultaneously Selectable from 2 x DRGB, 1 x RSDS, or 1 x LVDS (FPD-Link)	10	Number of display outputs: Option Maximum 2 outputs simultaneously	#210
Display output	11	Notes;- ,,,,- ,,,,	12	Notes;- ,,,,- ,,,,− Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn't support FPD-LINK is used for RSDS and DRGB. Display Output ch.1 is used for DRGB only.	#211
Revision B description	11	Note: - ,,, - The function digit A, B, C, and D supports Hyper SRAM. Its 3, 4, 5, and 6 doesn't support Hyper SRAM. Hyper Bus interface ch.2 on graphic sub system will be embedded on product which is specified with function digit 7and 8 after revision B. Revision A only has ch.0 and 1 of Hyper Bus interface.	12	Note: - ,,, - HyperBus Interface ch.1 of the function digit 3, 4, 5, and 6 support HyperRAM after Revision B.	#267

Summary	Error Page	Error	Correct Page	Correct	ID
CHIP ID information	12	-	12	Function digit: A, B, C, D Revision B: Chip ID: 0x10110000 JTAG ID: 0x100095CF	#140
Clock Supervisor output function	15	-	15	Clock Supervisor: See the platform manual in detail. This product series doesn't support clock supervisor output port. (Related register and internal circuit is implemented.)	#224
CR oscillation stabilization time	15	-	15	Embedded CR oscillation See the platform manual in detail. Stabilization time is as followings. − 5us for 4MHz (Fast clock) − 20us for 100kHz (Slow clock)	#259
MOST physical channel	19	MediaLB: --- MOST25 (512FS) 3 wires Maximum 15ch is available. (1ch is occupied by the system)	19	MediaLB: --- MOST25 (512FS) 3 wires Maximum 15ch is available.	#128
Pin assignment	23, 25	-	24, 27	(Figures are added)	#141
IO type	29	-	31	(X0 and X1 symbol are added in figure.)	#253
Absolute Maximum Rating	59,60	IOL3,,, When setting is 5 mA*9IOLAV3,,, When setting is 5 mA*9ΣIOL2 50mA *7ΣIOL3 250mA *8IOH3,,, When setting is 5 mA*9IOHAV3,,, When setting is 5 mA*9ΣIOH2 -50mA *7ΣIOH3 -250mA *8	61,62	IOL3,,, When setting is 5 mA*6, *7, *8, *9IOLAV3,,, When setting is 5 mA*6, *7, *8, *9ΣIOL2 250mA *7ΣIOL3 50mA *8IOH3,,, When setting is 5 mA*6, *7, *8, *9IOHAV3,,, When setting is 5 mA*6, *7, *8, *9ΣIOH2 -250mA *7ΣIOH3 -50mA *8	#234
8kB Backup RAM Current Consumption	68	-	70	ICCT5: 345uA(typ),675uA(max):When shutting down 8kB Backup RAM. 450uA(typ),820uA(max):Power only supplies to Backup RAM and system controllers. When using 8MHz crystal for main oscillator. 445uA(typ),795uA(max):When shutting down 8kB Backup RAM. ICCH5: 145uA(typ),425uA(max):When shutting down 8kB Backup RAM.	#206

Summary	Error Page	Error	Correct Page	Correct	ID
DC characterization of PSS	68	ICCT5: Timer mode ICCH5: Stop mode Notes: - ,,,	70	ICCT5: PSS Timer mode Shutdown (PD6=OFF) ICCH5: PSS Stop mode Shutdown Notes: - ,,, - The definition of timer mode and stop mode can be seen at the chapter of STATE transition of S6J3200 hardware manual.	#214
Current consumption	68	Icc12 -(typ) 1700mA(max):CPU:160MHz, HPM:80MHz, GDC:160MHz	70	Icc12 900(typ) 1700mA(max):CPU:160MHz, HPM:80MHz, GDC:160MHz	#260
Oscillator frequency range	71	Source oscillation clock frequency: X0, X1: 3.6MHz(min), 4.0MHz(max) Notes: ,,,	73	Source oscillation clock frequency: X0, X1: 3.6MHz(min), 16MHz(max) Notes: ,,, − Enough evaluation and adjustment are recommended using oscillator on your system board.	#230
PLL/SSCG maximum frequency	73	-	75, 76	FSSCG0:480,800(400),640,640 MHz, SSCG0 output clockFSSCG1:800(400),800(400), 800(400),800(400) MHz, SSCG1 output clockFSSCG2:800(400),800(400), 800(400),640 MHz, SSCG2 output clockFSSCG3:800,800,800,800 MHz, SSCG3 output clockFPLL0:720,800,800,640 MHz, PLL0 output clockFPLL1:800,800,800,640 MHz, PLL1 output clockFPLL2:800(400),800(400),800(400), 800 MHz, PLL2 output clockFPLL3:480,480,480,480 MHz, PLL3 output clockNotes:- ,,,,− The frequency described in () is not maximum value but recommended configuration value.	#208
Minimum PLL/SSCG frequency	74	Note: - ,,, - ,,,	76	Note: - ,,, - ,,, − The configurable minimum frequency of PLLn and SSCGn output is 400MHz.	#219
CAN clock frequency	74	-	76	FCLK_CAN 40MHz(Max)	#222

Summary	Error Page	Error	Correct Page	Correct	ID
"Unused" clock configuration	74	Notes: ,,, ,,,	76	Notes: ,,, ,,, - "Unused" means a clock source which doesn't have any supply destinations. Configure it as disable with performing at the lower clock frequency than the described maximum.	#229
Output short circuit current	104	Output short circuit current IOS:	106	(Removed)	#203
AC spec of DDRHSSPI	107,108	[SDR mode] toddata: 6.5ns (max) tohdata: 3.5ns (min) todsel: 5.5ns (max) tohsel: 4.5ns (min) [DDR mode] toddata: 6.5ns (max) todsel: 7.0ns (max)	109, 110	[SDR mode] toddata: tcyc/2 + 2ns (max) tohdata: 2.0ns (min) todsel: -12.0ns + (SS2CD+0.5)*tcyc ns (min) tohsel: 3.5ns (min) [DDR mode] toddata: tcyc/4 + 1.5ns (max) todsel: -15.75ns + (SS2CD+0.5)*tcyc ns (min) Notes: − This is target spec. − SS2CD [1:0] should be configured as 01, 10, or 11.	#164
SDR/DDR (HSSPI) remark	107,108	Remark:tcyc -3.5nstcyc -4.5nstcyc/2-1.5nstcyc -3.0ns	109,110	(Delete)	#232
ADC trigger input	119	-	121	A/D trigger input time:ADTRG 4tCLK_LCP1A ns (min) 4tCLK_LCP1A ≥ 100ns 100 ns (min) 4tCLK_LCP1A < 100ns	#231
ADC resumption time	119	-	121	Resumption time: 1us(max)	#239

Summary	Error Page	Error	Correct Page	Correct	ID
Original document code: DS708-00003-0v04-E, Previous document code: DS708-00003-0v03-E					
Rev. 1.0 June 30, 2015					
FPD-Link port definition	45	-	60-61	TxCLK- LVDS clock output pin: Described as TXOUT4M in FPD-Link Converter TxCLK+ LVDS clock output pin: Described as TXOUT4P in FPD-Link Converter TxDOUT0- LVDS data output pin: Described as TXOUT0M in FPD-Link Converter TxDOUT0+ LVDS data output pin: Described as TXOUT0P in FPD-Link Converter TxDOUT1- LVDS data output pin: Described as TXOUT1M in FPD-Link Converter TxDOUT1+ LVDS data output pin: Described as TXOUT1P in FPD-Link Converter TxDOUT2- LVDS data output pin: Described as TXOUT2M in FPD-Link Converter TxDOUT2+ LVDS data output pin: Described as TXOUT2P in FPD-Link Converter TxDOUT3- LVDS data output pin: Described as TXOUT3M in FPD-Link Converter TxDOUT3+ LVDS data output pin: Described as TXOUT3P in FPD-Link Converter	#146
Non support port	21, 23	-	25, 27, 28, 29, 32, 34, 35, 36	(Added the Note for non-supported pin condition on PCB)	#215
Current consumption of FPD link	70	VCC3_LVDS_Tx, AVCC3_LVDS_PLL: 70 mA(max)	92	VCC3_LVDS_TX: 56mA(max) AVCC3_LVDS_PLL: 7mA(max)	#246
AVcc and AVRH description	58	(AVCC0, AVCC1, AVRH0, and AVRH1)	73	(AVCC,AVRH)	#250
TEQFP256 support	11	Pin count N:320	12	Pin count M:256	#272

Summary	Error Page	Error	Correct Page	Correct	ID
TEQFP256 support	13, 14	BGA320 Notes: - ,,, - BGA is a package option under planning.	15, 16	TEQFP256 Notes: - ,,, - TEQFP-256 is a package option under planning.	#273
TEQFP256 support	17	A/D Converter: 50 channels of analog input for TEQFP216,,,24 channels of them are shared with the SMC for TEQFP216/208	19	A/D Converter: 50 channels of analog input for TEQFP256 and TEQPF216,,,24 channels of them are shared with the SMC for TEQFP256/216/208	#274
TEQFP256 support	19	LCD Controller: TEQFP216 : 4com x 32seg TEQFP208 : 4com x 30seg ,,,	21	LCD Controller: TEQFP256 : 4com x 32seg TEQFP216 : 4com x 32seg TEQFP208 : 4com x 30seg ,,,	#275
TEQFP256 support	20, 24	-	23, 38	(TEQFP256 assignment is added.)	#276
Chip ID	12	Revision:B, Chip ID:0x10100010	14	Revision:B, Chip ID:- Revision:C and D, Chip ID:0x10100100	#278

Summary	Error Page	Error	Correct Page	Correct	ID
Case Temperature issue	64, 65	Operating temperature TA: -40(min), +105(max)	80, 81	Operating temperature TA: -40(min), +105(max) TC: -40(min), +144(max) Notes: − Both rating of TA and TC should simultaneously be satisfied as maximum operation temperature. − The following condition should be satisfied in order to facilitate heat dissipation. 1. 4 or more layers PCB should be used. 2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard) 3. 1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground. 4. 35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer. 5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.	#283
Main clock frequency	15	Main and sub oscillator is available. − A wide range of 3.6 - 4MHz is available for main oscillator	17	Main and sub oscillator is available. − A wide range of 3.6 - 16MHz is available for main oscillator	#311
Revision description	11	-	12	(Inside Figure 2-1: Option and Part Number) C: Support MCAN 3.0.1. D: Support MCAN 3.2.	#313
CPU Clock Maximum	11	200MHz (CPU Clock of function digit A, B, C, and D)	13	160MHz (CPU Clock of function digit A, B, C, and D)	#314
Maximum gap between package and board	24	-	39	Note:− Same size is specified for MIN, NOM, MAX, then it should be regarded as maximum size.	#315

Summary	Error Page	Error	Correct Page	Correct	ID
Power dissipation and Operation temperature	62	-	77, 78	Power dissipation and Operation temperature Case 1, PD - 3300 mW, TA -40 +97 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 2, PD - 3150 mW, TA -40 +100 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 3, PD - 3000 mW TA -40 +102 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 4, PD - 2900 mW, TA -40 +105 degC, Both should be satisfied. TC -40 +144 degC, Power dissipation and Operation temperature Case 5, PD - 2800 mW, TA -40 +105 degC, Both should be satisfied. TC -40 +144 degC, System Thermal Resistance, Theta j-a - 16 degC/W, The minimum value depends on the system specification of heat radiation. The described value is estimated under the condition which is specified at Operation Assurance Condition. Package Thermal Resistance, Theta j-c - 7.5 degC/W,	#317

Summary	Error Page	Error	Correct Page	Correct	ID
HyperBus GPO Remark	18	HyperBus ,,,	21	HyperBus ,,, GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic Sub System.	#345
Chip Select Output	11	-	13	(Part Number is added to show Chip Select Output of MFS)	#346
Revision B description	12	Notes: ,,, - SCL4, 10, 12 and SDA4, 10, 12 of I2C is not supported yet, and will be enhanced after Revision B.	13	Notes: ,,, - Multi-function serial interface of the function digit 3, 4, 5, 6, 7, and 8 support SCL4, 10, 12 and SDA4, 10, 12 of I2C after Revision D.	#349
MPU lock and unlock value	16	-	18	To configure Lock or Unlock for both MPUXn_UNLOCK and MPUHn_UNLOCK, - Lock: 0x112ABB56 - Unlock: 0xACCABB56	#351
Flash Access Speed	17	1-wait-cycle with 80-160MHz. 2-wait-cycle with 160-240MHz.	19	0-wait-cycle: 80MHz or less. 1-wait-cycle: 160MHz or less. 2-wait-cycle: more than 160MHz. The maximum frequency should be referred in datasheet.	#357
Oscillator error	73	− The error of source oscillator frequency must be smaller than 300ppm.	97	− The error of source oscillator frequency must be smaller than 3000ppm.	#360
Input leakage current,Pull-up resistor,Pull-down resistor and Input capacitance for P4_25 to P4_31	69	Input leakage current:IIL:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 31 Input capacitance:CIN1:P0_00 to 31, P1_00 to 09, P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P5_21, 22, 27 to 31, P6_00 to 08, 17 to 26	89	Input leakage current:IIL:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31 Input capacitance:P0_00 to 31, P1_00 to 09, P2_16, 17, 19, 22, 24 to 31, P3_00 to 20, P4_25 to 31, P5_00 to 20, P5_21, 22, 27 to 31, P6_00 to 08, 17 to 26	#363
CLK_HPM Frequency	16	1 wait cycle is necessary to read at over 180MHz (target).	18	See the platform manual in detail. 1 wait cycle is necessary for RAM read at over 160MHz. No need to insert wait cycles for RAM write.	#366
nSRST description	15	− INITX - SRSTX - nSTRST	17	− INITX − SRSTX (and nSRST pin)	#367

Summary	Error Page	Error	Correct Page	Correct	ID
Hardware flow control	18	Multi-functional Serial (MFS):,,,	20	Multi-functional Serial (MFS):CTS/RTS is not mounted (hardware flow control is not supported for this series.)	#373
Pin assignment and pin list should be separately instead of the red characters	20	-	24-37	(The figure of pin assignment are added)	#374
DDR-HSSPI DDR Mode	110	Note: ,,, - SS2CD [1:0] should be configured as 01, 10, or 10.	140	Notes: ,,, - SS2CD [1:0] should be configured as 01, 10, or 11.	#376
Oscillator Error Issue	76	Notes:− *1: Target maximum clock frequencies when CPU clock = 240MHz- ,,,	100	Notes:− *1: Target maximum clock frequencies when CPU clock = 240MHz - 232MHz or less is available for SSCG Down Spread. - 240MHz or less is available for PLL.- ,,,	#380
Input Pulse Width	120	Port Noise Filter: Width for input removal: All GPIO: 25ns(max) *: Input pulse width less than at least 25nm is removed when Port noise filter is enabled.	151	Port Noise Filter: Width for input removal: All GPIO: 67ns(max) *: Input pulse width less than at least Typ 25ns to Max 67ns is removed when Port noise filter is enabled. *: Input pulse width 100ns or more is recommended to be effective.	#382
TYPO in 216 pin assign	21,22	P0_26 0 P0_27 0 P0_28 0	24-30	("0"s are removed) P0_26 P0_27 P0_28	#384
CHIP ID	12	-	14	Function Digit: 3,4,5,6,7,8 E and F: Chip ID: 0x10100101, JTAG ID: 0x1000C5CF --- Function Digit: A,B,C,D E and F: Chip ID: 0x10110001, JTAG ID: 0x100095CF	#409
RVD Detection/Release Voltage	99	-	124	(LVDL0 spec is added.)	#410
DDH-HSSPI AC Specification	109, 110	(Old value)	138, 140	(New values are added in the table)	#411
HyperBus AC Specification	111-114	(Old value)	142-145	(New values are added in the table)	#412

Summary	Error Page	Error	Correct Page	Correct	ID
Power Supply Current	72	-	92-96	(New table is added, and the value of Icc12, Icc5, Icct5, and Icch5 are improved.)	#413
Unsupport Partial Wakeup	15	Power Domain (PD): ,,,	17	Power Domain (PD): ,,,This series doesn't support partial wakeup for PD6.	#416
Vcc12 power supply limit	64	VSS12: 1.15 1.1*1 Notes: − *1. The value will be for the product series with revision digit B. - ,,,	80	VSS12: 1.15*1 1.1*1 Notes: - *1. The value is only applied to the product series with revision digit A. - ,,,	#417
FPD-Link DC Spec	106	VOD:270, 300, 340 mV310, 350, 400 mV360, 400, 450 mVVCM:1.120, 1.150, 1.175 V1.170, 1.200, 1.225 V1.220, 1.250, 1.280 V	135	VOD:210, 300, 390 mV250, 350, 450 mV295, 400, 505 mVVCM:1.075, 1.200, 1.325 V1.125, 1.250, 1.375 V	#418
Land Pattern for Thermal Via	65	-	81-84	(Land pattern of thermal via hole is added.)	#429
Power On Sequence Recommendation	64		80	Notes: -,,, − Power supply sequence is recommended as VCC5 -> [DVCC or AVCC5 or VCC3 or AVCC3] -> VCC12 -> [AVCC3_LVDS_PLL or VCC3_LVDS_TX]	#431

Summary	Error Page	Error	Correct Page	Correct	ID
Internal Clock Timing for FSSCG0-3 and FPLL0-3	75, 76	FSSCG0 480 800(400) 640 640 FSSCG1 800(400) 800(400) 800(400) 800(400) FSSCG2 800(400) 800(400) 800(400) 640 FSSCG3 800 800 800 800 FPLL0 720 800 800 640 FPLL1 800 800 800 640 FPLL2 800(400) 800(400) 800(400) 800 FPLL3 480 480 480 480 Notes: ,,, − The frequency described in () is not maximum value but recommended configuration value.	99, 100	FSSCG0 232(480) 200(800) 160(640) 160(640) FSSCG1 200(800) 200(800) 200(800) 200(800) FSSCG2 200(800) 200(800) 200(800) 160(640) FSSCG3 200(800) 200(800) 200(800) 200(800) FPLL0 240(720) 200(800) 200(800) 160(640) FPLL1 400(800) 400(800) 400(800) 320(640) FPLL2 200(800) 200(800) 200(800) 200(800) FPLL3 240(480) 240(480) 240(480) 240(480) Notes: ,,, − The frequency described in () is maximum output frequency of SSCG PLL / PLL multiplier circuit.	#432
VIH spec(TTL level) for JTAG-pins	65	VIH9: 2.0(Min)	85	VIH9: 2.3(Min)	#437
VIH of Media LB port	65	VIH12: 1.7(V)	85	VIH12: 1.8(V)	#438
Original document code: DS708-00003-1v0-E, Previous document code: DS708-00003-0v04-E					
Rev. 1.0 September 30, 2015					
Resource clock frequency	9	Resource clock frequency : 40MHz (Max)	8	Resource clock frequency : Option : See AC specification on the datasheet	#465
Description for up/down counter	10, 20	Up/Down Counter	9, 19	Quad Position & Revolution Counter(Up/Down Counter)	#530
Display output	13	Notes: ,,, - Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn’t support FPD-LINK is used for RSDS and DRGB. Display Output ch.1 is used for DRGB only.	12	Notes: ,,, - Display Output ch.0 is used for RSDS and FPD-LINK (LVDS) as well as DRGB (Digital RGB). The ch.0 of the product which doesn’t support FPD-LINK is used for RSDS and DRGB. - Display Output ch.1 is used for FPD-LINK (LVDS) and DRGB (Digital RGB). The ch.1 of the product which doesn't support FPD-LINK is used for DRGB only.	#452

Summary	Error Page	Error	Correct Page	Correct	ID
Relationship SYSC0_SYSIDR and ChipID	14	ID is specified for each function digit and revision which is defined at Figure 2-1.	13	ID is specified for each function digit and revision which is defined at Figure 2-1. Chip ID can be read from SYSC0_SYSIDR. For SYSC0_SYSIDR, see the TRAVEO™ T1G Platform hardware manual.	#471
Typo in trace buffer size	17	4kB Embedded Trace Buffer	16	4k Word Embedded Trace Buffer	#528
WUCR function	20	MFS: ,,,	19	MFS: ,,, WUCR function is not supported for this product.	#284
CS port availability	20	MFS: Chip select function of CSIO is not supported yet and will be enhanced with next revision.	19	MFS: The availability of chip select function can be seen at Function Digit Table.	#448
Not support CS input	20	-	19	Chip Select Input is not supported.	#467
Usage for I2S ch1	20	− I2S0 only supports the output of sound sources. − I2S1 supports both the input and the output. − ,,,	19	- I2S0 can output sound sources which are processed by Sound System. - I2S1 can input sound sources which are processed by Sound System. − ,,, See the "Sound System Configuration" of S6J3200 hardware manual in detail.	#529
Improvement of description for I2C	20	Note all pins do not necessarily support I2C, but the pins which have the dedicated I/O characteristics only support it.	19	Note - Not all pins support I2C. Only pins which have the I2C I/O characteristics support it.	#531
Reference for DDR High Speed SPI & CAN-FD	20	-	19, 20	(Added "See the platform manual in detail" for CAN-FD & DDR High Speed SPI)	#532
Reference information for GPO	21	GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic Sub System.	20	GPO signal can only be used for "Internal Control example by GPO" in this product, that is, it can select using HyperBus of PF or using HyperBus of Graphic Sub System. See the "HyperBus Interface Port Configuration" of S6J3200 hardware manual in detail.	#533
Delete unnecessary description for Graphic subsystem	21	Order replacement of RGB pins.	20	(Deleted)	#534

Summary	Error Page	Error	Correct Page	Correct	ID
Delete Ethernet restriction for product	22	Direct Memory Access Interface, MAC Filtering Block -VLAN tag, IEEE 1588 and IEEE 802.1AS Support, MAC PFC Priority Based Pause Frame Support, and 802.1Qav Support – Credit Based Shaping	21	(Delete)	#516
Improvement of description for Pin Assignment	23	Alphabets with pin numbers are signs specify I/O circuit type.	22	The characters next to the pin number in the pin assignment drawing specify the I/O circuit type. (figure added)	#535
Regarding "red" character in Pin Assignment	23-38	The pins which are described in "red" character are not supported, and will be enhanced with next revision products.	23-35	The pins which are described in "red" character are not supported product with revision A and C.	#524
Note for Input voltage and Max clamp current	76	Maximum clamp current:*A (Remarks) Total maximum clamp current:*A (Remarks)	75	Maximum clamp current:*12, *A (Remarks) Total maximum clamp current:*12, *A (Remarks)	#503
TYPO in Absolute Maximum Rating	76	Input voltage:VI2:VCC5+0.3(Max) ,,, Input voltage:VIE:VCC5+0.3(Max)	75	Input voltage:VI2:DVCC+0.3(Max) ,,, Input voltage:VIE:VCC53+0.3(Max)	#518
Note for Input voltage and Max clamp current	78	-	77	*12: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.	#470
Power supply sequence	80	Power supply sequence is recommended as VCC5 -> [DVCC or AVCC5 or VCC3 or AVCC3] -> VCC12 -> [AVCC3_LVDS_PLL or VCC3_LVDS_TX]	79	Power supply sequence is recommended as VCC5 -> [DVCC or AVCC5 or VCC3 or AVCC3] -> VCC12 -> [AVCC3_LVDS_PLL or VCC3_LVDS_TX]. Note that power supplies inside "[]" can be turned on in arbitrary order.	#474
VIH/VIL characteristics for I/O of DVCC	85, 86	-	84, 85	(Added the "*1" for note of some characteristics and the description)	#439
DS 8.3.1 Port Function Characteristics	86	VIL10(Max) 0.3xVcc5	85	VIL10(Max) 0.3xVcc3	#453
VOH characteristic for I/O of MediaLB	87	VOH16:VCC3-0.5(Min)	86	VOH16:2.0(Min)	#441

Summary	Error Page	Error	Correct Page	Correct	ID
VOH/L4, VOH/L5, VOH/L6 characteristics for I/O of VCC5 and DVCC	87, 88	-	86, 87	(Added the "*1" for note of some characteristics and the description)	#442
VOL4, VOL5 characteristics	88	VOL4:0.55(Max) VOL5:0.55(Max)	87	VOL4:0.4(Max) VOL5:0.4(Max)	#443
Pull-up/Pull-down resistor for 5V/3V pins (P4_25 to 31, P5_00 to 20)	89	PUP2:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 31:Pull-up register selected,,,Pdown2:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P6_02 to 31:Pull-down register selected	88	PUP2:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31:Pull-up register selected Vcc53 = 4.5V to 5.5V,,,Pdown2:P2_16, 17, 19, 22, 24 to 31, P3_00 to 31, P4_00 to 12, P4_25 to 31, P5_00 to 20, P6_02 to 31:Pull-down register selected Vcc53 = 4.5V to 5.5V	#430
Typo in condition of IIL characteristics for 3V I/O	89	VCC3=3.3 V VSS < VI < VCC3	88	VCC3=3.6 V VSS < VI < VCC3	#444
Typo in symbol for input capacitance	89	CIN1:P3_21 to 31, P4_00 to 12, P6_09 to 16	88	CIN2:P3_21 to 31, P4_00 to 12, P6_09 to 16	#445
Pull-up/Pull-down resistor for 5V/3V pins	89	-	88	Pull-up resistor:RUP2:P4_25 to 31, P5_00 to 20:Pull-up resistor Selected Vcc53 = 3.0V to 3.6V:40(Min):100(Typ):200(Max):kΩ:5V/3V pins ,,, Pull-down resistor:Rdown1:P4_25 to 31,P5_00 to 20:Pull-down resistor Selected Vcc53 = 3.0V to 3.6V:40(Min):100(Typ):200(Max):kΩ:5V/3V pins	#501
FPD-Link DC Spec	92	-	91	Note: - ,,, - The current consumption at Vcc3_LVDS_Tx is specified under R_L=100 Ω, C_L=5 pF, f=50 MHz, and 0/1 alternation pattern output.	#433
DS 8.3.2.1 Run Mode	93	(Icc5 is only defined)	92	(Current values related CPU operation should be specified as Icc12)	#454
Maximum clock frequency of SSCG3	99	FSSCG3:200(800), 200(800), 200(800), 200(800)	98	FSSCG3:400(800), 400(800), 400(800), 400(800)	#458

Summary	Error Page	Error	Correct Page	Correct	ID
Delete "Taget spec"	99, 100, 131-134, 138, 140,142-150, 159	-	98, 99, 100, 131-134, 138, 140, 142-150, 159	(Deleted explanation for target spec)	#504
SSCG Max Frequency	100	Notes: – *1: Target maximum clock frequencies when CPU clock = 240MHz - 232MHz or less is available for SSCG Down Spread. - 240MHz or less is available for PLL.	99	Notes: – *1: Target maximum clock frequencies when CPU clock = 240MHz - 232MHz or less is available for SSCG Down Spread on/off. - 240MHz or less is available for PLL.	#487
Internal Clock Timing	100	Notes:,,,- *3: Target maximum clock frequencies when CPU clock = 160MHz- From *1 to *3, they are not applied to the product series with function digit A, B, C, and D. - *4: Target maximum clock frequencies when CPU clock = 160MHz for the product series with thefunction digit A, B, C, and D.	100	Notes:,,,- *3: Target maximum clock frequencies when CPU clock = 160MHz. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.- From *1 to *3, they are applied to the product series with function digit 3, 4, 5, 6, 7, and 8.- *4: Target maximum clock frequencies when CPU clock = 160MHz for the product series with the function digit A, B, C, and D. This is also a combination of maximum clock frequencies for TC FLASH Programming or Erasing.	#406
Level detection hysteresis width	105	Level detection hysteresis width	104	(Delete)	#457
Default Value of LVDL1	126	LVDL1V=01(Default),,, LVDL1V=10	125	LVDL1V=01,,, LVDL1V=10(Default)	#502
Display AC specification	131	-	131	(- Updated the min/max value in |tDC0D| and tDC0V. - Added the new definition for DSP0_CTRL11-0 of tDC0V. - Update the note for *2 and delete the note for *4. - Updated figure for definition of tDC0V.)	#347

Summary	Error Page	Error	Correct Page	Correct	ID
Display AC specification	132	-	132	(- Updated the min/max value for |tRSD|, tRSV, tSPD, tSPV. - Delete the note for *2. - Updated figure for definition of tSPV and tRSV.)	#506
Display AC specification	133	-	133	(- Updated the min/max value for tDC1D, tDC1V and delete the remarks for tDC1V. - Updated figure for definition of tDC1V.)	#505
FPD-Link Output Clock Frequency	135	Output clock frequency: 1MHz(min),50MHz(max)	135	Output clock frequency: -(min),50MHz(max)	#522
Add "TxCLK+/-" in case of don't support FPD-Link	135	Note: − All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-.	135	Note: − All the corresponding ports of products which don't support FPD-Link should be connected to GND. AVCC3_LVDS_PLL, AVSS3_LVDS_PLL, VCC3_LVDS_Tx, VSS3_LVDS_Tx, TxDOUTn+/-, TxCLK+/-.	#525
DDRHSSPI (SDR) clock cycle for Quad Page Program	138	-	138	HSSPI clock cycle:20(Min):when Quad Page Program	#484
HyperBus AC specification	144	RDS↑↓> DQ (valid) Setup time ,,, RDS↑↓> DQ (invalid)Hold time	144	RDS↑↓> DQ Setup time ,,, RDS↑↓> DQ Hold time	#519
ADC Software Trimming	153	-	153	8.5.4 Calibration ConditionCalibration Condition A/D Converter should be calibrated under the following condition.AVCC=5.0V AVRH=5.0V Ta=25℃ system clock frequency (CLK_LCP1A)= 10MHz See A/D Converter Calibration on the S6J3200 hardware manual.	#358

Document History

Document Title: S6J3200 Series 32-bit Microcontroller TRAVEO™ T1G Family
Document Number: 002-05682

Revision	ECN	Submission Date	Description of Change
**	-	09/30/2015	Migrated to Cypress and assigned document number 002-05682. No change to document contents or format.
*A	5234352	04/22/2016	Updated formatting
*B	5340908	07/08/2016	2. Function List 2.1 Function List [Improve] Corrected the number of CRC unit. (1unit -> 4unit)
			2. Function List 2.2.1 Basic Option 2.2.2 ID [Improve] Updated the "Option and Part Number", "Function Digit table" and "ID" table for adding new revision and improving readability.
			2. Function List 2.2.2 ID [Improve] Added the value of Platform ID in SYSC0_SYSPFIDR
			3. Product Description 3.2 Product Description [Enhancement] Added support for center spread mode with limited condition
			3. Product Description 3.2 Product Description [Improve] Added the description for "MK_CEER" of security
			3. Product Description 3.2 Product Description [Improve] Added the description for hot swap function of I2C
			3. Product Description 3.2 Product Description [Improve] Added the explanation for function of PSC1.
			3. Product Description 3.2 Product Description [Improve] Added the explanation for reset of EX5VRST.
			3. Product Description 3.2 Product Description [Improve] Added the information of main oscillation stabilization wait time.
			3. Product Description 3.2 Product Description [Improve] Added the register information of "Interrupt Enable Register" (HYPERBUSIn_IEN) for clarifying "not support".
			3. Product Description 3.2 Product Description [Improve] Corrected the number of I2C support ports for MFS.
			3. Product Description 3.2 Product Description [Improve] Corrected the revision digit information for Ethernet AVB.
			3. Product Description 3.2 Product Description [Improve] Corrected the stabilization time for embedded CR oscillation.
			3. Product Description 3.2 Product Description [Improve] For convenience to understand power domain definition.

Revision	ECN	Submission Date	Description of Change
			3.Product Description 3.2 Product Description [Improve] Deleted the unnecessary description for PPU of I2S
			4. Package and Pin Assignment 4.1 Pin Assignment [Improve] Added the part number information for figure 4-8 and 4-15
			4. Package and Pin Assignment 4.1.1 TEQFP-216 Pin Assignment [Improve] Added the "M_CK_0" for TEQFP-216 Pin Assignment
			4. Package and Pin Assignment 4.1.2 TEQPF-208 Pin Assignment [Improve] Corrected part number in figure title. (S6J32xCL -> S6J32xCK)
			4. Package and Pin Assignment 4.1.3 TEQPF-256 Pin Assignment [Improve] Corrected the IO-circuit type for pin.217 to 256
			6. Port Description 6.1 Port Description List [Improve] Added the supplementary information for I2C pin name of SCL, SDA.
			7. Precautions and Handling Devices 7.2 Handling Devices [Improve] Deleted the obsolete description about power ramp rate ("About the Power-on Time")
			7. Precautions and Handling Devices 7.2 Handling Devices [Improve] Removed duplicated description
			7. Precautions and Handling Devices 7.2. Handling Devices [Limitation] Added description of how to turn off VCC12 during power off sequence.
			8. Electric Characteristics 8.1 Absolute Maximum Rating [Improve] Deleted "total maximum clamp current" for special spec.
			8. Electric Characteristics 8.1 Absolute Maximum Rating [Limitation] Added the condition to "Analog pin input voltage"
			8. Electric Characteristics 8.2 Operation Assurance Condition [Improve] clarified the rate of die stage area which is exposed at back surface of package for heat dissipation.
			8. Electric Characteristics 8.3.1 Port Function Characteristics [Improve] Remarks of VOH5 is modified.
			8. Electric Characteristics 8.3.2.1 Run Mode [Improve] Added information. "50 MHz" into AVCC3_LVDS_PLL.
			8. Electric Characteristics 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) [Enhance] PD4 shutdown support [Improve] Added remarks in osc mode spec
			8. Electric Characteristics 8.4.1 Source Clock Timing [Improve] Corrected the min value of source oscillation clock cycle time.
			8.Electric Characteristics 8.4.3 Internal Clock Timing [Enhancement] Added support for center spread mode with limited condition

Revision	ECN	Submission Date	Description of Change
			8. Electric Characteristics 8.4.3 Internal Clock Timing [Enhance] The series of port reference voltage level VIL/VIH/VOL/VOH for HyperBus AC specification is defined.
			8. Electric Characteristics 8.4.3 Internal Clock Timing [Improve] Corrected the maximum output frequency of SSCG0 and PLL0
			8. Electric Characteristics 8.4.4 Reset Input [Improve] Improved readability for width for reset input removal.
			8 Electric Characteristics 8.4.5 Power-On Conditions [Enhancement] Reduced Power off time to 1ms [Limitation] Defined Power ramp rate requirement for 1)when tOFF is satisfied 2)tOFF is not satisfied [Limitation] Increased Level detection time to 540us
			8.Electric Characteristics 8.4.5.2 VCC12 Stabilization Time during Power-On / PSS to RUN Transition [Limitation] Added VCC12 stabilization time requirement for power-up sequence and PSS to RUN transition
			8. Electric Characteristics 8.4.6.2 CSIO Timing (SMR:MD2-0=0b010) [Improve] Corrected min value of Serial clock "H" pulse width and Serial clock "L" pulse width
			8. Electric Characteristics 8.4.6.2 CSIO Timing (SMR:MD2-0=0b010) [Limitation] Changed AC spec of MFS CSIO mode
			8.Electric Characteristics 8.4.6.2 CSIO Timing (SMR:MD2-0=0b010) [Improve] Added CS output AC timing.
			8. Electric Characteristics 8.4.6.4 I2C Timing (SMR:MD2-0=0b100) [Improve] Corrected the name of "High-Speed Mode" to "Fast Mode".
			8. Electric Characteristics 8.4.7 Timer Input [Improve]Clock definition of remarks is modified
			8. Electric Characteristics 8.4.8 Trigger Input [Improve] Definition of RXx pin and limitation of stop mode is deleted.
			8. Electric Characteristics 8.4.10 Low-Voltage Detection [Limitation] Corrected release voltage for LVDL0, LVDH0 and LVDL1
			8 Electric Characteristics 8.4.10 Low-Voltage Detection [Limitation] Add note that this LVDL0 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage [Improve] Removed LVDH0 table due to duplication with 8.4.5 Power-On Conditions [Limitation] Add note that this LVDL1 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage with any setting [Limitation] Add note that this LVDH1 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage for some of the settings

Revision	ECN	Submission Date	Description of Change
			[Limitation] Add note that this LVDL2 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage with any setting [Limitation] Add note that this LVDH2 cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage for some of the settings
			8. Electric Characteristics 8.4.10.3 LVDL1 [Improve] Deleted the useless configuration of LVDL1. (LVDL1V=01)
			8.Electric Characteristics 8.4.10.6 LVDH2 [Improve] Typ value of release voltage at conditions of LVDH2V=0001 changes 2.75V to 2.85V.
			8. Electric Characteristics 8.4.11 High Current Output Slew Rate [Improve] Corrected the typo in figure. (VOL8, VOH8 -> VOL, VOH)
			8. Electric Characteristics 8.4.12.2 Display Controller0 Timing (RSDS) [Improve] Delete unnecessary characteristics
			8. Electric Characteristics 8.4.14 FPD-link [Improve] Corrected unit. "Ohm" -> "ohm" [Improve] Corrected remarks on "Common mode voltage". "One of three" -> "One of two" [Improve] Added missing information. "5 pF (differential)" [Improve] Corrected format. "25MHz" -> "25 MHz", "4/7" -> "4 / 7". [Improve] Added cycle to cycle jitter spec. [Improve] Added information. "Equals 1/f" into TCIP. [Improve] Corrected max time in "Cycle time of TXCLKP/M". [Improve] Added other frequency spec into "Output pulse position". [Limitation] Added PLL lock-up time. [Improve] Separately added specs for revision H.
			8. Electric Characteristics 8.4.14. FPD-Link (LVDS) [Limitation] Specified minimum output frequency 5MHz.
			8. Electric Characteristics 8.4.16 HyperBus [Enhance] Enhanced AC spec Hyper Bus read timing and corrected timing chart
			8. Electric Characteristics 8.4.16 HyperBus [Enhance] The series of port reference voltage level VIL/VIH/VOL/VOH for HyperBus AC specification is defined.
			8. Electric Characteristics 8.4.16 HyperBus [Improve] Added a note for clarifying the HyperBus clock cycle and source.
			8. Electric Characteristics 8.4.16 HyperBus [Improve] Corrected the revision digit information.
			8. Electric Characteristics 8.4.19 Port Noise Filter [Improve] Change the description of filter specification and note for GPIO [Improve] Added the filter specification for EINT, TIN [Improve] Added the filter specification for SCL, SDA of I2C

Revision	ECN	Submission Date	Description of Change
			9. Abbreviation [Improve] Added the word "QPRC" to abbreviation.
			10. Ordering Information [Improve] Updated "Order Part Number Table"
			11. Appendix 11.1 Application 1: JTAG tool connection [Improve] Figure of JTAG tool connection as an application example is added.
*C	5515119	11/10/2016	2. Function List 2.2.1.1 S6J320C [Improve] Added new function digit 9 to Function digit table
			2. Function List 2.2.1.1 S6J320C [Improve] Updated the Revision information
			2. Function List 2.2.1.2 S6J320A [Improve] Corrected the Revision information (Digit:G -> Digit:E)
			2. Function List 2.2.2 ID [Improve] Added the ID information for revision J, K, L, and M
			4. Package and Pin Assignment 4.2 Package Dimensions [Limitation] Updated PKG figure and changed parameter of symbol b, c and ddd for LEQ216 [Improve] Updated PKG figure for LET208 and LER208
			7. Precautions and Handling Devices 7.2 Handling Devices [Limitation] Added the "Method to Switch off VCC12 during Power-off Sequence" for except revision M
			8. Electric Characteristics 8.3.2.1 Run Mode [Limitation] Changed the power supply current of "AVcc3_LVDS_PLL" for after revision H.
			8. Electric Characteristics 8.4.4.2 Power supply voltage stability conditions [Limitation] Added the power supply voltage stability conditions for revision M
			8. Electric Characteristics 8.4.10.4 LVDH1 [Limitation] Added the note for power supply voltage stability conditions
			8. Electric Characteristics 8.4.14 FPD-Link (LVDS) [Improve] Added the revision information for AC specification table
			8. Electric Characteristics 8.7.2 Notes [Limitation] Added the note for shutdown of external power
*D	5638486	02/22/2017	2. Function List 2.2.1.1 S6J320C [Limitation] Sub clock stabilization time
			2. Function List 2.2.2 ID [Improve] Added the IPIdentifier information for graphic subsystem
			4. Package and Pin Assignment 4.1 Pin Assignment [Improve] Added "S6J329" for PKG figure information

Revision	ECN	Submission Date	Description of Change
			4. Package and Pin Assignment 4.2 Package Dimensions [Improve] Corrected "A1" value of LEQ216, LET208, LER208 (0.00(MIN)-0.20(MAX) -> 0.05(MIN)-0.15(MAX)) [Improve] Added figure for 256 pin PKG
			6. Port Description 6.1 Port Description List [Improve] Exposed pad connection recommendation
			7. Precautions and Handling Devices 7.2 Handling Devices [Improve] Corrected the typo in "Method to Switch off VCC12 during Power-off Sequence" (RTSX -> RSTX)
			8. Electric Characteristics 8.2 Operation Assurance Condition [Improve] Exposed pad connection recommendation
			8. Electric Characteristics 8.2 Operation Assurance Condition [Limitation] Added the note about the connection of Vcc53.
			8. Electric Characteristics 8.3.1 Port Function Characteristics [Improve] Corrected the VOH/VOL drive capacity when VCC53=3.0V.
			8. Electric Characteristics 8.3.2 Power Supply Current [Improve] Add revision E and J to 'Remarks' of AVCC3_LVDS_PLL.
			8.Electric Characteristics 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) [Enhance] Added external clock mode spec
			8. Electric Characteristics 8.3.2 Power Supply Current [Improve] Added note of regulator mode for measurement condition to 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) and 8.3.2.3 PSS Stop Mode Shutdown.
			8.Electric Characteristics 8.4.6.2 CSIO Timing (SMR: MD2-0=0b010) [Improve] Corrected the min. value of tSCYC [Improve] Corrected the min. value of tSOVLI and tSOVHI [Improve] Remove the Remarks for tSYSC, tSHSL and tSLSH
			8. Electric Characteristics 8.4.10.4 LVDH1 [Limitation] Added more setting needed for power supply voltage stability conditions
			8. Electric Characteristics 8.4.10.5 LVDL2 [Improve] Corrected the typo in Max release voltage of "LVDL2V=01" condition. (9.995 -> 0.995)
			8. Electric Characteristics 8.4.12 Display Controller [Improve] Corrected the min. value of Clock Cycle for DSP0_CLK in 8.4.12.1 Display Controller0 Timing (TTL Mode). [Improve] Corrected the min. value of Clock Cycle for DSP0_CLK+/- in 8.4.12.2 Display Controller0 Timing (RSDS).
			8.Electric Characteristics 8.4.15 DDR-HSSPI [Enhance] Add description for reference voltage of VIL, VIH, VOL and VOH

Revision	ECN	Submission Date	Description of Change
			8. Electric Characteristics 8.4.15.2 DDR-HSSPI Interface Timing (DDR Mode) [Improve] Corrected timing chart of "G_SDATA0_0-3", "GSDATA1_0-3" and "GSSEL0,1" for DDR mode.
			8. Electric Characteristics 8.4.16 HyperBus [Enhance] Added note with regard to HyperRAM refresh interval in 8.4.16.2 Hyper Bus Write Timing (HyperRAM). [Enhance] Added note with regard to HyperRAM refresh interval in 8.4.16.4 Hyper Bus Read Timing (HyperRAM).
			8.Electric Characteristics 8.4.20 JTAG [Enhance] Add JTAG AC specifications
			8.Electric Characteristics 8.4.21 QPRC [Enhance] Add AC specification for QPRC
			8.Electric Characteristics 8.4.22 I2S [Improve] Add AC specification for I2S
			10. Ordering Information [Improve] Updated "Ordering Information"
*E	5690647	04/18/2017	Updated Cypress Logo and Copyright.
*F	5879435	09/19/2017	1. Overview 1.1 Document Definition Table 1-1 [Improve] Added the "Document Code" information for Application note
			2.Function List 2.1 Function List [Enhance] Updated Description and Remark for System-RAM size enhance
			2. Function List 2.2.1 Basic Option Figure 2-1 [Improve] Updated "Revision version" information
			2.Function List 2.2.1.1 S6J320C Note [Improve] Updated revision digit information
			2.Function List 2.2.1.3 S6J320E [Enhance] Added the Basic option information for S6J320E Series
			2.Function 2.2.2 ID [Improve] Updated function digit information
			2.Function List 2.2.2 ID [Enhance] Added the ID information of Function Digit K, L, M, N for S6J320E Series
			3. Product Description 2. Product Description [Improve] Added the description for INITX
			3. Product Description 3.2 Product Description Table 3-1. [Limitation] Add limitation of FPD-Link converter.
			4. Package and Pin Assignment 4.1 Pin Assignment [Enhance] Added the figure of pin assignment for S6J320E Series
			4. Package and Pin Assignment 4.2 Package Dimensions [Enhance] Added the Function Digit information for S6J320E Series
			5. I/O Circuit Type 5.1 I/O Circuit Type

Revision	ECN	Submission Date	Description of Change
			[Improve] Corrected typo of pull-up/down resistance value in I/O circuit Type E
			7. Precautions and Handling Devices 7.2 Handling Devices About C Pin Processing [Improve] Deleted typo about other series product information.
			8.Electric Characteristics 8.2 Operation Assurance Condition [Enhance] Added two Power supply sequence
			8. Electric Characteristics 8.3.2 Power Supply Current [Enhance] Added the power supply current for S6J320E Series
			8.Electric Characteristics 8.3.2.1 Run Mode [Improve] Updated function digit information
			8.Electric Characteristics 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) [Improve] Updated function digit information
			8. Electric Characteristics 8.4.3 Internal Clock Timing Table 8-1 [Enhance] Added the Function Digit K, L, M, N for S6J320E Series
			8.Electric Characteristics 8.4.3 Internal Clock Timing [Improve] Updated function digit information
			8.Electric Characteristics 8.4.6.2 CSIO Timing (SMR: MD2-0=0b010) [Improve] Updated function digit information
			8. Electric Characteristics 8.4.6 Multi-Function Serial [Enhance] Added the Function Digit K, L, M, N for S6J320E Series
			8.Electric Characteristics 8.4.16.3 Hyper Bus Read Timing (HyperFlash) [Improve] Updated function digit information
			10. Ordering Information [Enhance] Updated "Order Part Number"
*G	5986519	12/07/2017	4. Package and Pin Assignment 4.1.1 TEQFP-216 Pin Assignment [Improve] Added "S6J329CLxx" for title of figure 4-2 of pin assignment.
			4. Package and Pin Assignment 4.1.2 TEQPF-208 Pin Assignment [Improve] Added "S6J329CKxx" for title of figure 4-10 of pin assignment.
			7. Precautions and Handling Devices 7.2 Handling Devices Power Supply Pin Processing of an A/D Converter [Improve] Removed "AVRL"
			7. Precautions and Handling Devices 7.2 Handling Devices Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter [Improve] Changed from "AVRL" to "AVSS"
			8.Electric Characteristics 8.4.4.2 Power supply voltage stability conditions [Improved] Improved timing chart
			8.Electric Characteristics 8.5 A/D Converter [Improve] Removed "AVRL5" from Pin Name of Reference voltage AVRL(Symbol)
*H	6054035	02/01/2018	8.Electric Characteristics 8.4.12 Display Controller [Improve] Change spec of display controller timing.

Revision	ECN	Submission Date	Description of Change
*I	6195638	05/31/2018	2.Function List 2.2.1.1 S6J320A [Enhance] Added revision P to Figure 2-1 [Enhance] Added remark 1), 2) of revision to Figure 2-1 [Improve] Removed the description of limitation of revision F from Notes
			2.Function List 2.2.1.2 S6J320A [Improve] Removed option Digit U and Pin count Digit L from Figure 2-2 [Improve] Removed function Digit A,C,D from Table 2-3
			2.Function List 2.2.1.3 S6J320E [Improve] Removed option Digit U from Figure 2-3
			2.Function List 2.2.2 ID [Enhance] Added Revision P of Function Digit 3,4,5,6,7,8,9 to table [Improve] Removed Function Digit A,C,D from table [Improve] Removed Option U of Function Digit B,K,L,M,N from table
			3. Product Description 3.2 Product Description [Enhance] Added revision P to FPD-Link Converter of Table 3-1 [Improve] Removed “Note: -The description of the preliminary documentation will be changed without any notification.”
			4. Package and Pin Assignment 4.1 Pin Assignment [Improve] Removed Function Digit A,C,D from table [Improve] Removed TEQFP-216 of Function Digit B from table
			4. Package and Pin Assignment 4.1.1 TEQFP-216 Pin Assignment [Improve] Removed Figure 4-9:TEQFP-216 (S6J32xALxx)
			6. Port Description 6.1 Port Description List [Improve] Revised Description of G_SSEL0, G_SSEL1, M_SSEL0, M_SSEL1 from “HS-SPIx select” to “HS-SPI select x”
			7. Precautions and Handling Devices 7.2 Handling Devices [Enhance] Added revision P to “Method to Switch off VCC12 during Power-off Sequence”
			8. Electric Characteristics 8.3.1 Port Function Characteristics [Enhance] Added Hysteresis voltage ($V_{HYS1-12}$)
			8. Electric Characteristics 8.3.2.1 Run Mode [Enhance] Added revision P to Remark of “ILVDS” [Improve] Removed function digit A,C,D from title
			8. Electric Characteristics 8.3.2.2 PSS Timer Mode Shutdown (PD6=OFF) [Improve] Removed function digit A,C,D from title
			8. Electric Characteristics 8.3.2.3 PSS Stop Mode Shutdown [Improve] Removed function digit A,C,D from title
			8. Electric Characteristics 8.4.3 Internal Clock Timing [Improve] Removed function digit A,C,D from Notes:
			8. Electric Characteristics 8.4.4.2 Power Supply voltage stability conditions [Enhance] Added revision P title and Notes:
			8. Electric Characteristics 8.4.6.2 CSIO Timing (SMR: MD2-0=0b010) [Improve] Removed function digit A,C,D from Remark

Revision	ECN	Submission Date	Description of Change
			8. Electric Characteristics 8.4.10.4 LVDH1 [Enhance] Added revision P to Note and title of t_{FV5}, t_{FV12}
			8. Electric Characteristics 8.4.12.1 Display Controller0 Timing (TTL Mode) [Enhance] Added revision P to Notes: [Improve] Removed function digit A,C,D from Note
			8. Electric Characteristics 8.4.12.2 Display Controller0 Timing (RSDS) [Enhance] Added revision P to Notes: [Improve] Removed function digit A,C,D from Notes:
			8. Electric Characteristics 8.4.12.3 Display Controller1 Timing [Enhance] Added revision P to Notes:
			8. Electric Characteristics 8.4.14.1 For Revision M [Enhance] Added revision P title and Notes:
			8. Electric Characteristics 8.4.16.3 Hyper Bus Read Timing (HyperFlash) [Enhance] Revised revision G to revision H, M, P of (C)
			8. Electric Characteristics 8.4.16.4 Hyper Bus Read Timing (HyperRAM) [Enhance] Revised after revision G to revision H, M, P of (C)
			8. Electric Characteristics 8.7.2 Notes [Enhance] Added revision P to Notes
			10. Ordering Information [Improve] Removed S6J32BALSExC2000x, S6J32DAKSExE2000x, S6J32DALSExC2000x and added S6J32K/L/M/N devices [Enhance] Added revision P devices [Enhance] Added option U devices [Improve] Defined ordering options for all devices
*J	6269495	08/01/2018	11. Errata [Improve] Added Errata chapter as new chapter
*K	6530775	04/04/2019	8. Electric Characteristics 8.4.1 Source Clock Timing [Enhance] CAN PLL jitter
			8. Electric Characteristics 8.4.15.1 DDR-HSSPI [Improve] Revised timing figure.
			10. Ordering Information Table 10 1: Order Part Number Table [Improve] Removed S6J323CKSMSE2000A, S6J323CLSMSC2000A, S6J324CLSMSC20000, S6J326CKSMSE20000, S6J328CKSMSE2000A, S6J328CLSMSC2000A, S6J329CLSMSC2000A [Enhance] Added S6J328CLSPSC2D000, S6J329CLSPSC2D000
*L	6577217	05/24/2019	Updated to new template.
*M	6669328	09/10/2019	4. Pin Assign [Enhance] Added the same color as the power supply to pin in Figure 4-2 to Figure 4-17
			8. Electric Characteristics 8.4.3 Internal Clock Timing [Improve] Updated the explanation of “Unused” in Notes

Revision	ECN	Submission Date	Description of Change
			8. Electric Characteristics 8.5.2 Notes on A/D Converters [Enhance] Added the formula of sampling time
			10. Ordering Information Table 10 1: Order Part Number Table [Improve] Removed S6J323CLUMSC20000 S6J325CKSMSE20000 S6J325CLSMSC20000 S6J325CLUMSC20000 S6J326CLSMSC20000 S6J327CKSMSE20000 S6J327CLSMSC20000 S6J327CLUMSC20000 S6J329CKSMSE20000 S6J329CKUMSE20000
*N	6934532	08/11/2020	2. Function List 2.1 Function List [Improve] Corrected Table 2-1: Display clock of ch0 80MHz -> 64MHz
			2. Function List 2.2.1.1 S6J320C [Improve] Revised Figure 2 1: Option and Part Number for S6J320C
			2. Function List 2.2.1.3 S6J320E [Improve] Revised Figure 2-3: Option and Part Number for S6J320E
			2. Function List 2.2.3 Restriction [Improve] Remove note “TEQFP-256 is a package option under planning”
			10. Ordering Information Table 10 1: Order Part Number Table [Improve] Remove “It is under planning.” from annotations below the table
*O	7100560	03/15/2021	Updated 11. Errata For details, see 13. Major Changes.
*P	7238483	08/23/2021	Updated Function List: Updated Optional Function: Updated Basic Option: Updated S6J320E: Updated Figure 2-3. Completing Sunset Review.
*Q	7402560	10/27/2021	Updated 11. Errata. For details, see 13. Major Changes.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

© Cypress Semiconductor Corporation, 2015-2021. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.