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Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

ADVANCE

CYW43012

Single-Chip, Ultra-Low Power, IEEE 802.11n, 802.11ac-friendly™ MAC/Baseband/Radio with Bluetooth 5.0

The Cypress® CYW43012 is a 28-nm, ultra-low power single-chip device that supports single-stream, dual-band IEEE 802.11n-compliant Wi-Fi MAC/baseband/radio and Bluetooth 5.0. When used with IEEE 802.11ac access points, the CYW43012 provides superior performance in terms of throughput and power consumption than other 802.11n products by leveraging 802.11ac-friendly™ features.

In IEEE 802.11n mode, rates of MCS0–MCS7 (up to 64-QAM) in 20 MHz channels are supported for data rates of up to 72.2 Mbps.

The CYW43012 provides 802.11ac friendliness by supporting 256-QAM (for 20 MHz channels in the 5 GHz band) enabling data rates of up to 78 Mbps with 802.11ac access points. All legacy rates specified in the IEEE 802.11a/b/g/n specifications are also supported. Included on-chip are 2.4 GHz and 5 GHz transmit power amplifiers and receive low-noise amplifiers.

CYW43012 includes a Bluetooth subsystem that is Bluetooth 5.0-compliant and supports Basic Rate/Enhanced Data Rate/BLE. In the BLE mode the new LE 2 Mbps data rate as well as existing 1 Mbps data rates are supported.

The WLAN section supports an SDIO v3.0 interface that can operate in 4b or 1b mode. The Bluetooth section supports a high-speed 4-wire UART interface.

The CYW43012 is designed to address the needs of IoT devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology while maximizing battery life.

The CYW43012 includes coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth simultaneous operation is optimized for maximum performance. In addition, coexistence support for external radios (such as LTE and GPS) is provided via an external interface.

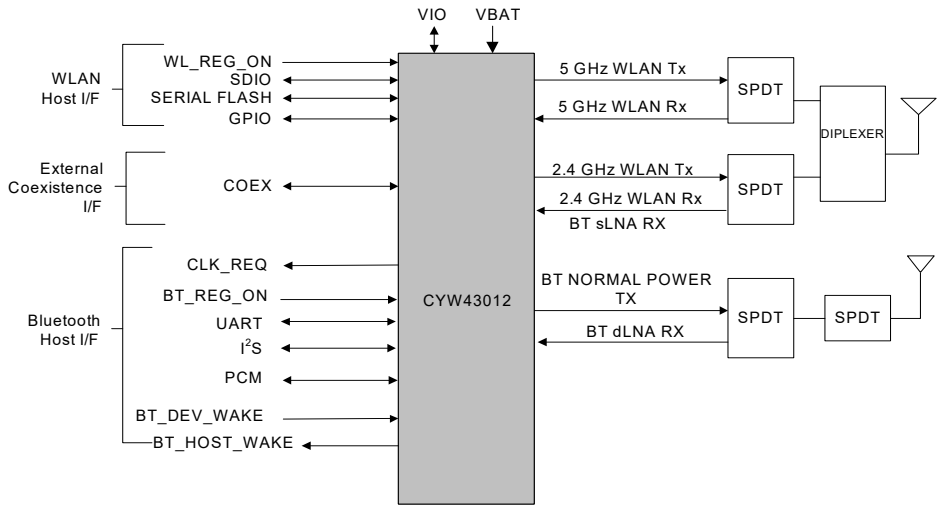
Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM43012	CYW43012
BCM43012WKWBG	CYW43012C0WKWBGT
BCM43012TC0KFFBH	CYW43012TC0KFFBH

Figure 1. Functional Block Diagram



Note a: IEEE 802.11ac full-compliance requires support for 40 MHz and 80 MHz channel bandwidths. CYW43012 is 802.11ac-friendly. It only supports 20 MHz channel bandwidth however it supports 802.11ac's 256-QAM for the 20 MHz channels in the 5 GHz band enabling it to offer higher throughput and lower energy per bit than 802.11n only products. In addition CYW43012, when used as a STA with an 802.11ac access point, supports 802.11ac's explicit beamformee feature to offer significantly higher throughputs than 802.11n chipsets at any given range.

Features

IEEE 802.11x Key Features

- Full IEEE 802.11a/b/g/n compatibility with enhanced performance.
- 802.11ac friendly, MCS8 (256-QAM) for 20 MHz channels in 5 GHz band.
- Single spatial stream with PHY data rates of up to 72.2 Mbps with 802.11n (MCS7) and 78 Mbps with 802.11ac (MCS8).
- 20 MHz channels with optional SGI support for MCS0-MCS7.
- IEEE 802.11ac explicit beamformer support.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Receive space-time block coding (STBC)
- On-chip power amplifier/low-noise amplifier for both bands.
- Embedded IPV6 network stack for use with WICED SDK.
- MCS8 in 20 MHz channels (5 GHz band) proven to be interoperable with 802.11ac access points.
- Support for front-end modules (FEMS).
- Supports RF front-end architecture with a single dual-band antenna shared between Bluetooth and WLAN.
- Shared Bluetooth and WLAN receive signal path.
- Supports standard SDIO v2.0 and SDIO v3.0 (SDR40 at 80 MHz and DDR40 at 40 MHz).
- Backward compatible with SDIO v2.0 host interfaces.
- Integrated ARM processor with on-chip RAM and ROM minimizes the need to wake-up the applications processor for standard WLAN functions.

Bluetooth Key Features

- Complies with Bluetooth Core Specification Version 5.0 with provisions for supporting future specifications.
  - QDID: 104548
  - Declaration ID: D035924
- Bluetooth 5.0 compliant with 2 Mbps GFSK data rate for BLE.
- All optional Bluetooth 4.2 features supported.
- Bluetooth Class 1 or Class 2 transmitter operation.
- Supports BDR (1Mbps), EDR (2/3Mbps), BLE (1/2Mbps).
- Host controller interface (HCI) using a high-speed UART interface.
- PCM for audio data.
- Ultra low TX o/p power mode to enable use cases like proximity pairing etc.
- Embedded Bluetooth host stack in ROM.
- Low power consumption improves battery life of handheld devices.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

General Features

- Supports battery voltage range from 3.2V to 4.6V supplies with internal switching regulator.
- Programmable dynamic power management.
- 6144 bits of OTP for storing board parameters.
- 40 GPIOs:
  - 16 WLAN
  - 4 Bluetooth (more available if I2S/PCM/JTAG are not used)
  - 20 shared
- Security:
  - WPA, WPA2 (Personal) with security improvements, WPA3 (Personal) support for powerful encryption and authentication
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
- Worldwide regulatory support: Global products supported with worldwide homologated design.
- Packages:
  - 251-pin WLCSP package (3.76 mm × 4.43 mm, 0.2 mm pitch) - IN PRODUCTION
  - 300-ball FCBGA package (9mm x 9mm, 0.4mm pitch) - IN PRODUCTION
  - 106-ball WLBGA package (3.76mm x 4.43mm, 0.35mm pitch) - IN PRODUCTION

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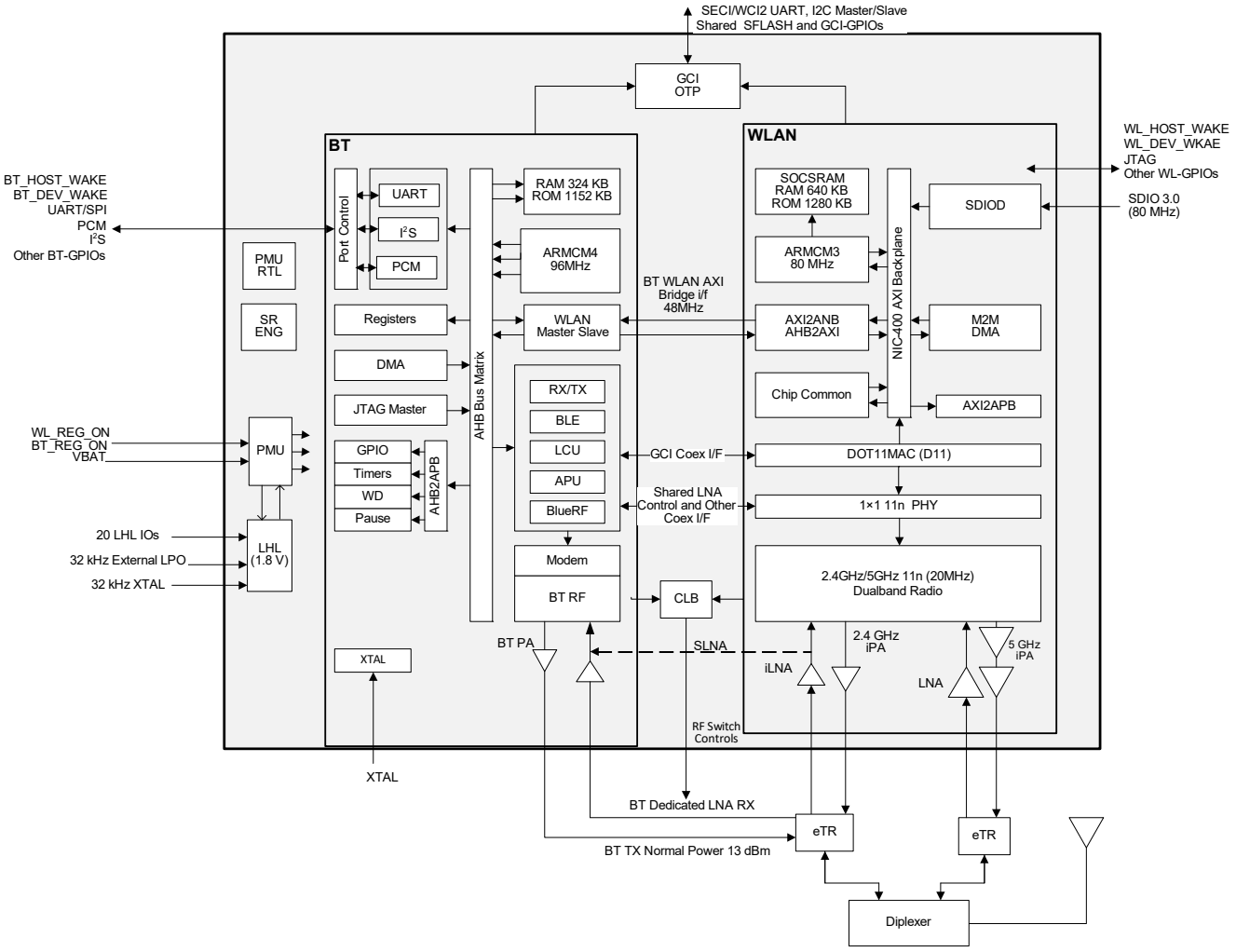
1. CYW43012 Overview

1.1 Overview

The Cypress CYW43012 single-chip device integrates a IEEE 802.11a/b/g/n compliant 802.11ac- friendly MAC/baseband/radio and Bluetooth 5.0 + EDR (enhanced data rate). It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. Comprehensive power management circuitry and software ensure the system can meet the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the CYW43012 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2. CYW43012 Block Diagram



1.2 Standards Compliance

The CYW43012 supports the following Bluetooth standards:

- Bluetooth 5.0 compliance with the optional 2 Mbps BLE (GFSK) data rate
- All optional Bluetooth 4.2 features
  - LE Secure Connections to enable secure connection establishment using the Elliptic-Curve Diffie-Hellman algorithm
  - LE Privacy 1.2 to enable low-power private address resolution
  - LE Data Length Extension to support longer Bluetooth Low Energy packets
- Bluetooth 2.1 + EDR, Bluetooth 3.0

The CYW43012 supports the following IEEE standards and Wi-Fi programs:

- IEEE 802.11V BSS Transition
- IEEE 802.11K Channel load/Beacon Measurement Report.
- IEEE 802.11a/b/g/n
- IEEE 802.11w (Protection management frames)
- IEEE 802.11e QoS Enhancements (as per the WMM specification is already supported)
- 802.11d: Additional regulatory domains
- Security:
  - WPA2 Personal with security improvements, WPA3 with SAE, WMM, WMM-PS (U-APSD), WMM-SA, AES (hardware accelerator), TKIP (hardware accelerator), and CKIP (software support).

2. Power Supplies and Power Management

2.1 Power Supply Topology

One Buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the CYW43012. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.

A single VBAT (3.2V to 4.6V DC max.) and VIO supply (1.62V to 1.98V) can be used, with all additional voltages being provided by the regulators in the CYW43012.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The CBUCK CLDO power-up when any of the reset signals are deasserted. All regulators are powered down only when both BT_REG_ON and WL REG ON are deasserted. The CLDO may be turned OFF/ON based on the dynamic demands of the digital baseband.

The CYW43012 allows for an extremely low power-consumption mode by completely shutting down the CBUCK and CLDO regulators. When in this state, the LPLDO (which is the low-power linear regulator that is supplied by the system VIO supply) provides the CYW43012 with all required voltage, further reducing leakage currents.

2.2 CYW43012 PMU Features

- VBAT to 1.22Vout (250 mA maximum) Core-Buck (CBUCK) switching regulator
- VBAT to 3.3Vout (400 mA maximum) BTLDO3P3
- VBAT to 3.3Vout (100 mA maximum) RFLDO3P3
- VBAT to 1.8Vout (60 mA maximum) HVLDO1P8
- 1.22V to 1.005Vout (100 mA maximum) CLDO with bypass mode for deep-sleep
- VDDIO 1.8V to 0.9V (60 mA maximum) MEMLPLDO
- Analog Mux and power switches for dynamic power scheme reconfiguration into different power modes
- Additional internal LDOs (not externally accessible)
- PMU internal timer auto-calibration by the crystal clock for precise wake-up timing from low-power modes

Figure 3, Figure 6, Figure 7, and Figure 8 show the regulators and a typical power topology.

Figure 3. Typical Power Topology FCBGA/WLCSP (Page 1 of 2)

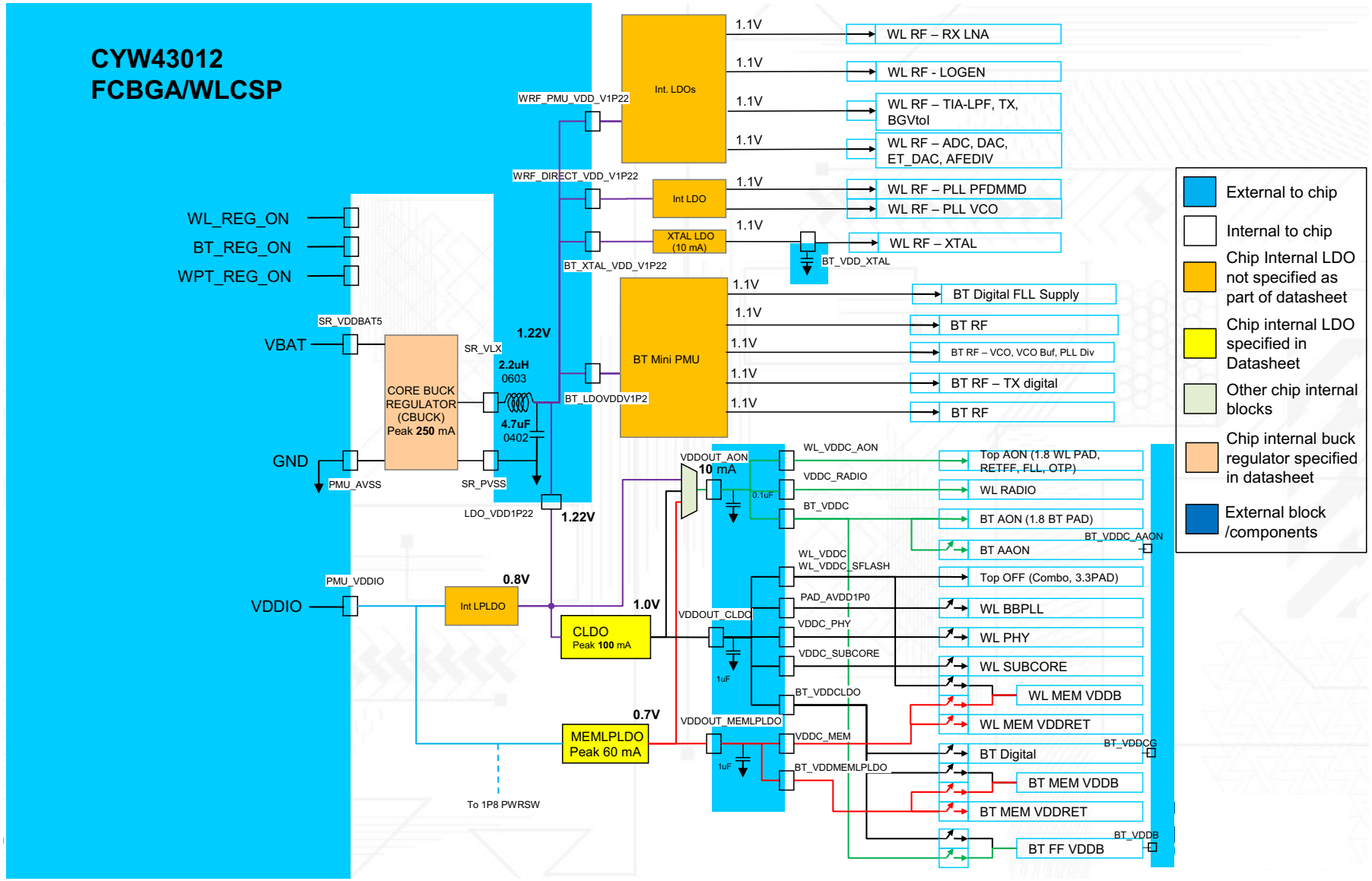
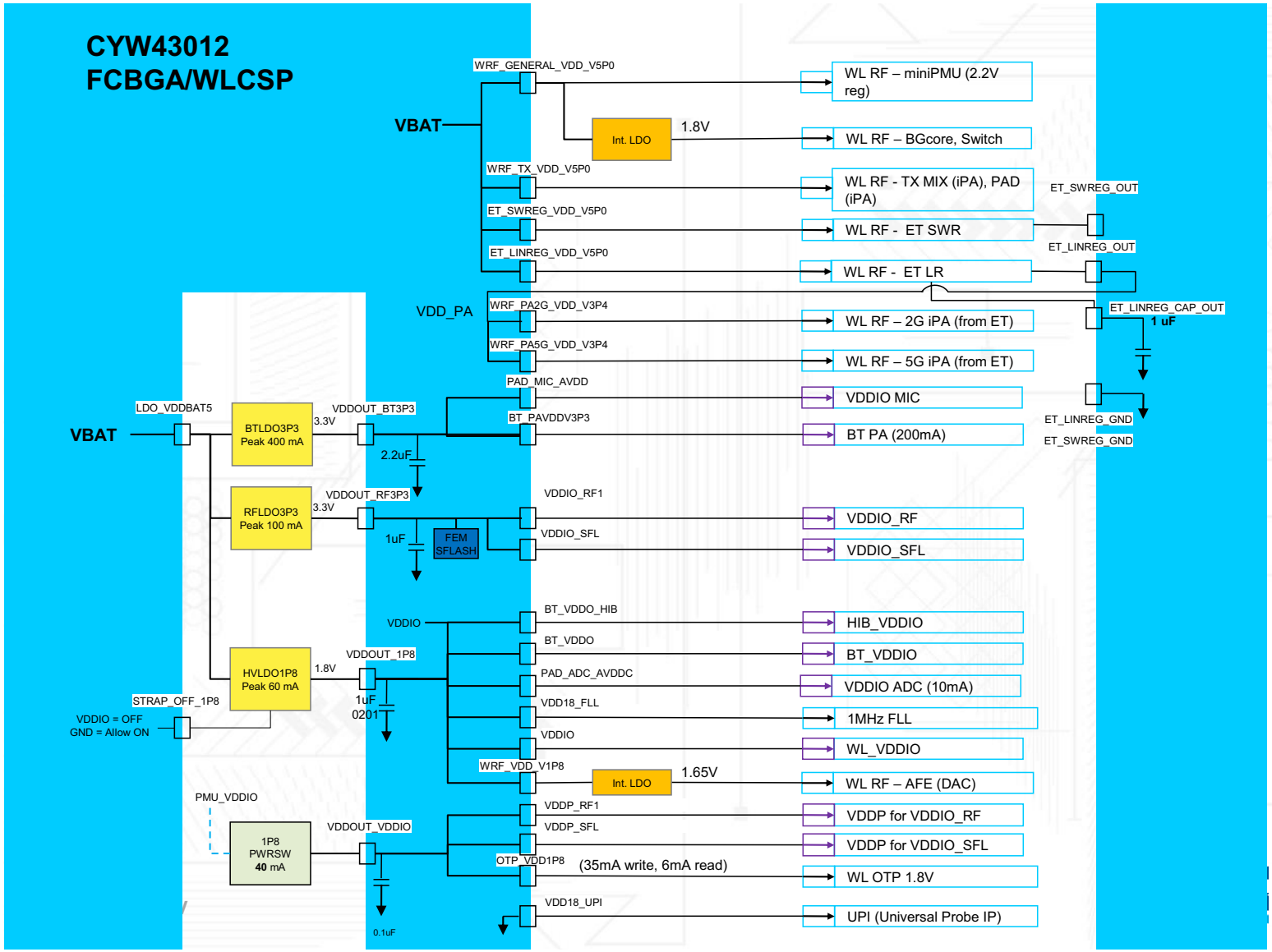


Figure 4. Typical Power Topology FCBGA/WLCSP (Page 2 of 2)



Note:

The HVLDO1P8 is currently not supported. An external 1.8V VDDIO is therefore connected to BT_VDDO_HIB, BT_VDDO, PAD_ADC_AVDDC, VDD18_FLL, VDDIO and WRF_VDD_V1P8 on Cypress's reference designs. The STRAP_OFF_1P8 is also tied to the 1.8V VDDIO. The specifications in this datasheet hold true only in this configuration.

The 1P8PWR switch is also currently not supported. On Cypress's reference designs an external 1.8V VDDIO is therefore connected to VDDP_RF1, VDDP_SFL and OTP_VDD1P8.

Figure 5. Typical Power Topology WLBGA (Page 1 of 2)

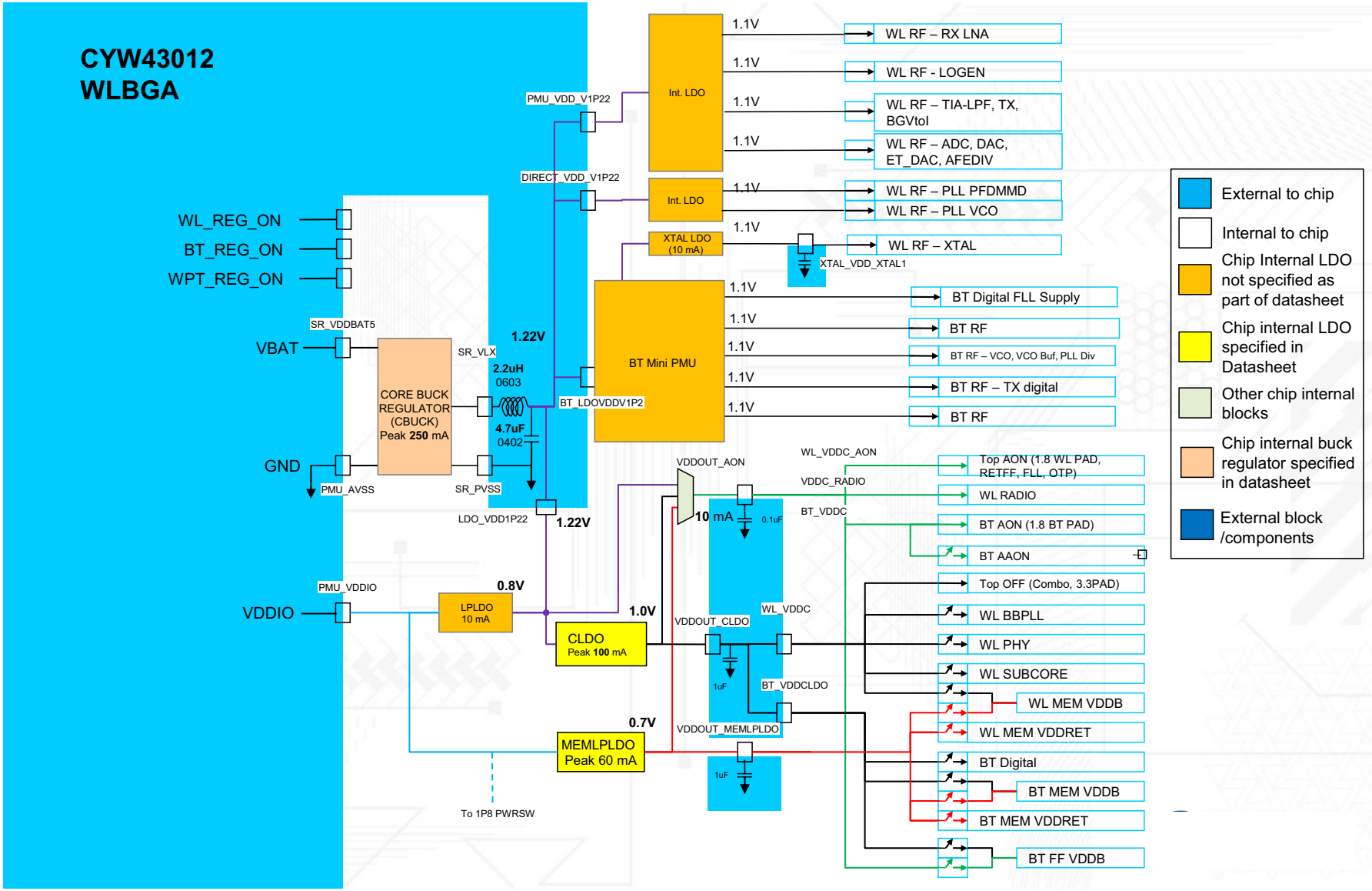
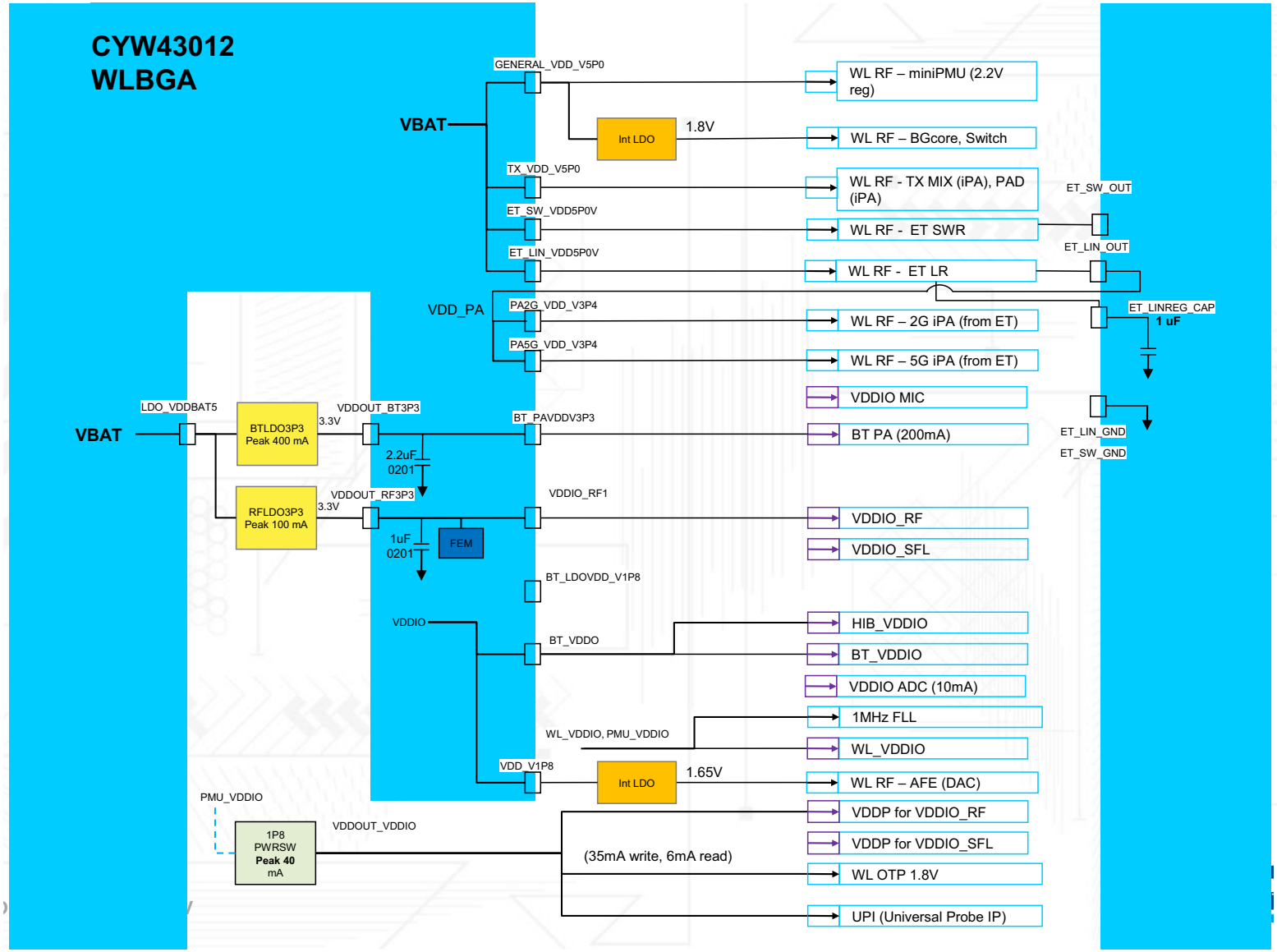


Figure 6. Typical Power Topology WLBGA (Page 2 of 2)



Note:
HVLDO1P8 is not available in WLBGA.

2.3 WLAN Power Management

The CYW43012 has been designed with the stringent power consumption requirements of battery-powered IoT devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW43012 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. Additionally, the CYW43012 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the CYW43012 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The CYW43012 WLAN power states are described as follows:

- Active mode— All WLAN blocks in the CYW43012 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer
- Doze or Sleep mode—The radio, analog domains, and most of the linear regulators are powered down. The rest of the CYW43012 remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator or TCXO) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake-up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current. CYW43012 only support DS0 internal sleep mode. In DS0 the complete RAM needed for WLAN firmware is retained.
- Power-down mode—The CYW43012 is effectively powered OFF by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU Sequencing

The PMU sequencer is used to minimize system power consumption. It enables and disables various system resources based on a computation of required resources and a table that describes the relationship between resources and the time required to enable and disable them.

Resource requests may derive from several sources: clock requests from cores, the minimum resources defined in the *Resource Min* register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states:

- enabled
- disabled
- transition_on
- transition_off

The timer contains 0 when the resource is enabled or disabled and non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when he PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can transition immediately from disabled to enabled. Similarly, a time off value of 0 indicates that the resource can transition immediately from enabled to disabled. The terms *enable sequence* and *disable sequence* refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches 0, the PMU clears the Resource Pending bit for the resource and inserts the Resource State bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.
- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-Off Shutdown

The CYW43012 provides a low-power shutdown feature that allows the device to be turned OFF while the host and any other devices in the system remain operational. When the CYW43012 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows the CYW43012 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to the CYW43012, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables the CYW43012 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When the CYW43012 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

The CYW43012 has an under-voltage lockout (ULVO) when it detects VBAT < 2.23V, it will shutdown the PMU (chip).

2.6 Power-Up/Power-Down/Reset Circuits

The CYW43012 has two signals (see Table 2) that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see WLAN Global Functions on page 42.

Table 2. Power-Up/Power-Down/Reset Control Signals

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43012 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal CYW43012 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled when the input is low and high, respectively.

Table 3. BT/WL REG ON Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high voltage	VIH	For WL and BT ON pins.	1	–	4.6	V
Input low voltage	VIL	–	VSS	–	0.3	V
Pull-down resistance (Internal)	RPD	–	–	50	–	kΩ
Leakage discharged Current	ILEAK_DIS	–	–	28	–	nA
REG OFF time	TREG_OFF	CREG_ON ≤10 pF	2	–	–	ms

2.7 Sequencing of Reset and Regulator Control Signals

The CYW43012 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 7, Figure 8 on page 15, and Figure 9 on page 15 and Figure 10 on page 15). The timing values indicated are minimum required values; longer delays are also acceptable.

Description of Control Signals

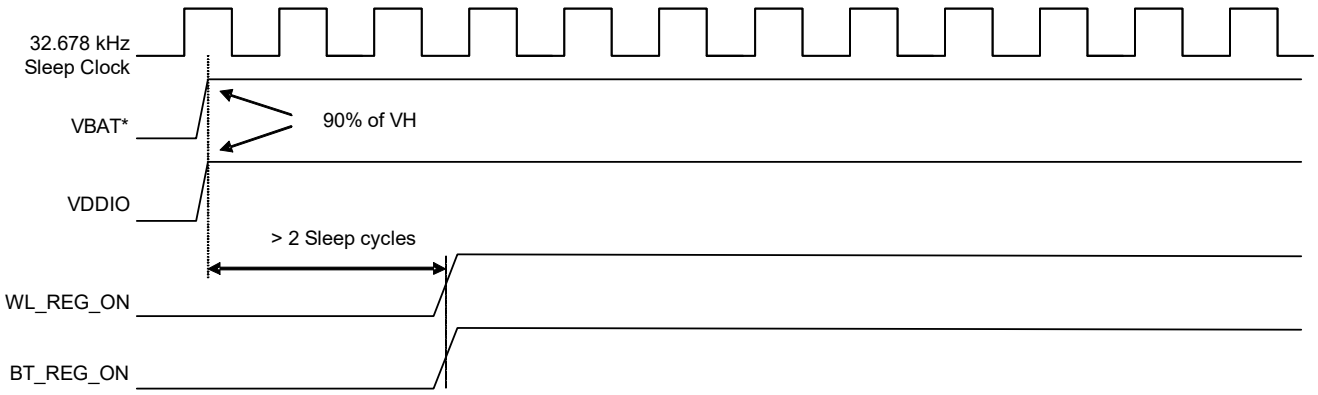
- WL_REG_ON: Used by the PMU to power-up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW43012 regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.
- BT_REG_ON: Used by the PMU (OR-gated with WL REG ON) to power-up the internal CYW43012 regulators. If both the BT_REG ON and WLREG ON pins are low, the regulators are disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset.

Note: The CYW43012 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 185 ms after VDDC and VDDIO are available before initiating Host SDIO or UART accesses.

Note: VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

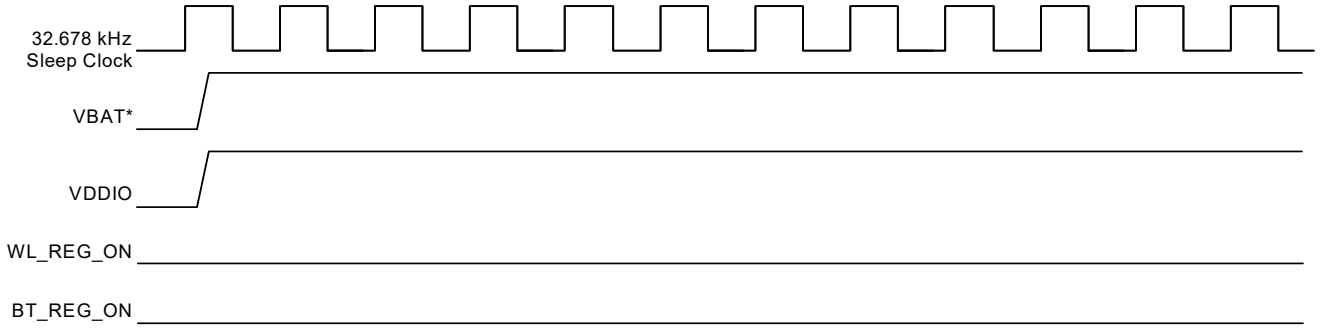
Control Signal Timing Diagrams

Figure 7. WLAN = ON, Bluetooth = ON



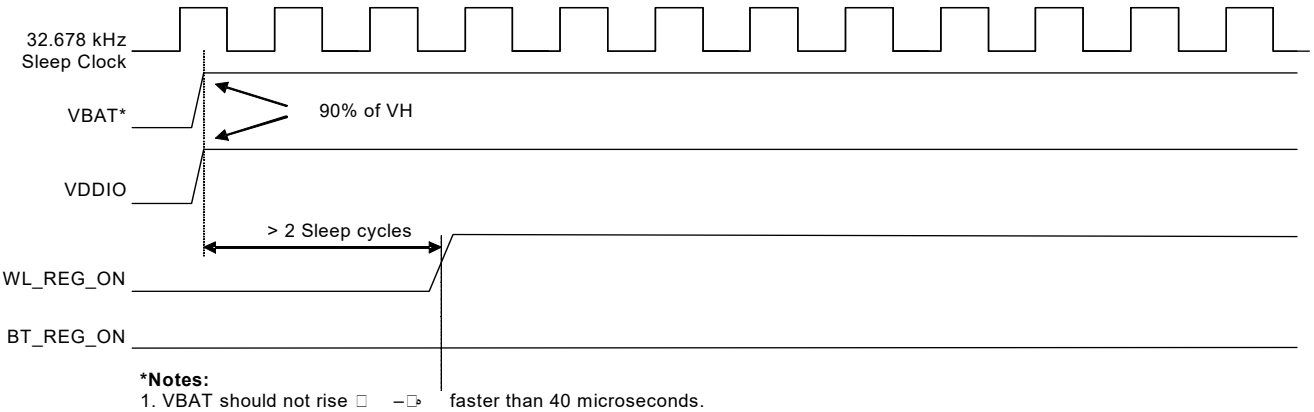
***Notes:**
1. VBAT should not rise □ –□ faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 8. WLAN = OFF, Bluetooth = OFF



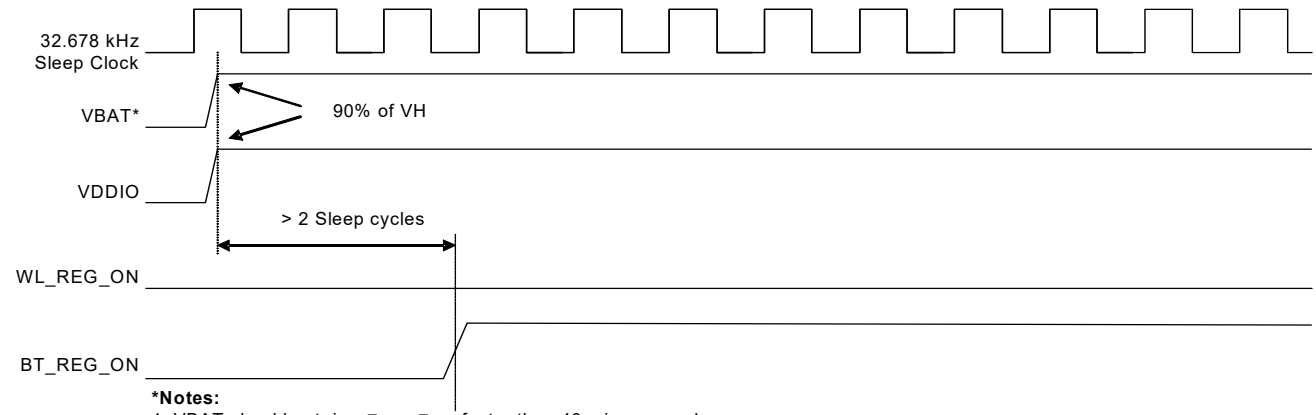
***Notes:**
1. VBAT should not rise □ –□ faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 9. WLAN = ON, Bluetooth = OFF



***Notes:**
1. VBAT should not rise □ –□ faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

Figure 10. WLAN = OFF, Bluetooth = ON



***Notes:**
1. VBAT should not rise □ –□ faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

3. Internal Regulator Electrical Specifications

3.1 Core Buck Switching Regulator

Note: Values in this data sheet are design goals and are subject to change based on device characterization results. Functional operation is not guaranteed outside of the specification limits provided in this section.

Table 4. Core Buck Switching Regulator (CBUCK) Specifications

Specification	Notes	Min.	Typ.	Max.	Unit
Input supply voltage (DC)	DC voltage range	3.2	3.6	4.6	V
PWM mode switching frequency	–	2.8	4	5	MHz
PWM output current	–	–	–	250	mA
Output overcurrent limit	Peak inductor current	–	1.66	–	A
Output voltage range	Programmable, 30 mV steps. default =1.22 V	–	1.22	–	V
PWM output voltage DC accuracy	Includes load and line regulation. Forced PWM.	–4	–	4	%
	Before trimming				
PWM ripple voltage, static	Measure with 20 MHz bandwidth limit. Static Load. V_{BAT} = 3.7 V, Vout = 1.22 V, Fsw = 4 MHz, 2.2 µH inductor L > 1.05 µH effective, Cap+Board total-ESR < 20 mΩ, Cout > 1.9 µF effective, Cout ESL < 200 pH	–	7	20	mVpp
PWM mode peak efficiency	Peak Efficiency at 200 mA load Fsw = 4 MHz PWM L > 2 µH effective inductor Tmax = 1 mm	–	–	–	–
	0603 inch Inductor DCR = 200 mΩ	80	87	–	%
LP-PFM mode efficiency	Efficiency at 20 mA load LP-PFM mode L > 2 µH effective inductor Tmax = 1 mm	–	–	–	–
	0603 inch Inductor DCR = 200 mΩ	70	78	–	%
Start-up time from power down	VDDIO = 1.8V always-on. Time from REG_ON rising edge to CBUCK reaching 1.22V.	–	234	400	µs
External inductor	0806 inch size, 2.2 µH, DCR = 110 mΩ, ACR = 1Ω at 4 MHz	–	2.2	–	µH
External output capacitor	Ceramic, X5R, 0402 inch, ESR < 10 mΩ at 4 MHz, 4.7 µF ± 20%, 6.3 V. Effective cap at 1.22 V include load-side caps.	1.3	4.7	7	µF
External input capacitor	For SR_VDDBATP5V pin, ceramic, X5R, 0402 inch, ESR < 10 mΩ at 4 MHz, 4.7 µF ± 20%, 10V Min value is effective cap at 5.5V	0.67	4.7	–	µF
Input supply voltage	0 to 4.3 V	40	–	1000	µs

3.2 3.3V BT LDO (BTLDO3P3)

Table 5. BTLDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. = V_o + 0.2 V = 3.5 V dropout voltage requirement must be met under maximum load for performance specifications.	3.2	3.6	4.6	V
Output current	–	0.2	–	400	mA
Nominal output voltage, Vo	Default = 3.3 V	–	3.3	–	V
Dropout voltage	At max. load	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation	–5	–	5	%
LDO current	No load	–	57	–	µA
	Maximum load (400 mA)	–	4	–	mA
Line regulation	V_{in} from 3.5 V to 5.5V, max. load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 400 mA, VBAT= 3.7 V	–	–	0.3	mV/ mA
PSRR	$V_{in} \geq V_o$ + 0.2 V, V_o = 3.3 V, C_o = 2.2 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Reference ready. Vo from 0 to 3.3V C_o = 2.2 µF	–	54	120	µs
In-rush current	C_o = 2.2 µF, no load.	–	200	400	mA
Output over-current limit	–	–	840	1200	mA
External output capacitor, Co	Ceramic, X5R, 0201 inch, 2.2 µF ± 20%, 6.3V. Effective cap at 3.3 V include load-side caps.	0.46	2.2	4.7	µF
External input capacitor	For LDO_VDDBAT5V pin, ceramic, X5R, 0402 inch, ESR < 10 mΩ at 4 MHz, 4.7 µF ± 20%, Min value is effective cap at 5.5 V. 10 V.	0.67	4.7	–	µF

3.3 3.3V RF LDO (RFLDO3P3)

Table 6. RFLDO3P3 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. = Vo + 0.2 V = 3.5 V dropout voltage requirement must be met under maximum load for performance specifications	3.2	3.6	4.6	V
Output current	–	0.1	–	100	mA
Output voltage range, Vo	Default = 3.3 V	–	3.3	–	V
Dropout voltage	At max. load	–	–	200	mV
Output voltage DC accuracy	Includes line/load regulation	–5	–	5	%
Quiescent current	No load	–	10	–	µA
	Maximum load at 100 mA	–	1.5	–	mA
Line regulation	Vin from 3.5V to 5.5V, max. load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 100 mA, V_{in} = 3.7V	–	–	0.3	mV/mA
PSRR	$V_{in} \geq V_o$ + 0.2 V, V_o = 3.3 V, C_o = 1 µF, Max. load, 100 Hz to 100 kHz	20	–	–	dB
LDO turn-on time	Reference ready. Vo from 0 to 3.3 V C_o = 1 µF	–	33	40	µs
In-rush current	C_o = 1 µF, no load.	90	120	150	mA
Output over-current limit	–	150	225	–	mA
External output capacitor, C_o	Ceramic, X5R, 0201 inch, 1 µF ± 20%, 6.3V. Effective cap at 3.3V include load-side caps.	0.25	1	–	µF
External input capacitor	For LDO VDDBAT5V pin, ceramic, X5R, 0402 inch, ESR < 10 mΩ at 4 MHz, 1 µF ± 20%, 6.3V. Min value is effective cap at 5.5 V	0.25	1	–	µF

3.4 CLDO

Table 7. CLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	Min. = 1.095 + 0.12 V = 1.215 V dropout voltage requirement must be met under maximum load.	1.1956	1.22	4.6	V
Output current	–	0.1	–	100	mA
Output voltage, V_o	Programmable in 15 mV steps. Default = 1.095.V	0.795	1	1.2	V
Dropout voltage	At max. load	–	–	120	mV
Output voltage DC accuracy	Includes line/load regulation				
	Before trimming	–3	–	3	%
Quiescent current	No load	–	10	–	µA
	100 mA load	–	3.64	–	mA
Line regulation	V_{in} from 1.095 V to 1.3 V, maximum load	–	–	1	mV/V
Load regulation	Load from 1 mA to 100 mA, V_{in} = 1.22V	–	–	4.5	mV/mA
Leakage current	Power down, V_{in} = 0.9V, typical at T_j = 25°C	–	0.73	–	µA
	Bypass mode, V_{in} = 0.9V, typical at T_j = 25°C	–	0.15	–	µA
PSRR	100 Hz to 100 kHz, V_{in} ≥ 1.22 V, C_o = 1 µF	13.9	–	–	dB
LDO turn-on time	Reference ready, V_o from 0 to 1.2 V, Co = 1 µF	–	21	42	µs
In-rush current	C_o = 1 µF, no load	–	47	71	mA
External output capacitor, C_o	Ceramic, X5R, 0201 inch, 1 µF ± 20%, 6.3 V. Effective cap at 1.095 V include load-side caps	0.5	1	–	µF
External input capacitor	Only use an external input capacitor at the VDD LDO pin if it is not supplied from CBUCK output.	–	2.2	–	µF

3.5 MEMLPLDO

Table 8. MEMLPLDO Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	–	1.62	1.8	1.98	V
Output current	–	0.001	–	60	mA
Output voltage, V_o	Default = 0.9 V	0.72	0.9	1.02	V
Output voltage DC accuracy	Includes line/load regulation	–5	–	5	%
Quiescent current	No load	–	0.9	–	µA
	Max. load	–	0.32	–	µA
Line regulation	V_{in} from 1.62V to 1.98V, 60 mA load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 6 mA, V_{in} = 1.8 V	–	–	0.07	mV/mA
Leakage current	Power-down, typical at T_j = 25°C, max. at T_j = 85°C	–	3	790	nA
PSRR	100 Hz to 100 kHz, Input = 1.8V, C_o= 1 µF,	20	–	–	dB
LDO turn-on time	Reference ready, V_o from 0 to 0.9 V, C_o = 1 µF	–	–	128	µs
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1 µ F ± 20%, 6.3 V. Effective cap at 0.9 V include load-side caps	0.5	1	1.2	µF
External input capacitor	Ceramic, X5R, 0201 inch, 1 µ F ± 20%, 6.3 V.	–	1	–	µF

3.6 HVLDO1P8

Table 9. HVLDO1P8 Specifications

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage, Vin	–	3.2	3.6	4.6	V
Output current	–	0.001	–	60	mA
Output voltage, V_o	Default = 1.8 V	–	1.8	–	V
Output voltage DC accuracy	Includes line/load regulation	–	–	5	%
Quiescent current	No load	–	1.1	–	µA
	60 mA load	–	0.28	–	mA
Line regulation	VIN from 2.7 to 5.5 V, 60 mA load	–	–	3.5	mV/V
Load regulation	Load from 1 mA to 60 mA. V_{in} = 3.7 V	–	–	0.13	mV/mA
Leakage current	Power-down, typical at T_j = 25°C, max. at T_j = 85°C	–	5	900	nA
PSRR	@ 1 kHz, input > 1.35 V, C_o= 2.2 µF, V_o = 1.2V	20	–	–	dB
LDO turn-on time	Reference ready, V_o from 0 to 1.8V, C_o = 1 µF	–	101	155	µs
External output capacitor, Co	Ceramic, X5R, 0201 inch, 1 µF ± 20%, 6.3V. Effective cap at 1.8V include load-side caps	0.5	1	1.2	µF
External Input Capacitor	For LDO VDDBAT5V pin, ceramic, X5R, 0402 inch, ESR < 10 mΩ at 4 MHz, 1 µF ± 20%, 6.3V. Min value is effective cap at 5.5V.	0.25	1	–	µF

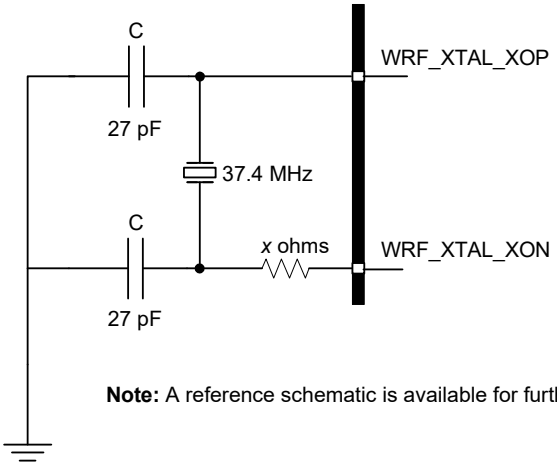
4. External Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

4.1 Crystal Interface and Clock Generation

The CYW43012 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 11. Consult the reference schematics for the latest configuration.

Figure 11. Recommended Oscillator Configuration



A fractional-N synthesizer in the CYW43012 generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references.

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal interface are listed in Table 10 on page 23.

4.2 External Frequency Reference

As an alternative to a crystal, an external precision frequency reference can be used, provided that it meets the Phase Noise requirements listed in Table 10.

If used, the external clock should be connected to the XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in Figure 12. The internal clock buffer connected to this pin will be turned OFF when the CYW43012 goes into sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation.

Figure 12. Recommended Circuit to Use With an External Reference Clock

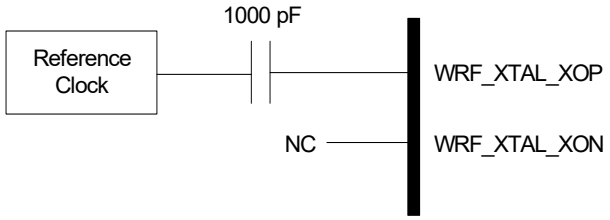


Table 10. Crystal Oscillator and External Clock —Requirements and Performance

Parameter	Condition notes	Crystal[a]			External Frequency Reference [b, c]			
		Min	Typ	Max.	Min.	Typ.	Max.	Units
Frequency	2.4G and 5G bands	–	37.4	–	–	37.4	–	MHz
Frequency tolerance Without trimming over the lifetime of the equipment, including Temperature[d]	Without trimming	–20	–	20	–20	–	20	ppm
ESR	–	–	–	60	–	–	–	Ω
Drive level	External crystal must be able to tolerate this drive level.	200	–	–	–	–	–	µW
Input impedance (XTAL_XOP)	Resistive	–	–	–	30k	100k	–	Ω
	Capacitive	–	–	7.5	–	–	7.5	pF
XTAL_XOP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	0.9	–	1.1	V
XTAL_XOP input voltage (see Figure 12 on page 22)	IEEE 802.11a/b/g operation only	–	–	–	400	–	1100	mVp-p
XTAL_XOP input voltage (see Figure 12 on page 22)	IEEE 802.11a/b/g operation only	–	–	–	1	–	–	Vp-p
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise[e] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise[e] (IEEE 802.11n,5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz

a. (Crystal) Use XTAL_XON and XTAL_XOP. Refer to CYW43012 reference design for Crystal selection.

b. See “External Frequency Reference on page 22” for alternative connection methods.

c. For a clock reference other than 37.4 MHz, 20 × log10(f/ 37.4) dB should be added to the limits, where f = the reference clock frequency in MHz.

d.It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

e. Assumes that external clock has a flat phase no se response above 100 kHz.

4.3 External 32.768 kHz Low-Power Oscillator

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 11.

Table 11. External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	500–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance [a]	>100k	Ω

a. When power is applied or switched OFF.

Note: The FCBGA and WLCSP packages allow an external 32.768kHz crystal or an external 32.768kHz clock (from an external oscillator) to be connected to the CYW43012. The WLBGA package only allows a 32.768kHz clock form an external oscillator to be connected to the CYW43012.

5. Bluetooth Subsystem Overview

The CYW43012 is a Bluetooth 5.0-compliant baseband processor with a 2.4 GHz transceiver. The CYW43012 incorporates Bluetooth 5.0's 2 Mbps LE data rates and all Bluetooth 4.2's optional new features i.e. LE Data Packet Length Extension, LE Secure Connections, and Link Layer Privacy.

The Bluetooth subsystem presents a standard host controller interface (HCI) via a high-speed UART and PCM for audio.

The CYW43012 transceiver's enhanced radio performance meets the most stringent requirements for compact integration into portable devices. The transmitter features multiple TX paths for optimized power consumption for different TX power levels. The CYW43012 provides full radio compatibility to operate simultaneously with WLAN, GPS and cellular radios.

The Bluetooth subsystem includes a high speed UART for BT HCI communications with the host. The Bluetooth subsystem also includes a stack for hostless operation. The Bluetooth subsystem also includes PCM and I2S interfaces for audio. Communications with additional external devices are provided by two SPI interfaces, an additional high speed UART, as well as an I^2C interface.

5.1 Features

Primary CYW43012 Bluetooth features include:

- Supports key features of upcoming Bluetooth standards
- Supports Bluetooth 5.0 with 2 Mbps BLE (GFSK) data rates

Fully supports Bluetooth Core Specification version 4.2 + EDR features:

- Adaptive frequency hopping (AFH)
- Extended synchronous connections (SCO)—voice connections
- Fast connect (interlaced page and inquiry scans)
- Secure simple pairing (SSP)
- Encryption pause resume (EPR)
- Extended inquiry response (EIR)
- Link supervision timeout (LST)

- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.1 packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Ultra-low TX o/p power mode to enable use cases like proximity pairing while reducing current consumption
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management on page 29)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep sleep modes and software regulator shutdown
- Supports a low-power crystal, which can be used during power save mode for better timing accuracy.

5.2 Bluetooth Radio

The CYW43012 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth Radio Specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmit

The CYW43012 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section also supports the Bluetooth Low Energy specification (1/2 Mbps GFSK). The transmitter PA bias can be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π/4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables the CYW43012 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate he desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low- IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYW43012 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYW43012 uses an internal RF and IF loop filter.

Calibration

The CYW43012 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

6. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

6.1 Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode Bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

6.2 Bluetooth 4.1 Features

The BBC supports all Bluetooth 4.1 features, with the following benefits:

- Dual-mode classic Bluetooth and classic low energy (BT and BLE) operation
- Low-energy physical layer
- Low-energy link layer
- Enhancements to HCI for low energy
- Low-energy direct test mode
- 128 AES-CCM secure connection for both BT and BLE

Note: The CYW43012 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

6.3 Bluetooth 4.2 Features

The CYW43012 supports the following Bluetooth 4.2 features:

- LE data packet length extension
- LE secure connections
- Link layer privacy

6.4 Bluetooth 5.0 Features

CYW43012 supports 2 Mbps LE data rates using GFSK modulation. This enables higher throughout when using Bluetooth Low Energy operating mode.

6.5 Bluetooth Low Energy

The CYW43012 supports the Bluetooth Low Energy operating mode.

6.6 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software and other controllers that are activated or configured by the command controller to perform the link control tasks. Each task performs a different state in the Bluetooth Link Controller.

- BR states:
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
- BLE states:
  - Advertising
  - Scanning
  - Connection

6.7 Test Mode Support

The CYW43012 fully supports Bluetooth Test mode as described in Part I:1 of the *Specification of the Bluetooth System Version 3.0*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW43012 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

6.8 Bluetooth Power Management Unit

The Bluetooth power management unit (PMU) provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core.

The power management functions provided by the CYW43012 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management
- Burst Buffer Operation

6.8.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

6.8.2 Host Controller Power Management

When running in UART mode, the CYW43012 may be configured so that dedicated signals are used for power management hand-shaking between the CYW43012 and the host. The basic power saving functions supported by those hand-shaking signals include the standard Bluetooth defined power savings modes and standby modes of operation. Table 12 describes the power-control handshake signals used with the UART interface.

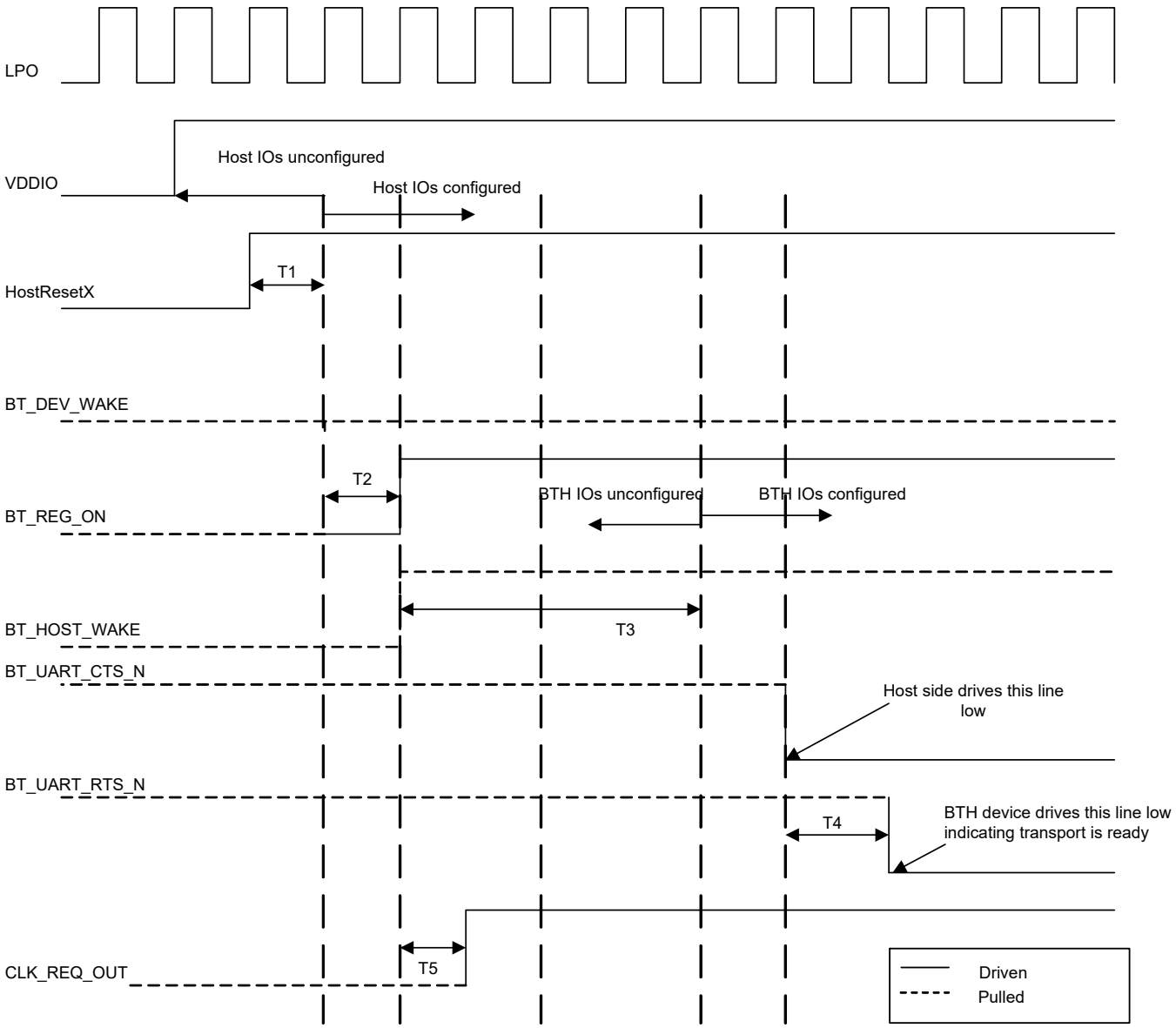
Note: Pad function Control Register is set to 0 for these pins. See Bluetooth RF Specifications on page 59 for more details.

Table 12. Power Control Pin Description

Signal	Mapped to Pin	Type	Description
BT_DEV_WAKE	P5	I	Bluetooth device wake-up: Signal from the host to the CYW43012 indicating that the host requires attention. ■ Asserted: The Bluetooth device must wake-up or remain awake. ■ Deasserted: The Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.
BT_HOST_WAKE	BT_GPIO_1	O	Host wake-up. Signal from the CYW43012 to the host indicating that the CYW43012 requires attention. ■ Asserted: host device must wake-up or remain awake. ■ Deasserted: host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.
CLK_REQ	CLK_REQ	O	The CYW43012 asserts CLK_REQ when Bluetooth or WLAN wants the host to turn on the reference clock (37.4MHz clock). The CLK_REQ polarity is active-high. Add an external 100 kΩ pull-down resistor to ensure the signal is deasserted when the CYW43012 powers up or resets when VDDIO is present. Note this pin is used for designs that use an external an reference clock source from the host. This pin is irrelevant for Crystal reference clock based designs where the CYW43012 device generates reference clock from external crystal, connected to the Oscillator circuit.

Figure 13 shows the startup signaling sequence prior to software download.

Figure 13. Startup Signaling Sequence Prior to Software Download



Notes :
T1 is the time for Host to settle its IOs after a reset.
T2 is the time for Host to drive BT_REG_ON high after the Host IOs are configured.
T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.
T4 is the time for BTH device to drive BT_UART_RTS_N low after the Host drives BT_UART_CTS_N low. This assumes the BTH device has already completed initialization.
T5 is the time for BTH device to drive CLK_REQ_OUT high after BT_REG_ON goes high. Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where CYW43012 device generates it's own reference clock from an external crystal connected to its oscillator circuit.
Timing diagram assumes VBAT is present.

6.8.3 BBC Power Management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF ON and OFF dynamically within transmit/receive packets.
- During periods of inactivity, the CYW43012 can run on the low-power oscillator and wake up for scheduled activity (such as connection, advertisement, and so forth) or because of external stimulus (such as host communication).
- A low-power shutdown feature allows the device to be turned OFF while the host and any other devices in the system remain operational. When the CYW43012 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows the CYW43012 to effectively be OFF while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/ O.

  During the low-power shutdown state, provided VDDIO remains applied to the CYW43012, all outputs are tristated, and most input signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables the CYW43012 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes.

  Two CYW43012 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (WRF_TCXO_IN) and the 32.768 kHz input (LPO). When the CYW43012 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

6.9 Adaptive Frequency Hopping

The CYW43012 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

6.10 Advanced Bluetooth/WLAN Coexistence

The CYW43012 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form-factor platforms, supporting applications such as VoWLAN + SCO and Video-over-WLAN + High Fidelity BT Stereo.

Support is provided for platforms that share a single antenna between Bluetooth and WLAN. Dual-antenna applications are also supported. The CYW43012 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm).

The CYW43012 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The CYW43012 also supports Transmit Power Control on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth AFH classification is also enhanced by the WLAN core’s channel information.

7. Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on the Arm® Cortex-M4 32-bit RISC processor.

Note: The M4 is capable of running at up to 96 MHz CPU clock. However currently Cypress tests and enables up to 48 MHz clock in its SDK.

7.1 RAM, ROM, Patch Memory and BT Stack

The ARM core is paired with a memory unit that contains 1152 KB of ROM memory for program storage and boot ROM, and 388 KB of RAM for data scratchpad and patch RAM code.

The internal ROM includes the full BT stack leaving a maximum of RAM for applications and patches. In standalone mode, the CYW43012 automatically loads the application (and necessary patches) from external serial flash or via the HCI UART interface into RAM. The application executes from RAM and utilizes the ROM-based stack for BT functions. For host applications the ROM based-stack is disabled above the HCI layer. Note that Cypress currently recommends and supports CYW43012 with an embedded stack via its SDK. Patches can be downloaded by the host via the UART interface or be provided by the external serial flash. At power-up, the lower layer protocol stack is executed from the internal ROM memory.

In typical cases ~70KB of the RAM is expected to be available for the customer's application code. The exact amount of RAM available for application logic is dependent on the Bluetooth features used that in turn affect patches to stack and controller code as well as the static and dynamic data memory needed.

7.2 Reset

The CYW43012 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The BT power-on reset (POR) circuit is out of reset after BT _REG ON goes High. If BT_REG_ON is low, then the POR circuit is held in reset.

8. Bluetooth Peripheral Transport Unit

8.1 PCM Interface

Note:

1. The CYW43012 PCM interface is not exposed to the customer's application code in Cypress's SDK. The PCM interface is used internally by Cypress's Bluetooth stack firmware for a SCO/eCO full duplex channel that can carry narrow or wideband speech data.
2. The PCM interface is available on its own dedicated pads in the CYW43012. The PCM interfaces is also multiplexed to the I2S pads. The Cypress SDK uses the PCM interface on the I2S pads.

CYW43012 can connect to linear PCM Codec devices in master or slave mode. In master mode, the CYW43012 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYW43012.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands. Note that Cypress's SDK only supports the PCM interface in I2S mode. In this mode the frame synchronization signal i.e. PCM_SYNC is used as the Word Select or the LR clock. CYW43012 use cases are expected to require both Advanced Audio Distribution (A2DP) sink that uses I2S master to send audio stream to an external codec and Hands Free Profile (HFP) that uses PCM master/slave for full duplex mono data exchange with an external codec. Using PCM in I2S mode simplifies the codec selection and circuitry externally.

8.1.1 Channels Supported

While it is possible to support multiple full-duplex SCO or eSCO connections through the PCM interface Cypress's SDK only supports one full-duplex SCO/eSCO channel over the PCM interface today.

8.1.2 Data formatting

Cypress's SDK uses the PCM interface in the I2S mode. The PCM_SYNC i.e. the frame synchronization signal acts as the word select or the LR clock in this case. Out of the 32 bit frame used only the L channel contains the valid 16 bits of information. The remaining 16 bits for the R channel are not valid. In the narrowband speech mode CYW43012 uses 16 bit samples with an 8kHz sample rate. In the wideband speech mode 16 bits data at 16kHz sample rate are encoded with SBC for transmission.

8.2 HCI UART Interface

The BT HCI UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 115200 bps to 3.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may be changed using a vendor-specific UART HCI command.

The UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI H4 specification. The default baud rate is 115.2 Kbaud.

The CYW43012 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW43012 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 13. Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16

Figure 14. UART Timing

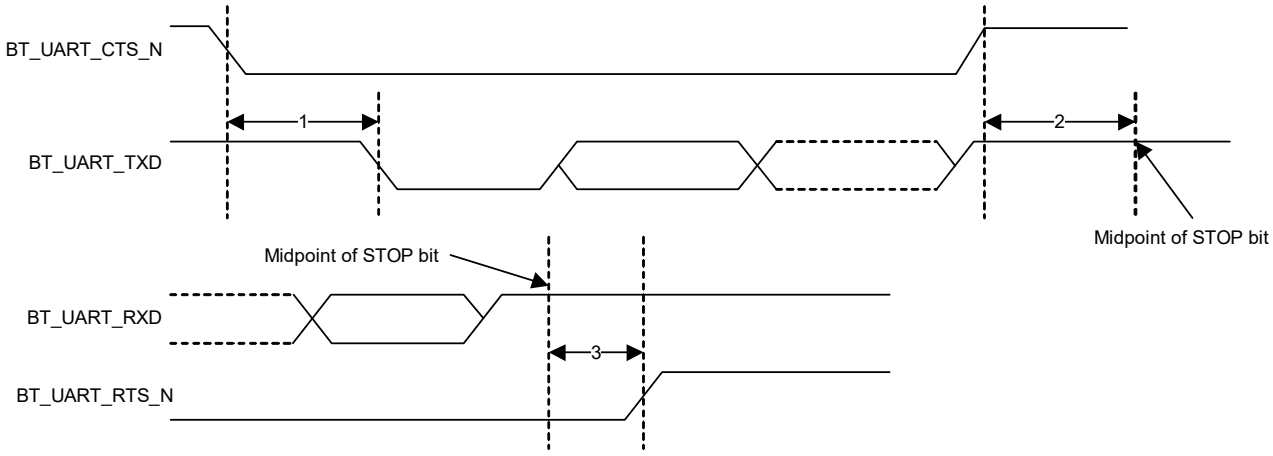


Table 14. UART Timing Specifications

	Reference Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

8.3 I²S Interface

The CYW43012 supports an I2S digital audio port for Bluetooth audio.

Note: The CYW43012 I²S interface is not exposed to the customer's application code in Cypress's SDK. The I²S interface is used internally by Cypress's Bluetooth stack firmware for a Advanced Audio Distribution Profile (A2DP) sink use case.

The CYW43012 supports an I²S digital aud**io** port for Bluetooth audio. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW43012 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:
48 kHz x 32 bits per frame = 1.536 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

8.3.1 I^2S Timing

Note: Timing values specified in Table 21 are relative to high and low threshold levels.

Table 15. Timing for I^2S Transmitters and Receivers

	Transmitter				Receiver				
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Notes
Clock Period T	T_{tr}	–	–	–	Tr	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–	–	–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

a. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.

b. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.

c. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.

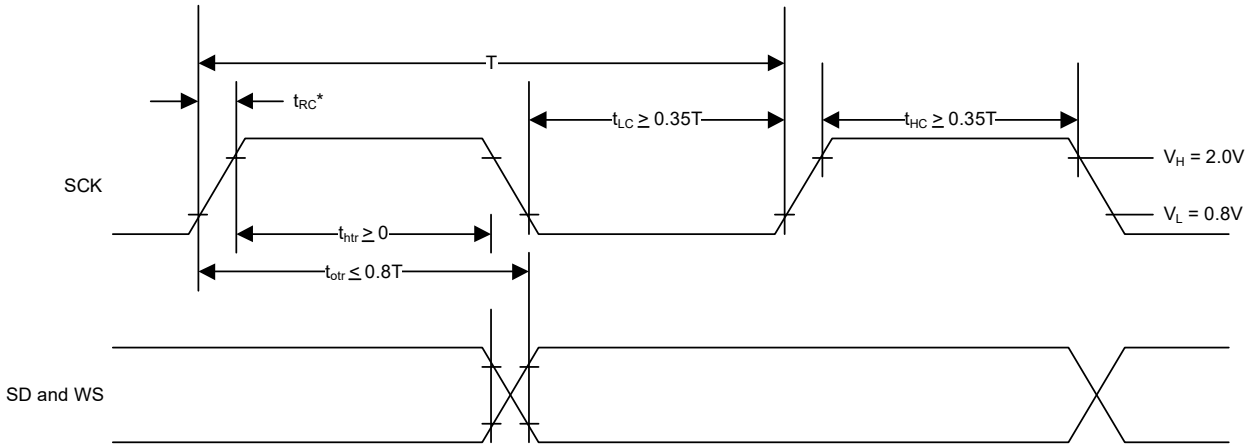
d. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

e. The data setup and hold time must not be less than the specified receiver setup and hold time.

f. The data setup and hold time must not be less than the specified receiver setup and hold time.

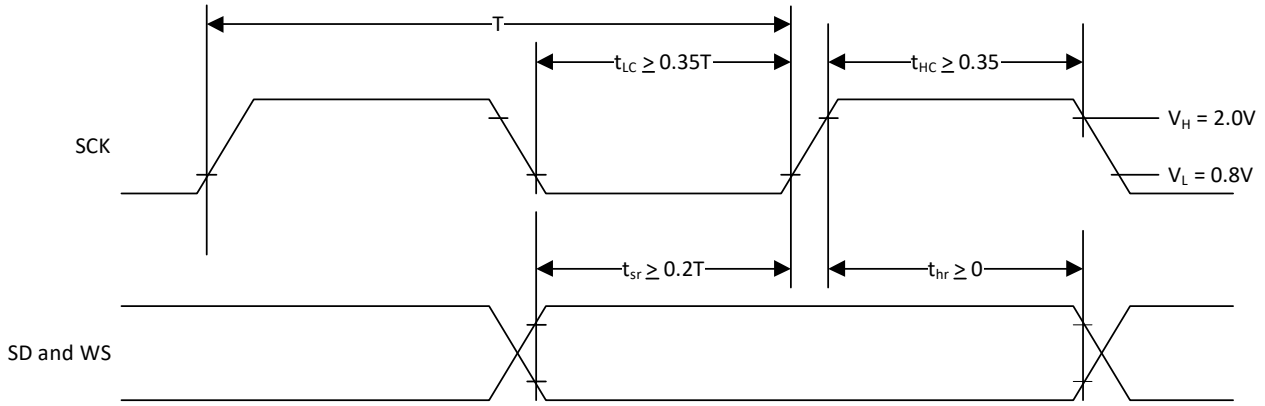
Note: The time periods specified in Figure 15 and Figure 16 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 15. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
T = T_{tr}
* t_{RC} is only relevant for transmitters in slave mode.

Figure 16. I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
T > T_r

8.4 Serial Peripheral Interface

The CYW43012 has two independent SPI interfaces. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW43012 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW43012 acts as a SPI master device that supports 1.8V or 3.3V SPI slaves.

SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported. One of these independent SPI interfaces supports Quad mode and is allocated as a shared Quad SPI Master between both

the WLAN and BT subsystem for accessing shared FLASH. The other independent SPI interface supports single/dual modes and is allocated as a Single SPI Master (multiplexed with

BT_UART. Currently the 43012 firmware supports only UART as a BT host interface. The Quad SPI capable SPI block supports a maximum clock of 28 MHz while the other SPI block supports a maximum clock of 24 MHz.

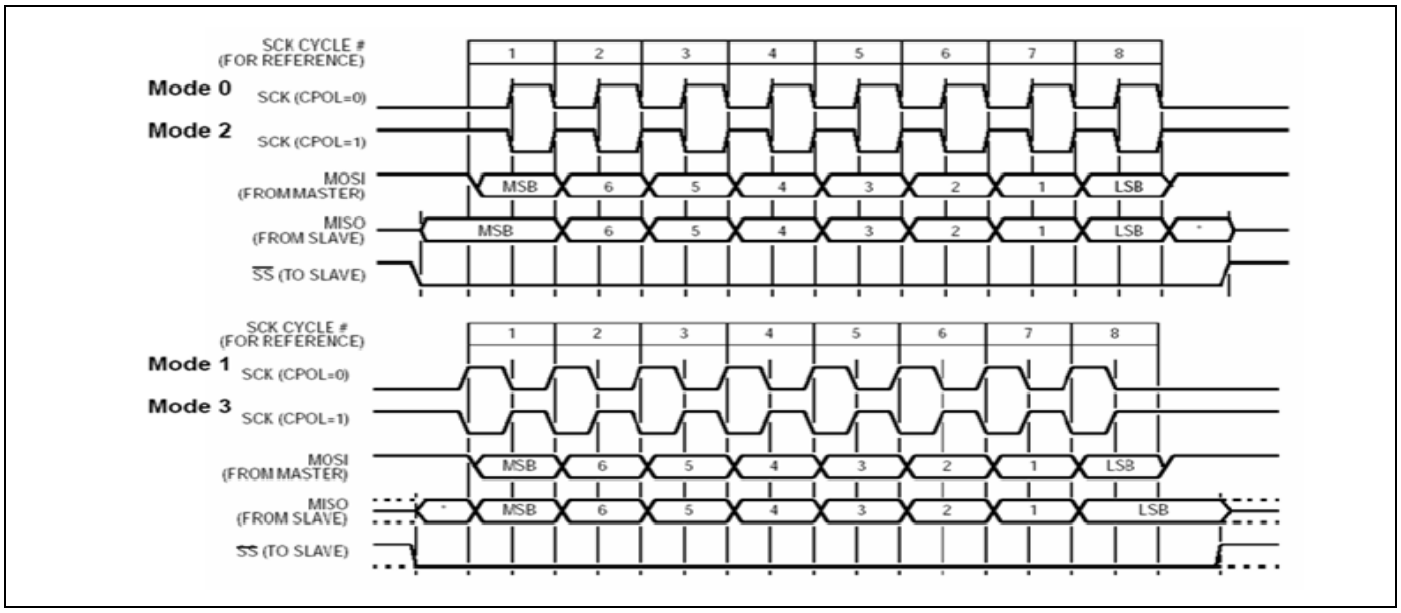
Note:

1. Both SPI interfaces support only master modes
2. The Bluetooth stack requires non volatile storage for various keys and pairing related information. This information can be stored in the QSPI based external flash or passed to the external processor via HCI UART.

Table 16. SPI Transfer Modes Supported

SPI mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 17. SPI Transfer Modes



8.5 PDM Microphone

Note: The PDM interface is yet to be enabled with the appropriate drivers in Cypress's SDK.

The CYW43012 accepts one-bit pulse density modulation (PDM) input signal The PDM signal is derives from an external microphone that can generate digital signals. The external digital microphone accepts a 2.4 MHz clock generated by the CYW43012 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock (selectable through a programmable control bit). The digital signal passes through the chip IO and is filtered inside the chip. CYW43012 includes CIC and FIR filters to enable 8kHz or 16kHz sampling rates. The CYW43012 also includes IIR filtering for High Pass Filtering and equalization to enhance voice quality. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible. The 2 PDM input channels and the 2.4 MHz clock output are available on any of the LHL pads mentioned in Table 56.

8.6 CSC Interface

The CYW43012 provides a 2-pin Cypress Serial Control (CSC) master to communicate with peripherals.

The CSC interface is compatible with I2C slave devices. CSC does not support multi-master capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by CSC:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I2C-compatible devices is not guaranteed.)

The following transfer types are supported by CSC:

- Read (Up to 8 bytes can be read.)
- Write (Up to 8 bytes can be written.)
- Read-then-Write (Up to 8 bytes can be read and up to 8 bytes can be written.)
- Write-then-Read (Up to 8 bytes can be written and up to 8 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW43012 are required on both the SCL and SDA pins for proper operation.

8.7 Peripheral UART Interface

The CYW43012 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW43012 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO.

Table 17. Common Baud Rates

Desired Rate	Actual Rate	Error (%)
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16

8.8 PWM

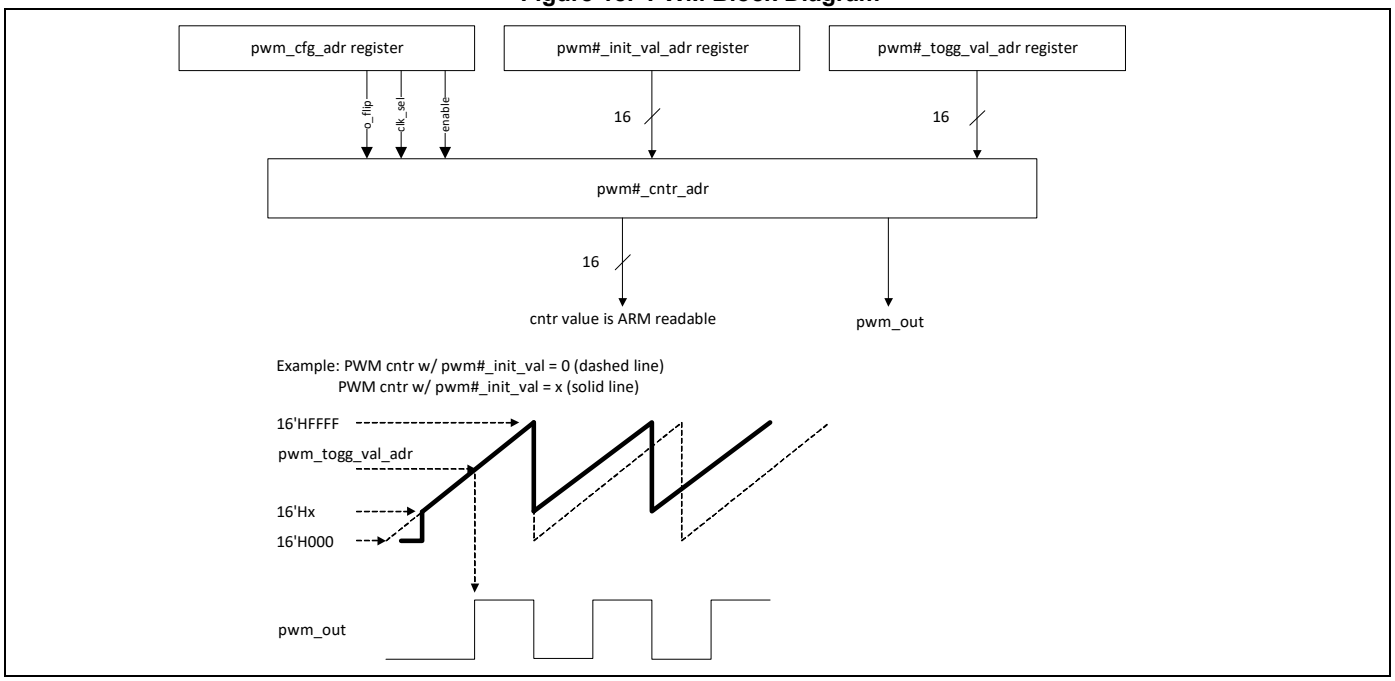
The CYW43012 has six internal PWMs. The PWM module consists of the following:

- PWM0–5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

PWM0-5 can be multiplexed on any LHL pad (P0 to P19 except on P5, P6 and P7)

Figure 18 shows the structure of one PWM.

Figure 18. PWM Block Diagram



8.9 ADC

The ADC is a single switched-cap Σ-Δ ADC for DC measurement. It operates at the 12 MHz clock rate and has 14 DC input channels, across the P0, P1,P8-P19 GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different

calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode. The ADC consumes ~2mA of current in typical operating conditions.

Table 18. ADC Specifications

Parameter	Symbol	Conditions/ Comments	Min.	Typ.	Max.	Unit
Analog Supply Voltage	VDD18	–	1.71	1.8	1.89	V
Current Consumption	ITOT	–	–	2	–	mA
Power Down Current	–	–	–	–	1	uA
DC Input Voltage	–	–	–	–	1.8	V
DC Input Source Impedance[a]	–	Resistance	–	–	1	kΩ
		Capacitance	–	–	10	pF
RF Rejection	–	Reject RF coupling at 2.4GHz	–20	–24	–	dB
ADC Reference Voltage	VREF	From BG with +/- 3% accuracy	–	1.22	–	V
ADC Sampling Clock	–	–	–	18.7	–	MHz
Absolute Error	–	Include gain error, offset and distortion without Calibration	–	–	5	%
	–	Include gain error, offset and distortion after Calibration	–	–	2	%
ENOB	–	–	10	–	–	Bit
ADC Input Full Scale	–	–	–	–	1.8	Vpp
Conversion Rate	–	–	–	374	–	KHz
Input Impedance	Rin	–	500	–	–	kΩ
Startup time	–	–	–	20	–	µs

a. Conditional requirement for the measurement time of 10us. Relaxed with longer measurement time for each GPIO input channels.

Note:

1. Firmware in WICED SDK reads ADC registers and averages the values before providing the same to the application. This puts a limit on the effective conversion rate seen by the application. Since the ADC is currently intended for battery monitoring and other static voltage measurements this approach meets use case requirements. DMA functionality for the ADC is not currently available.
2. Cypress draws the customer's attention to the low input impedance of the ADC (1kΩ). Customers must account for this when designing resistive voltage divider circuits for the ADC.

9. WLAN Global Functions

Note: The WLAN CPU is intended for Cypress's firmware and is not available for customer to run code on. Peripherals like UART and JTAG/SWD mentioned in this section are only available to enable the debugging/development of Cypress's firmware on the WLAN CPU. The host processor can interact with the WLAN section using the SDIO interface along with the relevant GPIOs (for interrupt, wake etc.). External coexistence interfaces when required for external radios require support from Cypress's firmware teams to enable.

9.1 WLAN CPU and Memory Subsystem

The CYW43012 WLAN section includes an integrated ARM Cortex-M3 32-bit processor with 640 KB SRAM and 1280 KB ROM.

9.2 One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 6144-bit (768 bytes) One-Time Programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Cypress WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

9.3 GPIO Interface

The following number of general-purpose I/O (GPIO) pins are available on the WLAN section of the CYW43012 that can be used to connect to various external devices:

■ WLCSP package – 16 GPIOs

Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions.

9.4 External Coexistence Interface

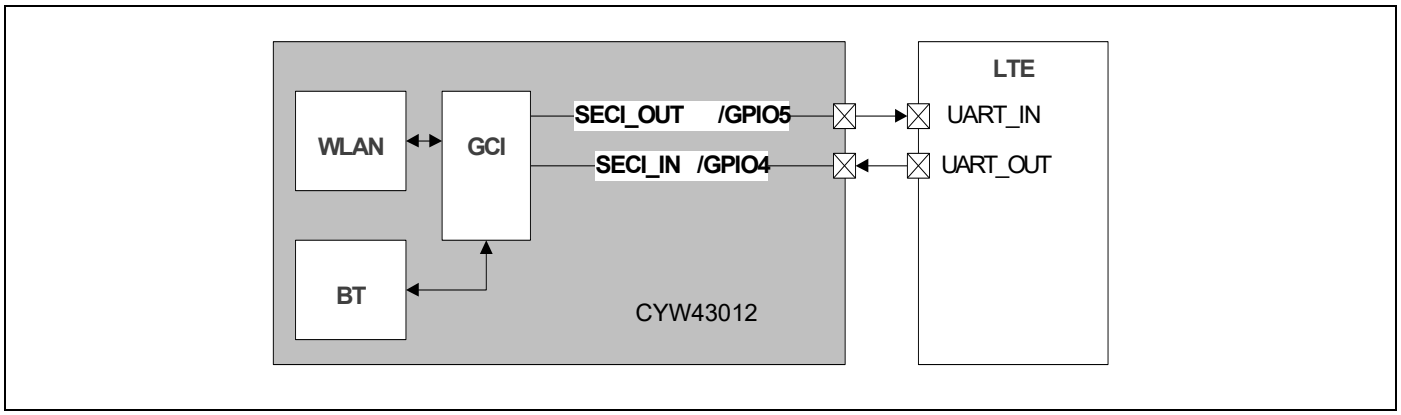
Note: Customers can control these GPIOs using their code that is running on the ARM Cortex-M4 on the Bluetooth side.

External handshake interface is available to enable signaling between the device and an external co-located wireless device, such as Zigbee or LTE to manage wireless medium sharing for optimum performance.

9.4.1 LTE Coexistence Interface

Figure 19 shows the WCI-2 LTE coexistence interface. See Table 14. “UART Timing Specifications,” on page 35 for UART baud rate.

Figure 19. Cypress GCI or BT-SIG WCI-2 Coexistence Interface for Cypress BT/ZigBee radios or LTE radios



9.4.2 3- Wire (Zigbee) Coexistence Interface

Figure 20, Figure 21 and Table 19 define external 3-wire interface.

Figure 20. 3-Wire Coexistence Interface for 3rd party BT/ZigBee radios

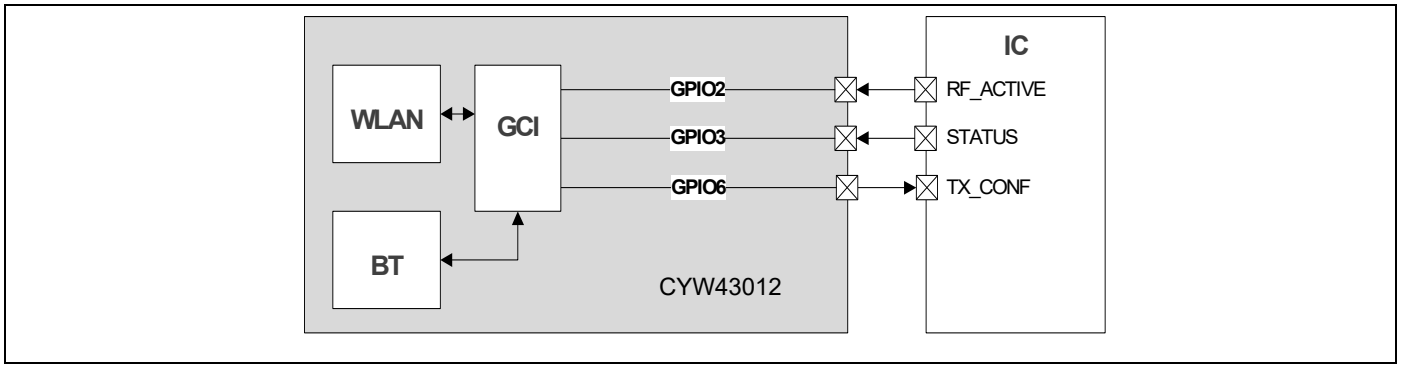
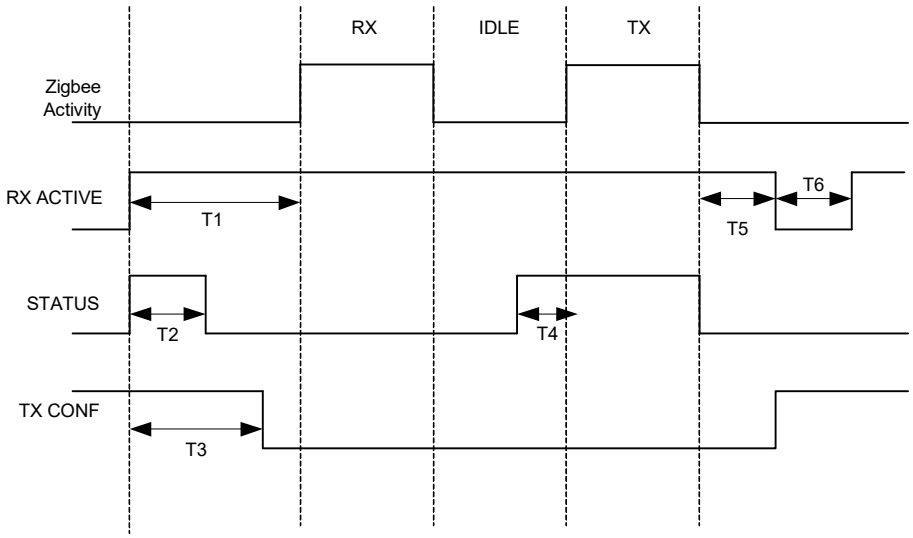


Table 19. 3-Wire External Coexistence Interface

GPIO Name	Coexistence Signal	Type	Comment
GPIO_2	RF_ACTIVE	Input	Request indication from external device for access
GPIO_3	STATUS	Input	Indicates priority (within T2) and TX/RX (after T2)
GPIO_6	TX_CONF	Output	Grant of access indication to external device

Figure 21. 3-Wire External Coexistence Interface Timing Diagram



Notes on Timing Diagram

- T1: Advance assertion time of RF Active from actual TX or RX
  - Minimum 100 us
- T2: Priority indication on Status Line
  - Expected to start at the same time as RF Active
  - Minimum 30 us
  - Maximum 50 us
  - 1 – High Priority, 0 – Low Priority
- After 50 us, the Status line is used to indicate TX/RX
  - 1 – TX, 0 – RX
- T3 – TX CONF assertion delay from RF ACTIVE
  - Maximum 90 us
- T4 – Advance assertion time of TX/RX indication on status line for subsequent frames without RF ACTIVE toggling
  - Minimum 30 us
- T5 – RF ACTIVE de-assertion delay after end of frame exchange
  - Expected to be as low as possible (~0 us) to improve overall efficiency
- T6 – RF ACTIVE de-assertion
  - Minimum 16 us

3-wire Coexistence interface protocol details:

- External device asserts RF ACTIVE (in advance) when it wants access to the wireless medium
  - 1 – Access Requested
  - 0 – Access not requested
- It indicates priority of the access requested in a specified window (50 us counted from assertion of RF ACTIVE) on STATUS line
  - 1 – High Priority
  - 0 – Low Priority
- After indicating priority on STATUS line it indicates TX/RX indication on the same STATUS line (after 50 us window)
  - 1 – TX
  - 0 – RX
- Arbitrating device (WiFi) will decide based on the relative priority of the different requests (WiFi internal and external) and either grant or reject the request. This is indicated using the TX CONF signal
  - 1 – Access Denied
  - 0 – Access Granted

9.5 UART Interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Provided primarily for debugging during development, this UART enables the CYW43012 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

9.6 SDIO v3.0

All three package options of the CYW43012 WLAN section provide support for SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (1.8V signaling).
- HS: High speed up to 50 MHz (1.8V signaling).
- SDR12: SDR up to 25 MHz (1.8V signaling).
- SDR25: SDR up to 50 MHz (1.8V signaling).
- SDR50: SDR up to 80 MHz (1.8V signaling).
- DDR50: DDR up to 40 MHz (1.8V signaling).

Note:
1. At this point the Cypress FMAC driver as well as the Cypress WICED SDK do not support SDR50 and DDR50 rates for CYW43012. Module partners that use the CYW43012 in their module offerings may therefore restrict the SDIO interface to supported rates via OTP. In this scenario CYW43012 will support the following modes:

- **DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (1.8V signaling).**
- **HS: High speed up to 50 MHz (1.8V signaling).**
- **SDR12: SDR up to 25 MHz (1.8V signaling).**
- **SDR25: SDR up to 50 MHz (1.8V signaling).**

The UHS-1 rates, SDR50 & DDR50, that are part of the SDIO 3.0 specification are not supported by these modules and the current. Cypress driver/SDK.

2. The CYW43012 is backward compatible with SDIO v2.0 host interfaces. Note however that the CYW43012 device can only support 1.8V signaling. It cannot support 3.3V signaling during initialization post power cycle and in default/high speed SDIO 2.0 modes. The host must use 1.8V signalling to work with CYW43012.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

The following three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max BlockSize/ByteCount = 512B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B).

9.6.1 SDIO Pins

Table 20. SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

Figure 22. Signal Connections to SDIO Host (SD 4-Bit Mode)

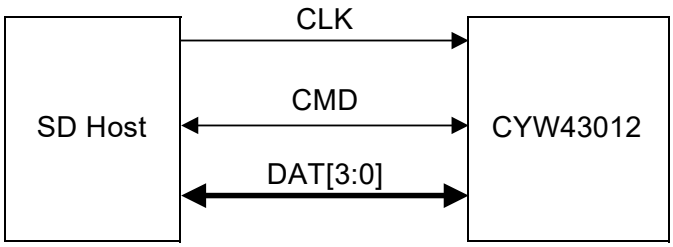
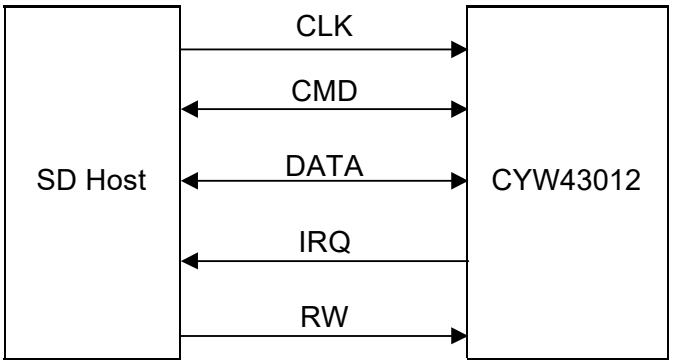


Figure 23. Signal Connections to SDIO Host (SD 1-Bit Mode)



Note: As per Section 6 of the SDIO specification, pull-ups in the 10 kOhm to 100 kOhm range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

9.7 SDIO Timing

9.7.1 SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 24 and Table 21.

Figure 24. SDIO Bus Timing (Default Mode)

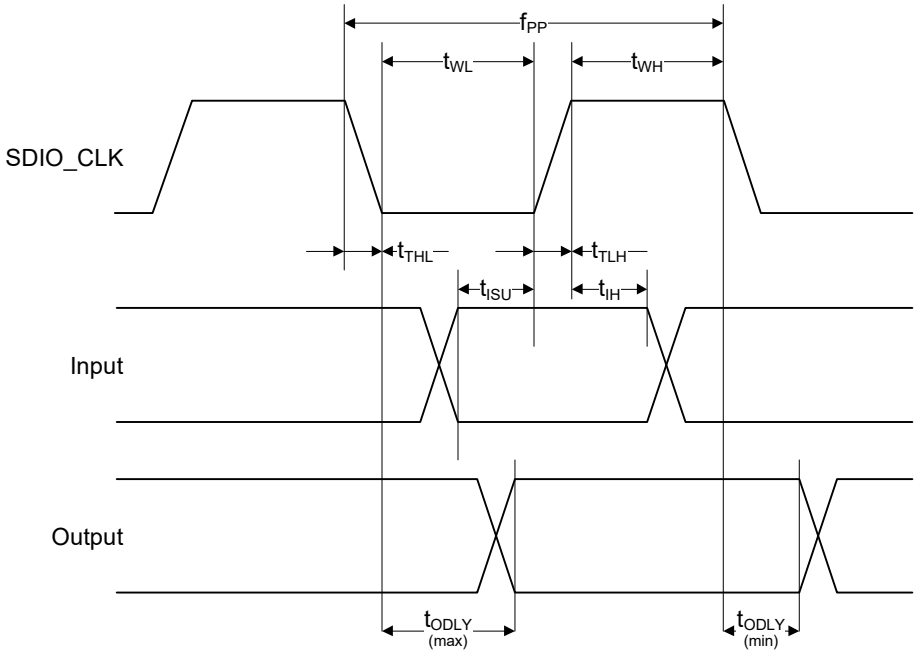


Table 21. SDIO Bus Timing[a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

9.7.2 SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 25 and Table 22.

Figure 25. SDIO Bus Timing (High-Speed Mode)

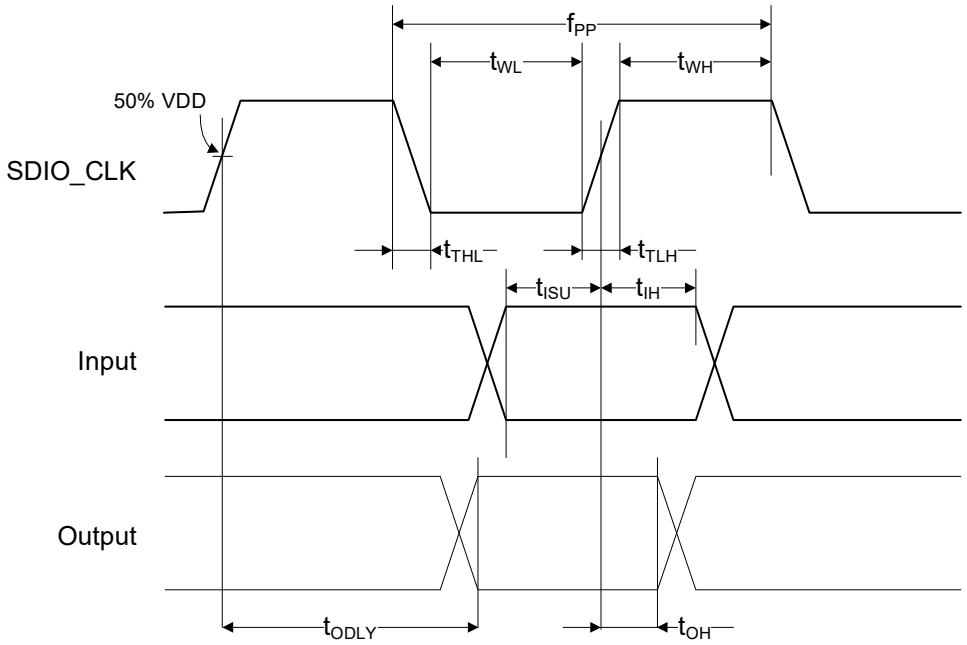


Table 22. SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b]					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

9.7.3 SDIO Bus Timing Specifications in SDR Modes

Clock Timing

Figure 26. SDIO Clock Timing (SDR Modes)

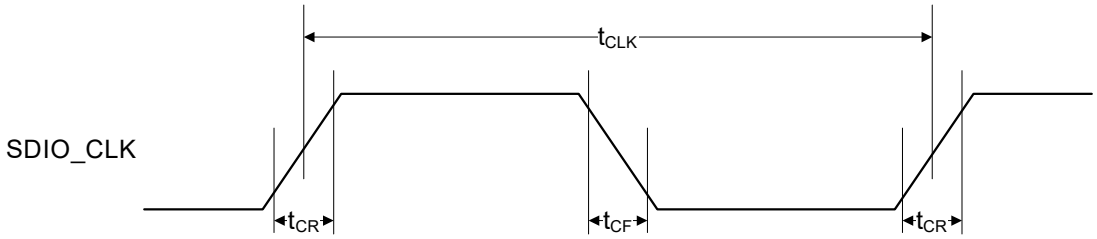


Table 23. SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		12.5	–	ns	SDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @ 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @ 208 MHz, C_{CARD} = 10 pF
Clock duty Cycle	–	30	70	%	–

Card Input Timing

Figure 27. SDIO Bus Input Timing (SDR Modes)

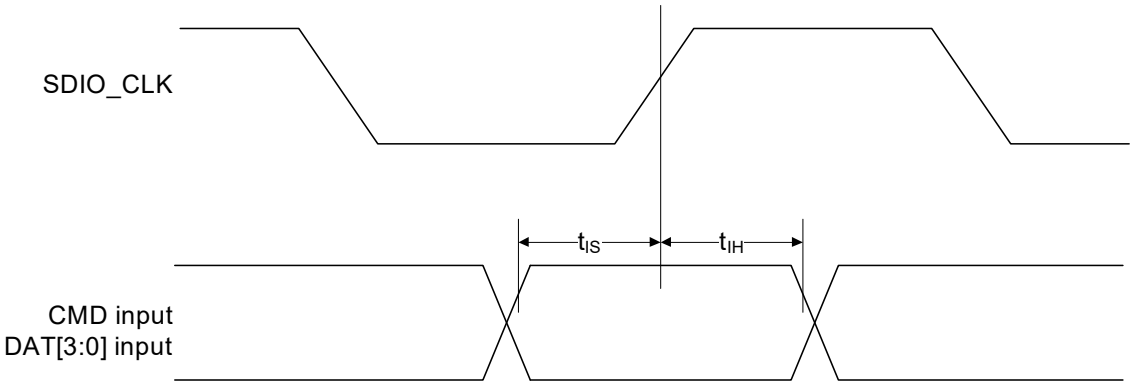


Table 24. SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Minimum	Maximum	Unit	Comments
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Card Output Timing

Figure 28. SDIO Bus Output Timing (SDR Modes up to 80 MHz)

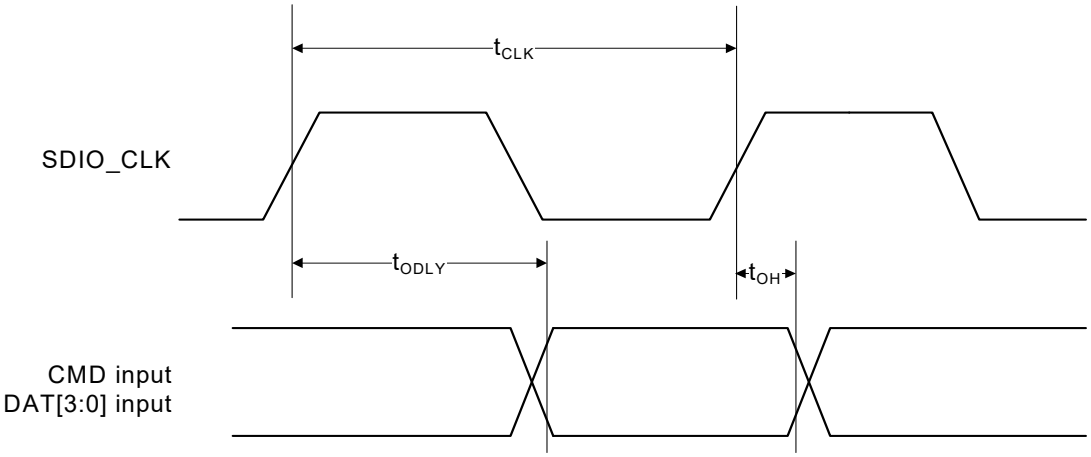


Table 25. SDIO Bus Output Timing Parameters (SDR Modes up to 80 MHz)

Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) C_L= 15 pF

9.7.4 SDIO Bus Timing Specifications in DDR50 Mode

Figure 29. SDIO Clock Timing (DDR50 Mode)

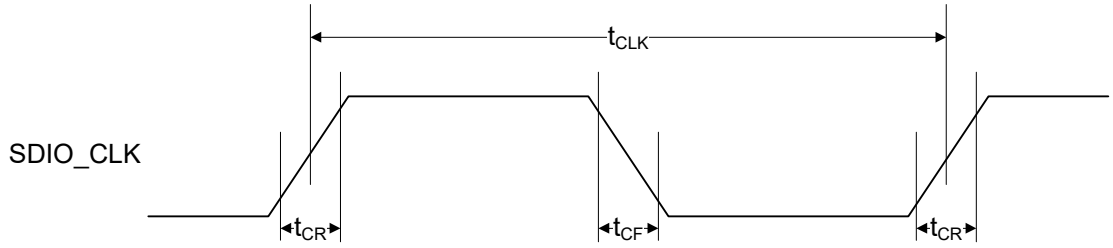


Table 26. SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	25	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty Cycle	–	45	55	%	–

Data Timing

Figure 30. SDIO Data Timing (DDR50 Mode)

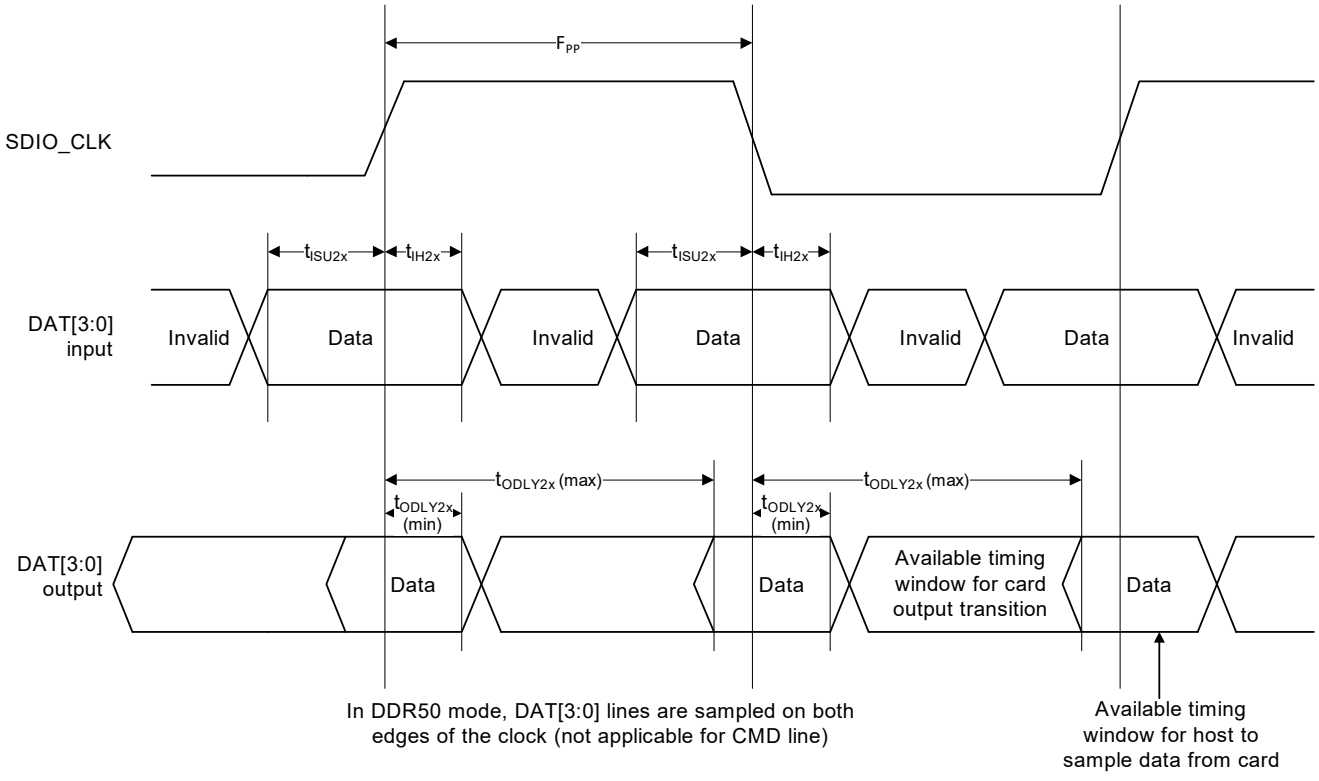


Table 27. SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

9.8 JTAG/SWD Interface

The CYW43012 supports IEEE 1149.1 JTAG boundary scan and reduced pin-count SWD mode to access the chip's internal blocks and backplane for system bring-up and debugging. This interface allows Cypress to assist customers with proprietary debug and characterization test tools. It is highly recommended that access be provided to at least the SWD pins by using either test points or a header on all PCB designs.

The SWD interface uses two of the JTAG signals: TMS for bidirectional data (SWDIO) and TCK for the clock (SWCLK). The debug access port (DAP) embedded in the ARM processor supports both SWD and JTAG interfaces and can be switched from one to the other via a specific sequence on the TMS/SWD lines. In addition to the ARM debug interface, an internal JTAG master on the DAP allows access to test access points (TAPs) in the CYW43012 for hardware debugging.

9.8.1 JTAG Timing

Table 28. JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Set up	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

9.8.2 SWD Timing

The probe outputs data to SWDIO on the falling edge of SWDCLK and captures data from SWDIO on the rising edge of SWDCLK. The target outputs data to SWDIO on the rising edge of SWDCLK and captures data from SWDIO on the rising edge of SWDCLK.

SWD timing is shown through the combination of Figure 31 on page 53 and Table 29 on page 53.

Figure 31. SWD Read and Write Timing

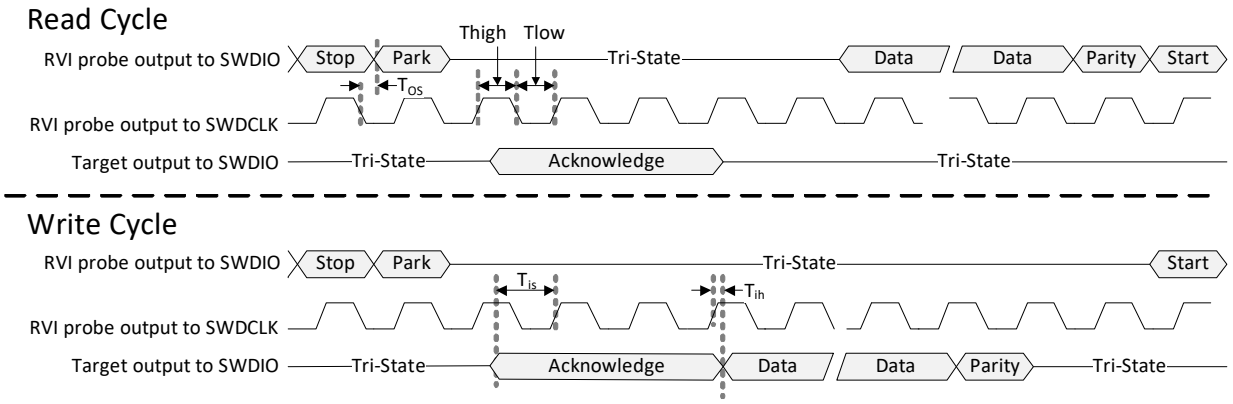


Table 29. SWD Read and Write Timing Parameters

Parameter	Description	Min.	Max.	Unit
T_{cyc}	SWDCLK cycle time	125	–	ns
T_{high}	SWDCLK high period	50	–	ns
T_{low}	SWDCLK low period	50	–	ns
T_{os}	SWDIO output skew to the falling edge of SWDCLK	–5	5	ns
Tis	Input setup time between SWDIO and the rising edge of SWDCLK	20	–	ns
T_{ih}	Input hold time between SWDIO and the rising edge of SWDCLK	0	100	ns

9.8.3 SFLASH Timing

Note: The SFLASH timing below is only when WLAN is using SFLASH pins of the chip. When BT uses SFLASH interface of the chip, the SFLASH timing will be different.

Figure 32. Input Timing

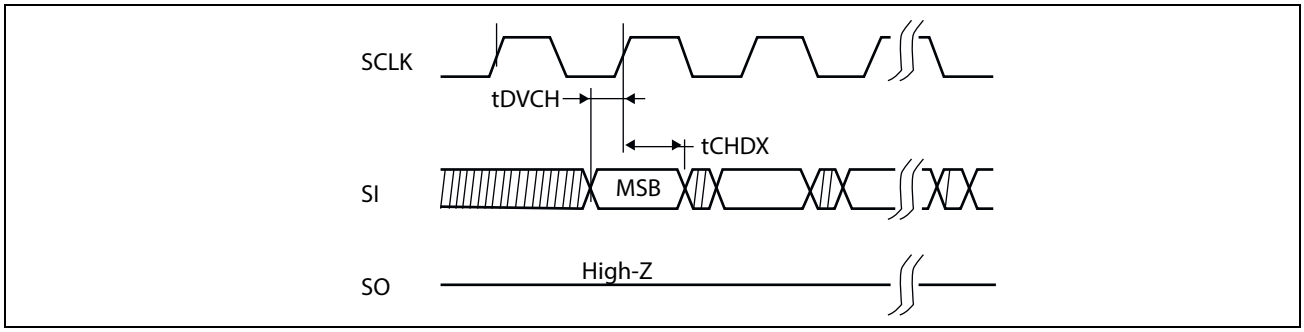


Figure 33. Output Timing

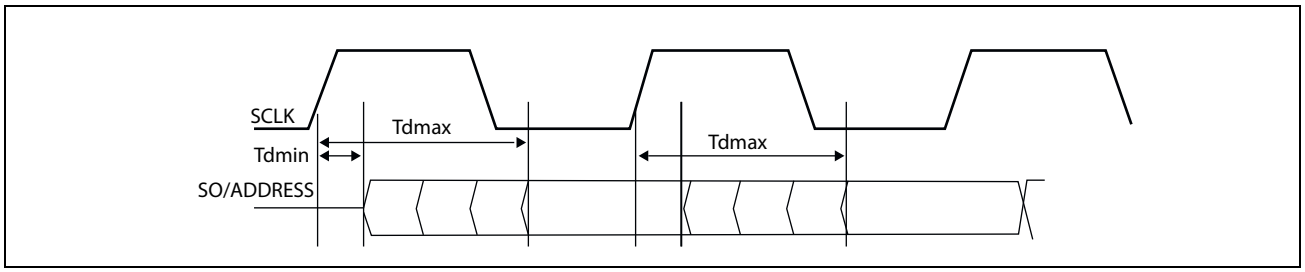


Table 30. SFLASH Timing

Parameter and Description
High-Speed Mode:
Max. SFLASH clock frequency = 80 MHz
Tdmax (tCLQV) = 10.5 ns or {Clock Period T (12.5 ns) – SFLASH setup time (2 ns)}
Tdmin (tCLQX) = 5 ns or (SFLASH hold time)
Tsetup (tDVCH) = –1.25 ns (It is negative because clock has been delayed by 3 ns inside the chip.)
Thold (tCHDX) = 3.0 ns
Non High-Speed Mode:
Max. SFLASH clock frequency = 26.67 MHz
Tdmax (tCLQV) = ½ SCLK + 10.5 ns
Tdmin (tCLQX) = ½ SCLK
Tsetup (tDVCH) = +1.75 ns
Thold (tCHDX) = 3.0 ns

10. Wireless LAN MAC and PHY

10.1 MAC Features

The CYW43012 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization.

The CYW43012 WLAN media access controller (MAC) supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The key MAC features include:

- Transmission and reception of aggregated MPDUs (A-MPDU) for high throughput (HT)
- Support for power management schemes, including WMM power-save, power-save multi-poll (PSMP) and multiphase PSMP operation
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware offload for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

The CYW43012 MAC supports MCS8 (256-QAM with a 3/4 coding rate) when operating with IEEE 802.11ac access points.

10.2 PHY Description

The CYW43012 WLAN Digital PHY is designed to comply IEEE 802.11a/b/g/n single-stream specifications to provide wireless LAN connectivity supporting data rates from 1 Mbps to 72.2 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking.

The CYW43012 PHY can also support rates of up to 78 Mbps using MCS8 when operating with IEEE 802.11ac access points.

The key PHY features include:

- Programmable data rates from MCS0–MCS7 in 20 MHz channels.
- Optional Short GI mode in TX and RX for MCS0 to MCS7 rates.
- MCS8 data rates for 20 MHz channels in the 5 GHz band
- TX and RX LDPC for improved range and power efficiency.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction and inverse operations in the receive direction.
- Receive space-time block coding (STBC).
- Supports IEEE 802.11h/k for worldwide operation.
- Advanced algorithms for low power, enhanced sensitivity, range, and reliability.
- Algorithms to improve performance in presence of Bluetooth.
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications.
- Closed loop transmit power control.
- Digital RF chip calibration algorithms to handle CMOS RF chip non-idealities.
- On-the-fly channel frequency and transmit power selection.
- Available per-packet channel quality and signal strength measurements.
- Designed to meet FCC and other worldwide regulatory requirements.
- IEEE 802.11ac beamformee support with NDP sounding and explicit, compressed V-matrix feedback.

11. DC Characteristics

Note: Values in this section of the datasheet are measured on a board that uses the CYW43012 FCBGA package. The performance may vary based on board design, front end and the 43012 package/module used.

Customers must use NVRAM obtained from Cypress or one of Cypress's qualified module partners and must refrain from changing NVRAM settings without consulting Cypress. Changes to NVRAM settings will impact multiple areas of chip performance including reliability across lifetime.

11.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 31 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect the long-term reliability of the device.

Table 31. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply for the VBAT and PA driver supply	VBAT	–0.5 to +5.0	V
DC supply voltage for digital I/O	V IO	–0.5 to 2.20	V
DC supply voltage for RF switch I/Os	VDDIO RF	–0.5 to 4.10	V
DC input supply voltage for CLDO	–	–0.5 to 1.4	V
DC supply voltage for Serial Flash	VDDIO_SFL	–0.5 to 4.10	V
DC supply voltage for RF analog	VDDRF	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.2	V
Maximum undershoot voltage for I/O[a]	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O[a]	$V_{overshoot}$	VDDIO + 0.5	V
Maximum junction temperature	T_j	125	°C
Maximum input power for RX input ports[b]	–	0	dBm

a. Duration not to exceed 25% of the duty cycle.

b. Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 0 dBm at a 1.5% duty-cycle derated from a seven year lifetime.

11.2 Environmental Ratings

The environmental ratings are shown in Table 32.

Table 32. Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	-20 to +70	°C	–
Storage Temperature	–40 to +125	°C	–
Relative Humidity	Less than 60	%	Storage
Relative Humidity	Less than 85	%	Operation

11.3 Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 33. ESD Specifications

Pin Type	Symbol	Condition	Minimum ESD Rating	Unit
ESD Handling	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	2.0	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	500	V

11.4 Recommended Operating Conditions and DC Characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 34. Operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Note: For DC absolute maximum rating (AMR), see Table 31 on page 57.

Table 34. Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBAT	VBAT	3.2[a]	3.6	4.6[b]	V
DC supply voltage for core	VDDC	0.97	1.0	1.03	V
DC supply voltage for RF blocks in chip	VDDRF	1.056	1.1	1.144	V
DC supply voltage for digital I/O	VDDIO	1.62	1.8	1.98	V
DC supply voltage for RF switch I/Os	VDDIO_RF	3.13	3.3	3.46	V
DC supply voltage for SFLASH I/O	VDDIO_SFL	1.62/2.97	1.8/3.3	1.98/3.46	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.53	0.56	0.59	V
Other Digital I/O Pins[c]					
For VDDIO = 1.8V:					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–	–	0.35 × VDDIO	V
Output high voltage @ 2 mA	VOH	VDDIO – 0.45	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.45	V
RF Switch Control Output Pins[d]					
For VDDIO_RF = 3.3V:					
Output high voltage @ 2 mA	VOH	VDDIO – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–	–	0.40	V
Output capacitance	C_{OUT}	–	–	5	pF

a. The CYW43012 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.6V < VBAT < 4.6V.

b. The maximum continuous voltage is TBD.

c. Refer Table 3 for BT/WL REG ON input high/low voltages (VIH/VIL).

d. Programmable 2 mA to 16 mA drive strength. Default is 6 mA.

12. Bluetooth RF Specifications

Notes:

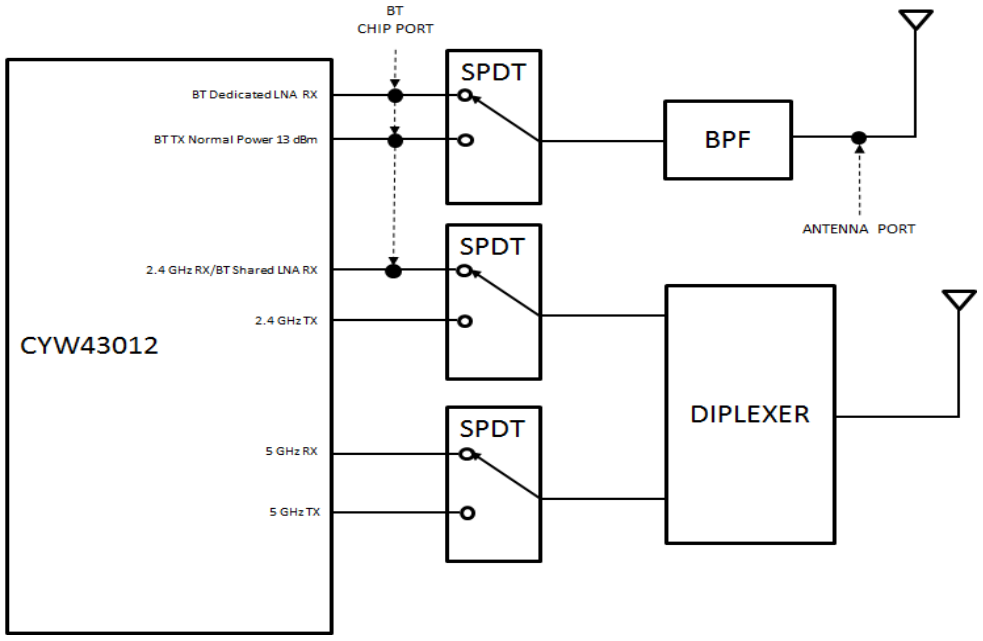
- Values in this section of the datasheet are measured on a board that uses the CYW43012 FCBGA package. The performance may vary based on board design, front end and the 43012 package/module used.
- Dedicated-LNA is only supported with WLCSP & WLBGA packages.

Customers must use NVRAM obtained from Cypress or one of Cypress's qualified module partners and must refrain from changing NVRAM settings without consulting Cypress. Changes to NVRAM settings will impact multiple areas of chip performance including reliability across lifetime.

Unless otherwise stated, limit values apply for the conditions specified in Table 32. "Environmental Ratings," on page 57 and Table 33. "ESD Specifications," on page 58. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 34. Port Locations for Bluetooth Testing



Note: All Bluetooth specifications are measured at the chip port, unless otherwise defined.

Table 35. Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Receive sensitivity with dirty transmit off (dLNA_HP and sLNA_HP)	1 Mbps, GFSK BDR, 0.1% BER	–	–94	–	dBm
	2 Mbps, B9 π/4-DQPSK EDR-2, 0.01% BER	–	–96	–	dBm
	3 Mbps, 8-DQPSK EDR-3, 0.01% BER	–	–90	–	dBm
	1 Mbps, GFSK BLE, 0.1% BER	–	–96	–	dBm
Maximum input at chip port	–	–	–	–20	dBm
RX LO Leakage					
2.4 GHz band	–	–	–90	–80	dBm
Interference Performance [a, b]					
C/I co-channel	GFSK, 0.1% BER	–	8	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–35	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–34	–9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–47	–20	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	10	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–42	–30	dB
C/I ≥ 3 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–51	–40	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–33	–7	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–38	–20	dB
C/I co-channel	8-DPSK, 0.1% BER	–	18	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–2	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–38	–25	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–39	–33	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–24	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–39	–13	dB
Out-of-Band Blocking Performance (CW) [b]					
30–2000 MHz	0.1% BER	–	–10	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer [c]					
GFSK (1 Mbps) [d]					

Table 35. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
698–716 MHz	WCDMA	–	–13	–	dBm
776–849 MHz	WCDMA	–	–14	–	dBm
824–849 MHz	GSM850	–	–13	–	dBm
824–849 MHz	WCDMA	–	–14	–	dBm
880–915 MHz	E-GSM	–	–13	–	dBm
880–915 MHz	WCDMA	–	–13	–	dBm
1710–1785 MHz	GSM1800	–	–18	–	dBm
1710–1785 MHz	WCDMA	–	–18	–	dBm
1850–1910 MHz	GSM1900	–	–19	–	dBm
1850–1910 MHz	WCDMA	–	–19	–	dBm
1880–1920 MHz	TD-SCDMA	–	–20	–	dBm
1920–1980 MHz	WCDMA	–	–20	–	dBm
2010–2025 MHz	TD–SCDMA	–	–20	–	dBm
2500–2570 MHz	WCDMA	–	–26	–	dBm
2510 MHz	LTE band, 7 FDD, 20 MHz BW	–	–34	–	dBm
2530 MHz	LTE band, 7 FDD, 20 MHz BW	–	–34	–	dBm
2550 MHz	LTE band, 7 FDD, 20 MHz BW	–	–32	–	dBm
2570 MHz	LTE band, 7 FDD, 20 MHz BW	–	–32	–	dBm
2310 MHz	LTE band, 40 FDD, 20 MHz BW	–	–34	–	dBm
2330 MHz	LTE band, 40 FDD, 20 MHz BW	–	–34	–	dBm
2350 MHz	LTE band, 40 FDD, 20 MHz BW	–	–34	–	dBm
2370 MHz	LTE band, 40 FDD, 20 MHz BW	–	–34	–	dBm
2570–2620 MHz	Band 38	–	–33	–	dBm
2545–2575 MHz	XGP Band	–	–33	–	dBm
π/4-DPSK (2 Mbps) [d]					
698–716 MHz	WCDMA	–	–10	–	dBm
776–794 MHz	WCDMA	–	–10	–	dBm
824–849 MHz	GSM850	–	–11	–	dBm
824–849 MHz	WCDMA	–	–11	–	dBm
880–915 MHz	E-GSM	–	–10	–	dBm
880–915 MHz	WCDMA	–	–10	–	dBm
1710–1785 MHz	GSM1800	–	–16	–	dBm
1710–1785 MHz	WCDMA	–	–15	–	dBm
1850–1910 MHz	GSM1900	–	–17	–	dBm
1850–1910 MHz	WCDMA	–	–16	–	dBm
1880–1920 MHz	TD-SCDMA	–	–18	–	dBm
1920–1980 MHz	WCDMA	–	–17	–	dBm
2010–2025 MHz	TD-SCDMA	–	–19	–	dBm
2500–2570 MHz	WCDMA	–	–34	–	dBm
2510 MHz	LTE band, 7 FDD, 20 MHz BW	–	–34	–	dBm

Table 35. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
2530 MHz	LTE band, 7 FDD, 20 MHz BW	–	–33	–	dBm
2550 MHz	LTE band, 7 FDD, 20 MHz BW	–	–33	–	dBm
2570 MHz	LTE band, 7 FDD, 20 MHz BW	–	–33	–	dBm
2310 MHz	LTE band, 40 FDD, 20 MHz BW	–	–35	–	dBm
2330 MHz	LTE band, 40 FDD, 20 MHz BW	–	–35	–	dBm
2350 MHz	LTE band, 40 FDD, 20 MHz BW	–	–35	–	dBm
2370 MHz	LTE band, 40 FDD, 20 MHz BW	–	–35	–	dBm
2570–2620 MHz [e]	Band 38	–	–34	–	dBm
2545–2575 MHz [f]	XGP Band	–	–34	–	dBm
8-DPSK (3 Mbps)[g]					
698-716 MHz	WCDMA	–	–13	–	dBm
776-794 MHz	WCDMA	–	–13	–	dBm
824-849 MHz	GSM850	–	–13	–	dBm
824-849 MHz	WCDMA	–	–14	–	dBm
880-915 MHz	E-GSM	–	–13	–	dBm
880-915 MHz	WCDMA	–	–13	–	dBm
1710-1785 MHz	GSM1800	–	–18	–	dBm
1710-1785 MHz	WCDMA	–	–17	–	dBm
1850-1910 MHz	GSM1900	–	–19	–	dBm
1850-1910 MHz	WCDMA	–	–19	–	dBm
1880-1920 MHz	TD-SCDMA	–	–19	–	dBm
1920-1980 MHz	WCDMA	–	–19	–	dBm
2010-2025 MHz	TD-SCDMA	–	–20	–	dBm
2500-2570 MHz	WCDMA	–	–23	–	dBm
2510 MHz	LTE band, 7 FDD, 20 MHz BW	–	–32	–	dBm
2530 MHz	LTE band, 7 FDD, 20 MHz BW	–	–31	–	dBm
2550 MHz	LTE band, 7 FDD, 20 MHz BW	–	–31	–	dBm
2570 MHz	LTE band, 7 FDD, 20 MHz BW	–	–31	–	dBm
2310 MHz	LTE band, 40 FDD, 20 MHz BW	–	–33	–	dBm
2330 MHz	LTE band, 40 FDD, 20 MHz BW	–	–33	–	dBm
2350 MHz	LTE band, 40 FDD, 20 MHz BW	–	–33	–	dBm
2370 MHz	LTE band, 40 FDD, 20 MHz BW	–	–33	–	dBm
2570–2620 MHz [e]	Band 38	–	–32	–	dBm
2545–2575 MHz [f]	XGP Band	–	–32	–	dBm
Spurious Emissions [b]					
30 MHz–1 GHz		–	–95	–	dBm
1–12.75 GHz		–	–70	–	dBm
Out -of -Band Noise Floor[b]					
851–894 MHz		–	–147	–	dBm/ Hz

Table 35. Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
925–960 MHz		–	–147	–	dBm/ Hz
1805–1880 MHz		–	–147	–	dBm/ Hz
1930–1990 MHz		–	–147	–	dBm/ Hz
2110–2170 MHz		–	–147	–	dBm/ Hz

a. The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 4.1 specification.

b. Applicable for all RX

c. Applicable for dLNA_HP and sLNA_HP

d. Bluetooth reference level for the required signal at the Bluetooth chip port is –91 dBm

e. Interferer: 2380 MHz, BW = 10 MHz, measured at 2480 MHz.

f. Interferer: 2355 MHz, BW = 10 MHz, measured at 2480 MHz.

g. Bluetooth reference level for the required signal at the Bluetooth chip port is –83 dBm.

Table 36. Bluetooth Transmitter RF Specification

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Note: The specifications in this table are measured at the Bluetooth chip port output, unless otherwise defined.					
General – BT Output Power Mode					
Frequency range	–	2402	–	2480	MHz
TX power at chip output that meets Bluetooth Test Specification RF.TS.4.0.0 ACP/EVM requirements	BDR, GFSK	–	13	–	dBm
	EDR-2, π/4-DQPSK	–	10	–	dBm
	EDR-3, 8-DPSK	–	10	–	dBm
	BLE, GFSK	–	13	–	dBm
Power control step	–	2	4	8	dB
O/P power in ultra-low TX o/p power mode	–	–	–45	–	dBm
Note: Output power is with TCA and TSSI enabled.					
GFSK In-Band Spurious Emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz		–	–	–20	dBm
|M – N| ≥ 2.5 MHz [a]		–	–	–40	dBm
Out-of-Band Spurious Emissions					
TX harmonics (HD2, HD3, HD4) in BT normal-power mode: ■ Chip Pout = 13 dBm in BDR and BLE mode ■ Chip Pout = 10 dBm in EDR-2 and EDR-3 mode	HD2	–	–24	–	dBm/MHz
	HD3	–	–12	–	dBm/MHz
	HD4	–	–44	–	dBm/MHz
GLONASS BAND Spurious Emissions					
FDMA L1 Band (1598.0625-1606.375MHz)[b]		–	–113	–	dBm/Hz
FDMA L2 Band (1242.9375-1248.625MHz)		–	–156	–	dBm/Hz
CDMA L1 Signal (1202.025MHz)		–	–158	–	dBm/Hz
CDMA L2 Signal (1248.06MHz)		–	–158	–	dBm/Hz
CDMA L3 Signal (1202.025MHz)		–	–158	–	dBm/Hz
GPS Band Spurious Emissions					
CDMA L1 Signal (1575.42MHz)		–	–153	–	dBm/Hz
CDMA L2 Signal (1227.60MHz)		–	–158	–	dBm/Hz
Out-of-Band Noise Floor [c]					
65–108 MHz	FMRX	–	–150	–	dBm/Hz

Table 36. Bluetooth Transmitter RF Specification (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
776–794 MHz	CDMA2000	–	–150	–	dBm/Hz
869–960 MHz	cdmaOne, GSM850	–	–150	–	dBm/Hz
925–960 MHz	E-GSM	–	–150	–	dBm/Hz
1570–1580 MHz	GPS	–	–150	–	dBm/Hz
1805–1880 MHz	GSM1800	–	–147	–	dBm/Hz
1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–145	–	dBm/Hz
2500–2570 MHz	Band 7	–	–133	–	dBm/Hz
2300–2400 MHz	Band 40	–	–133	–	dBm/Hz
2570–2620 MHz	Band 38	–	–136	–	dBm/Hz
2545–2575 MHz	XGP Band	–	–135	–	dBm/Hz

a. The typical number is measured at ± 3 MHz offset.

b. Spurs are only in L1 band for channels in the 2402MHz to 2410MHz range

c. Transmitted power in cellular and FM bands at the antenna port. See Figure 40 on page 62 for location of the port.

Table 37. Local Oscillator Performance

Parameter	Minimum	Typical	Maximum	Unit
LO Performance				
Lock time	–	72	–	µs
Initial carrier frequency tolerance	–	± 25	± 75	kHz
Frequency Drift				
DH1 packet	–	± 10	± 25	kHz
DH3 packet	–	± 10	± 40	kHz
DH5 packet	–	± 10	± 40	kHz
Drift rate	–	5	20	kHz/50 µs
Frequency Deviation				
00001111 sequence in payload[a]	140	155	175	kHz
10101010 sequence in payload[b]	115	140	–	kHz
Channel spacing	–	1	–	MHz

a. This pattern represents an average deviation in payload
b. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

13. WLAN RF Specifications

13.1 Introduction

The CYW43012 includes an integrated dual-band direct conversion radio that supports the 2.4 GHz and the 5 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5 GHz radio.

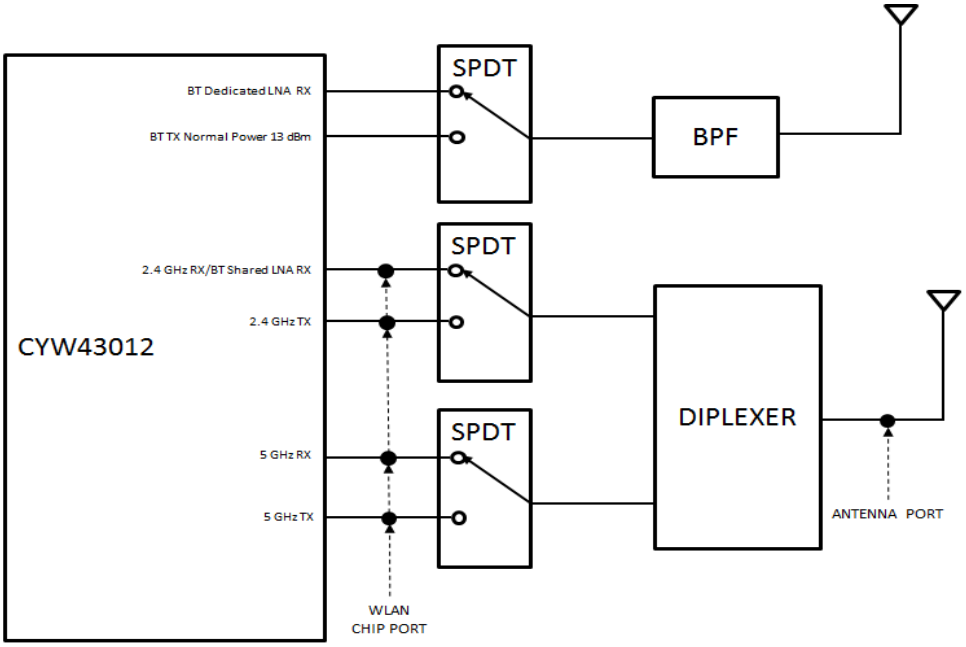
Note: Values in this section of the datasheet are measured on a board that uses the CYW43012 FCBGA package. The performance may vary based on board design, front end and the 43012 package/module used.

Customers must use NVRAM obtained from Cypress or one of Cypress's qualified module partners and must refrain from changing NVRAM settings without consulting Cypress. Changes to NVRAM settings will impact multiple areas of chip performance including reliability across lifetime.

Unless otherwise stated, limit values apply for the conditions specified in Table 32. "Environmental Ratings," on page 57 and Table 34. "Recommended Operating Conditions and DC Characteristics," on page 58 Typical values apply for the following conditions:

- VBAT = 3.6 V
- Ambient temperature +25 °C

Figure 35. Port Locations for WLAN Testing



Note: Unless otherwise defined, all WLAN specifications are provided at the chip port.

13.2 WLAN Radio Subsystem

The CYW43012 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz and 5 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Ten RF control signals are available to drive external RF switches. See the reference board schematics for further details.

Note that integrated on-chip baluns (not shown) convert the fully differential transmit and receive paths to single-ended signal pins.

13.3 Receiver Path

The CYW43012 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN receivers, while the 5 GHz receive path has a dedicated on-chip LNA. Control signals are available that can support the use of optional LNAs for each band.

13.4 Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5-GHz U-NII bands, respectively.

13.5 Calibration

The CYW43012 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

13.6 WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications shown in the following table are provided at the chip port, unless otherwise defined.

Table 38. WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	–98	–98	–	dBm
	2 Mbps DSSS	–	–96	–	dBm
	5.5 Mbps DSSS	–	–95	–	dBm
	11 Mbps DSSS	–89	–90	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM	–93	–94	–	dBm
	9 Mbps OFDM	–	–93	–	dBm
	12 Mbps OFDM	–	–92	–	dBm
	18 Mbps OFDM	–89	–90	–	dBm
	24 Mbps OFDM	–	–87	–	dBm
	36 Mbps OFDM	–82	–83	–	dBm
	48 Mbps OFDM	–	–79	–	dBm
	54 Mbps OFDM	–76	–77	–	dBm
RX sensitivity IEEE 802.11n 20 MHz channel spacing for all MCS rates (10% PER for 4096 octet PSDU)[a] Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS0	–93	–94	–	dBm
	MCS1	–	–94	–	dBm
	MCS2	–90	–91	–	dBm
	MCS3	–	–88	–	dBm
	MCS4	–84	–85	–	dBm
	MCS5	–	–81		dBm
	MCS6	–	–79	–	dBm
	MCS7	–76	–77		dBm

Table 38. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Blocking level for 1dB RX sensitivity degradation (without external filtering)[b]	776–794 MHz	CDMA2000	–17	–17	–	dBm
	824–849 MHz[c]	cdmaOne	–17	–16	–	dBm
	824–849 MHz	GSM850	–17	–16	–	dBm
	880–915 MHz	E-GSM	–16	–16	–	dBm
	1710–1785 MHz	GSM1800	–19	–18	–	dBm
	1850–1910 MHz	GSM1800	–19	–18	–	dBm
	1850–1910 MHz	cdmaOne	–20	–19	–	dBm
	1850–1910 MHz	WCDMA	–21	–21	–	dBm
	1920–1980 MHz	WCDMA	–20	–18	–	dBm
	2500–2570 MHz	Band 7	–24	–26	–	dBm
	2300–2400 MHz	Band 40	–25	–26	–	dBm
	2570–2620 MHz	Band 38	–25	–23	–	dBm
	2545–2575 MHz	XGP Band	–	–23	–	dBm
In-band static CW jammer immunity (fc – 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for:(RxSens + 23 dB < Rxlevel < max. input level)	–	–82	–	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)	–	–5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)	–	–9	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)	–	–9	–	–	dBm
	@ MCS0–MCS7 rates (10% PER, 4095 octets)	–	–9	–	–	dBm
Adjacent channel rejection-DSSS 8% PER for 1024 octet PSDU with 6 dB sensitivity degradation from minimum sensitivity in spec.	Desired and interfering signal 25 MHz apart					
	11 Mbps DSSS	–70 dBm	35	45	–	dB
Adjacent channel rejection-OFDM 10% PER for 1000 octet PSDU 3 dB sensitivity degradation from minimum sensitivity in spec.	6 Mbps OFDM	–79 dBm	16	41	–	dB
	18 Mbps OFDM	–74 dBm	11	36	–	dB
	36 Mbps OFDM	–67 dBm	4	29	–	dB
	54 Mbps OFDM	–62 dBm	–1	24	–	dB
Adjacent channel rejection HT 10% PER for 4096 octet PSDU 3 dB sensitivity degradation from minimum sensitivity in spec.	MCS0	–79 dBm	16	35	–	dB
	MCS2	–74 dBm	11	28	–	dB
	MCS4	–67 dBm	4	23	–	dB
	MCS7	–61 dBm	–2	15	–	dB
Gain control step	–	–	–	3	–	dB

Table 38. WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
RSSI accuracy[d]	Range –95 dBm to –30 dBm	–	–3.5	–	3.5	dB
	Range above –30 dBm	–	–4	–	5	dB
Return loss	Zo = 50Ω, across the dynamic range	–	–	11	–	dB
Receiver cascaded noise figure	At maximum gain	–	–	4	–	dB

a. Sensitivity degradations for alternate settings in MCS modes. SGI: 2 dB drop.

b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.

c. The blocking levels are valid for channels 1 to 11. (For higher channels, the performance may be lower due to third harmonic signals (3 × 824 MHz) falling within band.)

d. The minimum and maximum values shown have a 95% confidence level.

13.7 WLAN 2.4 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the WLAN chip port output.

Table 39. WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands (at - 5 dBm, 100% duty cycle, 1 Mbps CCK)[a]	76–108 MHz	FM RX	–	–164	–	dBm/Hz
	776–794 MHz	–	–	–164	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–162	–	dBm/Hz
	925–960 MHz	E-GSM	–	–162	–	dBm/Hz
	1570–1580 MHz	GPS	–	–149	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–142	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne WCDMA	–	–136	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–129	–	dBm/Hz
	2620–2690 MHz	Band 7	–	–123	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–67	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–121	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–115	–	dBm/Hz
EVM Does Not Exceed						
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6 V with spectral mask and EVM compliance[b]	802.11b (DSSS/CCK) 1Mbps	–9 dB	20	20	–	dBm
	802.11b (DSSS/CCK) 11Mbps	–9 dB	21	22	–	dBm
	802.11g (BPSK 1/2) 6Mbps	–5 dB	20	20	–	dBm
	802.11g (QPSK 3/4) 18Mbps	–13 dB	20	20	–	dBm
	802.11g (16-QAM 3/4) 36Mbps	–19 dB	20	20	–	dBm
	802.11g (64-QAM 3/4) 54Mbps	–25 dB	19	20	–	dBm
	802.11n (BPSK 1/2) MCS0	–5 dB	20	20	–	dBm
	802.11n (QPSK 3/4) MCS2	–13 dB	19	20	–	dBm
	802.11n (16-QAM 3/4) MCS4	–19 dB	19	19	–	dBm
	802.11n (64-QAM 5/6) MCS7	–28 dB	18	19	–	dBm
TX power control dynamic range	–		13	–	–	dB
Closed-loop TX power variation at highest power level setting	Across full temperature and voltage range. Applies to 10 dBm to 20 dBm output power range.		2.0 to -1.5	2.0 to -1.5	–	dB
Carrier suppression	–		30	–	–	dBc
Gain control step	–		–	0.25	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. Typical TX powers apply to typical silicon only. The minimum TX power in this table is guaranteed by design. The TX power at the chip output port is controlled by firmware and is in the best case approximately 1.5dB to 2.0dB lower from the minimum numbers mentioned, to account for closed loop TX power control variation and other factors. The actual TX power seen by customers at the antenna port will also be affected by board related losses and regulatory performance limitations.

13.8 WLAN 5 GHz Receiver Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the chip port input.

Table 40. WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900		5845	MHz
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM		–91	–95	–	dBm
	9 Mbps OFDM		–91	–94	–	dBm
	12 Mbps OFDM		–	–94	–	dBm
	18 Mbps OFDM		–88	–91	–	dBm
	24 Mbps OFDM		–	–88	–	dBm
	36 Mbps OFDM		–81	–84	–	dBm
	48 Mbps OFDM		–	–80	–	dBm
	54 Mbps OFDM		–75	–78	–	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters: 800 ns GI and non-STBC.	20 MHz channel spacing for all MCS rates					
	MCS0		–92	–95	–	dBm
	MCS1		–	–94	–	dBm
	MCS2		–89	–92	–	dBm
	MCS3		–	–89	–	dBm
	MCS4		–83	–86	–	dBm
	MCS5		–	–82	–	dBm
	MCS6		–	–80	–	dBm
	MCS7		–75	–78	–	dBm
	MCS8		–71	–74	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps (10% PER for 1000 octet PSDU)		–9	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps (10% PER for 1000 octet PSDU)		–9	–	–	dBm
	@ MCS0-MCS8 rates (10% PER for 4096 octet PSDU)		–9	–	–	dBm
Adjacent channel rejection desired signal (20 MHz apart) 10% PER for 1000 octet PSDU (11a) 3 dB sensitivity degradation from minimum sensitivity in spec.	6 Mbps	–79 dBm	16	29	–	dB
	18 Mbps	–74 dBm	11	24	–	dB
	36 Mbps	–67 dBm	4	18	–	dB
	54 Mbps	–62 dBm	–1	13	–	dB
Adjacent channel rejection desired signal (20 MHz apart) 10% PER for 4096 octets (VHT) 3 dB sensitivity degradation from minimum sensitivity in spec.	mcs0	–79 dBm	16	26	–	dB
	mcs2	–74 dBm	11	22	–	dB
	mcs4	–67 dBm	4	16	–	dB
	mcs7	–61 dBm	–2	8	–	dB
	mcs8nss1	–56 dBm	–7	6	–	dB
Gain control step	–		–	3	–	dB

Table 40. WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
RSSI accuracy[a]	Range –90 dBm to –30 dBm	–4	–	5	dB
	Range above –30 dBm	–6	–	3	dB
Return loss	Zo = 50Ω, across the dynamic range	–	11	–	dB
Receiver cascaded noise At maximum gain figure	–	–	5	–	dB

a. The minimum and maximum values shown have a 95% confidence level.

13.9 WLAN 5 GHz Transmitter Performance Specifications

Note: Unless otherwise noted, the values shown in the following table are provided at the WLAN chip port output.

Table 41. WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Transmitted power in cellular and FM bands (at -5 dBm, 100% duty cycle, 1 Mbps CCK) [a]	Frequency	Band				
	76–108 MHz	FM RX	–	–172	–	dBm/Hz
	776–794 MHz	–	–	–171	–	dBm/Hz
	869–960 MHz	cdmaOne, GSM850	–	–171	–	dBm/Hz
	925–960 MHz	E-GSM	–	–171	–	dBm/Hz
	1570–1580 MHz	GPS	–	–171	–	dBm/Hz
	1805–1880 MHz	GSM1800	–	–171	–	dBm/Hz
	1930–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–158	–	dBm/Hz
	2110–2170 MHz	WCDMA	–	–161	–	dBm/Hz
	2620–2690 MHz	Band 7	–	–159	–	dBm/Hz
	2300–2400 MHz	Band 40	–	–161	–	dBm/Hz
	2570–2620 MHz	Band 38	–	–159	–	dBm/Hz
	2545–2575 MHz	XGP Band	–	–160	–	dBm/Hz

Table 41. WLAN 5 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
EVM Does Not Exceed						
TX power at the chip port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[b]	802.11g (BPSK 1/2) 6Mbps	–5 dB	20	20	–	dBm
	802.11g (QPSK 3/4) 18Mbps	–13 dB	20	20	–	dBm
	802.11g (16-QAM 3/4) 36Mbps	–19 dB	19	20	–	dBm
	802.11g (64-QAM 3/4) 54Mbps	–25 dB	17	20	–	dBm
	802.11n (BPSK 1/2) MCS0	–5 dB	20	20	–	dBm
	802.11n (QPSK 3/4) MCS2	–13 dB	20	20	–	dBm
	802.11n (16-QAM 3/4) MCS4	–19 dB	19	20	–	dBm
	802.11n (64-QAM 5/6) MCS7	–28 dB	16	19	–	dBm
	802.11ac (256-QAM 3/4) MCS8	–30 dB	14	18	–	dBm
TX power control dynamic range	–		13	–	–	dB
Closed loop TX power variation at highest power level setting	Across full-temperature and voltage range. Applies across 10 to 20 dBm output power range.		2.5 to –2.5	2 to –2	–	dB
Carrier suppression	–		30	–	–	dBc
Gain control step	–		–	0.25	–	dB

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. Typical TX powers apply to typical silicon only. The minimum TX power in this table is guaranteed by design. The TX power at the chip output port is controlled by firmware and is in the best case approximately 2dB to 2.5dB lower from the minimum numbers mentioned, to account for closed loop TX power control variation and other factors. The actual TX power seen by customers at the antenna port will also be affected by board related losses and regulatory performance limitations.

13.10 General Spurious Emissions Specifications

This section provides the TX and RX spurious emissions specifications for both the WLAN 2.4 GHz and 5 GHz bands. The recommended spectrum analyzer settings for the spurious emissions specifications are provided in Table 44.

Table 42. Recommended Spectrum Analyzer Settings

Parameter	Setting
Resolution Bandwidth (RBW)	1 MHz
Video Bandwidth (VBW)	1 MHz
Sweep	Auto
Span	100 MHz
Detector	Maximum peak
Trace	Maximum hold
Modulation	OFDM (orthogonal frequency-division multiplexing)

13.10.1 Receiver Spurious Emissions Specifications

Table 43. 2G and 5G General Receiver Spurious Emissions

Band	Frequency Range	Typical	Unit
2G	2.4 GHz < f < 2.5 GHz	–81	dBm
	3.6 GHz < f < 3.8 GHz	–81	
5G	5150 MHz < f < 5850 MHz	–82	dBm
	3.45 GHz < f < 3.9 GHz	–57	dBm

13.10.2 Transmitter Spurious Emissions

Table 44. 2.4 GHz Band, 20 MHz Channel Spacing TX Spurious Emissions Specifications

Emissions Frequency Range (MHz)	Channel Power (dBm)	Typical Spurious Emission Level (dBm)[a]	
		CH2412	CH2472
1000-2000	21	-55	-51
2000-2400	21	-37	-37
2500-3000	21	-30	-32
3000-4000	21	-49	-50
4000-5000	21	-17	-17
5000-6000	21	-48	-49
6000-7000	21	-49	-49
7000-8000	21	-9	-8
8000-10000	21	-19	-18
10000-12000	21	-51	-52
12000-15000	21	-27	-26
15000-20000	21	-45	-43

a. Measured at chip out using max hold operating mode.

Table 45. 5 GHz Band, 20 MHz Channel Spacing TX Spurious Emissions Specifications

Emissions Frequency Range (MHz)	Channel Power (dBm)	Typical Spurious Emission Level (dBm)[a]					
		CH5180	CH5320	CH5500	CH5700	CH5745	CH5825
1000 – 2000	19	-51	-51	-51	-52	-51	-51
2000 - 3000	19	-50	-50	-50	-50	-50	-49
3000 - 4000	19	-50	-50	-50	-51	-51	-50
4000 - 5000	19	-48	-49	-49	-49	-49	-49
5000 – 6000	19	-46	-36	-46	-40	-40	-44
6000 – 7000	19	-50	-50	-49	-49	-48	-48
7000 – 8000	19	-49	-50	-50	-49	-50	-50
8000 – 10000	19	-53	-53	-53	-53	-53	-53
10000 – 12000	19	-13	-16	-18	-17	-17	-14
12000 – 15000	19	-50	-51	-50	-50	-50	-51
15000 – 20000	19	-21	-20	-21	-22	-25	-23

a. Measured at chip out using max hold operating mode.

14. System Power Consumption

Note: Values in this section of the datasheet are measured on a board that uses the CYW43012 FCBGA package. The performance may vary based on board design, front end and the 43012 package/module used.

Customers must use NVRAM obtained from Cypress or one of Cypress's qualified module partners and must refrain from changing NVRAM settings without consulting Cypress. Changes to NVRAM settings will impact multiple areas of chip performance including reliability across lifetime**.**

Note: Unless otherwise stated, these values apply for the conditions specified in Table 34. "Recommended Operating Conditions and DC Characteristics," on page 58.

14.1 WLAN Current Consumption

The tables in this subsection show the total current consumed by the CYW43012 measured across typical units and for the stated voltage and temperature conditions. For the active transmit cases, internal PA scenarios are given. All values shown are with the Bluetooth core in reset mode with Bluetooth off.

2.4 GHz Mode

Table 46. 2.4 GHz Mode WLAN Power Consumption

Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, T_A = 25°C	
Sleep Modes	**V_{BAT}, µA**	**V_{IO}, µA [a]**
Radio OFF[b]	1.2	0.3
Sleep current[c]	3.0	88
IEEE Power save, DTIM = 1 – single RX [d]	447	93
IEEE Power save, DTIM = 3 – single RX	156	88
IEEE Power save, DTIM = 10 – single RX	46	87
Active RX Modes	**V_{BAT}, mA**	**V_{IO}, mA [a]**
CRS – HT20 [e]	18.5	0.375
Continuous RX mode 1 Mbps	20.5	0.375
Continuous RX mode MCS7 – HT20 – 1SS [f, g]	21	0.375
Active TX Modes	**V_{BAT}, mA**	**V_{IO}, mA [a]**
Continuous TX mode MCS7 – HT20 – 1SS – 18 dBm [h]	187	1.4
Peak PHY Calibration Current	**VBAT, mA**	**VIO, mA[a]**
Unassociated	322.3	1.4
Associated	261.5	1.4

a. VIO is specified with all pins idle (not switching) and not driving any loads.

b. WL_REG_ON and BT_REG_ON are both low. All supplies are present.

c. Idle, not associated, or inter-beacon.

d. Beacon Interval = 102.4 ms. Beacon duration = 1 ms @ 1 Mbps. Average current over 3x DTIM intervals.

e. Carrier sense (CCA) when no carrier present.

f. Duty cycle is 100%. Carrier sense (CS) detect/packet receive

g. Measured using packet engine test mode

h. Duty cycle in 100%. Includes internal PA contribution

5 GHz Mode

Table 47. 5 GHz Mode WLAN Power Consumption

Mode	V_{BAT} = 3.6 V, VDDIO = 1.8 V, T_A = 25°C	
Sleep Modes	**V_{BAT}, µA**	**V_{IO}, µA [a]**
Radio OFF[b]	1.2	0.3
Sleep current[c]	3.0	88
IEEE Power save, DTIM = 1 – single RX [d]	255	90
IEEE Power save, DTIM = 3 – single RX	88	87
IEEE Power save, DTIM = 10 – single RX	31	88
Active RX Modes	**V_{BAT}, mA**	**V_{IO}, mA [a]**
CRS – HT20 [e]	19.7	0.77
Continuous RX mode MCS7 – HT 20 – 1SS [f, g]	21.5	0.77
Active TX Modes	**V_{BAT}, mA**	**V_{IO}, mA [a]**
Continuous TX mode MCS7 – HT20 – 1SS –18 dBm[h]	265	1.6
Peak PHY Calibration Current	**VBAT, mA**	**VIO, mA[a]**
Unassociated	322.3	1.4
Associated	308.5	1.4

a. V_{IO} is specified with all pins idle (not switching) and not driving any loads.

b. WL_REG_ON and BT_REG_ON are both low. All supplies present

c. Idle, not associated, or inter-beacon.

d. Beacon Interval = 102.4 ms. Beacon duration = 300 µs @ 6 Mbps. Average current over 3× DTIM intervals.

e. Carrier sense (CCA) when no carrier present.

f. Duty cycle is 100%. Carrier sense (CS) detect/packet receive.

g. Measured using packet engine test mode.

h. Duty cycle is 100%. Includes internal PA contribution.

14.2 Bluetooth Current Consumption

The Bluetooth and BLE current consumption measurements are shown in Table 51. The tables in this subsection show the total current consumed by the CYW43012 measured across typical units and for the stated voltage and temperature conditions.

Note:

- Dedicated-LNA current consumption data only applicable to WLCSP & WLBGA packages.
- The WLAN core is in reset (WLAN_REG_ON = low) for all measurements provided in Table 51.
- The current consumption in the table below is measure with the following chip TX o/p power settings:

Index 0 (Max OP) = 13dBm
Index 1 = 9dBm
Index 2 = 5dBm
Index 3 = 1dBm

Table 48. Bluetooth and BLE Current Consumption

Operating Mode	With BT dLNA at T_A = 25°C		With BT sLNA at T_A = 25°C	
	Typical VBAT Current (VBAT = 3.6 V) (mA)	Typical VDDIO Current (VDDIO = 1.8 V) (mA)	Typical VBAT Current (VBAT = 3.6 V) (mA)	Typical VDDIO Current (VDDIO = 1.8 V) (mA)
Sleep	0.002	0.08	0.002	0.08
Standard 1.28s inquiry scan	0.09	0.08	0.09	0.08
500 ms Sniff Att = 1 Master	0.07	0.08	0.06	0.08
500ms Sniff Att = 1 Slave	0.06	0.08	0.05	0.08
DM1 DH1 Master TX RX	14.87	0.26	16.26	0.27
DM1 DH1 Slave TX RX	14.78	0.26	15.62	0.30
DM3 DH3 Master TX RX	17.62	0.29	19.21	0.29
DM3 DH3 Slave TX RX	17.43	0.29	19.84	0.27
DM5 DH5 Master TX RX	17.89	0.26	19.58	0.30
DM5 DH5 Master TX RX	17.66	0.32	18.88	0.29
3DH5 3DH1 TX RX Master	16.47	0.38	17.59	0.38
3DH5 3DH1 TX RX Slave	16.34	0.41	17.46	0.38
2DH5 Master TX-330KBPS	9.16	0.22	9.96	0.22
2DH5 Slave TX-330KBPS	9.13	0.22	9.92	0.23
3DH5 Master TX-330KBPS	7.22	0.21	7.93	0.22
3DH5 Slave TX-330KBPS	7.91	0.22	8.66	0.22
HV3 Master	6.68	0.18	7.65	0.26
HV3 Slave	7.46	0.25	8.46	0.26
HV3 Master | 500ms Sniff	5.69	0.23	6.08	0.24
HV3 Slave | 500ms Sniff	5.76	0.26	6.15	0.23
Transmit 100% On – index 3 BDR	16.07	0.25	17.76	0.22
Transmit 100% On – index 3 EDR	16.65	0.22	18.45	0.22
Transmit 100% On – index 2 BDR	18.14	0.29	20.03	0.29
Transmit 100% On – index 2 EDR	17.35	0.25	18.94	0.22
Transmit 100% On – index 1 BDR	23.03	0.29	24.11	0.30

Table 48. Bluetooth and BLE Current Consumption (Cont.)

Operating Mode	With BT dLNA at T_A = 25°C		With BT sLNA at T_A = 25°C	
	Typical VBAT Current (VBAT = 3.6 V) (mA)	Typical VDDIO Current (VDDIO = 1.8 V) (mA)	Typical VBAT Current (VBAT = 3.6 V) (mA)	Typical VDDIO Current (VDDIO = 1.8 V) (mA)
Transmit 100% On – index 1 EDR	22.41	0.25	24.04	0.26
Transmit 100% On - Max OP BDR	27.99	0.26	30.11	0.27
Transmit 100% On - Max OP EDR	24.42	0.29	26.18	0.29
Receive 100% On	10.15	0.24	11.47	0.22
Passive Scan 10ms	10.60	0.19	10.53	0.25
Active Scan 1.28sec	0.09	0.08	0.11	0.08
Adv - Unconnectable 1.00sec	0.03	0.08	0.03	0.08
Connected 300 ms Interval - Master	0.08	0.08	0.07	0.08
Connected 300ms Interval - Slave	0.08	0.08	0.08	0.08
Connected 1.00sec Interval - Master	0.03	0.08	0.02	0.08
Connected 1.00sec Interval - Slave	0.03	0.08	0.03	0.08

14.3 Processor Current Consumption

The Arm Cortex M4 in the Bluetooth core runs Bluetooth controller firmware, Bluetooth stack & profiles and customer code. The core is programmable via the WICED SDK. The table below provides the current consumption of the core across various modes. The tables in this subsection show the total current consumed by the CYW43012 measured across typical units and for the stated voltage and temperature conditions.

Table 49. Processor Current Consumption

	Typical Current at T_A = 25°C	
	VBAT = 3.6 V (mA)	VDDIO = 1.8 V (µA)
Hibernate/HID-OFF	0.0012	0.3
Sleep Current with 388KB RAM retained	0.003	80
Active current at 4 MHz	2.164	80
Active current at 24 MHz	2.984	80
Active current at 48 MHz	3.968	80
Active current at 96 MHz	5.936	80

15. Package Information

15.1 Package Thermal Characteristics

Table 50. Package Thermal Characteristics

Characteristic	WLCSP
Ambient air temperature T_A (°C)	70
θ_{JA} in still air (°C/W)	45.28
θ_{JB} (°C/W)	13.58
θ_{JC} (°C/W)	3.63
Ψ_{JT} (°C/W)	14.39
Ψ_{JB} (°C/W)	22.18
Maximum junction temperature T_j (°C)	125
Maximum power dissipation (W)	1.21
Characteristic	**FCBGA**
Ambient air temperature T_A (°C)	70
θ_{JA} in still air (°C/W)	44.06
θ_{JB} (°C/W)	26.63
θ_{JC} (°C/W)	28.09
Ψ_{JT} (°C/W)	20.27
Ψ_{JB} (°C/W)	31.45
Maximum junction temperature T_j (°C)	125
Maximum power dissipation (W)	1.14
Characteristic	**WLBGA**
Ambient air temperature T_A (°C)	70
θ_{JA} in still air (°C/W)	41.93
θ_{JB} (°C/W)	10.66
θ_{JC} (°C/W)	4.52
Ψ_{JT} (°C/W)	11.10
Ψ_{JB} (°C/W)	17.83
Maximum junction temperature T_j (°C)	125
Maximum power dissipation (W)	1.31

Note: Absolute junction temperature limits are maintained through active thermal monitoring.

15.2 Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI–J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta–J_C (θ_{JC}). The reason for this is that θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$T_J = T_T + P \times \Psi_{JT}$

Where:

- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

15.3 Environmental Characteristics

For environmental characteristics data, see Table 32. “Environmental Ratings,” on page 57.

16. Bump Map and Descriptions

16.1 300-ball FCBGA MAP

Figure 36. 330-ball FCBGA: 9mm x 9mm, 0.4mm ball pitch (Package Top View - Ball Pads shown of far side-Die Bumps die facing down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	VSSC			SR_VLX	SR_PVSS	SR_VDDBAT5	LDO_VDD1P22	VDDOUT_1P8	VDDOUT_BT3P3	VDDOUT_BTLDO_SNS	WL_REG_ON	VDDIO_RF1	ET_LINREG_GND	ET_LINREG_CAP_OUT	ET_LINREG_VDD_V5P0	ET_LINREG_OUT	ET_SWREG_OUT	ET_SWREG_VDD_V5P0	ET_SWREG_GND	ET_SWREG_GND	ET_SWREG_GND	A
B	VSSC			SR_VLX	SR_PVSS	SR_VDDBAT5	VDDOUT_MEMLPLDO	VDDOUT_CLDO	VDDOUT_BT3P3		BT_REG_ON	VDDP_RF1	ET_LINREG_GND	ET_LINREG_GND	ET_LINREG_GND	ET_SWREG_GND	ET_SWREG_GND	ET_SWREG_GND	ET_SWREG_GND	ET_SWREG_GND	ET_SWREG_GND	B
C	BT_GPIO_4	GPIO_9		SR_VLX																ET_SWREG_GND	RVSS	C
D	BT_GPIO_5	GPIO_0		SR_VLX	SR_PVSS	SR_VDDBAT5		VDDOUT_CLDO	VDDOUT_BT3P3	LDO_VDDBAT5	RF_SW_CTRL_7	PAD_AVSS	RF_SW_CTRL_8	RF_SW_CTRL_4	ET_LINREG_GND	RF_SW_CTRL_0	ET_SWREG_GND	ET_SWREG_GND		RVSS	RVSS	D
E	CLK_REQ	GPIO_8		VDD18_UPI	SR_PVSS	SR_VDDBAT5				LDO_VDDBAT5	RF_SW_CTRL_6	RF_SW_CTRL_5	PAD_AVDD1P0	RF_SW_CTRL_9	ET_LINREG_GND	RF_SW_CTRL_2	ET_SWREG_GND	ET_SWREG_GND		RVSS	WRF_GENERAL_VDD_V5P0	E
F	SDIO_DATA_2	GPIO_2		PACKAGEOPTION_1	PACKAGEOPTION_2		STRAP_OFF_1P8			LDO_VDDBAT5	VDD18_FLL	RF_SW_CTRL_10	RF_SW_CTRL_3				RF_SW_CTRL_11	RVSS		WRF_PMU_VDD_V1P22	RVSS	F
G	SDIO_DATA_1	GPIO_3		VDDC_MEM	PACKAGEOPTION_0	PMU_VDDIOA		PMU_AVSS		VDDOUT_RF3P3		VDDC_PHY		ET_LINREG_GND			RF_SW_CTRL_12	RVSS		RVSS	WRF_RFIN_5G	G
H	SDIO_DATA_3	GPIO_5		VDDIO_SFL	GPIO_1	PMU_VDDIOP	VDDOUT_AON		WPT_REG_ON		VDDC_SUBCORE		WRF_VDD_V1P8		RVSS		RVSS	WRF_GPAIO_EXT_TSSIG		RVSS	RVSS	H
J	SDIO_CLK	GPIO_6		VDDIO	OTP_VDD1P8			VDDOUT_VDDIO			VSSC	RVSS		WRF_EXT_TSSIA			RVSS	RVSS		RVSS	WRF_PAOUT_5G	J
K	SDIO_DATA_0	BT_GPIO_3		GPIO_12	GPIO_4	WL_VDDC_AON	VDDC_SUBCORE		VDDC_SUBCORE		VDDC_PHY		RVSS		WRF_PA5G_VDD_V3P4		RVSS	RVSS		RVSS	RVSS	K
L	SDIO_CMD	GPIO_11		GPIO_10	GPIO_15	GPIO_7		WL_VDDC		VSSC		VDDC_RADIO		WRF_TX_VDD_V5P0			WRF_DIRECT_VDD_V1P22	RVSS		RVSS	WRF_PAOUT_2G	L
M	BT_GPIO_2	WL_VDDC_SFLASH		GPIO_14	GPIO_13	WL_VDDC	WL_VDDC		VSSC		VSSC		RVSS		WRF_PA2G_VDD_V3P4		RVSS	RVSS		RVSS	RVSS	M
N	BT_PCM_IN	VDDP_SFL		BT_I2S_CLK	P12			WL_VDDC_AON		WL_VDDC_AON		P2		RVSS			RVSS	RVSS		RVSS	WRF_RFIN_2G	N
P	BT_PCM_OUT	BT_UART_CTS_N		BT_I2S_DI	BT_VDDC_AAON		VSSC		VSSC		VSSC		RVSS	RVSS	P1		RF_SW_CTRL_1	P10		RVSS	RVSS	P
R	BT_PCM_SYNC	BT_UART_RTS_N		BT_I2S_DO	BT_VDDO			BT_VDDC		VSSC		RVSS	RVSS	RVSS			RVSS	P3		RVSS	BT_RFOP	R
T	BT_PCM_CLK	BT_UART_TXD		BT_I2S_WS	P16												P18	P0		RVSS	RVSS	T
U	BT_GPIO_0	BT_UART_RXD		BT_VDDCG	VSSC	BT_VDDC	BT_VDDC	BT_VDDCLDO	BT_VDDO_HIB	P17	P5	P7	P9	RVSS	RVSS	RVSS	P8	P14		RVSS	BT_13DBMOP	U
V	BT_HOST_WAKE	JTAG_SEL		VSSC	BT_VDDMEMLPLDO	BT_VDDB	PAD_ADC_REFGND	P19	P13	P4	P6	PAD_MIC_AVSS	P15	RVSS	RVSS	RVSS	P11	RVSS		RVSS	BT_20DBMOP	V
W	BT_TM1	PAD_ADC_AVDDC																		RVSS	BT_PAVDD_V3P3	W
Y	VSSC	VSSC	SFL_IO3	SFL_CLK	BT_AJTAG_TDI	BT_AJTAG_TMS	BT_AJTAG_TCK	BT_AJTAG_TDO	PAD_ADC_AVSS	PAD_MIC_AVDD	RVSS	RVSS	BT_XTAL_GND	RVSS	RVSS	RVSS	RVSS	RVSS	RVSS	RVSS	RVSS	Y
AA	VSSC	VSSC	SFL_IO0	SFL_IO2	SFL_IO1	SFL_CS	RVSS	LPO_IN	BT_XTALI	BT_XTALO	RVSS	BT_VDD_XTAL	BT_XTAL_XON	BT_XTAL_XOP	BT_XTAL_VDD_V1P22	RVSS	BT_LDOVDD_1P8	BT_LDOVDD_V1P22	RVSS	RVSS	RVSS	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

16.2 FCBGA Ball List

Table 51. Ball List

Ball Number	Ball name
A1	VSSC
A4	SR_VLX
A5	SR_PVSS
A6	SR_VDDBAT5
A7	LDO_VDD1P22
A8	VDDOUT_1P8
A9	VDDOUT_BT3P3
A10	VDDOUT_BTLDO_SNS
A11	WL_REG_ON
A12	VDDIO_RF1
A13	ET_LINREG_GND
A14	ET_LINREG_CAP_OUT
A15	ET_LINREG_VDD_V5P0
A16	ET_LINREG_OUT
A17	ET_SWREG_OUT
A18	ET_SWREG_VDD_V5P0
A19	ET_SWREG_GND
A20	ET_SWREG_GND
A21	ET_SWREG_GND
B1	VSSC
B4	SR_VLX
B5	SR_PVSS
B6	SR_VDDBAT5
B7	VDDOUT_MEMLPLDO
B8	VDDOUT_CLDO
B9	VDDOUT_BT3P3
B11	BT_REG_ON
B12	VDDP_RF1
B13	ET_LINREG_GND
B14	ET_LINREG_GND
B15	ET_LINREG_GND
B16	ET_SWREG_GND
B17	ET_SWREG_GND
B18	ET_SWREG_GND
B19	ET_SWREG_GND
B20	ET_SWREG_GND

Table 51. Ball List (Cont.)

Ball Number	Ball name
B21	ET_SWREG_GND
C1	BT_GPIO_4
C2	GPIO_9
C4	SR_VLX
C20	ET_SWREG_GND
C21	RVSS
D1	BT_GPIO_5
D2	GPIO_0
D4	SR_VLX
D5	SR_PVSS
D6	SR_VDDBAT5
D8	VDDOUT_CLDO
D9	VDDOUT_BT3P3
D10	LDO_VDDBAT5
D11	RF_SW_CTRL_7
D12	PAD_AVSS
D13	RF_SW_CTRL_8
D14	RF_SW_CTRL_4
D15	ET_LINREG_GND
D16	RF_SW_CTRL_0
D17	ET_SWREG_GND
D18	ET_SWREG_GND
D20	RVSS
D21	RVSS
E1	CLK_REQ
E2	GPIO_8
E4	VDD18_UPI
E5	SR_PVSS
E6	SR_VDDBAT5
E10	LDO_VDDBAT5
E11	RF_SW_CTRL_6
E12	RF_SW_CTRL_5
E13	PAD_AVDD1P0
E14	RF_SW_CTRL_9
E15	ET_LINREG_GND
E16	RF_SW_CTRL_2
E17	ET_SWREG_GND

Table 51. Ball List (Cont.)

Ball Number	Ball name
E18	ET_SWREG_GND
E20	RVSS
E21	WRF_GENERAL_VDD_V5P0
F1	SDIO_DATA_2
F2	GPIO_2
F4	PACKAGEOPTION_1
F5	PACKAGEOPTION_2
F7	STRAP_OFF_1P8
F10	LDO_VDDBAT5
F11	VDD18_FLL
F12	RF_SW_CTRL_10
F13	RF_SW_CTRL_3
F17	RF_SW_CTRL_11
F18	RVSS
F20	WRF_PMU_VDD_V1P22
F21	RVSS
G1	SDIO_DATA_1
G2	GPIO_3
G4	VDDC_MEM
G5	PACKAGEOPTION_0
G6	PMU_VDDIOA
G8	PMU_AVSS
G10	VDDOUT_RF3P3
G12	VDDC_PHY
G14	ET_LINREG_GND
G17	RF_SW_CTRL_12
G18	RVSS
G20	RVSS
G21	WRF_RFIN_5G
H1	SDIO_DATA_3
H2	GPIO_5
H4	VDDIO_SFL
H5	GPIO_1
H6	PMU_VDDIOP
H7	VDDOUT_AON
H9	WPT_REG_ON
H11	VDDC_SUBCORE

Table 51. Ball List (Cont.)

Ball Number	Ball name
H13	WRF_VDD_V1P8
H15	RVSS
H17	RVSS
H18	WRF_GPAIO_EXT_TSSIG
H20	RVSS
H21	RVSS
J1	SDIO_CLK
J2	GPIO_6
J4	VDDIO
J5	OTP_VDD1P8
J8	VDDOUT_VDDIO
J11	VSSC
J12	RVSS
J14	WRF_EXT_TSSIA
J17	RVSS
J18	RVSS
J20	RVSS
J21	WRF_PAOUT_5G
K1	SDIO_DATA_0
K2	BT_GPIO_3
K4	GPIO_12
K5	GPIO_4
K6	WL_VDDC_AON
K7	VDDC_SUBCORE
K9	VDDC_SUBCORE
K11	VDDC_PHY
K13	RVSS
K15	WRF_PA5G_VDD_V3P4
K17	RVSS
K18	RVSS
K20	RVSS
K21	RVSS
L1	SDIO_CMD
L2	GPIO_11
L4	GPIO_10
L5	GPIO_15
L6	GPIO_7

Table 51. Ball List (Cont.)

Ball Number	Ball name
L8	WL_VDDC
L10	VSSC
L12	VDDC_RADIO
L14	WRF_TX_VDD_V5P0
L17	WRF_DIRECT_VDD_V1P22
L18	RVSS
L20	RVSS
L21	WRF_PAOUT_2G
M1	BT_GPIO_2
M2	WL_VDDC_SFLASH
M4	GPIO_14
M5	GPIO_13
M6	WL_VDDC
M7	WL_VDDC
M9	VSSC
M11	VSSC
M13	RVSS
M15	WRF_PA2G_VDD_V3P4
M17	RVSS
M18	RVSS
M20	RVSS
M21	RVSS
N1	BT_PCM_IN
N2	VDDP_SFL
N4	BT_I2S_CLK
N5	P12
N8	WL_VDDC_AON
N10	WL_VDDC_AON
N12	P2
N14	RVSS
N17	RVSS
N18	RVSS
N20	RVSS
N21	WRF_RFIN_2G
P1	BT_PCM_OUT
P2	BT_UART_CTS_N
P4	BT_I2S_DI

Table 51. Ball List (Cont.)

Ball Number	Ball name
P5	BT_VDDC_AAON
P7	VSSC
P9	VSSC
P11	VSSC
P13	RVSS
P14	RVSS
P15	P1
P17	RF_SW_CTRL_1
P18	P10
P20	RVSS
P21	RVSS
R1	BT_PCM_SYNC
R2	BT_UART_RTS_N
R4	BT_I2S_DO
R5	BT_VDDO
R8	BT_VDDC
R10	VSSC
R12	RVSS
R13	RVSS
R14	RVSS
R17	RVSS
R18	P3
R20	RVSS
R21	BT_RFOP
T1	BT_PCM_CLK
T2	BT_UART_TXD
T4	BT_I2S_WS
T5	P16
T17	P18
T18	P0
T20	RVSS
T21	RVSS
U1	BT_GPIO_0
U2	BT_UART_RXD
U4	BT_VDDCG
U5	VSSC
U6	BT_VDDC

Table 51. Ball List (Cont.)

Ball Number	Ball name
U7	BT_VDDC
U8	BT_VDDCLDO
U9	BT_VDDO_HIB
U10	P17
U11	P5
U12	P7
U13	P9
U14	RVSS
U15	RVSS
U16	RVSS
U17	P8
U18	P14
U20	RVSS
U21	BT_13DBMOP
V1	BT_HOST_WAKE
V2	JTAG_SEL
V4	VSSC
V5	BT_VDDMEMLPLDO
V6	BT_VDDB
V7	PAD_ADC_REFGND
V8	P19
V9	P13
V10	P4
V11	P6
V12	PAD_MIC_AVSS
V13	P15
V14	RVSS
V15	RVSS
V16	RVSS
V17	P11
V18	RVSS
V20	RVSS
V21	Reserved for future use
W1	BT_TM1
W2	PAD_ADC_AVDDC
W20	RVSS
W21	BT_PAVDD_V3P3

Table 51. Ball List (Cont.)

Ball Number	Ball name
Y1	VSSC
Y2	VSSC
Y3	SFL_IO3
Y4	SFL_CLK
Y5	BT_AJTAG_TDI
Y6	BT_AJTAG_TMS
Y7	BT_AJTAG_TCK
Y8	BT_AJTAG_TDO
Y9	PAD_ADC_AVSS
Y10	PAD_MIC_AVDD
Y11	RVSS
Y12	RVSS
Y13	BT_XTAL_GND
Y14	RVSS
Y15	RVSS
Y16	RVSS
Y17	RVSS
Y18	RVSS
Y19	RVSS
Y20	RVSS
Y21	RVSS
AA1	VSSC
AA2	VSSC
AA3	SFL_IO0
AA4	SFL_IO2
AA5	SFL_IO1
AA6	SFL_CS
AA7	RVSS
AA8	LPO_IN
AA9	BT_XTALI
AA10	BT_XTALO
AA11	RVSS
AA12	BT_VDD_XTAL
AA13	BT_XTAL_XON
AA14	BT_XTAL_XOP
AA15	BT_XTAL_VDD_V1P22
AA16	RVSS

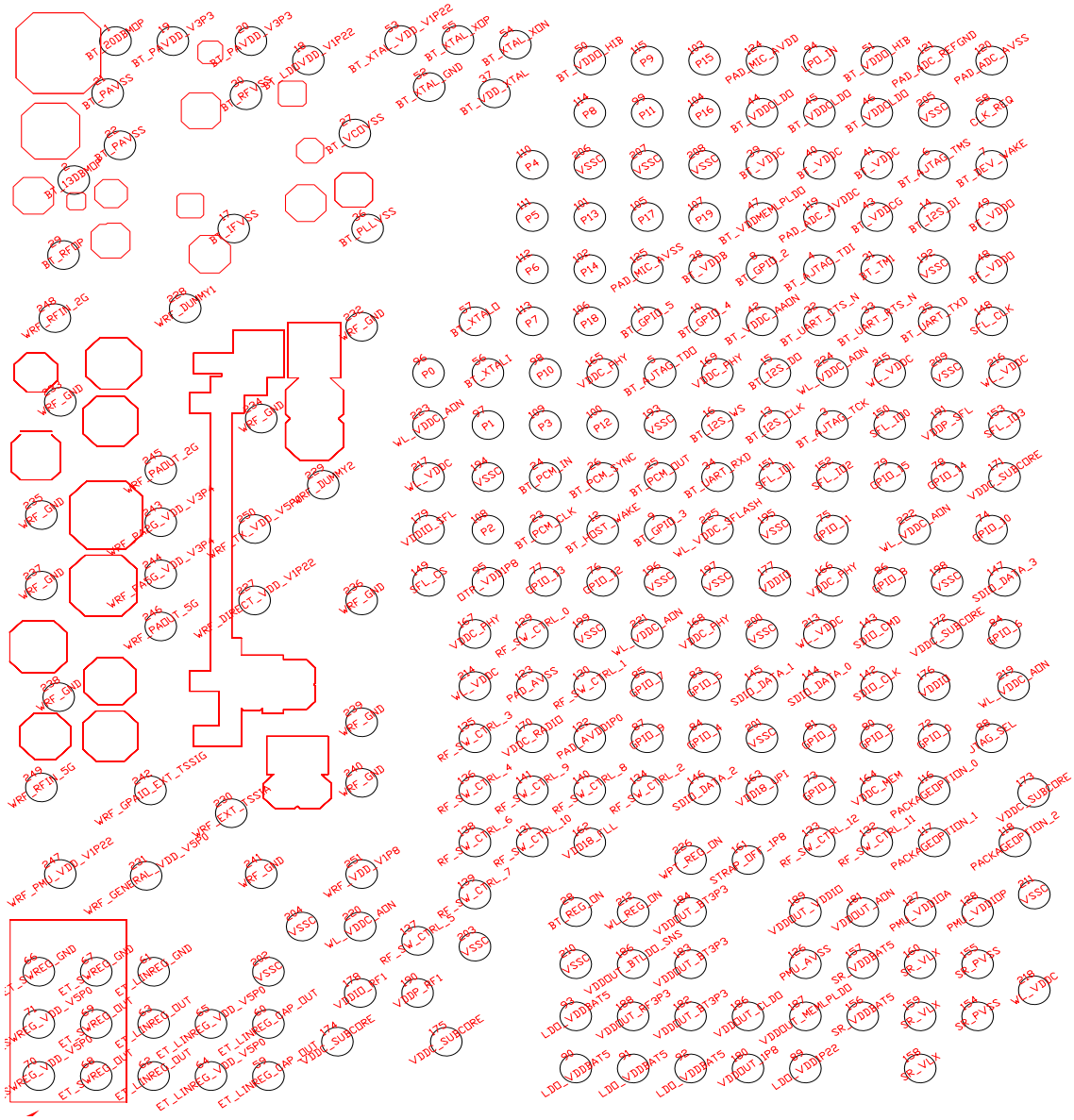
Table 51. Ball List (Cont.)

Ball Number	Ball name
AA17	BT_LDOVDD_1P8
AA18	BT_LDOVDD_V1P22
AA19	RVSS
AA20	RVSS
AA21	RVSS

16.3 251-Bump WLCSP Map

Figure 37 shows the package top view with bumps facing down.

Figure 37. 251-Bump WLCSP Map (Package Top View, Bumps Facing Down)



Note: : The bump map above shows bump 7 labeled as BT_DEV_WAKE. This will be changed to BT_GPIO_0 in subsequent revisions. BT_DEV_WAKE functionality is available on the P5 LHL GPIO that is exposed on bump number 111.

16.4 251-Bump WLCSP X-Y Coordinates

Table 52. 251-Bump WLCSP Coordinates

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
1	Reserved for future use	-1477.84	-1917.24	-1477.84	1917.24
2	BT_13DBMOP	-1623.10	-1383.87	-1623.10	1383.87
3	BT_AJTAG_TCK	1019.70	-443.97	1019.70	443.97
4	BT_AJTAG_TDI	974.70	-1042.17	974.70	1042.17
5	BT_AJTAG_TDO	419.71	-643.97	419.71	643.97
6	BT_AJTAG_TMS	1374.70	-1442.17	1374.70	1442.17
7	BT_GPIO_0	1574.69	-1442.17	1574.69	1442.17
8	BT_GPIO_2	774.70	-1042.17	774.70	1042.17
9	BT_GPIO_3	419.71	-42.18	419.71	42.18
10	BT_GPIO_4	574.70	- 842.17	574.70	842.17
11	BT_GPIO_5	374.71	-842.17	374.71	842.17
12	BT_HOST_WAKE	219.71	-42.18	219.71	42.18
13	BT_I2S_CLK	819.70	-443.97	819.70	443.97
14	BT_I2S_DI	1374.70	-1242.17	1374.70	1242.17
15	BT_I2S_DO	819.70	-643.97	819.70	643.97
16	BT_I2S_WS	619.70	-443.97	619.70	443.97
17	BT_IFVSS	-1065.73	-1197.69	-1065.73	1197.69
18	BT_LDOVDD_V1P22	-805.90	-1843.21	-805.90	1843.21
19	BT_PAVDD_V3P3	-1277.84	-1917.24	-1277.84	1917.24
20	BT_PAVDD_V3P3	-1005.89	-1917.24	-1005.89	1917.24
21	BT_PAVSS	-1505.03	-1717.24	-1505.03	1717.24
22	BT_PAVSS	-1462.14	-1517.24	-1462.14	1517.24
23	BT_PCM_CLK	19.71	-42.18	19.71	42.18
24	BT_PCM_IN	19.71	-243.97	19.71	243.97
25	BT_PCM_OUT	419.71	-243.97	419.71	243.97
26	BT_PCM_SYNC	219.71	-243.97	219.71	243.97
27	BT_VCOVSS	-643.98	-1562.44	-643.98	1562.44
28	BT_REG_ON	126.02	1425.02	126.02	-1425.02
29	BT_RFOP	-1658.81	-1096.03	-1658.81	1096.03
30	BT_RFVSS	-1023.15	-1709.39	-1023.15	1709.39
31	BT_TM1	1174.70	-1042.17	1174.70	1042.17
32	BT_UART_CTS_N	974.70	-842.17	974.70	842.17
33	BT_UART_RTS_N	1174.70	-842.17	1174.70	842.17
34	BT_UART_RXD	619.70	-243.97	619.70	243.97
35	BT_UART_TXD	1374.70	-842.17	1374.70	842.17
36	BT_PLLVSS	-599.27	-1197.69	-599.27	1197.69
37	BT_VDD_XTAL	-157.63	-1716.50	-157.63	1716.50

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
38	BT_VDDB	574.70	-1042.17	574.70	1042.17
39	BT_VDDC	774.70	-1442.17	774.70	1442.17
40	BT_VDDC	974.70	-1442.17	974.70	1442.17
41	BT_VDDC	1174.70	-1442.17	1174.70	1442.17
42	BT_VDDC_AAON	774.70	-842.17	774.70	842.17
43	BT_VDDCG	1174.70	-1242.17	1174.70	1242.17
44	BT_VDDCLDO	774.70	-1642.16	774.70	1642.16
45	BT_VDDCLDO	974.70	-1642.16	974.70	1642.16
46	BT_VDDCLDO	1174.70	-1642.16	1174.70	1642.16
47	BT_VDDMEMLPLDO	774.70	-1242.17	774.70	1242.17
48	BT_VDDO	1574.69	-1042.17	1574.69	1042.17
49	BT_VDDO	1574.69	-1242.17	1574.69	1242.17
50	BT_VDDO_HIB	174.71	-1842.16	174.71	1842.16
51	BT_VDDO_HIB	1174.70	-1842.16	1174.70	1842.16
52	BT_XTAL_GND	-384.62	-1740.62	-384.62	1740.62
53	BT_XTAL_VDD_V1P22	-484.62	-1920.99	-484.62	1920.99
54	BT_XTAL_XON	-84.63	-1902.99	-84.63	1902.99
55	BT_XTAL_XOP	-284.63	-1920.99	-284.63	1920.99
56	BT_XTALI	-180.29	-643.97	-180.29	643.97
57	BT_XTALO	-225.29	-842.17	-225.29	842.17
58	CLK_REQ	1574.69	-1642.16	1574.69	1642.16
59	ET_LINREG_CAP_OUT	-945.01	2054.04	-945.01	-2054.04
60	ET_LINREG_CAP_OUT	-945.01	1854.04	-945.01	-1854.04
61	ET_LINREG_GND	-1345.01	1654.04	-1345.01	-1654.04
62	ET_LINREG_OUT	-1345.01	2054.04	-1345.01	-2054.04
63	ET_LINREG_OUT	-1345.01	1854.04	-1345.01	-1854.04
64	ET_LINREG_VDD_V5P0	-1145.01	2054.04	-1145.01	-2054.04
65	ET_LINREG_VDD_V5P0	-1145.01	1854.04	-1145.01	-1854.04
66	ET_SWREG_GND	-1745.00	1654.04	-1745.00	-1654.04
67	ET_SWREG_GND	-1545.00	1654.04	-1545.00	-1654.04
68	ET_SWREG_OUT	-1545.00	2054.04	-1545.00	-2054.04
69	ET_SWREG_OUT	-1545.00	1854.04	-1545.00	-1854.04
70	ET_SWREG_VDD_V5P0	-1745.00	2054.04	-1745.00	-2054.04
71	ET_SWREG_VDD_V5P0	-1745.00	1854.04	-1745.00	-1854.04
72	GPIO_0	1374.70	757.81	1374.70	-757.81
73	GPIO_1	974.70	957.81	974.70	-957.81
74	GPIO_10	1574.69	-42.18	1574.69	42.18
75	GPIO_11	1019.70	-42.18	1019.70	42.18

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
76	GPIO_12	219.71	157.82	219.71	-157.82
77	GPIO_13	19.71	157.82	19.71	-157.82
78	GPIO_14	1419.70	-243.97	1419.70	243.97
79	GPIO_15	1219.70	-243.97	1219.70	243.97
80	GPIO_2	1174.70	757.81	1174.70	-757.81
81	GPIO_3	974.70	757.81	974.70	-757.81
82	GPIO_4	574.70	757.81	574.70	-757.81
83	GPIO_5	574.70	557.81	574.70	-557.81
84	GPIO_6	1619.69	357.82	1619.69	-357.82
85	GPIO_7	374.71	557.81	374.71	-557.81
86	GPIO_8	1219.70	157.82	1219.70	-157.82
87	GPIO_9	374.71	757.81	374.71	-757.81
88	JTAG_SEL	1574.69	757.81	1574.69	-757.81
89	LDO_VDD1P22	926.01	2025.01	926.01	-2025.01
90	LDO_VDDBAT5	126.02	2025.01	126.02	-2025.01
91	LDO_VDDBAT5	326.02	2025.01	326.02	-2025.01
92	LDO_VDDBAT5	526.01	2025.01	526.01	-2025.01
93	LDO_VDDBAT5	126.02	1825.01	126.02	-1825.01
94	LPO_IN	974.70	-1842.16	974.70	1842.16
95	OTP_VDD1P8	-180.29	157.82	-180.29	-157.82
96	P0	-387.41	-643.97	-387.41	643.97
97	P1	-180.29	-443.97	-180.29	443.97
98	P10	19.71	-643.97	19.71	643.97
99	P11	374.71	-1642.16	374.71	1642.16
100	P12	219.71	-443.97	219.71	443.97
101	P13	174.71	-1242.17	174.71	1242.17
102	P14	174.71	-1042.17	174.71	1042.17
103	P15	574.70	-1842.16	574.70	1842.16
104	P16	574.70	-1642.16	574.70	1642.16
105	P17	374.71	-1242.17	374.71	1242.17
106	P18	174.71	-842.17	174.71	842.17
107	P19	574.70	-1242.17	574.70	1242.17
108	P2	-180.29	-42.18	-180.29	42.18
109	P3	19.71	-443.97	19.71	443.97
110	P4	-25.29	-1442.17	-25.29	1442.17
111	P5	-25.29	-1242.17	-25.29	1242.17
112	P6	-25.29	-1042.17	-25.29	1042.17
113	P7	-25.29	-842.17	-25.29	842.17

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
114	P8	174.71	-1642.16	174.71	1642.16
115	P9	374.71	-1842.16	374.71	1842.16
116	PACKAGEOPTION_0	1374.70	957.81	1374.70	-957.81
117	PACKAGEOPTION_1	1374.70	1157.81	1374.70	-1157.81
118	PACKAGEOPTION_2	1655.94	1157.81	1655.94	-1157.81
119	PAD_ADC_AVDDC	974.70	-1242.17	974.70	1242.17
120	PAD_ADC_AVSS	1574.69	-1842.16	1574.69	1842.16
121	PAD_ADC_REFGND	1374.70	-1842.16	1374.70	1842.16
122	PAD_AVDD1P0	174.71	757.81	174.71	-757.81
123	PAD_AVSS	-25.29	557.81	-25.29	-557.81
124	PAD_MIC_AVDD	774.70	-1842.16	774.70	1842.16
125	PAD_MIC_AVSS	374.71	-1042.17	374.71	1042.17
126	PMU_AVSS	926.01	1625.02	926.01	-1625.02
127	PMU_VDDIOA	1326.01	1425.02	1326.01	-1425.02
128	PMU_VDDIOP	1526.00	1425.02	1526.00	-1425.02
129	RF_SW_CTRL_0	-25.29	357.82	-25.29	-357.82
130	RF_SW_CTRL_1	174.71	557.81	174.71	-557.81
131	RF_SW_CTRL_10	-25.29	1157.81	-25.29	-1157.81
132	RF_SW_CTRL_11	1174.70	1157.81	1174.70	-1157.81
133	RF_SW_CTRL_12	974.70	1157.81	974.70	-1157.81
134	RF_SW_CTRL_2	374.71	957.81	374.71	-957.81
135	RF_SW_CTRL_3	-225.29	757.81	-225.29	-757.81
136	RF_SW_CTRL_4	-225.29	957.81	-225.29	-957.81
137	RF_SW_CTRL_5	-425.29	1535.30	-425.29	-1535.30
138	RF_SW_CTRL_6	-225.29	1157.81	-225.29	-1157.81
139	RF_SW_CTRL_7	-225.29	1357.81	-225.29	-1357.81
140	RF_SW_CTRL_8	174.71	957.81	174.71	-957.81
141	RF_SW_CTRL_9	-25.29	957.81	-25.29	-957.81
142	SDIO_CLK	1174.70	557.81	1174.70	-557.81
143	SDIO_CMD	1174.70	357.82	1174.70	-357.82
144	SDIO_DATA_0	974.70	557.81	974.70	-557.81
145	SDIO_DATA_1	774.70	557.81	774.70	-557.81
146	SDIO_DATA_2	574.70	957.81	574.70	-957.81
147	SDIO_DATA_3	1619.69	157.82	1619.69	-157.82
148	SFL_CLK	1574.69	-842.17	1574.69	842.17
149	SFL_CS	-387.41	157.82	-387.41	-157.82
150	SFL_IO0	1219.70	-443.97	1219.70	443.97
151	SFL_IO1	819.70	-243.97	819.70	243.97

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
152	SFL_IO2	1019.70	-243.97	1019.70	243.97
153	SFL_IO3	1619.69	-443.97	1619.69	443.97
154	SR_PVSS	1526.00	1825.01	1526.00	-1825.01
155	SR_PVSS	1526.00	1625.02	1526.00	-1625.02
156	SR_VDDBAT5	1126.01	1825.01	1126.01	-1825.01
157	SR_VDDBAT5	1126.01	1625.02	1126.01	-1625.02
158	SR_VLX	1326.01	2025.01	1326.01	-2025.01
159	SR_VLX	1326.01	1825.01	1326.01	-1825.01
160	SR_VLX	1326.01	1625.02	1326.01	-1625.02
161	STRAP_OFF_1P8	726.01	1225.02	726.01	-1225.02
162	VDD18_FLL	174.71	1157.81	174.71	-1157.81
163	VDD18_UPI	774.70	957.81	774.70	-957.81
164	VDDC_MEM	1174.70	957.81	1174.70	-957.81
165	VDDC_PHY	219.71	-643.97	219.71	643.97
166	VDDC_PHY	1019.70	157.82	1019.70	-157.82
167	VDDC_PHY	-225.29	357.82	-225.29	-357.82
168	VDDC_PHY	574.70	357.82	574.70	-357.82
169	VDDC_PHY	619.70	-643.97	619.70	643.97
170	VDDC_RADIO	-25.29	757.81	-25.29	-757.81
171	VDDC_SUBCORE	1619.69	-243.97	1619.69	243.97
172	VDDC_SUBCORE	1419.70	357.82	1419.70	-357.82
173	VDDC_SUBCORE	1721.26	966.81	1721.26	-966.81
174	VDDC_SUBCORE	-704.62	1922.25	-704.62	-1922.25
175	VDDC_SUBCORE	-325.29	1922.25	-325.29	-1922.25
176	VDDIO	1374.70	557.81	1374.70	-557.81
177	VDDIO	819.70	157.82	819.70	-157.82
178	VDDIO_RF1	-625.28	1735.30	-625.28	-1735.30
179	VDDIO_SFL	-387.41	-42.18	-387.41	42.18
180	VDDOUT_1P8	726.01	2025.01	726.01	-2025.01
181	VDDOUT_AON	1126.01	1425.02	1126.01	-1425.02
182	VDDOUT_BT3P3	526.01	1825.01	526.01	-1825.01
183	VDDOUT_BT3P3	526.01	1625.02	526.01	-1625.02
184	VDDOUT_BT3P3	526.01	1425.02	526.01	-1425.02
185	VDDOUT_BTLDO_SNS	326.02	1625.02	326.02	-1625.02
186	VDDOUT_CLDO	726.01	1825.01	726.01	-1825.01
187	VDDOUT_MEMLPLDO	926.01	1825.01	926.01	-1825.01
188	VDDOUT_RF3P3	326.02	1825.01	326.02	-1825.01
189	VDDOUT_VDDIO	926.01	1425.02	926.01	-1425.02

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
190	VDDP_RF1	-425.29	1735.30	-425.29	-1735.30
191	VDDP_SFL	1419.70	-443.97	1419.70	443.97
192	VSSC	1374.70	-1042.17	1374.70	1042.17
193	VSSC	419.71	-443.97	419.71	443.97
194	VSSC	-180.29	-243.97	-180.29	243.97
195	VSSC	819.70	-42.18	819.70	42.18
196	VSSC	419.71	157.82	419.71	-157.82
197	VSSC	619.70	157.82	619.70	-157.82
198	VSSC	1419.70	157.82	1419.70	-157.82
199	VSSC	174.71	357.82	174.71	-357.82
200	VSSC	774.70	357.82	774.70	-357.82
201	VSSC	774.70	757.81	774.70	-757.81
202	VSSC	-945.01	1654.04	-945.01	-1654.04
203	VSSC	-225.29	1557.80	-225.29	-1557.80
204	VSSC	-827.46	1480.45	-827.46	-1480.45
205	VSSC	1374.70	-1642.16	1374.70	1642.16
206	VSSC	174.71	-1442.17	174.71	1442.17
207	VSSC	374.71	-1442.17	374.71	1442.17
208	VSSC	574.70	-1442.17	574.70	1442.17
209	VSSC	1419.70	-643.97	1419.70	643.97
210	VSSC	126.02	1625.02	126.02	-1625.02
211	VSSC	1723.44	1357.81	1723.44	-1357.81
212	WL_REG_ON	326.02	1425.02	326.02	-1425.02
213	WL_VDDC	974.70	357.82	974.70	-357.82
214	WL_VDDC	-225.29	557.81	-225.29	-557.81
215	WL_VDDC	1219.7	-643.97	1219.70	643.97
216	WL_VDDC	1619.69	-643.97	1619.69	643.97
217	WL_VDDC	-387.41	-243.97	-387.41	243.97
218	WL_VDDC	1723.44	1725.01	1723.44	-1725.01
219	WL_VDDC_AON	1651.19	557.81	1651.19	-557.81
220	WL_VDDC_AON	-625.28	1480.45	-625.28	-1480.45
221	WL_VDDC_AON	374.71	357.82	374.71	-357.82
222	WL_VDDC_AON	1307.20	-40.61	1307.20	40.61
223	WL_VDDC_AON	-387.41	-443.97	-387.41	443.97
224	WL_VDDC_AON	1019.70	-643.97	1019.70	643.97
225	WL_VDDC_SFLASH	619.70	-42.18	619.70	42.18
226	WPT_REG_ON	526.01	1225.02	526.01	-1225.02

Table 52. 251-Bump WLCSP Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
227	WRF_DIRECT_VDD _V1P22	-993.06	229.04	-993.06	-229.04
228	WRF_DUMMY1	-1235.09	-891.49	-1235.09	891.49
229	WRF_DUMMY2	-753.99	-214.50	-753.99	214.50
230	WRF_EXT_TSSIA	-1074.38	1045.56	-1074.38	-1045.56
231	WRF_GENERAL_VDD_V5P0	- 1371.02	1285.82	-1371.02	-1285.82
232	WRF_GND	-619.97	-820.99	-619.97	820.99
233	WRF_GND	-1670.00	-532.94	-1670.00	532.94
234	WRF_GND	-969.98	-468.62	-969.98	468.62
235	WRF_GND	-1736.00	-98.44	-1736.00	98.44
236	WRF_GND	-619.97	229.04	-619.97	-229.04
237	WRF_GND	-1736.00	172.41	-1736.00	-172.41
238	WRF_GND	-1675.58	600.28	-1675.58	-600.28
239	WRF_GND	-619.97	696.89	-619.97	-696.89
240	WRF_GND	-619.97	929.06	-619.97	-929.06
241	WRF_GND	-969.98	1279.07	-969.98	-1279.07
242	WRF_GPAIO_EXT_TSSIG	-1355.99	958.26	-1355.99	-958.26
243	WRF_PA2G_VDD_V3P4	-1319.99	-70.98	-1319.99	70.98
244	WRF_PA5G_VDD_V3P4	-1319.99	129.02	-1319.99	-129.02
245	WRF_PAOUT_2G	-1319.99	-270.98	-1319.99	270.98
246	WRF_PAOUT_5G	-1319.99	329.02	-1319.99	-329.02
247	WRF_PMU_VDD_V1P22	-1670.00	1279.07	-1670.00	-1279.07
248	WRF_RFIN_2G	-1689.08	-854.36	-1689.08	854.36
249	WRF_RFIN_5G	-1736.00	946.79	-1736.00	-946.79
250	WRF_TX_VDD_V5P0	-993.06	-44.97	-993.06	44.97
251	WRF_VDD_V1P8	-619.97	1279.07	-619.97	-1279.07

16.5 251-WLCSP Bump List

Table 53 lists the CYW43012 WLCSP 251-Bump by number.

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
1	Reserved for future use
2	BT_13DBMOP
3	BT_AJTAG_TCK
4	BT_AJTAG_TDI
5	BT_AJTAG_TDO
6	BT_AJTAG_TMS
7	BT_GPIO_0
8	BT_GPIO_2
9	BT_GPIO_3
10	BT_GPIO_4
11	BT_GPIO_5
12	BT_HOST_WAKE
13	BT_I2S_CLK
14	BT_I2S_DI
15	BT_I2S_DO
16	BT_I2S_WS
17	BT_IFVSS
18	BT_LDOVDD_V1P22
19	BT_PAVDD_V3P3
20	BT_PAVDD_V3P3
21	BT_PAVSS
22	BT_PAVSS
23	BT_PCM_CLK
24	BT_PCM_IN
25	BT_PCM_OUT
26	BT_PCM_SYNC
27	BT_VCOVSS
28	BT_REG_ON
29	BT_RFOP
30	BT_RFVSS
31	BT_TM1
32	BT_UART_CTS_N
33	BT_UART_RTS_N
34	BT_UART_RXD
35	BT_UART_TXD
36	BT_PLLVSS
37	BT_VDD_XTAL

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
38	BT_VDDB
39	BT_VDDC
40	BT_VDDC
41	BT_VDDC
42	BT_VDDC_AAON
43	BT_VDDCG
44	BT_VDDCLDO
45	BT_VDDCLDO
46	BT_VDDCLDO
47	BT_VDDMEMLPLDO
48	BT_VDDO
49	BT_VDDO
50	BT_VDDO_HIB
51	BT_VDDO_HIB
52	BT_XTAL_GND
53	BT_XTAL_VDD_V1P22
54	BT_XTAL_XON
55	BT_XTAL_XOP
56	BT_XTALI
57	BT_XTALO
58	CLK_REQ
59	ET_LINREG_CAP_OUT
60	ET_LINREG_CAP_OUT
61	ET_LINREG_GND
62	ET_LINREG_OUT
63	ET_LINREG_OUT
64	ET_LINREG_VDD_V5P0
65	ET_LINREG_VDD_V5P0
66	ET_SWREG_GND
67	ET_SWREG_GND
68	ET_SWREG_OUT
69	ET_SWREG_OUT
70	ET_SWREG_VDD_V5P0
71	ET_SWREG_VDD_V5P0
72	GPIO_0
73	GPIO_1
74	GPIO_10
75	GPIO_11

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
76	GPIO_12
77	GPIO_13
78	GPIO_14
79	GPIO_15
80	GPIO_2
81	GPIO_3
82	GPIO_4
83	GPIO_5
84	GPIO_6
85	GPIO_7
86	GPIO_8
87	GPIO_9
88	JTAG_SEL
89	LDO_VDD1P22
90	LDO_VDDBAT5
91	LDO_VDDBAT5
92	LDO_VDDBAT5
93	LDO_VDDBAT5
94	LPO_IN
95	OTP_VDD1P8
96	P0
97	P1
98	P10
99	P11
100	P12
101	P13
102	P14
103	P15
104	P16
105	P17
106	P18
107	P19
108	P2
109	P3
110	P4
111	P5
112	P6
113	P7
114	P8

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
115	P9
116	PACKAGEOPTION_0
117	PACKAGEOPTION_1
118	PACKAGEOPTION_2
119	PAD_ADC_AVDDC
120	PAD_ADC_AVSS
121	PAD_ADC_REFGND
122	PAD_AVDD1P0
123	PAD _AVSS
124	PAD_MIC_AVDD
125	PAD_MIC_AVSS
126	PMU_AVSS
127	PMU_VDDIOA
128	PMU_VDDIOP
129	RF_SW_CTRL_0
130	RF_SW_CTRL_1
131	RF_SW_CTRL_10
132	RF_SW_CTRL_11
133	RF_SW_CTRL_12
134	RF_SW_CTRL_2
135	RF_SW_CTRL_3
136	RF_SW_CTRL_4
137	RF_SW_CTRL_5
138	RF_SW_CTRL_6
139	RF_SW_CTRL_7
140	RF_SW_CTRL_8
141	RF_SW_CTRL_9
142	SDIO_CLK
143	SDIO_CMD
144	SDIO_DATA_0
145	SDIO_DATA_1
146	SDIO_DATA_2
147	SDIO_DATA_3
148	SFL_CLK
149	SFL_CS
150	SFL_IO0
151	SFL_IO1
152	SFL_IO2
153	SFL_IO3

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
154	SR_PVSS
155	SR_PVSS
156	SR_VDDBAT5
157	SR_VDDBAT5
158	SR_VLX
159	SR_VLX
160	SR_VLX
161	STRAP_OFF_1P8
162	VDD18_FLL
163	VDD18_UPI
164	VDDC_MEM
165	VDDC_PHY
166	VDDC_PHY
167	VDDC_PHY
168	VDDC_PHY
169	VDDC_PHY
170	VDDC_RADIO
171	VDDC_SUBCORE
172	VDDC_SUBCORE
173	VDDC_SUBCORE
174	VDDC_SUBCORE
175	VDDC_SUBCO E
176	VDDIO
177	VDDIO
178	VDDIO_RF1
179	VDDIO_SFL
180	VDDOUT_1P8
181	VDDOUT_AON
182	VDDOUT_BT3P3
183	VDDOUT_BT3P3
184	VDDOUT_BT3P3
185	VDDOUT_BTLDO_SNS
186	VDDOUT_CLDO
187	VDDOUT_MEMLPLDO
188	VDDOUT_RF3P3
189	VDDOUT_VDDIO
190	VDDP_RF1

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
191	VDD_SFL
192	VSSC
193	VSSC
194	VSSC
195	VSSC
196	VSSC
197	VSSC
198	VSSC
199	VSSC
200	VSSC
201	VSSC
202	VSSC
203	VSSC
204	VSSC
205	VSSC
206	VSSC
207	VSSC
208	VSSC
209	VSSC
210	VSSC
211	VSSC
212	WL_REG_ON
213	WL_VDDC
214	WL_VDDC
215	WL_VDDC
216	WL_VDDC
217	WL_VDDC
218	WL_VDDC
219	WL_VDDC_AON
220	WL_VDDC_AON
221	WL_VDDC_AON
222	WL_VDDC_AON
223	WL_VDDC_AON
224	WL_VDDC_AON
225	WL_VDDC_SFLASH
226	WPT_REG_ON
227	WRF_DIRECT_VDD_V1P22
228	WRF_DUMMY1
229	WRF_DUMMY2

Table 53. CYW43012 WLCSP Bump List by Bump Number

Bump Number	NET_Number
230	WRF_EXT_TSSIA
231	WRF_GENERAL_VDD_V5P0
232	WRF_GND
233	WRF_GND
234	WRF_GND
235	WRF_GND
236	WRF_GND
237	WRF_GND
238	WRF_GND
239	WRF_GND
240	WRF_GND
241	WRF_GND
242	WRF_GPAIO_EXT_TSSIG
243	WRF_PA2G_VDD_V3P4
244	WRF_PA5G_VDD_V3P4
245	WRF_PAOUT_2G
246	WRF_PAOUT_5G
247	WRF_PMU_VDD_V1P22
248	WRF_RFIN_2G
249	WRF_RFIN_5G
250	WRF_TX_VDD_V5P0
251	WRF_VDD_V1P8

16.6 106-ball WLBGA

Figure 38. 106-ball WLBGA: 3.76mm x 4.43mm, 0.35mm ball pitch (Package Bottom View - Balls facing up)

	1	2	3	4	5	6	7	8	9	10	
M	ET_SW_OUT	ET_LIN_OUT	ET_LIN_VDD5P0V	ET_LINREG_CAP	RF_SW_CTRL_0	VDDIO_RF1	LDO_VDDBAT5	LDO_VDD1P22	SR_VDDBAT5	SR_PVSS	M
L	ET_SW_VDD5P0V	ET_SW_GND	ET_LIN_GND		RF_SW_CTRL_3	RF_SW_CTRL_4	VDDOUT_RF3P3	VDDOUT_BT3P3	PMU_AVSS	SR_VLX	L
K	PMU_VDD_V1P22	GENERAL_VDD_V5P0	RADIO_GND	VDD_1P8	VSSC		WL_REG_ON	VDDOUT_CLDO	VDDOUT_MEMLPLDO	PMU_VDDIO	K
J	RFIN_5G	GPAIO_EXT_TSSIG		RADIO_GND	RF_SW_CTRL_2	WL_VDDC	RF_SW_CTRL_5	BT_REG_ON	WPT_REG_ON	VDDOUT_AON	J
H	RADIO_GND	PA5G_VDD_V3P4		RADIO_GND	RF_SW_CTRL_6	RF_SW_CTRL_7	GPIO_6	GPIO_5	GPIO_2	JTAG_SEL	H
G		PAOUT_5G	DIRECT_VDD_V1P22	RADIO_GND	RF_SW_CTRL_1	RF_SW_CTRL_8	GPIO_4	GPIO_1_P7	GPIO_3	SDIO_CMD_P6	G
F		PAOUT_2G	TX_VDD_V5P0	EXT_TSSIA	RF_SW_CTRL_9		VSSC	BT_PCM_SYNC	BT_HOST_WAKE	SDIO_CLK	F
E	RADIO_GND	PA2G_VDD_V3P4	RADIO_GND		BT_GPIO_4	GPIO_0		BT_PCM_CLK	WL_VDDC	SDIO_DATA_3	E
D	RFIN_2G			RADIO_GND	BT_GPIO_3	BT_GPIO_2	VSSC	BT_PCM_IN	BT_UART_CTS_N	SDIO_DATA_2	D
C	BT_13DBMOP	BT_RFOP	BT_IFVSS	BT_VCOVSS	BT_PLLVSS	BT_GPIO_5	VSSC	BT_VDDCLDO	BT_UART_TXD	SDIO_DATA_1	C
B		BT_PAVSS	BT_RFVSS		XTAL_GND	XTAL_VDD_XTAL1	BT_PCM_OUT	BT_DEV_WAKE_P5	BT_UART_RTS_N	SDIO_DATA_0	B
A		BT_20DBMOP	BT_PAVDD_V3P3	BT_LDOVDD_V1P22	XTAL_XOP	XTAL_XON	CLK_REQ	BT_UART_RXD	LPO_IN	BT_VDDO	A
	1	2	3	4	5	6	7	8	9	10	

16.7 106-Bump WLBGA X-Y Coordinates

Table 54. 106 WLBGA Coordinates

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
A2	Reserved for future use	-1319.985	-1871.00	-1319.99	1871.00
A3	BT_PAVDD_V3P3	-969.975	-1871.00	-969.98	1871.00
A4	BT_LDOVDD_V1P22	-619.965	-1871.00	-619.97	1871.00
A5	XTAL_XOP	-269.955	-1871.00	-269.96	1871.00
A6	XTAL_XON	80.055	-1871.00	80.05	1871.00
A7	CLK_REQ	430.11	-1870.91	430.11	1870.91
A8	BT_UART_RXD	780.102	-1870.91	780.10	1870.91
A9	LPO_IN	1130.094	-1870.91	1130.09	1870.91
A10	BT_VDDO	1480.086	-1870.91	1480.09	1870.91
B2	BT_PAVSS	-1319.985	-1520.99	-1319.99	1520.99
B3	BT_RFVSS	-969.975	-1520.99	-969.98	1520.99
B5	XTAL_GND	-269.955	-1520.99	-269.96	1520.99
B6	XTAL_VDD_XTAL1	80.055	-1520.99	80.05	1520.99
B7	BT_PCM_OUT	430.11	-1520.92	430.11	1520.92
B8	BT_DEV_WAKE	780.102	-1520.92	780.10	1520.92
B9	BT_UART_RTS_N	1130.094	-1520.92	1130.09	1520.92
B10	SDIO_DATA_0	1480.086	-1520.92	1480.09	1520.92
C1	BT_13DBMOP	-1669.995	-1170.98	-1670.00	1170.98
C2	BT_RFOP	-1319.985	-1170.98	-1319.99	1170.98
C3	BT_IFVSS	-969.975	-1170.98	-969.98	1170.98
C4	BT_VCOVSS	-619.965	-1170.98	-619.97	1170.98
C5	BT_PLLVSS	-269.955	-1170.98	-269.96	1170.98
C6	BT_GPIO_5	80.118	-1170.93	80.12	1170.93
C7	VSSC	430.11	-1170.93	430.11	1170.93
C8	BT_VDDCLDO	780.102	-1170.93	780.10	1170.93
C9	BT_UART_TXD	1130.094	-1170.93	1130.09	1170.93
C10	SDIO_DATA_1	1480.086	-1170.93	1480.09	1170.93
D1	RFIN_2G	-1669.842	-820.94	-1669.84	820.94
D4	RADIO_GND	-619.866	-820.94	-619.87	820.94
D5	BT_GPIO_3	-269.874	-820.94	-269.87	820.94
D6	BT_GPIO_2	80.118	-820.94	80.12	820.94
D7	VSSC	430.11	-820.94	430.11	820.94
D8	BT_PCM_IN	780.102	-820.94	780.10	820.94
D9	BT_UART_CTS_N	1130.094	-820.94	1130.09	820.94
D10	SDIO_DATA_2	1480.086	-820.94	1480.09	820.94
E1	RADIO_GND	-1669.842	-470.95	-1669.84	470.95
E2	PA2G_VDD_V3P4	-1319.85	-470.95	-1319.85	470.95

Table 54. 106 WLBGA Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
E3	RADIO_GND	-969.858	-470.95	-969.86	470.95
E5	BT_GPIO_4	-269.874	-470.95	-269.87	470.95
E6	GPIO_0	80.118	-470.95	80.12	470.95
E8	BT_PCM_CLK	780.102	-470.95	780.10	470.95
E9	WL_VDDC	1130.094	-470.95	1130.09	470.95
E10	SDIO_DATA_3	1480.086	-470.95	1480.09	470.95
F2	PAOUT_2G	-1319.85	-120.95	-1319.85	120.95
F3	TX_VDD_V5P0	-969.858	-120.95	-969.86	120.95
F4	EXT_TSSIA	-619.866	-120.95	-619.87	120.95
F5	RF_SW_CTRL_9	-269.874	-120.95	-269.87	120.95
F7	VSSC	430.11	-120.95	430.11	120.95
F8	BT_PCM_SYNC	780.102	-120.95	780.10	120.95
F9	BT_HOST_WAKE	1130.094	-120.95	1130.09	120.95
F10	SDIO_CLK	1480.086	-120.95	1480.09	120.95
G2	PAOUT_5G	-1319.85	229.04	-1319.85	-229.04
G3	DIRECT_VDD_V1P22	-969.858	229.04	-969.86	-229.04
G4	RADIO_GND	-619.866	229.04	-619.87	-229.04
G5	RF_SW_CTRL_1	-269.874	229.04	-269.87	-229.04
G6	RF_SW_CTRL_8	80.118	229.04	80.12	-229.04
G7	GPIO_4	430.11	229.04	430.11	-229.04
G8	GPIO_1_P7	780.102	229.04	780.10	-229.04
G9	GPIO_3	1130.094	229.04	1130.09	-229.04
G10	SDIO_CMD_P6	1480.086	229.04	1480.09	-229.04
H1	RADIO_GND	-1669.842	579.03	-1669.84	-579.03
H2	PA5G_VDD_V3P4	-1319.85	579.03	-1319.85	-579.03
H4	RADIO_GND	-619.866	579.03	-619.87	-579.03
H5	RF_SW_CTRL_6	-269.874	579.03	-269.87	-579.03
H6	RF_SW_CTRL_7	80.118	579.03	80.12	-579.03
H7	GPIO_6	430.11	579.03	430.11	-579.03
H8	GPIO_5	780.102	579.03	780.10	-579.03
H9	GPIO_2	1130.094	579.03	1130.09	-579.03
H10	JTAG_SEL	1480.086	579.03	1480.09	-579.03
J1	RFIN_5G	-1669.842	929.02	-1669.84	-929.02
J2	GPAIO_EXT_TSSIG	-1319.85	929.02	-1319.85	-929.02
J4	RADIO_GND	-619.866	929.02	-619.87	-929.02
J5	RF_SW_CTRL_2	-269.874	929.02	-269.87	-929.02
J6	WL_VDDC	80.118	929.02	80.12	-929.02
J7	RF_SW_CTRL_5	430.11	929.02	430.11	-929.02

Table 54. 106 WLBGA Coordinates (Cont.)

Bump Number	NET_NAME	Package Bottom View (Bumps Facing Up) Package Center (0,0)		Package Top View (Bumps Facing Down) Package Center (0,0)	
		Bump_X	Bump_Y	Bump_X	Bump_Y
J8	BT_REG_ON	780.102	929.02	780.10	-929.02
J9	WPT_REG_ON	1130.094	929.02	1130.09	-929.02
J10	VDDOUT_AON	1480.086	929.02	1480.09	-929.02
K1	PMU_VDD_V1P22	-1669.842	1279.01	-1669.84	-1279.01
K2	GENERAL_VDD_V5P0	-1319.85	1279.01	-1319.85	-1279.01
K3	RADIO_GND	-969.858	1279.01	-969.86	-1279.01
K4	VDD_1P8	-619.866	1279.01	-619.87	-1279.01
K5	VSSC	-269.874	1279.01	-269.87	-1279.01
K7	WL_REG_ON	430.11	1279.01	430.11	-1279.01
K8	VDDOUT_CLDO	780.102	1279.01	780.10	-1279.01
K9	VDDOUT_MEMLPLDO	1130.094	1279.01	1130.09	-1279.01
K10	PMU_VDDIO	1480.086	1279.01	1480.09	-1279.01
L1	ET_SW_VDD5P0V	-1669.842	1629.01	-1669.84	-1629.01
L2	ET_SW_GND	-1319.85	1629.01	-1319.85	-1629.01
L3	ET_LIN_GND	-969.858	1629.01	-969.86	-1629.01
L5	RF_SW_CTRL_3	-269.874	1629.01	-269.87	-1629.01
L6	RF_SW_CTRL_4	80.118	1629.01	80.12	-1629.01
L7	VDDOUT_RF3P3	430.11	1629.01	430.11	-1629.01
L8	VDDOUT_BT3P3	780.102	1629.01	780.10	-1629.01
L9	PMU_AVSS	1130.094	1629.01	1130.09	-1629.01
L10	SR_VLX	1480.086	1629.01	1480.09	-1629.01
M1	ET_SW_OUT	-1669.842	1979.00	-1669.84	-1979.00
M2	ET_LIN_OUT	-1319.85	1979.00	-1319.85	-1979.00
M3	ET_LIN_VDD5P0V	-969.858	1979.00	-969.86	-1979.00
M4	ET_LINREG_CAP	-619.866	1979.00	-619.87	-1979.00
M5	RF_SW_CTRL_0	-269.874	1979.00	-269.87	-1979.00
M6	VDDIO_RF1	80.118	1979.00	80.12	-1979.00
M7	LDO_VDDBAT5	430.11	1979.00	430.11	-1979.00
M8	LDO_VDD1P22	780.102	1979.00	780.10	-1979.00
M9	SR_VDDBAT5	1130.094	1979.00	1130.09	-1979.00
M10	SR_PVSS	1480.086	1979.00	1480.09	-1979.00

16.8 106- WLBGA Bump List

Table 55. CYW43012 WLBGA Bump List by Bump Number

Bump Number	NET_Number
A2	Reserved for future use
A3	BT_PAVDD_V3P3
A4	BT_LDOVDD_V1P22
A5	XTAL_XOP
A6	XTAL_XON
A7	CLK_REQ
A8	BT_UART_RXD
A9	LPO_IN
A10	BT_VDDO
B2	BT_PAVSS
B3	BT_RFVSS
B5	XTAL_GND
B6	XTAL_VDD_XTAL1
B7	BT_PCM_OUT
B8	BT_DEV_WAKE
B9	BT_UART_RTS_N
B10	SDIO_DATA_0
C1	BT_13DBMOP
C2	BT_RFOP
C3	BT_IFVSS
C4	BT_VCOVSS
C5	BT_PLLVSS
C6	BT_GPIO_5
C7	VSSC
C8	BT_VDDCLDO
C9	BT_UART_TXD
C10	SDIO_DATA_1
D1	RFIN_2G
D4	RADIO_GND
D5	BT_GPIO_3
D6	BT_GPIO_2
D7	VSSC
D8	BT_PCM_IN
D9	BT_UART_CTS_N
D10	SDIO_DATA_2
E1	RADIO_GND
E2	PA2G_VDD_V3P4
E3	RADIO_GND

Table 55. CYW43012 WLBGA Bump List by Bump Number

Bump Number	NET_Number
E5	BT_GPIO_4
E6	GPIO_0
E8	BT_PCM_CLK
E9	WL_VDDC
E10	SDIO_DATA_3
F2	PAOUT_2G
F3	TX_VDD_V5P0
F4	EXT_TSSIA
F5	RF_SW_CTRL_9
F7	VSSC
F8	BT_PCM_SYNC
F9	BT_HOST_WAKE
F10	SDIO_CLK
G2	PAOUT_5G
G3	DIRECT_VDD_V1P22
G4	RADIO_GND
G5	RF_SW_CTRL_1
G6	RF_SW_CTRL_8
G7	GPIO_4
G8	GPIO_1_P7
G9	GPIO_3
G10	SDIO_CMD_P6
H1	RADIO_GND
H2	PA5G_VDD_V3P4
H4	RADIO_GND
H5	RF_SW_CTRL_6
H6	RF_SW_CTRL_7
H7	GPIO_6
H8	GPIO_5
H9	GPIO_2
H10	JTAG_SEL
J1	RFIN_5G
J2	GPAIO_EXT_TSSIG
J4	RADIO_GND
J5	RF_SW_CTRL_2
J6	WL_VDDC
J7	RF_SW_CTRL_5
J8	BT_REG_ON
J9	WPT_REG_ON

Table 55. CYW43012 WLBGA Bump List by Bump Number

Bump Number	NET_Number
J10	VDDOUT_AON
K1	PMU_VDD_V1P22
K2	GENERAL_VDD_V5P0
K3	RADIO_GND
K4	VDD_1P8
K5	VSSC
K7	WL_REG_ON
K8	VDDOUT_CLDO
K9	VDDOUT_MEMLPLDO
K10	PMU_VDDIO
L1	ET_SW_VDD5P0V
L2	ET_SW_GND
L3	ET_LIN_GND
L5	RF_SW_CTRL_3
L6	RF_SW_CTRL_4
L7	VDDOUT_RF3P3
L8	VDDOUT_BT3P3

Table 55. CYW43012 WLBGA Bump List by Bump Number

Bump Number	NET_Number
L9	PMU_AVSS
L10	SR_VLX
M1	ET_SW_OUT
M2	ET_LIN_OUT
M3	ET_LIN_VDD5P0V
M4	ET_LINREG_CAP
M5	RF_SW_CTRL_0
M6	VDDIO_RF1
M7	LDO_VDDBAT5
M8	LDO_VDD1P22
M9	SR_VDDBAT5
M10	SR_PVSS

16.9 WLCSP/FCBGA Pin Descriptions

The signal name, type, and description of each pin in the CYW43012 is listed in Table 56. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 56. WLCSP/FCBGA Signal Descriptions

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
WLAN SDIO Interface				
SDIO_CLK	J1	142	I/O	SDIO clock.
SDIO_CMD	L1	143	I/O	SDIO command line.
SDIO_DATA_0	K1	144	I/O	SDIO data line 0.
SDIO_DATA_1	G1	145	I/O	SDIO data line 1.
SDIO_DATA_2	F1	146	I/O	SDIO data line 2.
SDIO_DATA_3	H1	147	I/O	SDIO data line 3.
WLAN GPIO Interface - Programmable GPIO Lines				
GPIO_0	D2	72	I/O	WL_HOST_WAKE
GPIO_1	H5	73	I/O	WLAN general-purpose I/Os.
GPIO_2	F2	80	I/O	
GPIO_3	G2	81	I/O	
GPIO_4	K5	82	I/O	
GPIO_5	H2	83	I/O	
GPIO_6	J2	84	I/O	
GPIO_7	L6	85	I/O	
GPIO_8	E2	86	I/O	
GPIO_9	C2	87	I/O	
GPIO_10	L4	74	I/O	
GPIO_11	L2	75	I/O	
GPIO_12	K4	76	I/O	
GPIO_13	M5	77	I/O	
GPIO_14	M4	78	I/O	
GPIO_15	L5	79	I/O	
WLAN/BT SFLASH Interface				
SFL_CLK	Y4	148	I/O	SFLASH clock.
SFL_CS	AA6	149	I/O	SFLASH chip select.
SFL_IO0	AA3	150	I/O	SFLASH data line 0.
SFL_IO1	AA5	151	I/O	SFLASH data line 1.
SFL_IO2	AA4	152	I/O	SFLASH data line 2.
SFL_IO3	Y3	153	I/O	SFLASH data line 3.
JTAG Interface				
JTAG_SEL	V2	88	I/O	JTAG select, pull-high to select the JTAG interface.
Package Option Pins				
PACKAGEOPTION_0	G5	116	I/O	Connect to VSS.

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
PACKAGEOPTION_1	F4	117	I/O	Connect to VSS.
PACKAGEOPTION_2	F5	118	I/O	Connect to VSS.
WLAN Radio				
WRF_GPAIO_EXT_TSSIG	H18	242	O	For debug purpose.
WRF_PAOUT_2G	L21	245	O	2.4 GHz WLAN PA output.
WRF_PAOUT_5G	J21	246	O	5 GHz WLAN PA output.
WRF_RFIN_2G	N21	248	I	2.4 GHz WLAN receiver.
WRF_RFIN_5G	G21	249	I	5 GHz WLAN receiver.
WRF_EXT_TSSIA	J14	230	I	TSSI input.
RF Switch Control Lines				
RF_SW_CTRL_0	D16	129	I/O	Programmable RF switch-control lines.
RF_SW_CTRL_1	P17	130	I/O	
RF_SW_CTRL_2	E16	134	I/O	
RF_SW_CTRL_3	F13	135	I/O	
RF_SW_CTRL_4	D14	136	I/O	
RF_SW_CTRL_5	E12	137	I/O	
RF_SW_CTRL_6	E11	138	I/O	
RF_SW_CTRL_7	D11	139	I/O	
RF_SW_CTRL_8	D13	140	I/O	
RF_SW_CTRL_9	E14	141	I/O	
RF_SW_CTRL_10	F12	131	I/O	
RF_SW_CTRL_11	F17	132	I/O	
RF_SW_CTRL_12	G17	133	I/O	

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
LHL/HIB Pads				
P0	T18	96	I/O	Programmable LHL/HIB pads. P5 is used as BT_DEV_WAKE. P7 is used as WL_DEV_WAKE (For DS0) Note P8 is output only.
P1	P15	97	I/O	
P2	N12	108	I/O	
P3	R18	109	I/O	
P4	V10	110	I/O	
P5	U11	111	I/O	
P6	V11	112	I/O	
P7	U12	113	I/O	
P8	U17	114	O	
P9	U13	115	I/O	
P10	P18	98	I/O	
P11	V17	99	I/O	
P12	N5	100	I/O	
P13	V9	101	I/O	
P14	U18	102	I/O	
P15	V13	103	I/O	
P16	T5	104	I/O	
P17	U10	105	I/O	
P18	T17	106	I/O	
P19	V8	107	I/O	
Clocks				
CLK_REQ	E1	58	I/O	Reference clock request.
LPO_IN	AA8	94	I	External sleep-clock input.
BT_XTALI	AA9	56	I/O	32 kHz XTAL input.
BT_XTALO	AA10	57	I/O	32 kHz XTAL output.
XTAL_XON	AA13	54	I	XTAL oscillator input.
XTAL_XOP	AA14	55	O	XTAL oscillator output.
Bluetooth Transceiver				
BT_RFOP	R21	29	I	Bluetooth dedicated LNA input.
Reserved for future use	V21	1	O	No Connect.
BT_13DBMOP	U21	2	O	Bluetooth normal-power PA output.
Bluetooth General-Purpose I/Os				
BT_HOST_WAKE	V1	12	I/O	Bluetooth host wake.
BT_GPIO_0	U1	7	I/O	Bluetooth general-purpose I/Os.
BT_GPIO_2	M1	8	I/O	
BT_GPIO_3	K2	9	I/O	
BT_GPIO_4	C1	10	I/O	
BT_GPIO_5	D1	11	I/O	

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
Bluetooth I^2S				
BT_I2S_CLK	N4	13	I/O	I2S serial clock.
BT_I2S_DI	P4	14	I/O	I2S serial data input.
BT_I2S_DO	R4	15	I/O	I2S serial data output.
BT_I2S_WS	T4	16	I/O	I2S serial word select.
Bluetooth AJTAG				
BT_AJTAG_TCK	Y7	3	I/O	Test clock.
BT_AJTAG_TDI	Y5	4	I/O	Test data in.
BT_AJTAG_TDO	Y8	5	I/O	Test data out.
BT_AJTAG_TMS	Y6	6	I/O	Test mode select.
Bluetooth PCM				
BT_PCM_CLK	T1	23	I/O	PCM clock, can be master (output) or slave (input).
BT_PCM_IN	N1	24	I/O	PCM data input.
BT_PCM_OUT	P1	25	I/O	PCM data output.
BT_PCM_SYNC	R1	26	I/O	PCM sync, can be master (output) or slave (input).
Bluetooth UART				
BT_UART_CTS_N	P2	32	I/O	UART clear-to-send.
BT_UART_RTS_N	R2	33	I/O	UART request-to-send.
BT_UART_RXD	U2	34	I/O	UART serial input.
BT_UART_TXD	T2	35	I/O	UART serial output.
Miscellaneous				
WL_REG_ON	A11	212	I	Used by the PMU to power up or power down the internal regulators used by the WLAN section.
BT_REG_ON	B11	28	I	Used by the PMU to power-up or power-down the internal regulators used by the Bluetooth section.
WPT_REG_ON	H9	226	I	Ground (Wireless Charging Power-up)
BT_TM1	W1	31	I/O	Ground (Bluetooth test mode pin)
Integrated Voltage Regulators				
ET_LINREG_CAP_OUT	A14	59, 60	O	Bypass capacitor connection for internal linear regulator inside envelope tracking module.
ET_LINREG_OUT	A16	62, 63	O	Supplies WLAN 2G and 5G PAs
ET_SWREG_OUT	A17	68, 69	O	No Connect.
SR_VDDBAT5	A6, B6, D6, E6	156, 157	I	Battery supply for CSR power-stage.
SR_VLX	A4, B4, C4, D4	158, 159, 160	O	CBUCK switching regulator output to inductor.
LDO_VDDBAT5	D10, E10, F10	90, 91, 92, 93	I	Clean battery supply for HVLDO1P8, BTLDO, and RFLDO.
LDO_VDD1P22	A7	89	I/O	Input for CLDO and output for LPLDO.

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
STRAP_OFF_1P8	F7	161	I	Sets HVLDO1P8 to off by default.
VDDOUT_1P8	A8	180	O	HVLDO1P8 output
VDDOUT_BT3P3	A9, B9, D9	182, 183, 184	O	Output of 3.3V Bluetooth LDO.
VDDOUT_BTLDO_SNS	A10	185	I	BTLDO sense pin.
VDDOUT_CLDO	B8	186	O	CLDO output.
VDDOUT_RF3P3	G10	188	O	Output of 3.3V RF LDO.
VDDOUT_VDDIO	J8	189	O	output for 1.8V power switch.
VDDOUT_AON	H7	181	O	Muxed output of MEM, core, and LP LDOs.
VDDOUT_MEMLPLDO	B7	187	O	Output of 0.7V LDO for low-power memory.
Bluetooth Power Supplies				
BT_LDOVDD_V1P8	AA17	-	-	No Connect. (Dummy ball not connected to die on FCBGA package)
BT_LDOVDD_V1P22	AA18	18	PWR	Bluetooth LDO 1.2V power supply.
BT_PAVDDV3P3	W21	19, 20	PWR	Bluetooth PA power supply.
BT_VDDO	R5	48, 49	PWR	1.8V BT VDDO supply for WLAN. Must be directly connected to PMU_VDDIO and VDDIO.
BT_VDDO_HIB	U9	50, 51	PWR	
BT_VDD_XTAL	AA12	37	PWR	Power supply to the XTAL.
BT_XTAL_VDD_V1P22	AA15	53	PWR	Power supply to the XTAL.
WLAN Power Supplies				
WRF_DIRECT_VDD_V1P22	L17	227	PWR	Input from 1.22V buck regulator driving radio cap-less LDOs inside frequency synthesizer.
WRF_PMU_VDD_V1P22	F20	247	PWR	Input from 1.22V buck regulator driving radio cap-less LDOs and transmitter blocks.
WRF_PA2G_VDD_V3P4	M15	244	PWR	Power supply pin for 2 GHz internal power amplifier (iPA version only).
WRF_GENERAL_VDD_V5P0	E21	231	PWR	VBAT input to cap-less LDOs
WRF_TX_VDD_V5P0	L14	250	PWR	Power supply pin for transmitter blocks.
WRF_PA5G_VDD_V3P4	K15	243	PWR	Power supply pin for 5 GHz internal power amplifier (iPA version only).
WRF_VDD_V1P8	H13	251	PWR	Power supply input pin for internal cap-less LDO.
Miscellaneous Power Supplies				
BT_VDDB	V6	38	PWR	Core supply for Bluetooth.
BT_VDDC	R8, U6, U7	39, 40, 41	PWR	Core supply for Bluetooth.
BT_VDDC_AAON	P5	42	PWR	Almost always-on supply.
BT_VDDCG	U4	43	PWR	Core supply for Bluetooth power-off island (for observation).
BT_VDDCLDO	U8	44, 45, 46	PWR	Core supply for Bluetooth CLDO domain.
BT_VDDMEMLPLDO	V5	47	PWR	Supply for Bluetooth memories (for sleep).
PAD_ADC_AVDDC	W2	119	PWR	1.8V supply for ADC/PGA.
PAD_AVDD1P0	E13	122	PWR	1.0V supply for PLL.

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
PAD_MIC_AVDD	Y10	124	PWR	3.3V supply for MICBIAS.
WL_VDDC	L8, M6, M7	213, 214, 215, 216, 217, 218	PWR	Core supply for WLAN.
WL_VDDC_AON	K6, N8, N10	219, 220, 221,222, 223, 224	PWR	Always-on core supply for WLAN.
WL_VDDC_SFLASH	M2	225	PWR	SFLASH core supply.
VDD18_FLL	F11	162	PWR	FLL 1.8V supply.
VDD18_UPI	E4	163	PWR	UPI 1.8V supply.
VDDC_MEM	G4	164	PWR	Memory core supply.
VDDC_PHY	G12, K11	165, 166, 167, 168, 169	PWR	PHY core supply.
VDDC_RADIO	L12	170	PWR	Radio core supply.
VDDC_SUBCORE	H11, K7, K9	171, 172, 173,174, 175	PWR	Core supply for subcore.
ET_LINREG_VDD_V5P0	A15	64, 65	PWR	Connected to VBAT
ET_SWREG_VDD_V5P0	A18	70, 71	PWR	
OTP_VDD1P8	J5	95	PWR	OTP 1.8V supply.
PMU_VDDIOA	G6	127	PWR	Analog 1.8V I/O supply.
PMU_VDDIOP	H6	128	PWR	CSR 1.8V I/O supply.
VDDIO	J4	176, 177	PWR	1.8V supply for GPIOs.
VDDIO_RF1	A12	178	PWR	I/O supply for RF switch control pads (3.3V).
VDDIO_SFL	H4	179	PWR	I/O supply for SFLASH pads (3.3V).
VDDP_RF1	B12	190	PWR	1.8V bias supply for 3.3V RF switch control pads.
VDDP_SFL	N2	191	PWR	1.8V bias supply for 3.3V SFLASH pads.
VSSC	A1, B1, J11, L10, M9, M11, P7, P9, P11, R10, U5, V4, Y1, Y2, AA1, AA2	192, 193 194, 195,196, 197, 198,199, 200, 201,202, 203, 204,205, 206, 207,208, 209, 210,211	GND	Core ground for WLAN and Bluetooth.
BT_PLLVSS	-	36	GND	Bluetooth PLL ground.
BT_VCOVSS	-	27	GND	Bluetooth VCO ground.
BT_IFVSS	-	17	GND	Bluetooth IF block ground.
BT_RFVSS	-	30	GND	Bluetooth RF ground
BT_PAVSS	-	21, 22	GND	Bluetooth PA ground.
ET_LINREG_GND	A13, B13, B14, B15, D15, E15, G14	61	GND	Ground

Table 56. WLCSP/FCBGA Signal Descriptions (Cont.)

Signal Name	FCBGA Ball Number	WLCSP Bump no	Type	Description
ET_SWREG_GND	A19, A20, A21, B16, B17, B18, B19, B20, B21, C20, D17, D18, E17, E18	66, 67	GND	Ground
SR_PVSS	A5, B5, D5, E5	154, 155	GND	Power ground.
PAD_ADC_AVSS	Y9	120	GND	ADC ground.
PAD_ADC_REFGND	V7	121	GND	ADC reference ground.
PAD_AVSS	D12	123	GND	BBPLL ground.
PAD_MIC_AVSS	V12	125	GND	MIC ground.
PMU_AVSS	G8	126	GND	Quiet ground.
WRF_GND	-	232, 233, 234, 235,236, 237, 238,239, 240, 241	GND	Radio ground
BT_XTAL_GND	Y13	52	GND	XTAL ground

16.10 WLBGA Signal Description

Table 57. WLGBA Signal Descriptions

Signal Name	WLGBA Ball Number	Type	Description
WLAN SDIO Interface			
SDIO_CLK	F10	I/O	SDIO clock
SDIO_CMD_P6	G10	I/O	SDIO command line
SDIO_DATA_0	B10	I/O	SDIO data line 0
SDIO_DATA_1	C10	I/O	SDIO data line 1
SDIO_DATA_2	D10	I/O	SDIO data line 2
SDIO_DATA_3	E10	I/O	SDIO data line 3
WLAN GPIO interface - programmable GPIO lines			
GPIO_0	E6	I/O	WL_HOST_WAKE
GPIO_1_P7	G8	I/O	WL_DEV_WAKE (For DS0)
GPIO_2	H9	I/O	
GPIO_3	G9	I/O	
GPIO_4	G7	I/O	
GPIO_5	H8	I/O	
GPIO_6	H7	I/O	
JTAG interface			
JTAG_SEL	H10	I/O	JTAG select, pull-high to select the JTAG interface.
WLAN Radio			
GPAIO_EXT_TSSIG	J2	O	For debug purpose
PAOUT_2G	F2	O	2.4 GHz WLAN PA output.
PAOUT_5G	G2	O	5 GHz WLAN PA output.
RFIN_2G	D1	I	2.4 GHz WLAN receiver.
RFIN_5G	J1	I	5 GHz WLAN receiver.
EXT_TSSIA	F4	I	TSSI input
RF Switch Control Lines			
RF_SW_CTRL_0	M5	I/O	Programmable RF switch-control lines
RF_SW_CTRL_1	G5	I/O	
RF_SW_CTRL_2	J5	I/O	
RF_SW_CTRL_3	L5	I/O	
RF_SW_CTRL_4	L6	I/O	
RF_SW_CTRL_5	J7	I/O	
RF_SW_CTRL_6	H5	I/O	
RF_SW_CTRL_7	H6	I/O	
RF_SW_CTRL_8	G6	I/O	
RF_SW_CTRL_9	F5	I/O	
Clocks			
CLK_REQ	A7	I/O	Reference clock request.

Table 57. WLGBA Signal Descriptions (Cont.)

Signal Name	WLGBA Ball Number	Type	Description
LPO_IN	A9	I	External sleep-clock input.
XTAL_XON	A6	I	XTAL oscillator input.
XTAL_XOP	A5	O	XTAL oscillator output.
Bluetooth Transceiver			
Reserved for future use	A2	O	No connect
BT_13DBMOP	C1	O	Bluetooth normal-power PA output.
BT_RFOP	C2	I	Bluetooth dedicated LNA input.
Bluetooth General-Purpose I/Os			
BT_HOST_WAKE	F9	I/O	Bluetooth host wake
BT_DEV_WAKE	B8	I/O	Bluetooth device wake
BT_GPIO_2	D6	I/O	Bluetooth general purpose I/Os
BT_GPIO_3	D5	I/O	
BT_GPIO_4	E5	I/O	
BT_GPIO_5	C6	I/O	
Bluetooth PCM			
BT_PCM_CLK	E8	I/O	PCM clock, can be master (output) or slave (input).
BT_PCM_IN	D8	I/O	PCM data input.
BT_PCM_OUT	B7	I/O	PCM data output.
BT_PCM_SYNC	F8	I/O	PCM sync, can be master (output) or slave (input).
Bluetooth UART			
BT_UART_CTS_N	D9	I/O	UART clear-to-send.
BT_UART_RTS_N	B9	I/O	UART request-to-send.
BT_UART_RXD	A8	I/O	UART serial input.
BT_UART_TXD	C9	I/O	UART serial output.
Miscellaneous			
BT_REG_ON	J8	I	Used by the PMU to power-up or power-down the internal regulators used by the Bluetooth section.
WPT_REG_ON	J9	I	Ground (Wireless Charging Power-up)
WL_REG_ON	K7	I	Used by the PMU to power up or power down the internal regulators used by the WLAN section.
Integrated Voltage Regulators			
ET_LINREG_CAP	M4	O	Bypass capacitor connection for internal linear regulator inside envelope tracking module.
ET_SW_OUT	M1	O	No Connect.
ET_LIN_OUT	M2	O	Supplies WLAN 2G and 5G PAs
SR_VDDBAT5	M9	I	Battery supply for CSR power-stage.
SR_VLX	L10	O	CBUCK switching regulator output to inductor.
LDO_VDDBAT5	M7	I	Clean battery supply for HVLDO1P8,BTLDO, and RFLDO.
LDO_VDD1P22	M8	I/O	Input for CLDO and output for LPLDO.

Table 57. WLGBA Signal Descriptions (Cont.)

Signal Name	WLGBA Ball Number	Type	Description
VDDOUT_BT3P3	L8	O	Output of 3.3V Bluetooth LDO.
VDDOUT_CLDO	K8	O	CLDO output
VDDOUT_RF3P3	L7	O	Output of 3.3V RF LDO.
VDDOUT_AON	J10	O	Muxed output of MEM, core, and LP LDOs.
VDDOUT_MEMLPLDO	K9	O	Output of 0.7V LDO for low-power memory.
Bluetooth Power Supplies			
BT_LDOVDD_V1P22	A4	PWR	Bluetooth LDO 1.2V power supply.
BT_PAVDD_V3P3	A3	PWR	Bluetooth PA power supply.
BT_VDDO	A10	PWR	1.8V BT VDDO supply for WLAN. Must be directly connected to PMU_VDDIO and VDDIO on the PCB.
XTAL_VDD_XTAL1	B6	PWR	Power supply to the XTAL.
WLAN Power Supplies			
DIRECT_VDD_V1P22	G3	PWR	Input from 1.22V buck regulator driving radio cap-less LDOs inside frequency synthesizer.
PMU_VDD_V1P22	K1	PWR	Input from 1.22V buck regulator driving radio cap-less LDOs and transmitter blocks.
PA2G_VDD_V3P4	E2	PWR	Power supply pin for 2 GHz internal power amplifier (iPA version only).
GENERAL_VDD_V5P0	K2	PWR	VBAT input to cap-less LDOs.
TX_VDD_V5P0	F3	PWR	Power supply pin for transmitter blocks.
PA5G_VDD_V3P4	H2	PWR	Power supply pin for 5 GHz internal power amplifier (iPA version only).
VDD_1P8	K4	PWR	Power supply input pin for internal cap-less LDO.
Miscellaneous Power Supplies			
BT_VDDCLDO	C8	PWR	Core supply for Bluetooth CLDO domain.
WL_VDDC	E9, J6	PWR	Core supply for WLAN.
ET_SW_VDD5P0V	L1	PWR	Envelope tracking VBAT connection.
ET_LIN_VDD5P0V	M3	PWR	Envelope tracking VBAT connection.
PMU_VDDIO	K10	PWR	Core switching regulator I/O, analog I/O and GPIO 1.8V supply
VDDIO_RF1	M6	PWR	I/O supply for RF switch control pads (3.3V).
VSSC	C7, D7, F7, K5	GND	Core ground for WLAN and Bluetooth
BT_PLLVSS	C5	GND	Bluetooth PLL ground
BT_IFVSS	C3	GND	Bluetooth IF block ground.
BT_RFVSS	B3	GND	Bluetooth RF ground
BT_PAVSS	B2	GND	Bluetooth PA ground
BT_VCOVSS	C4	GND	Bluetooth VCO ground
ET_SW_GND	L2	GND	Envelope tracking ground.
ET_LIN_GND	L3	GND	Envelope tracking ground.
SR_PVSS	M10	GND	Power ground
PMU_AVSS	L9	GND	Quiet ground

Table 57. WLGBA Signal Descriptions (Cont.)

Signal Name	WLGBA Ball Number	Type	Description
XTAL_GND	B5	GND	XTAL ground
RADIO_GND	D4, E1, E3, G4, H1, H4, J4, K3	GND	Radio ground

16.11 Strapping Options

This section describes strapping options. The pins are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 58. CYW43012 Strapping Options

Signal Name	FCBGA Ball Number	WLCSP Bump Number	WLBGA Ball Number	STRAP Description	Note
JTAG_SEL	V2	88	H10	1 (i.e. pull up to VDDIO) to enable Wi-Fi side JTAG	Wi-Fi JTAG interface is intended to be used by Cypress's internal teams only
BT_GPIO_2	M1	8	D6	1 (i.e. pull up to VDDIO) to enable shared flash usage on the BT side	Refer section 8.4 for details - presence of flash is optional for CYW43012
STRAP_OFF_1P8	F7	161	N/A	1 (i.e. pull up to VDDIO) to disable HVLDO1P8	HVLDO1P8 is currently not supported in FCBGA/WLCSP - see figure 4 for details HVLDO1P8 and this strap are not available in WLBGA

16.12 Multiplexed Bluetooth GPIO Signals

The Bluetooth GPIO pins (BT_GPIO_0 to BT_GPIO_7) are multiplexed pins and can be programmed to be used as GPIOs or for other Bluetooth interface signals such as I2S. The specific function for a given BT_GPIO_X pin is chosen by programming the Pad Function Control register for that specific pin. Table 54 and Table 55 on page 131 shows the possible options for each BT_GPIO_X pin. Note that each BT_GPIO_X pin's Pad Function Control register setting is independent (BT_GPIO_5 can be set to pad function 7 at the same time that BT_GPIO_3 is set to pad function 0). When the Pad Function Control register is set to 0, the BT_GPIOs do not have specific functions assigned to them and behave as generic GPIOs. The A_GPIO_X pins described below are multiplexed behind the CYW43012's PCM and I2S interface pins.

Table 59. Pad Function Control Register Settings

Pad Names	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BT_UART_CTS_N	UART_CTS_N(I)	SPI_SCK (IO)	–	–	–	UART2_RTS_N(O)	–	–	–	–	–	–	–	–	–	–
BT_UART_RTS_N	UART_RTS_N(O)	SPI_CSN (IO)	–	–	–	UART2_CTS_N(I)	–	–	–	–	–	–	–	–	–	–
BT_UART_RXD	UART_RXD(I)	SPI_MOSI (IO)	–	–	IIC_SDA (IO)	UART2_RXD(I)	–	–	–	–	–	–	–	–	–	–
BT_UART_TXD	UART_TXD(O)	SPI_MISO (IO)	–	–	IIC_SCL (IO)	UART2_TXD(O)	–	–	–	–	–	–	–	–	–	–
BT_PCM_IN	A_GPIO[3] (IO)	PCM_IN(I)	–	–	–		–	–	–	–	–	–	IIC_SCL (IO)	–	–	–
BT_PCM_OUT	A_GPIO[2] (IO)	PCM_OUT (O)	–	–	–	I2S_MSD(O)	–	–	–	–	–	–	IIC_SDA (IO)	–	–	–
BT_PCM_SYNC	A_GPIO[1] (IO)	PCM_SYNC(IO)	–	–	–	I2S_WS(IO)	–	–	–	–	–	–	–	–	–	–
BT_PCM_CLK	A_GPIO[0] (IO)	PCM_CLK (IO)	–	–	–	I2S_SCK(IO)	–	–	–	–	–	–	–	–	–	–
BT_I2S_DO	A_GPIO[5] (IO)	PCM_OUT (O)	–	–	I2S_SSD(O)	I2S_MSD(O)	–	–	–	–	–	UART2_RTS_N (O)	IIC_SCL (IO)	–	–	–
BT_I2S_DI	A_GPIO[6] (IO)	PCM_IN(I)	–	–	I2S_SDI (I)	–	–	–	–	–	–	UART2_CTS_N (I)	–	IIC_SDA (IO)	–	–
BT_I2S_WS	GPIO[7] (IO)	PCM_SYNC(IO)	–	GPIO[7] (I)	–	I2S_WS(IO)	–	–	–	–	–	UART2_RXD (I)	–	–	–	–
BT_I2S_CLK	GPIO[6] (IO)	PCM CLK(IO)	–	GPIO[6] (I)	–	I2S_SCK(IO)	–	–	–	–	–	UART2_TXD (O)	–	–	–	–
BT_GPIO_5	GPIO[5] (IO)	–	–	I2S_SCK(IO)	–	–	–	–	–	–	–	UART2_CTS_N (I)	–	–	–	IIC_SCL (IO)
BT_GPIO_4	GPIO[4] (IO)	–	–	I2S_MSD(O)	I2S_SSD(O)	–	–	–	–	–	–	UART2_RTS_N (O)	–	–	–	IIC_SDA (IO)
BT_GPIO_3	GPIO[3] (IO)	–	–	I2S_WS (IO)	–	–	–	–	–	–	–	–	–	–	–	–
BT_GPIO_2	GPIO[2] (IO)	–	–	–	I2S_SDI (I)	–	–	–	–	–	–	–	–	–	–	PDM_2p4M_CLK
BT_HOST_WAKE	GPIO[1] (IO)	–	–	–	–	PDM_CH2(I)	–	–	–	–	–	–	–	–	–	–
BT_GPIO_0	GPIO[0] (IO)	–	–	–	–	PDM_CH1(I)	–	–	–	–	–	–	–	–	–	–

Table 59. Pad Function Control Register Settings (Cont.)

Pad Names	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BT_AJTAG_TDI	–	–	I2S SDI(I)	PCM_IN (I)	–	GPIO[5](IO)	GPIO[6] (IO)	–	–	–	–	–	A_GPIO [4] (IO)	A_GPIO[5] (IO)	A_GPIO[6] (IO)	IIC_SDA (IO)
BT_AJTAG_ TDO	–	I2S MSD (O)	I2S SSD(O)	PCM_ OUT(O)	–	GPIO[5](IO)	GPIO[6] (IO)	–	–	–	–	–	A_GPIO [4] (IO)	A_GPIO [5] (IO)	A_GPIO[6] (IO)	IIC_SCL (IO)
BT_AJTAG_ TMS	–	I2S WS (IO)	–	–	–	GPIO[5](IO)	GPIO[6] (IO)	–	–	–	–	–	A_GPIO [4] (IO)	A_GPIO [5] (IO)	A_GPIO[6] (IO)	A_GPOUT [7](O)
BT_AJTAG_TCK	–	I2S_SCK (IO)	–	–	–	GPIO[5](IO)	GPIO[6] (IO)	–	–	–	–	–	A_GPIO [4] (IO)	A_GPIO [5] (IO)	A_GPIO[6] (IO)	–
CLK_REQ	–	–	–	–	–	–	–	A_GPIO[7] (IO)	–	–	–	–	–	–	–	–

Table 60. BT_GPIO_X Drive Strength Control (@0.4V from rail, VDDO=1.8V)

Drive	sel1	sel2	sel0
2mA	0	0	0
4mA	0	0	1
6mA	0	1	0
8mA	1	0	1
10mA	1	0	0
12mA	1	0	1
14mA	1	0	0
16mA	1	0	1

Table 61. Peripherals Multiplexed On Any LHL/HIB Pad (P0 to P19 except on P5, P6 and P7)

Supported peripherals	UART	UART2 (pUART)	Single mode SPI	IIC	PDM	PWM	GPIO
Signals	UART_CTS_N (I)	UART2_CTS_N (I)	SPI_SCK(IO)	IIC_SCL(IO)	PDM_CH1(I)	PWM0(O)	
	UART_RTS_N (O)	UART2_RTS_N (O)	SPI_CSN(IO)	IIC_SDA(IO)	PDM_CH2(I)	PWM1(O)	
	UART_RXD(I)	UART2_RXD(I)	SPI_MOSI(IO)		PDM_2p4M_CLK	PWM2(O)	
	UART_TXD(O)	UART2_TXD(O)	SPI_MISO(IO)			PWM3(O)	
						PWM4(O)	
						PWM5(O)	

Table 62. LHL Pad Drive Strength Control (@0.4V from rail, VDDO=1.8V)

Drive	sel2_1p8v	sel1_1p8v	sel0_1p8v
2mA	0	0	0
4mA	0	0	1
6mA	0	1	0
8mA	1	0	1
10mA	1	0	0
12mA	1	0	1
14mA	1	0	0
16mA	1	0	1

16.13 I/O States

The following notations are used in Table 63:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up (40 kOhm resistance)
- PD = Pulled down (40 kOhm resistance)
- NoPull = Neither pulled up nor pulled down

Table 63. I/O States

Name	I/O	Keeper[a]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[b] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset;Before SW Download(BT_REG_ON High;WL_REG_ON High)
WL_REG_ON	I	N	Input; PD (pull-down auto disabled)	Input; PD (pull-down auto disabled)	Input; PD (of 50K)	Input;PD (of 50K)
BT_REG_ON	I	N	Input; PD (pull-down auto disabled)	Input; PD (pull-down auto disabled)	Input; PD (of 50K)	Input;PD (of 50K)
CLK_REQ	I/O	Y	Input; PD (of 50K)Open drain or push-pull (programmable). Active high.	Input; PD (of 50K)Open drain or push-pull (programmable). Active high.	High-Z, NoPull	Open drain. Active high
BT_HOST_WAKE	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU
BT_GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD
BT_GPIO_2, BT_GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD
BT_GPIO_4, BT_GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU
BT_UART_CTS_N	I	Y	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; PU
BT_UART_RTS_N	O	Y	Output; NoPull	Output; NoPull	High-Z, NoPull	Input; PU
BT_UART_RXD	I	Y	Input; PU	Input; PU	High-Z, NoPull	Input; PU
BT_UART_TXD	O	Y	Output;NoPull	Output;NoPull	High-Z, NoPull	Input; PU
SDIO_DATA[0:3]	I/O	N	Input/Output; PU (SDIO Mode)	Input/Output; PU (SDIO Mode)	High-Z, NoPull	Input; PU (SDIO Mode)

Table 63. I/O States (Cont.)

Name	I/O	Keeper[a]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[b] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset;Before SW Download(BT_REG_ON High;WL_REG_ON High)
SDIO_CMD	I/O	N	Input/Output; PU (SDIO Mode)	Input/Output; PU (SDIO Mode)	High-Z, NoPulL	Input; PU (SDIO Mode)
SDIO_CLK	I	N	Input; NoPull	Input; NoPull	High-Z, NoPull	Input; noPull
BT_PCM_CLK	I/O	Y	Input; NoPull[c]	Input; NoPull[c]	High-Z, NoPull	Input, PD
BT_PCM_IN	I/O	Y	Input; NoPull[c]	Input; NoPull[c]	High-Z, NoPull	Input, PD
BT_PCM_OUT	I/O	Y	Input; NoPull[c]	Input; NoPull[c]	High-Z, NoPull	Input, PD
BT_PCM_SYNC	I/O	Y	Input; NoPull [c]	Input; NoPull [c]	High-Z, NoPull	Input, PD
BT_I2S_WS	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	Input, PD
BT_I2S_CLK	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	Input, PD
BT_I2S_DI	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	Input, PD
BT_I2S_DO	I/O	Y	Input; NoPull[d]	Input; NoPull[d]	High-Z, NoPull	Input, PD
GPIO_0	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU,PD,NoPull (programmable [Default: PD])	High-Z, NoPull	Input; PD
GPIO_1	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD,NoPull(program-mable[Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_2	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD,NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: PD])	Input/Output; PU, PD,NoPull (programmable [Default: PD])	High-Z, NoPull	Input; NoPull
GPIO_4	I/O	Y	Input/Output; PU, PD,NoPull (programmable [Default: NoPull])	Input/Output; PU,PD,NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_5	I/O	Y	Input/Output; PU, PD,NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; NoPull
GPIO_6	I/O	Y	Input/Output; PU, PD,NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; NoPull
GPIO_7	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull(program-mable[Default: NoPull])	High-Z, NoPull	Input; NoPull

Table 63. I/O States (Cont.)

Name	I/O	Keeper[a]	Active Mode	Low Power State/Sleep (All Power Present)	Power-down[b] (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset;Before SW Download(BT_REG_ON High;WL_REG_ON High)
GPIO_8	I/O	Y	Input/Output; PU, PD,NoPull (programmable [Default: PD])[e]	Input/Output; PU, PD, NoPull (programmable [Default: PD])[e]	High-Z, NoPull	Input; NoPull
GPIO_9	I/O	Y	Input/Output; PU, PD,NoPull (programmable [Default: PD])	Input/Output; PU, PD, NoPull (programmable [Default: PD])	High-Z, NoPull	Input; NoPull
GPIO_10	I/O	Y	Input/Output;PU, PD,NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_13	I/O	Y	Input/Output;PU, PD, NoPull (programmable [Default: NoPull])	Input/Output;PU, PD,NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_14	I/O	Y	Input/Output;PU, PD,NoPull (programmable [Default: NoPull])	Input/Output;PU, PD,NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
GPIO_15	I/O	Y	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	Input/Output; PU, PD, NoPull (programmable [Default: NoPull])	High-Z, NoPull	Input; NoPull
RF [12:0]	I/O	Y	Output; NoPull	Output; NoPull	High-Z	Output; NoPull

a. Keeper column: N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in power-down state. If there is nand there is NoPull, then the pad should be driven to prevent leakage due to floating pad (SDIO_CLK, for example).

b. In the power-down state (xx_REG_ON=0): High-Z; NoPull => the pad is disabled because power is not supplied.

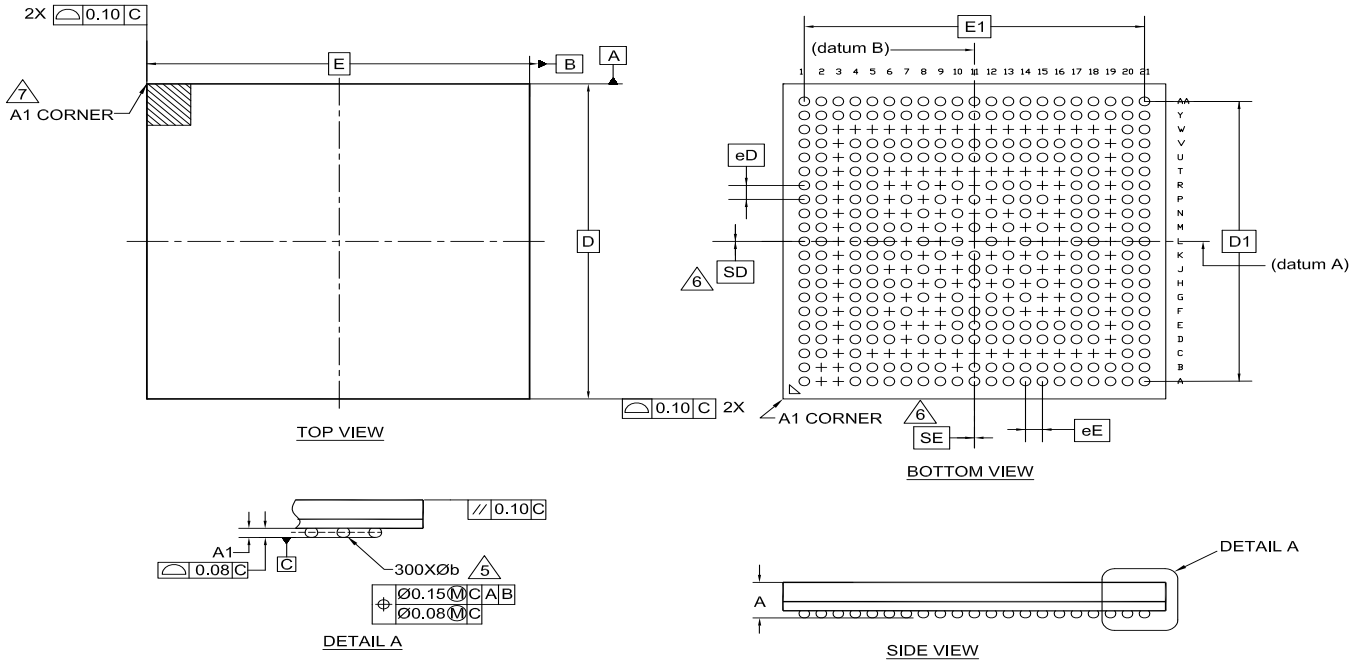
c. Depending on whether the PCM interface is enabled and the configuration of PCM is in master or slave mode, it can be either output or input

d. Depending on whether the I2S interface is enabled and the configuration of I2S is in master or slave mode, it can be either output or input. NoPull when in SDIO mode.

17. Mechanical Information

17.1 FCBGA

Figure 39. FCBGA Package Mechanical Information



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.850	0.950	1.050
A1	0.150	0.180	0.210
D		9.00 BSC	
E		9.00 BSC	
D1		8.00 BSC	
E1		8.00 BSC	
MD		21	
ME		21	
N		300	
∅ b	0.20	0.25	0.30
eD		0.40 BSC	
eE		0.40 BSC	
SD		0	
SE		0	

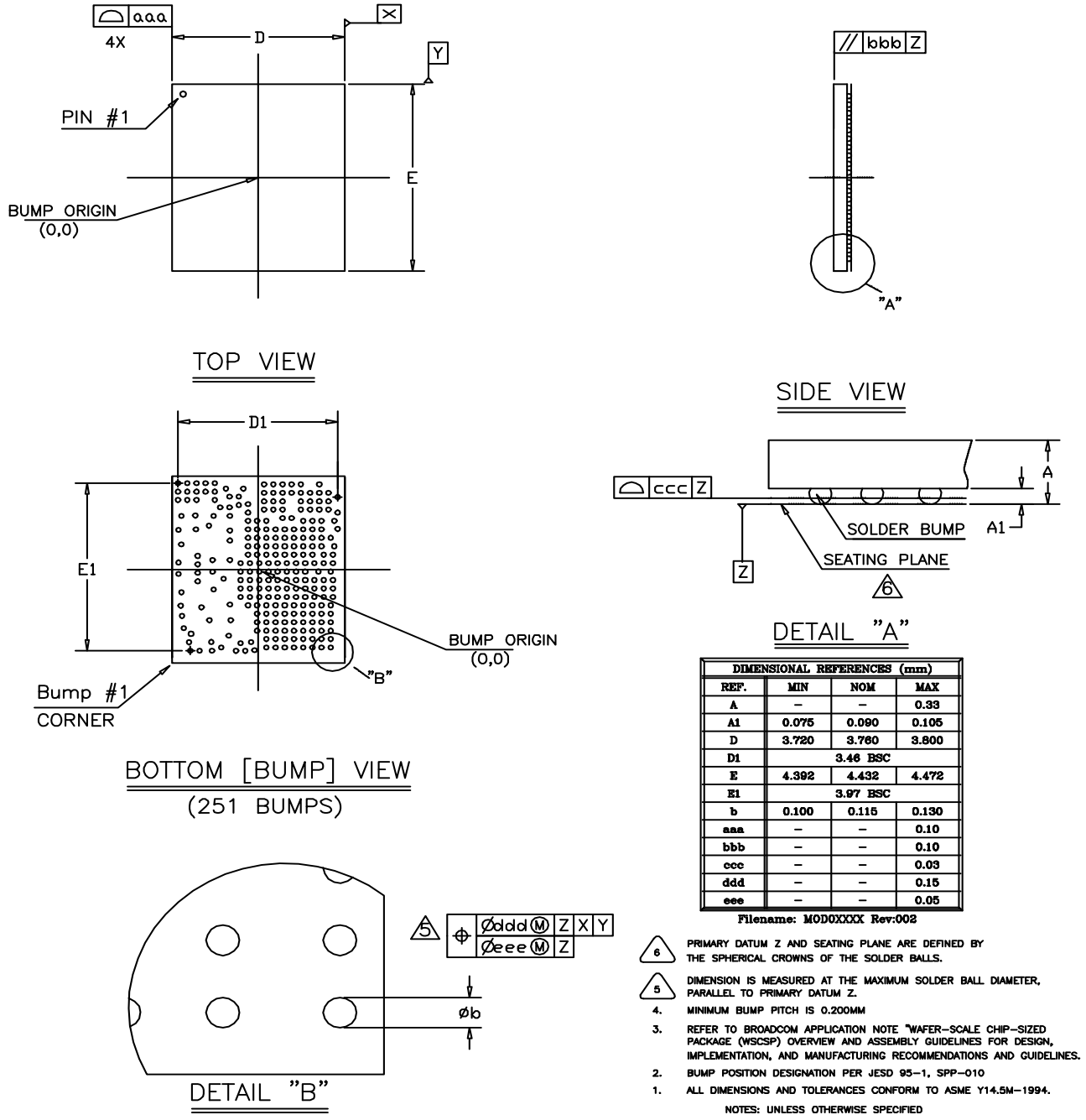
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

17.2 WLCSP

Figure 40 shows the mechanical information for the WLCSP package.

Figure 40. WLCSP Package Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.33
A1	0.075	0.090	0.105
D	3.720	3.760	3.800
D1		3.46 BSC	
E	4.392	4.432	4.472
E1		3.97 BSC	
b	0.100	0.115	0.130
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD0XXXX Rev:002

6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
4. MINIMUM BUMP PITCH IS 0.200MM
3. REFER TO BROADCOM APPLICATION NOTE "WAFER–SCALE CHIP–SIZED PACKAGE (WSCSP) OVERVIEW AND ASSEMBLY GUIDELINES FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.
2. BUMP POSITION DESIGNATION PER JESD 95–1, SPP–010
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

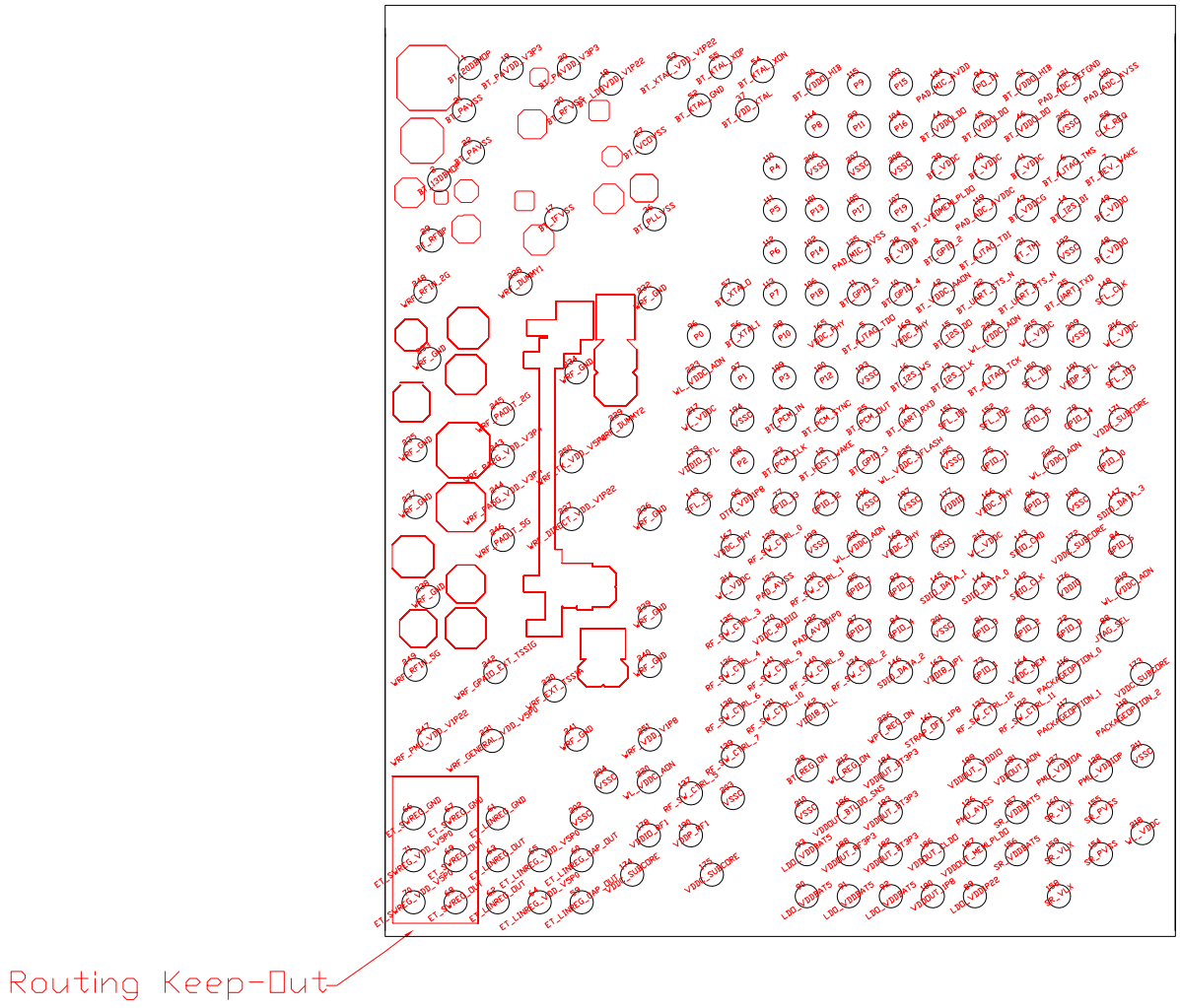
NOTES: UNLESS OTHERWISE SPECIFIED

Figure 41 shows the keep-out areas for the WLCSP package.

Note:

- No top-layer metal is allowed in the keep-out areas.
- A DXF file containing WLCSP keep-outs can be imported into a layout program. Contact your Cypress FAE for more information.

Figure 41. Keep-Out Areas (Package Top View, Bumps Facing Down)

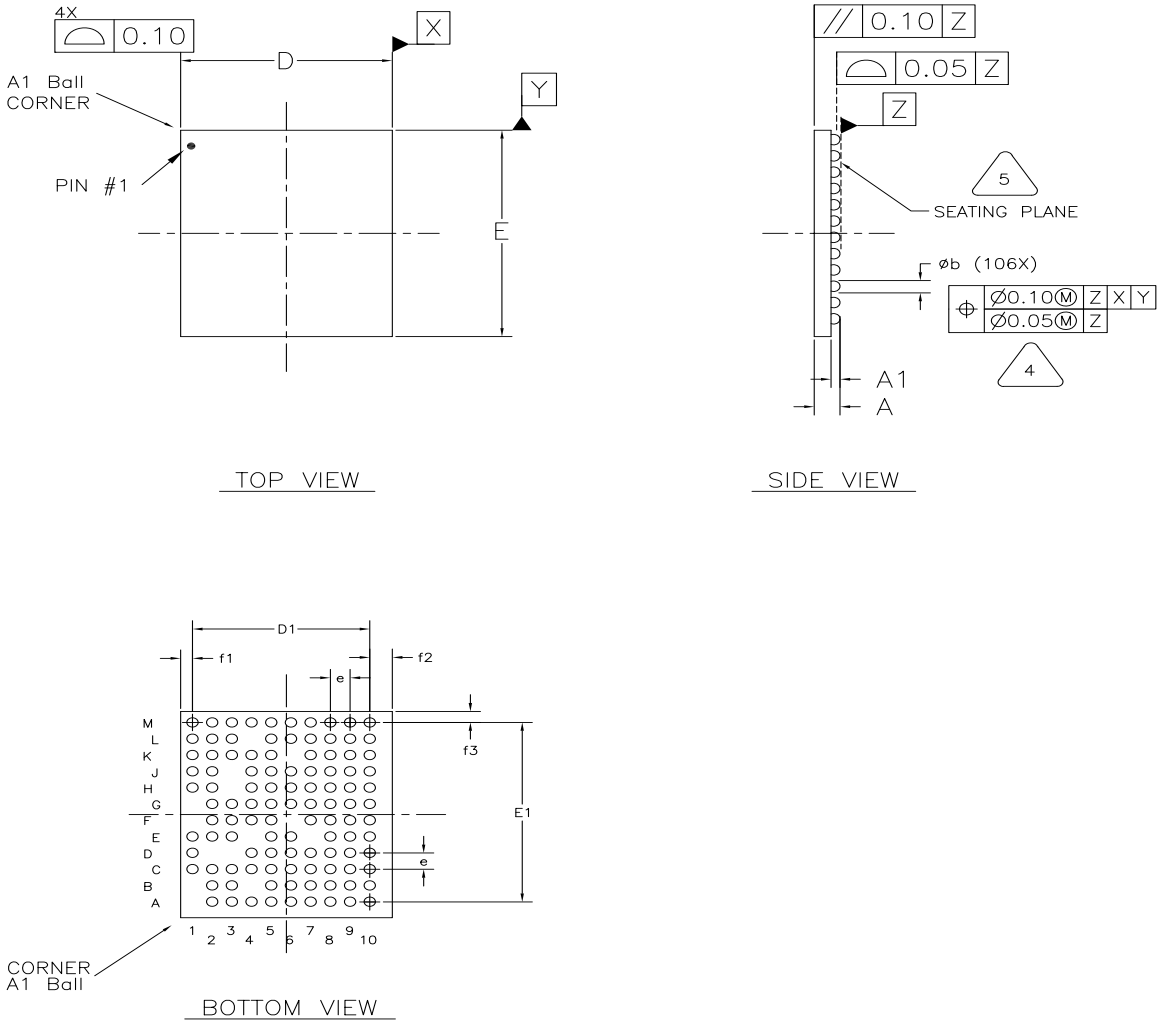


Note: The bump map above shows bump 7 labeled as BT_DEV_WAKE. This will be changed to BT_GPIO_0 in subsequent revisions. BT_DEV_WAKE functionality is available on the P5 LHL GPIO that is exposed on bump number 111.

17.3 WLBGA

Figure 42 shows the mechanical information for the WLBGA package.

Figure 42. 106 BALL WLBGA 3.76X4.43X0.53 MM



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.53
A1	0.14	0.17	0.20
D	3.72	3.76	3.80
E	4.39	4.43	4.47
D1	3.15 REF		
E1	3.85 REF		
N	106		
∅ b	0.18	0.23	0.28
e	0.35 BSC		
f1	0.21 BSC		
f2	0.40 BSC		
f3	0.23 BSC		

NOTES:

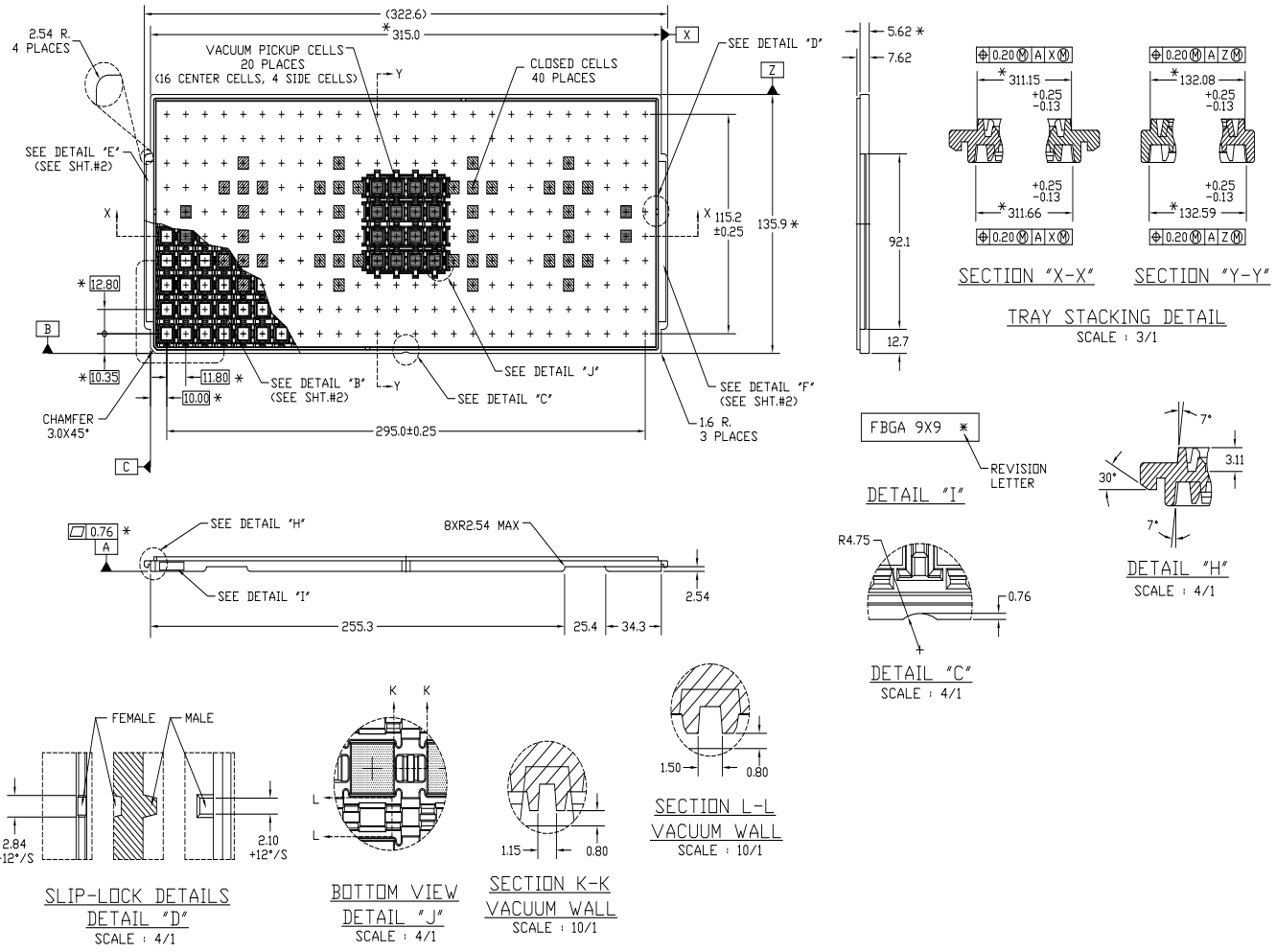
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.
3. THE BASIC SOLDER BALL PITCH IS 0.35mm
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDEL

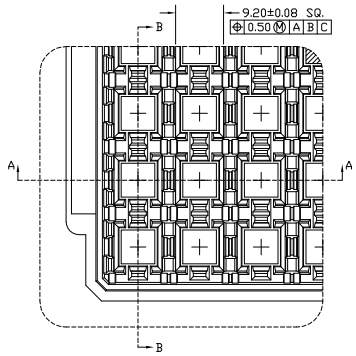
002-19474 Rev. **

18. Packing

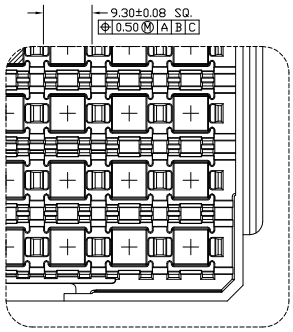
18.1 FCBGA

Figure 43. FCBGA Tray Information

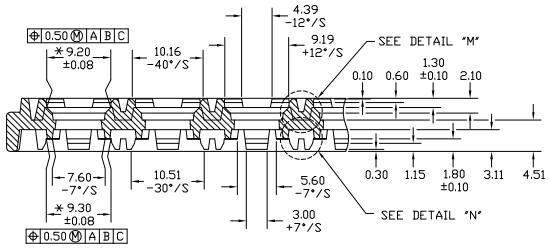




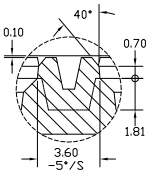
TOP VIEW
DETAIL "B"
SCALE : 3/1
(FROM SHT.#1)



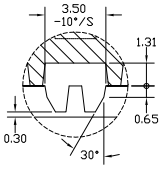
BOTTOM VIEW
DETAIL "B"
SCALE : 3/1
(FROM SHT.#1)



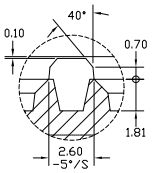
SECTION "B-B"
SCALE : 4/1



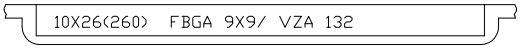
DETAIL "M"
SCALE : 10/1



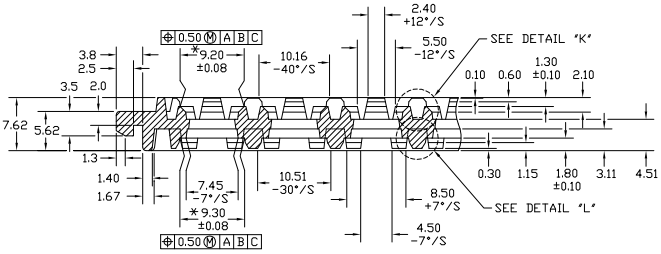
DETAIL "N"
SCALE : 10/1



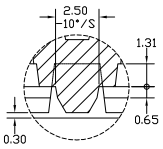
DETAIL "K"
SCALE : 10/1



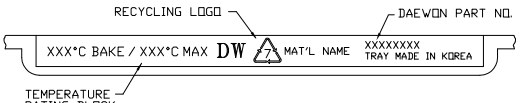
DETAIL "E"
(FROM SHT.#1)



SECTION "A-A"
SCALE : 4/1



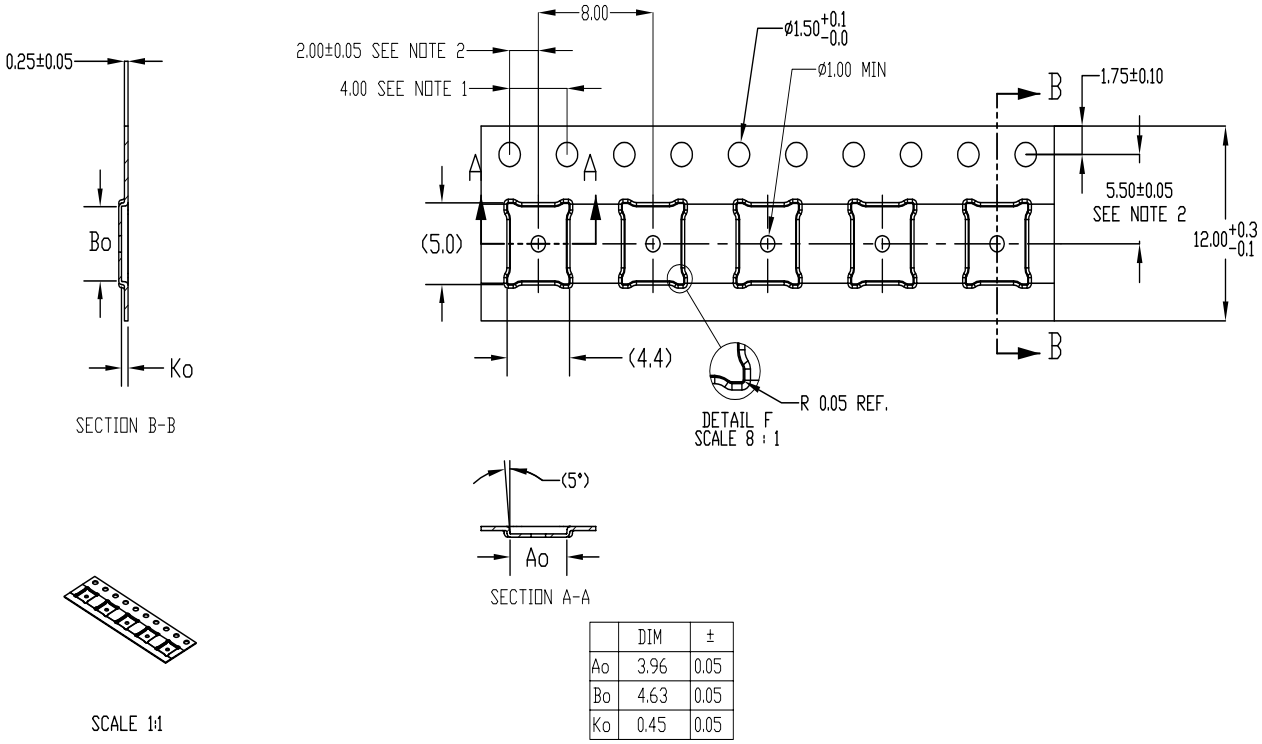
DETAIL "L"
SCALE : 10/1



DETAIL "F"
(FROM SHT.#1)

18.2 WLCSP

Figure 44. WLCSP Tape and Reel Information



	DIM	±
Ao	3.96	0.05
Bo	4.63	0.05
Ko	0.45	0.05

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.
4. ADVANTEK P/N: BCH116-A

19. Ordering Information

Table 64. Part Ordering Information

Part Number	Package	Description	Operating Ambient Temperature
CYW43012C0WKWBG	251-pin WLCSP package (3.76 mm × 4.43 mm, 0.2 mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN+ BT 5.0	–20 °C to +70 °C
CYW43012TC0KFFBH	300-ball FCBGA package (9mm x 9mm, 0.4mm pitch)	Dual-band 2.4GHz and 5GHz WLAN + BT 5.0 sLNA only	–20 °C to +70 °C
CYW43012TC0EKUBG	106-ball WLBGA package (3.76mm x 4.43mm, 0.35mm pitch)	Dual-band 2.4 GHz and 5 GHz WLAN+ BT 5.0	–20 °C to +70 °C

Note: Add “T” suffix to part number for ordering in Tape and Reel for WLCSP. Refer to section 18.2 for the WLSCP tape and reel specifications. FCBGA is only available in tray. Refer to section 18.1 for tray specifications.

20. Additional Information

20.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary

20.2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

20.3 References

The references in this section may be used in conjunction with this document

Note: Cypress provides customer access to technical documentation and software through its

Customer Support Portal (CSP) and Downloads & Support site (see community.cypress.com).

Document (or Item) Name	Number	Source
1] Bluetooth MWS Coexistence 2-wire Transport Interface Specification	–	www.bluetooth.com

20.4 Errata

1. From Rev *L onwards ball U1 on FCBGA and bump 7 on WLCSP are referred to as BT_GPIO_0. This done to align with the firmware that uses P5 LHL GPIO on ball U11 for FCBGA and bump 111 on WLCSP as BT_DEV_WAKE.
2. 2Mbps LE rates on the BT dLNA Rx path show the low receive sensitivity for channels 2430 and 2432. The BT sLNA Rx path does not show this issue.
3. Bluetooth current consumption measurements have increased from Rev *G to Rev *H of the datasheet.
4. In Rev *J of the datasheet a clarification is added to section specifying that the WLAN section ARM Cortex M3 along with peripherals like UART and JTAG/SWD is used for Cypress's firmware and is not available for customers to run firmware on.
5. In Rev *J of the datasheet the UART baud rates supported by HCI UART (section 8.2) and Peripheral UART (section 8.7) were corrected to match the support tested/provided by the UART drivers provided as part of the Cypress SDK. Both these UART interfaces support up to 3Mbps baud rate. Note that the Peripheral UART baud rate is yet to be tested/confirmed and may be corrected in subsequent revisions.
6. Section 9.6 SDIO v3.0 was modified to state limitations to SDIO 3.0 rates supported by CYW43012 due to current driver/SDK implementation. A note was added to the section to document the fact that CYW43012 only supports 1.8V signaling.

7. Rev *J highlights interfaces that are not currently enabled via drivers in Cypress's SDK. These include PCM (section 8.1), I2S (section 8.3), PDM (section 8.5) and single mode SPI (section 8.4). Notes added to interfaces like PCM and I2S to clarify that these are not exposed to customer application code in the SDK.
8. The SPI and Quad SPI interfaces mentioned in section 8.4 are master only. Slave mode is not supported on either of these.
9. In Rev *J note added to section 8.9 ADC highlighting the low impedance of 1kΩ.
10. In Rev *K power supply topology updated in Figure 3 and Figure 6 for FCBGA/WLCSP. Figures 5 and 6 added for power supply topology in the case of WLBGA package.
11. Corrected figures in section 2.7 to reflect that WLAN_REG_ON and/or BT_REG_ON should be asserted more than 2 sleep clock cycles after VBAT & VDDIO are up.
12. WLBGA package details added in sections 16., 17. and 19..
13. Added BT_LDOVDD_V1P8 i.e. ball AA17 on FCBGA in Table 56 and clarified that this is a dummy ball that is not connected to the die and must be a no connect on FCBGA package.
14. CBUCK specifications in Table 4 changed to account for 0603 inductor only.
15. Quiescent current for BTLDO3P3 (Table 5), RFLDO3P3 (Table 6) and HVLDO1P8 (Table 9) are specified for Typical only.
16. Dropout voltage specification for MEMLPLDO (Table 8) removed
17. TX output power across rates in 2.4GHz (Table 39) and 5GHz (Table 40) changed to align with qualified power numbers.
18. Input IP3 specifications removed from Table 35, Table 38 and Table 40.
19. System power consumption in Table 49 modified to reflect measured data.
20. Package Thermal Characteristics in Table 50 updated for all packages.
21. WLCSP bump coordinates in Table 52 corrected for bump numbers 53 to 70 and bump number 215.
22. Table 55 updated to reflect correct WLBGA bump list
23. Removed notes “P6 is used as SDIO_CMD_WAKE for DS1 Power state” from Table 56. P6 usage as SDIO_CMD_WAKE is for extreme low power modes wherein only LHL domain timer and IOs are powered on. This mode referred to as Hibernate mode is currently not supported by the device.
24. Added notes to the datasheet in relevant places highlighting that the DS1 sleep mode is currently not supported by the 43012 firmware.
25. Added restriction in Table 56 documenting that the P8 LHL GPIO can be used as Output only.

Document History

Document Title: CYW43012 Single-Chip, Ultra-Low Power, IEEE 802.11n, 802.11ac-friendly™ MAC/Baseband/Radio with Bluetooth 5.0 Document Number: 002-18925			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	5688162	05/18/2017	Migrated IoT document from 430121_IOT-DS300-R to Cypress format.
*A	5766026	06/07/2017	Updated the Figures 1, 2, 39,40 Updated the Tables 39, 40
*B	5827642	07/21/2017	Added “IEEE 802.11ac-friendly” related details to this document.
*C	5844643	08/29/2017	Added “FCBGA” related details to this document.
*D	5883770	09/14/2017	Table 49 and Table 50 updated.
*E	5943906	10/25/2017	Added Table 22, Figure 24 and Sections 8.5, 8.6, 8.7. Updated the Table 52.
*F	5969958	11/17/2017	Updated Notes on Page1. Removed 28HPL from Figure 3. Changed “Thick Oxide” to LHL in the Figure 6. Updated Title in Table 3. Updated Min, Typ and Max values for “Input Supply Voltage” in Table 4, Table 5, Table 6, Table 7, Table 9. Updated SDR40 to SDR50 and DDR40 to DDR50 under the section SDIO v3.0 on page 45. Updated the contents in Table 36, Table 46, Table 47, Table 59(merged Pad functions). Added Table 61, Table 62. Added Errata.
*G	6003245	12/22/2017	Updated Table 38, Table 39, Table 40, Table 41, Table 53 and Table 56. Updated the note below Figure 1 as “IEEE 802.11ac full-compliance requires support for 40 MHz and 80 MHz channel bandwidths. CYW43012 is 802.11ac-friendly™. It only supports 20 MHz channel bandwidth however it supports 802.11ac's 256-QAM for the 20 MHz channels in the 5 GHz band enabling it to offer higher throughput and lower energy per bit than 802.11n only products. In addition CYW43012, when used as a STA with an 802.11ac access point, supports 802.11ac's explicit beamformee feature to offer significantly higher throughputs than 802.11n chipsets at any given range”. Updated Figure 1 to Figure 31 as Visio images.

Document Title: CYW43012 Single-Chip, Ultra-Low Power, IEEE 802.11n, 802.11ac-friendly™ MAC/Baseband/Radio with Bluetooth 5.0 Document Number: 002-18925			
*H	6169677	05/14/2018	Updated Features. Updated Figure 2 and Figure 13. Added “CYW43012 supports 2 internal sleep modes DS0 and DS1. In DS0 the complete RAM needed for WLAN firmware is retained. In DS1 a small subset of the firmware is retained and very few WLAN functions can be supported. When waking up from DS1 the WLAN firmware must be downloaded again therefore the wakeup latency from DS1 is higher though it offers very low power consumption” in the section WLAN Power Management. Added “Note this pin is used for designs that use an external reference clock source from the Host. This pin is irrelevant for Crystal reference clock based designs where the CYW43012 device generates it’s own reference clock from an external crystal connected to its oscillator circuit” in the section Host Controller Power Management. Added section PWM, ADC and Bluetooth Current Consumption Updated Table 35, Table 36 and Table 53 and Table 59. Table 53: Changed WRFVSSCPA5G_VDD_V3P4 to VSSC for Bump number 204. Added Packing (FCBGA and WLCSP). Added “Note that the DS1 state has higher wakeup latency than DS0. Therefore DS1 should be used to minimize the overall power consumption only in scenarios when no activity is expected for a significantly large amount of time and with larger DTIM intervals in the section WLAN Current Consumption. Removed (WL_R BT_R VDDIO) column from Table 62. Added ADC Specifications. Updated the footnote in Table 63. Added the footnote “HVLDO1P8 supplying 1.8V VDDIO is not currently supported. An external 1.8V VDDIO is recommended and all specifications in this datasheet hold true only when an external 1.8V VDDIO is used” in Figure 6. Added Note “Firmware in WICED SDK reads ADC registers and averages values before providing the same to the application. This puts a limit on the effective conversion rate seen by the application. Since the ADC is currently intended for battery monitoring and other static voltage measurements this approach meets use case requirements. DMA functionality for the ADC is not currently available” in ADC section. Added “2Mbps LE rates on the BT dLNA Rx path show low receive sensitivity for channels 2430 and 2432. The BT sLNA Rx path does not show this issue” and “Bluetooth current consumption measurements have increased from Rev *G to Rev *H of the datasheet. Firmware changes to optimize the Bluetooth current consumption are being investigated. Subsequent revisions of the datasheet are expected to have updated Bluetooth current consumption data” in Errata section. Added “Ultra low TX o/p power mode to enable use cases like proximity pairing etc” in the Features section. Replaced “Trigger Broadcom fast connect (TBFC)” with “Ultra-low TX o/p power mode to enable use cases like proximity pairing while reducing current consumption” in theBluetooth Subsystem Overview section.
*I	6242816	07/12/2018	Updated Table 38, Table 39, Table 40 and Table 41. Changed “Values in this section of the datasheet are design goals and are subject to change based on device characterization results.” to “Values in this section of the datasheet are measured on a board that uses the CYW43012 FCBGA package. The performance may vary based on board design, front end and the 43012 package/module used. Customers must use NVRAM obtained from Cypress or one of Cypress’s qualified module partners and must refrain from changing NVRAM settings without consulting Cypress. Changes to NVRAM settings will impact multiple areas of chip performance including reliability across lifetime.” in the following sections: DC Characteristics, Bluetooth RF Specifications, WLAN RF Specifications and System Power Consumption. Added footnote “The TX power at the chip output port is controlled by firmware and is approximately 1.5dB lower from the minimum numbers mentioned in Table 45, to account for closed loop TX power control variation and other factors” in Table 39 and Table 41.

Document Title: CYW43012 Single-Chip, Ultra-Low Power, IEEE 802.11n, 802.11ac-friendly™ MAC/Baseband/Radio with Bluetooth 5.0 Document Number: 002-18925			
*J	6285689	08/30/2018	Updated Symbol and Value for “Maximum input power for RX input ports” in Table 31. Added Typical value for the “Interference Performance” in Table 35. Updated Typical for “General BT” in Table 36. Updated Microprocessor and Memory Unit for Bluetooth and Errata sections. Added Note in WLAN Global Functions, PDM Microphone, External Coexistence Interface. Updated Bluetooth Peripheral Transport Unit section. Removed “PCM Interface Timing Diagrams”. Updated the Note in ADC and Ordering Information. Updated “Bluetooth AJTAG” description in Table 56.
*K	6333801	10/12/2018	Updated General Features. Updated Figure 3, Figure 4, Figure 9 and Figure 10. Added Figure 5 and Figure 6. Added Figure 38, Table 54, Table 55 and WLBGA section. Added BT_LDOVDD_V1P8 i.e. ball AA17 on FCBGA in Table 56. Updated Strapping Options and added Table 58. Quiescent current for BTLDO3P3 (Table 5), RFLDO3P3 (Table 6) and HVLDO1P8 (Table 9) Typical values specified. Input IP3 specifications removed from Table 35, Table 38 and Table 40. TX output power across rates in 2.4GHz (Table 39) and 5GHz (Table 40) changed to align with qualified power numbers. Removed “Frequency Selection” section. Added Note “The FCBGA and WLCSP packages allow an external 32.768kHz crystal or an external 32.768kHz clock (from an external oscillator) to be connected to the CYW43012. The WLBGA package only allows a 32.768kHz clock form an external oscillator to be connected to the CYW43012” in External 32.768 kHz Low-Power Oscillator. Updated Ordering Information and Errata sections.
*L	6438642	01/11/2019	Updated Table 55 to reflect the correct WLBGA ball list. Updated WLCSP part number in Table 1. Added notes to the datasheet in relevant places highlighting that the DS1 sleep mode is currently not supported by the 43012 firmware. WLCSP bump coordinates in Table 52 corrected for bump numbers 53 to 70 and bump number 215. Updated Table 56 LHL/HIB pads description. Updated Errata section.
*M	6713065	06/30/2020	Updated 106-ball WLBGA package to production in General Features. Updated Table 36. Added Note in Bluetooth RF Specifications and Bluetooth Current Consumption. Changed the description for the part number CYW43012TC0KFFBH in Table 64. Updated description on page 105 in Table 56. Removed Table in section WLAN Current Consumption. Removed DS1 information in section WLAN Power Management, Table 56, and Table 57. Removed Crystal load capacitance in Table 10. Updated HBM rating from 2.2 to 2.0 kV in Table 33. Removed iLPO information in External 32.768 kHz Low-Power Oscillator. Removed iLPO information and updated Foot note in Table 38. Updated maximum DC Input Voltage from 4.4 V to 4.6 V

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