12-CH Level Shifter for GOA TFT-LCD Panel

General Description

The RT8935 is a high voltage level shifter. This device is suitable for GOA TFT-LCD panel applications.

The level shifter is designed for generating a high voltage signal to drive the TFT-LCD panel. Twelve outputs are provided to switch between VGL and VGH to charge and discharge capacitive loads up to 5nF.

Ordering Information

RT8935 □□

Package Type
QW : WQFN-32L 4x4 (W-Type)

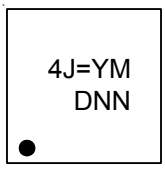
Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



4J= : Product Code

YMDNN : Date Code

Features

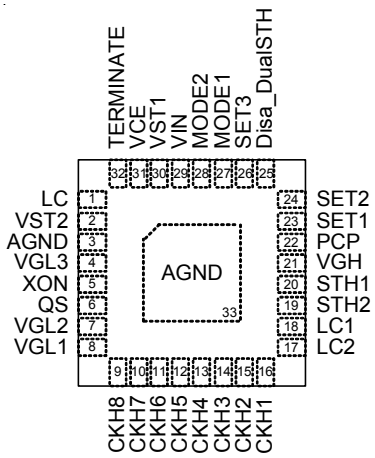
- **2.6V to 5.5V Input Logic Level Range**
- **–15V to 40V Output Voltage Range**
- **Rise/Fall Time 700ns (Max)**
- **Protection Functions: UVLO, OTP**
- **RoHS Compliant and Halogen Free**

Applications

- GOA TFT-LCD Panel

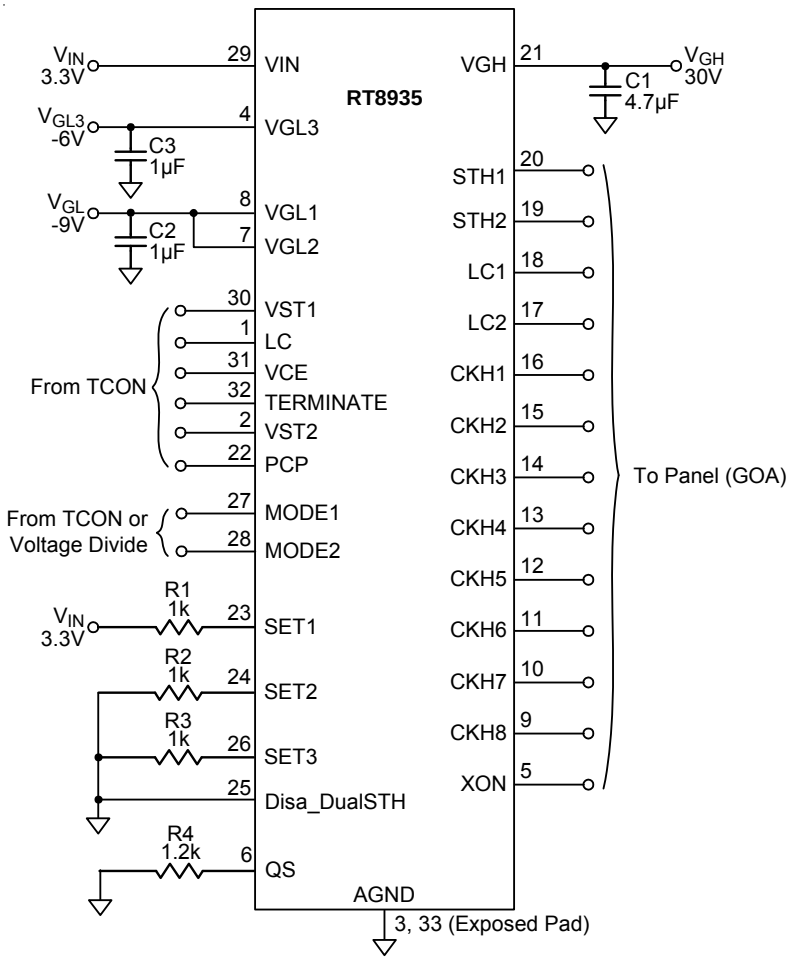
Pin Configuration

(TOP VIEW)



WQFN-32L 4x4

Typical Application Circuit

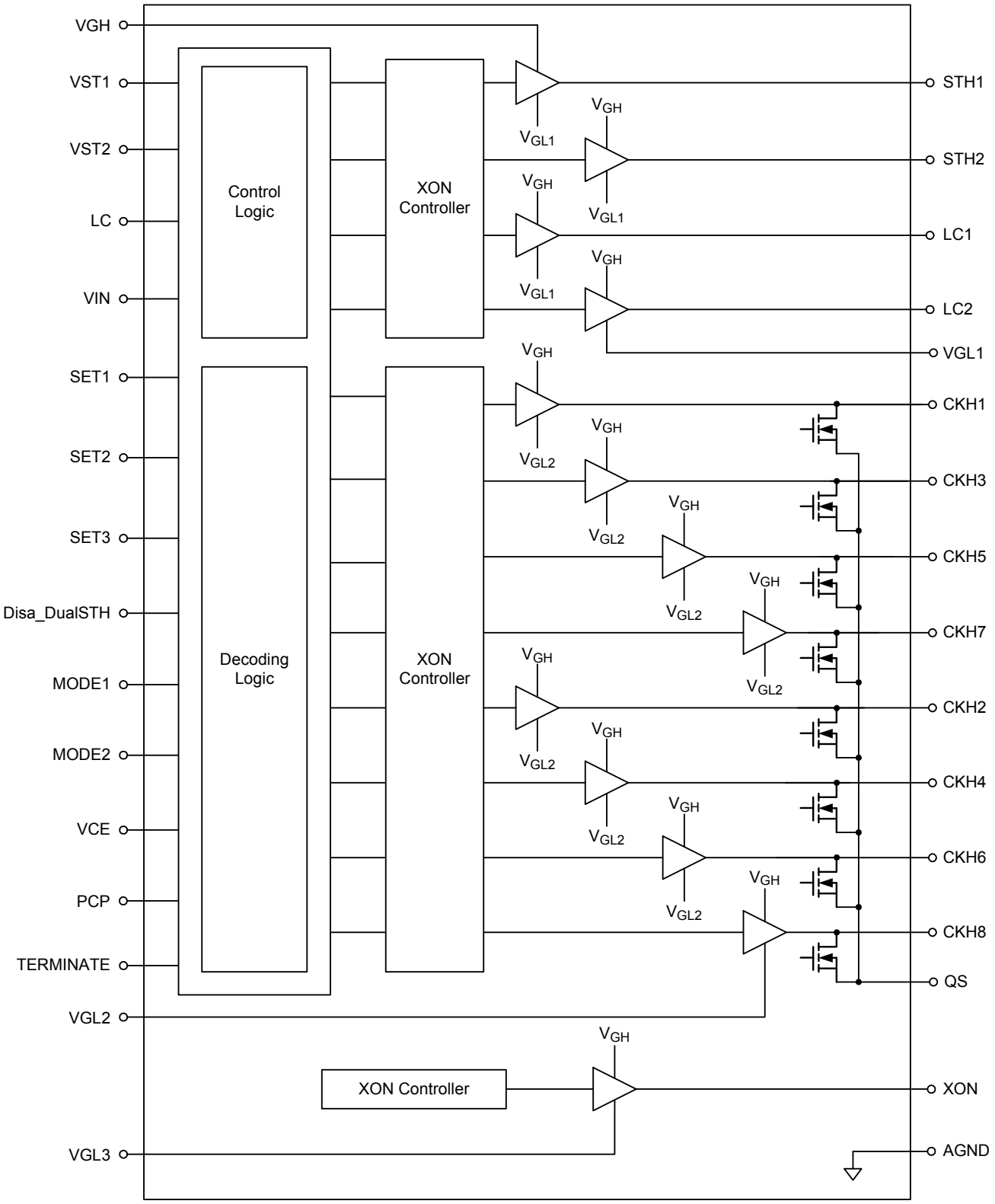


Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LC	Level shifter input signal (Low frequency clock).
2	VST2	Level shifter input signal (Start Pulse for GOA Share) The VST2 is the rising edge trigger.
3, 33 (Exposed Pad)	AGND	Analog ground for logic block. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.
4	VGL3	Negative power supply for XON.
5	XON	Discharge function for liquid crystal capacitor.
6	QS	Charge shaping resistor connection.
7	VGL2	Negative power supply for CKH1 to CKH8.
8	VGL1	Negative power supply for STH1, STH2, LC1 and LC2.
9 to 16	CKH8 to CKH1	Level shifter output with charge sharing function.
17	LC2	Level shifter output signal (Low Frequency Clock 2).
18	LC1	Level shifter output signal (Low Frequency Clock 1).
19	STH2	Level shifter output signal (Start Pulse for Rotate).
20	STH1	Level shifter output signal.
21	VGH	Positive power supply.
22	PCP	Set pin for charge sharing timing.
23	SET1	Setting pin for phase selection. High Level : 8 phase Low Level : 6 phase Floating : 4 phase. The setting will trigger and latch the phase selection function by each VST1 rising edge. (Note : It is suggested that the pin is fixed by VIN or GND or not connect in the application.) High Level : Connected to VIN Low Level : Connected to GND Floating : Not Connect
24	SET2	Setting pin for clocks interval. High Level : There is no time interval between CKHs. Low Level or floating : There is some time interval between CKHs. The setting will trigger and latch the Clocks Interval function by each VST1 rising edge. (Note : It is suggested that the pin is fixed by VIN or GND or Not Connect in the application.) Connected 400kΩ to GND inside RT8935. High Level : Connected to VIN Low Level : Connected to GND Floating : Not Connect

Pin No.	Pin Name	Pin Function
25	Disa_DualSTH	Disable control input for dual STH output. High Level : STH1 On (follow VST1), STH2 keeps in VGL1 Low Level : STH1 On (follow VST1), STH2 On (follow VST2) Connected 400kΩ to GND and 400kΩ to VIN inside RT8935. High Level : Connected to VIN Low Level : Connected to GND Floating is not allowed
26	SET3	Set pin for charge sharing mode. High level : Enable charge sharing mode1 Low level : Enable charge sharing mode2 Floating : Disable charge sharing mode The setting will trigger and latch the charge sharing mode function by VST1 rising edge. (Note : It is suggested that the pin is fixed by VIN or GND or Not Connect in the application) High level : Connected to VIN Low level : Connected to GND Floating : Not Connect
27	MODE1	Receiving signal for pre-charge selection. High Level : 1-line pre-charge Low Level : No pre-charge Middle : 2-line pre-charge The mode1 will trigger and latch by each VST1 rising edge. The signal can change real time. High Level : 1.5V to 5.5V (ex : Connected to VIN) Low Level : 0 to 0.8V (ex : Connected to GND) Middle Level : 0.9V to 1.4V (ex : Voltage Divide)
28	MODE2	Receiving signal for pre-charge selection High level : Enable 3-line pre-charge function Low level or Middle: Keep MODE1 Setting The setting will trigger and latch the charge sharing mode function by VST1 rising edge. (Note : It is suggested that the pin is fixed by VIN or GND or Not Connect in the application) High level : 1.5V to 5.5V (ex: Connected to VIN) Low level : 0 to 0.8V (ex: Connected to GND) Middle : 0.9V to 1.4V (ex: Voltage Divide)
29	VIN	Supply voltage input.
30	VST1	Level shifter input signal (Start Pulse).
31	VCE	Level shifter input signal (Condensed Clock).
32	TERMINATE	Level shifter input signal (turn off all buffers in blanking time).

Functional Block Diagram



Operation

Control Logic and Decoding Logic

The low voltage input signal will transfer to high voltage output to drive the panel. The output waveform will follow decoding logic command which is based on setting pins results.

Low voltage input pin: VST1, VST2, LC, VCE, PCP, and TERMINAL Setting pin: SET1, SET2, SET3, Disa_DualSTH, MODE1, and MODE2. High voltage output pin: STH1, STH2, LC1, LC2, CKH1~8, XON, and QS

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage VIN ---------- –0.3 to 7V
- AGND ---------- –0.3 to 0.3V
- VST1 to VST2, LC, VCE, Disa_DualSTH, PCP
  SET1 to SET3, TERMINATE, MODE1 to MODE2 ---------- –0.3 to 7V
- VGH ---------- –0.3 to 45V
- VGL1 to VGL3 ---------- –20 to 0.3V
- VGH – (VGL1 or VGL2 or VGL3) ---------- –0.3 to 60V
- STH1 and 2, LC1 and 2, CKH1 to CKH8, XON, QS ---------- (V_{GL} + 0.3)V to (V_{GH} – 0.3)V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN 32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 2)
  WQFN 32L 4x4, θ_{JA} ---------- 27.8°C/W
  WQFN 32L 4x4, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, V_{GH} = 30V, V_{GL1} = V_{GL2} = –10V, V_{GL3} = –6V, AGND = 0V with typical values T_A = 0°C to 85°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Supply Voltage	V_{IN}		2.6	--	5.5	V
VIN Quiescent Current	I_{Q_VIN}		--	60	--	μA
VIN Under Voltage NG Lockout Threshold	V_{UVLO}	VIN rising, hysteresis 200mV	1.9	2	2.1	V
		VIN falling	1.7	1.8	1.9	
VGH Under-Voltage Lockout Threshold	V_{UVLOGH}	VIN rising, hysteresis 200mV	6.2	--	6.9	V
		VGH falling	6	--	6.7	
Thermal Shutdown	T_{SD}	Junction temperature rising	150	--	160	°C
Internal Pull Up or Down Resistor			--	400	--	kΩ
Level Shifter						
VGH to GND	V_{GH}		7	--	40	V
VGL1 Operating Voltage Range	V_{GL1}		–15	--	0	V
VGL2 Operating Voltage Range	V_{GL2}		–15	--	0	V
VGL3 Operating Voltage Range	V_{GL3}		–15	--	0	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VGH Quiescent Current		I_{Q_VGH}		--	340	--	μA
VGL1 Quiescent Current		I_{Q_GL1}		--	10	--	μA
VGL2 Quiescent Current		I_{Q_GL2}		--	70	--	μA
VGL3 Quiescent Current		I_{Q_GL3}		--	20	--	μA
STH1 to STH2, LC1 and LC2		V_{OUT}		0.3 + V_{GL1}	--	V_{GH} – 0.3	V
CKH1 to CKH8		V_{OUT}		0.3 + V_{GL2}	--	V_{GH} – 0.3	V
VCE, Terminate, Disa_DualSTH, VST1 and VST2, and LC PCP Input Voltage	Logic-High	V_{IH}	V_{IN} = 2.6V to 5.5V	1.5	--	--	V
	Logic-High	V_{IL}	V_{IN} = 2.6V to 5.5V	--	--	0.8	
MODE 1	High-Level			1.5	--	5.5	V
	Middle-Level			0.9	--	1.4	V
	Low Level			0	--	0.8	V
MODE 2	High-Level			1.5	--		V
	Low-Level			--	--	0.8	V
VGH – (VGL1 or 2 or 3)				--	--	55	V
CKH1 to CKH8, STH1 and 2, LC1 and 2, Positive Output Swing		VCK+	All inputs high, I_{OUT} = –10mA	V_{GH} – 0.5	V_{GH} – 0.2	V_{GH}	V
STH1 and 2, LC1 and 2, Negative Output Swing		VCK–	All inputs low, I_{OUT} = –10mA	V_{GL1}	V_{GL1} + 0.2	V_{GL1} + 0.5	V
CKH1 to CKH8 Negative Output Swing		VCK–	All inputs low, I_{OUT} =10mA	V_{GL2}	V_{GL2} + 0.2	V_{GL2} + 0.5	V
QS Switch On-Resistance		R_{LS_On}	I_{OUT} = ±10mA	--	20	50	Ω
CKH1 to CKH8, STH1 and 2, LC1 and 2	Rising Time	t_R	V_{GH} = 30V, V_{GL}1, 2 = –10V, R_L = 50J, C_L = 4.7nF, 10% to 90%	--	--	700	ns
	Falling Time	t_F	V_{GH} = 30V, $V_{GL1, 2}$ = –10V, R_L = 50J, C_L = 4.7nF, 90% to 10%	--	--	700	
CKH1 to CKH8, STH1 and 2, LC1 and 2, Delay Time	Rising Time	t_{RD}	V_{GH} = 30V, $V_{GOL1, 2}$ = –10V 50% of input to 10% of output	--	150	250	ns
	Falling Time	t_{FD}	V_{GH} = 30V, $V_{GL1, 2}$ = –10V 50% of input to 90% of output	--	150	250	
XON Rising Time		t_{XON}	V_{GH} = 30V, V_{GL2} = V_{GL3} = –6V, C_L = 4.7nF, 10% to 90%	--	1	--	μs

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

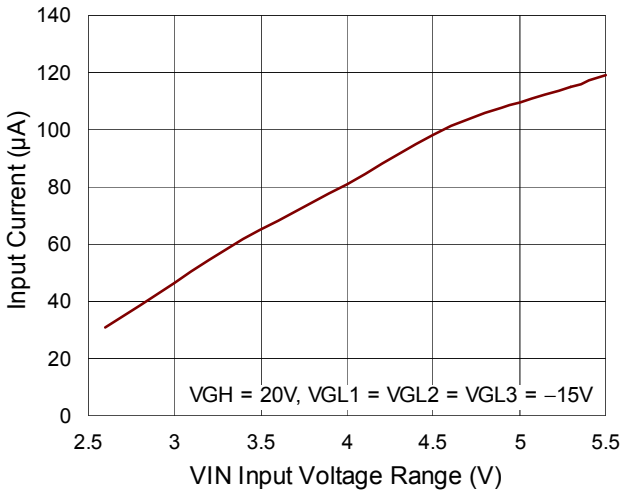
Note 2. $_{JA}$ is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

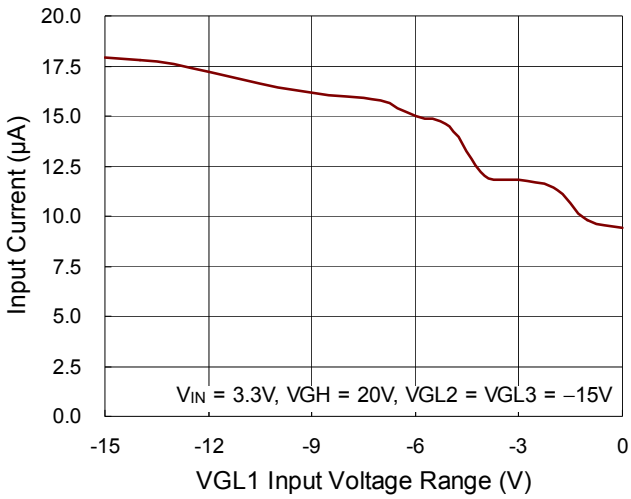
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

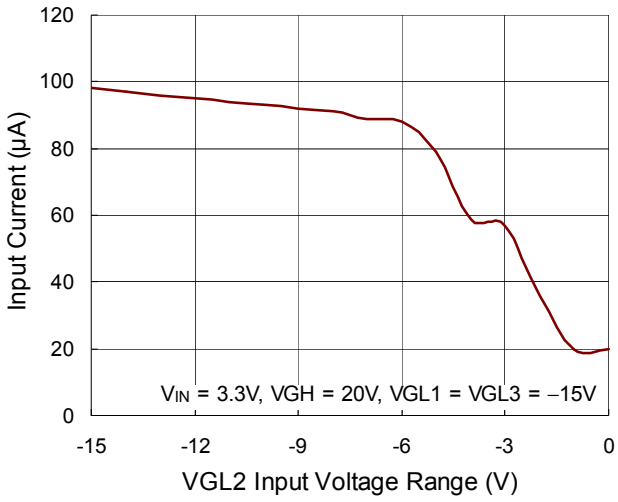
Input Current vs. VIN Voltage Range



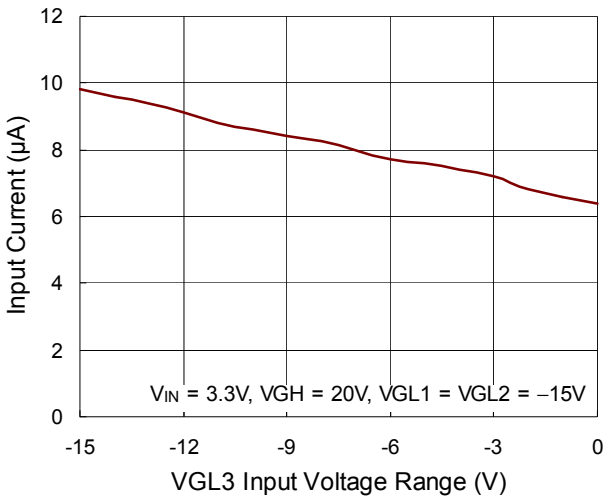
Input Current vs. VGL1 Voltage Range



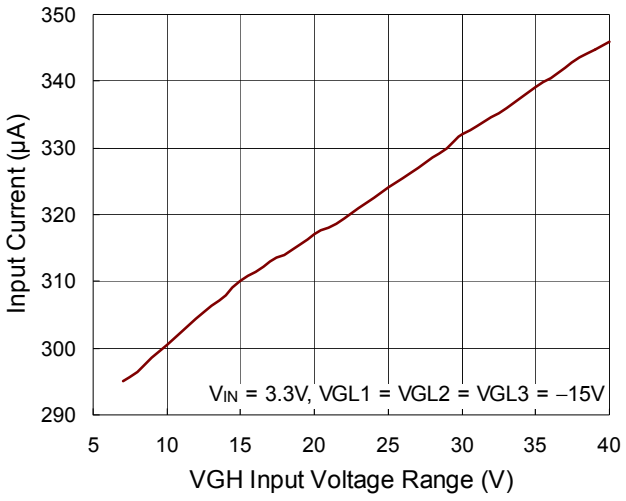
Input Current vs. VGL2 Voltage Range



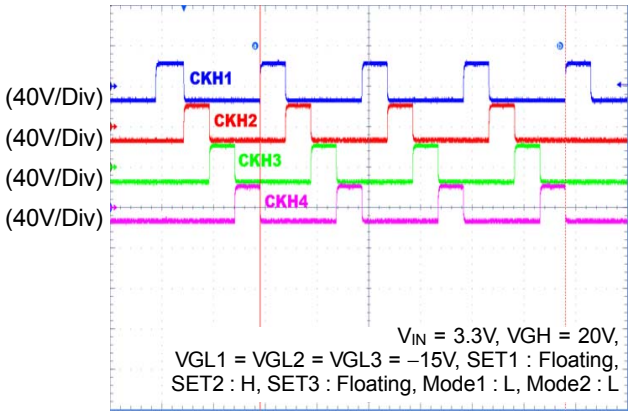
Input Current vs. VGL3 Voltage Range



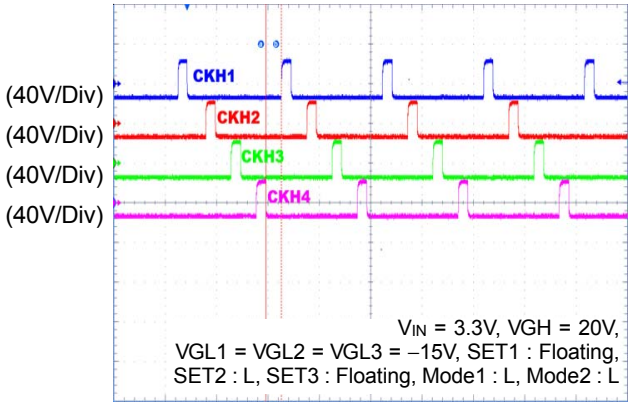
Input Current vs. VGH Voltage Range



CKHx Ouput Waveform vs. Setting

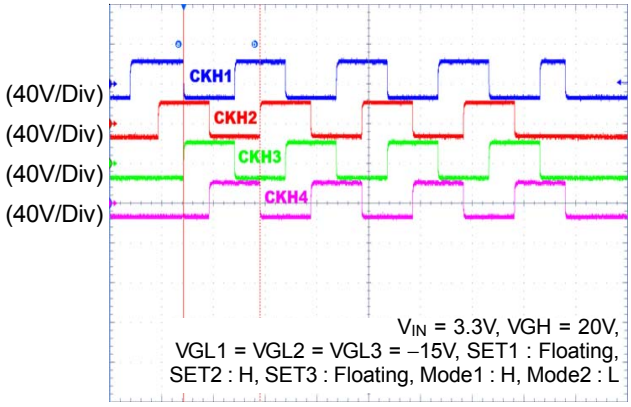


CKHx Ouput Waveform vs. Setting



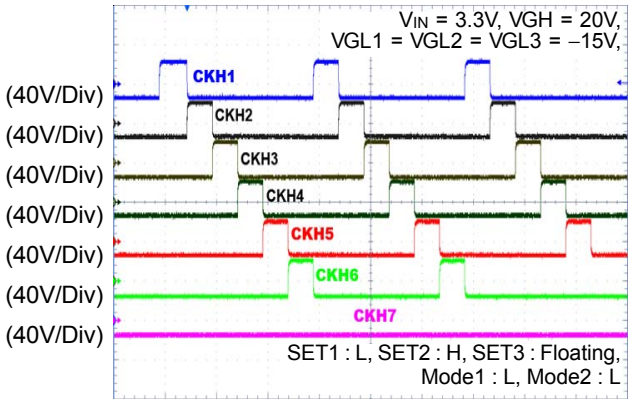
Time (20µs/Div)

CKHx Ouput Waveform vs. Setting



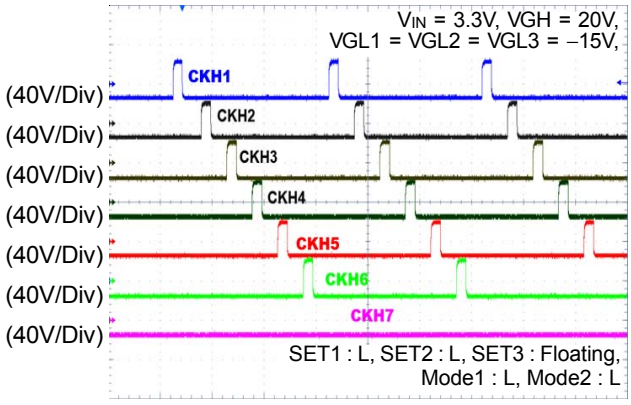
Time (20µs/Div)

CKHx Ouput Waveform vs. Setting



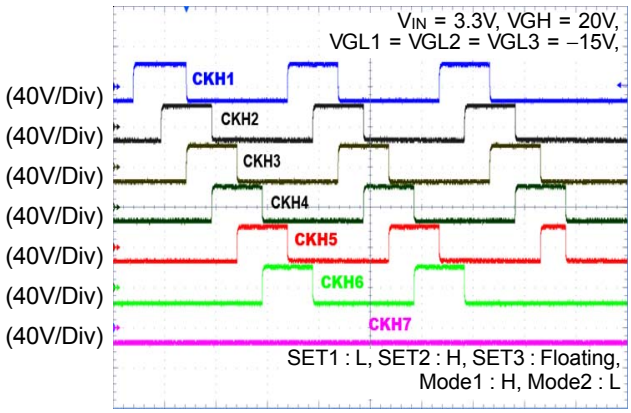
Time (20µs/Div)

CKHx Ouput Waveform vs. Setting



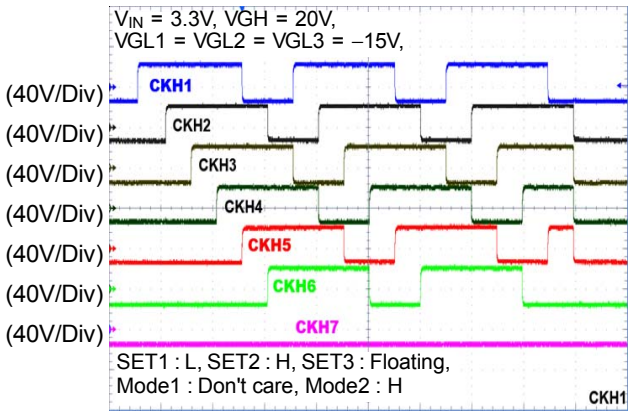
Time (20µs/Div)

CKHx Ouput Waveform vs. Setting



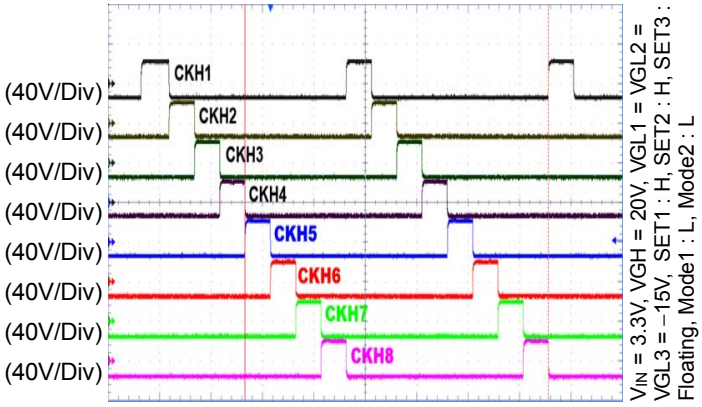
Time (20µs/Div)

CKHx Ouput Waveform vs. Setting

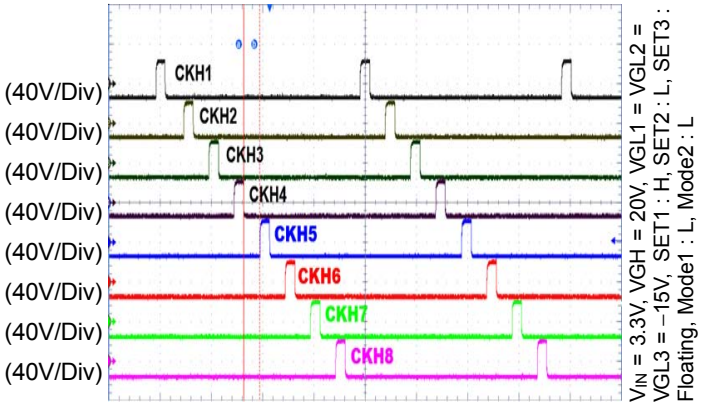


Time (20µs/Div)

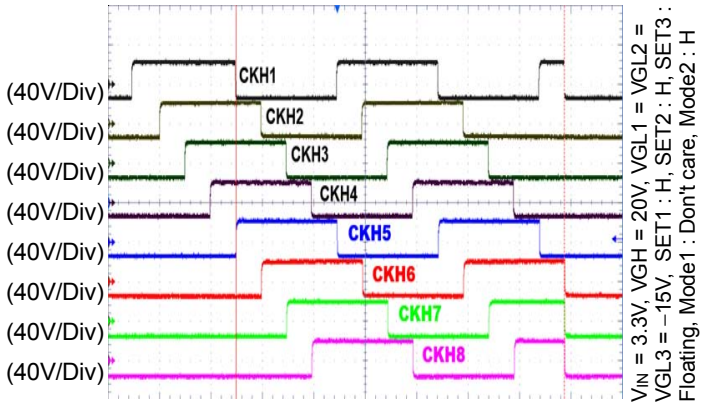
CKHx Ouput Waveform vs. Setting



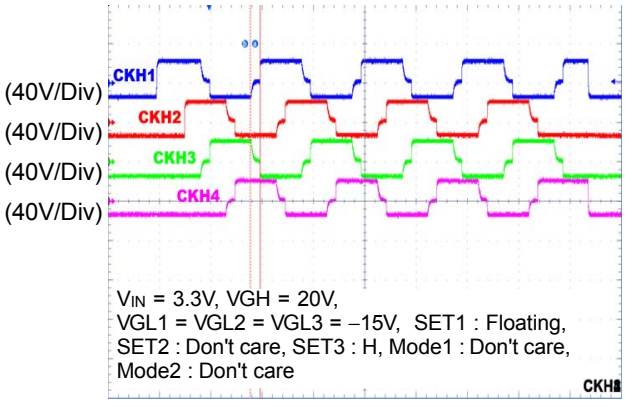
CKHx Ouput Waveform vs. Setting



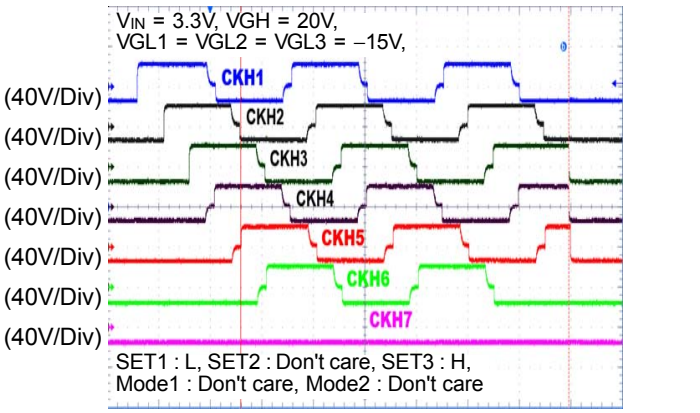
CKHx Ouput Waveform vs. Setting



CKHx Ouput Waveform vs. Setting



CKHx Ouput Waveform vs. Setting



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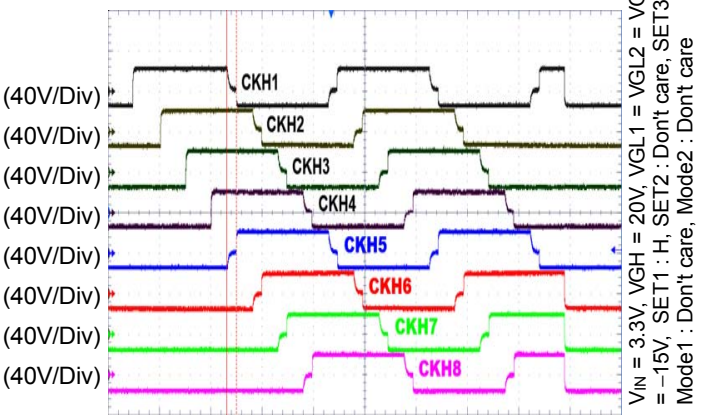
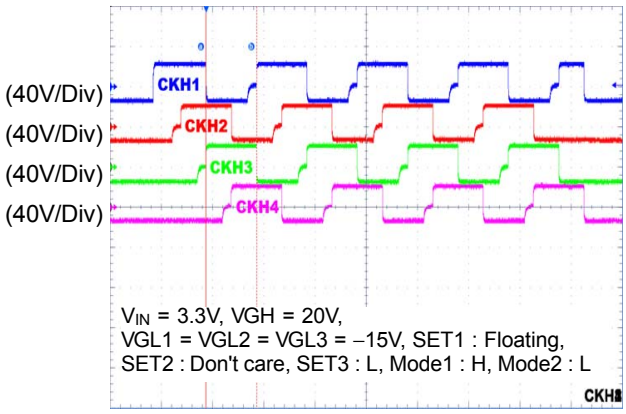
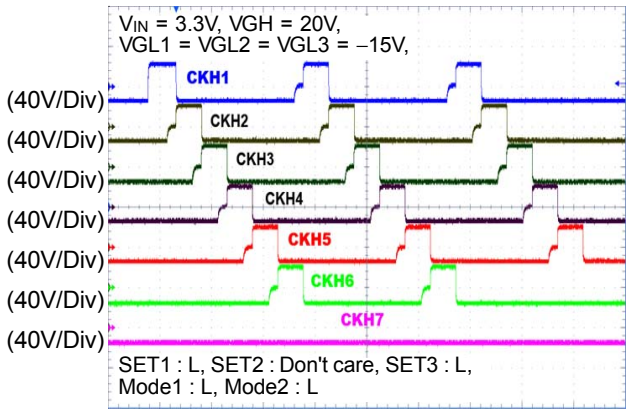


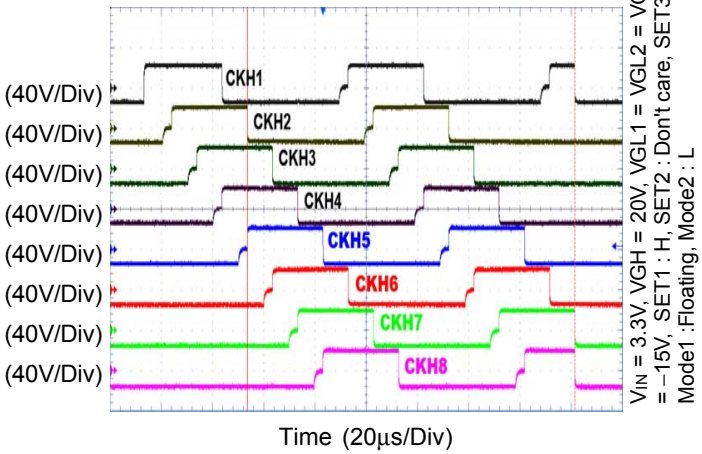
CKHx Ouput Waveform vs. Setting



CKHx Ouput Waveform vs. Setting



CKHx Ouput Waveform vs. Setting



Application Information

General Description

The RT8935 provides 12-channel level shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (T-CON) to high-level signals required by GOA panel.

Power On Sequence

When the VIN exceeds UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter CKH1 to CKH8, and XON should follow V_{GL3} level since VIN exceeds UVLO. The outputs of Level Shifter LC1, LC2, STH1, and STH2 should follow V_{GL1} level since VIN exceeds UVLO. After ENA is high, CKH1 to CKH8 do not output since receiving the first VST1 rising edge. After ENA is high, LC1 will start to follow LC and LC2 will start to be inverting of LC as the 1st LC transition or the 1st VST1 rising.

According to GOA experience, it is recommended that 1. LC1 and LC2 start to work earlier than the 1st STH1 or STH2. Logic signal (VST1 to VST2, LC, VCE) must be sent after negative power ready.

Table 1. Power On (from 0 to VIN) Condition List-1

Case	Analog Power Input			Logic Input			Analog Output			
	VIN	VGH	VGL1 to VGL3	VST1	VCE	LC	STH1	CKH1 to CKH8	LC1, LC2	XON
1	> UVLO	> UVLOGH	Don't Care	w/ Signal	w/ Signal	w/ Signal	Normal Operation	Normal Operation	Normal Operation	VGL3
2	> UVLO	> UVLOGH	Don't Care	w/ Signal	w/o Signal	w/ Signal	Normal Operation	VGL2	Normal Operation	VGL3
3	> UVLO	> UVLOGH	Don't Care	w/o Signal	w / Signal	w / Signal	VGL1	VGL2	Normal Operation	VGL3
4	> UVLO	> UVLOGH	Don't Care	w/ Signal	w/ Signal	w/o Signal	Normal Operation	Normal Operation	LC1 = LC2 initial state analog level. LC2 = $\overline{LC1}$ after 1st VST	VGL3
5	> UVLO	> UVLOGH	Don't Care	w/o Signal	w/ Signal	w/o Signal	VGL1	VGL2	VGL1	VGL3
6	> UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL2	VGL1	VGL3
7	< UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/ o Signal	w/ or w/o Signal	VGL1	VGL2	VGL1	VGL3
8	< UVLO	> UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL2	VGL1	VGL3

Table 2. Power On (from 0 to VIN) Condition List-2

Case	Analog Power Input			Logic Input		Analog Output	
	VIN	VGH	VGL1 to VGL3	VST1	VST2 (Disa_DualSTH = 0)	STH1 (follow VST1)	STH2 (follow VST2)
1	> UVLO	> UVLOGH	Don't Care	w/Signal	w/Signal	Normal Operation	Normal Operation
2	> UVLO	> UVLOGH	Don't Care	w/Signal	w/o Signal	Normal Operation	VGL1
3	> UVLO	> UVLOGH	Don't Care	w/o Signal	w/Signal	VGL1	Normal Operation
4	> UVLO	> UVLOGH	Don't Care	w/o Signal	w/o Signal	VGL1	VGL1
5	> UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL1
6	< UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL1
7	< UVLO	> UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL1

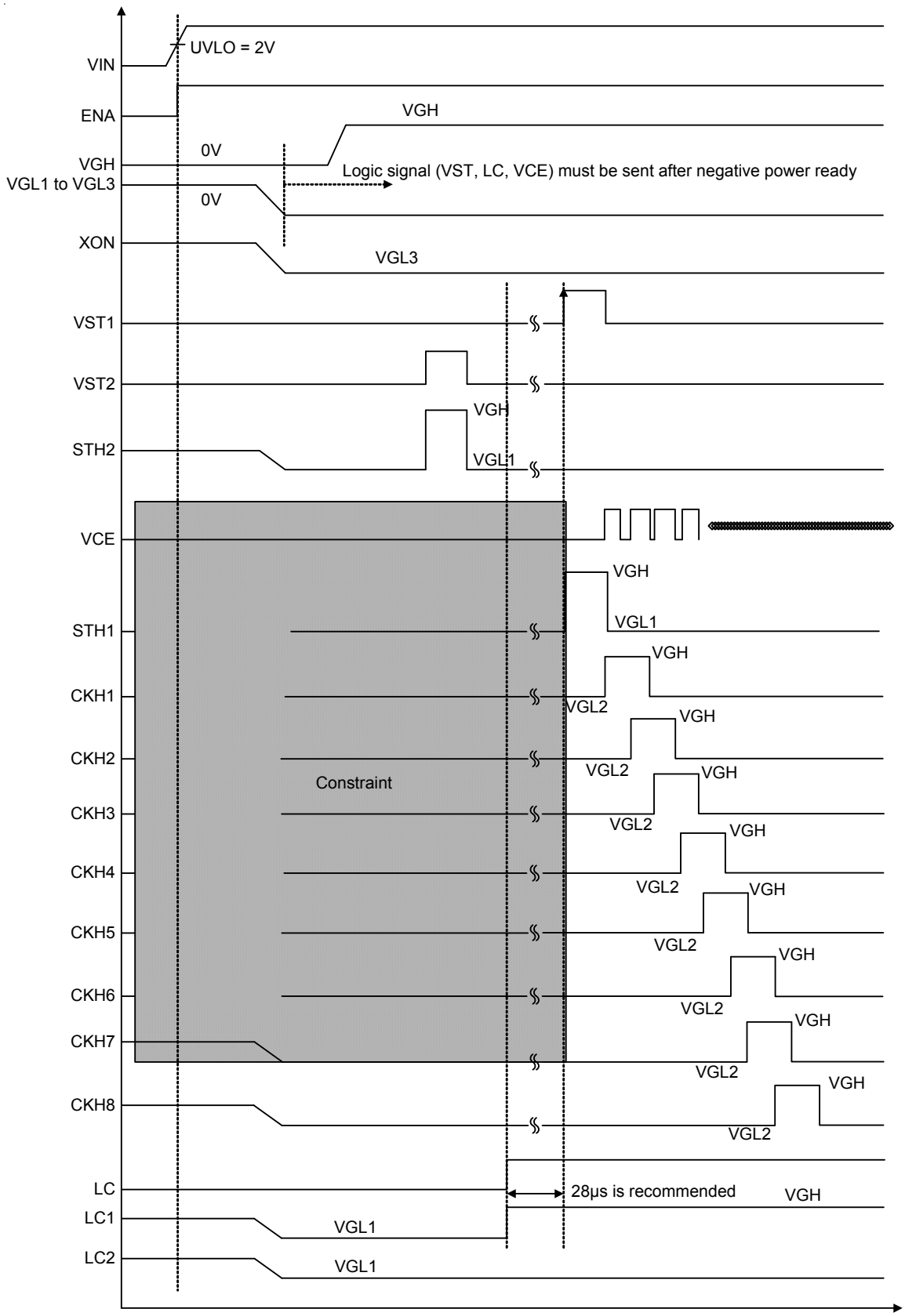


Figure 1. Power On Sequence

Power Off Sequence

Once the VIN falls below the UVLO threshold, the RT8935 will have the following actions. Pull all level-shift outputs as high level (Note 5) (including XON, STH1 to STH2, LC1 to LC2, and CKH1 to CKH8). (Note 6)

Note 5. For the tri-state setting pin, it is connected an internal 400kΩ resistor to VIN and internal 400kΩ resistor to GND.

Note 6. V_{GH} has internal regulator for logic power. We suggest don't repower no at 1V V_{GH} 4V.

Table 3. Power Off (from VIN to 0) Condition List

Case	Analog Power Input			Logic Input			Analog Output			
	VIN	VGH	VGL1 to VGL3	VST1, VST2 (Disa_DualSTH = 0 or 1)	VCE	LC	STH1, STH2	CKH1 to CKH8	LC1, LC2	XON
1	< UVLO	> UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	Follow VGH	Follow VGH	Follow VGH	Follow VGH
2	> UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL2	VGL1	VGL3
3	< UVLO	< UVLOGH	Don't Care	w/ or w/o Signal	w/ or w/o Signal	w/ or w/o Signal	VGL1	VGL2	VGL1	VGL3

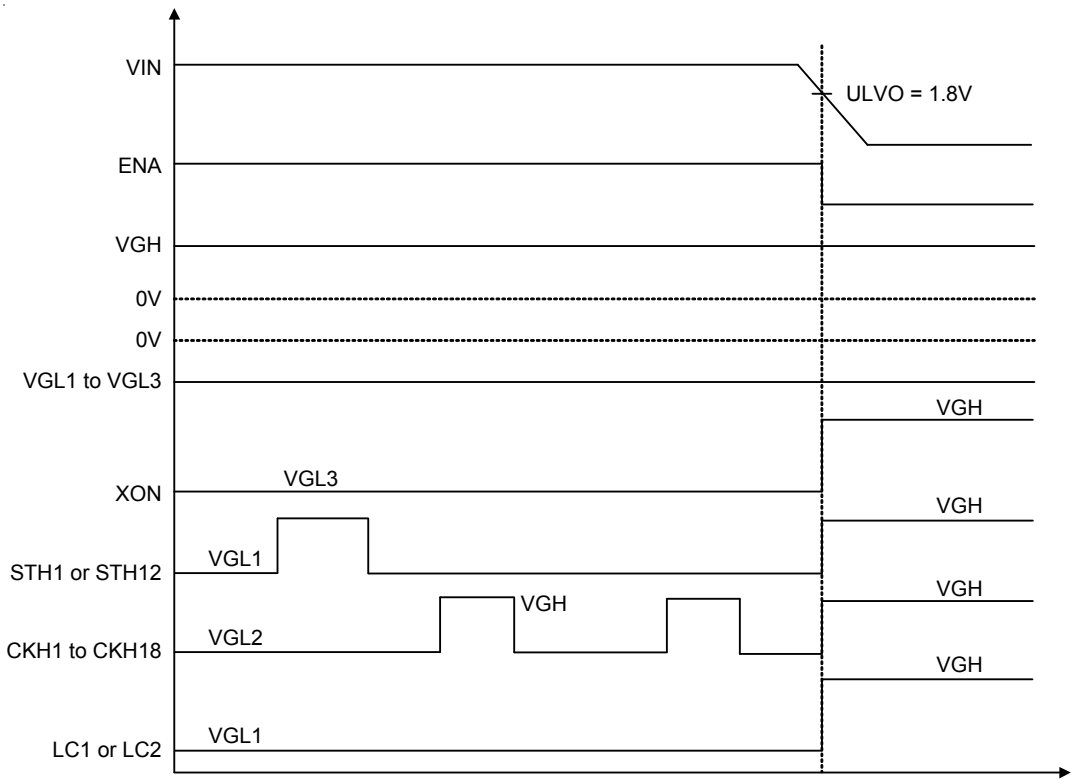


Figure 2. Power Off Sequence

Protection

The RT8935 provides Over-Temperature Protection (OTP), Under-Voltage Lockout (UVLO). The following table shows the main behavior of each protection.

Protection \ Function	Level Shifter
UVLO (Falling), VIN High to Low	V_{GON}
OTP T > 150°C	OFF (Hi-Z)

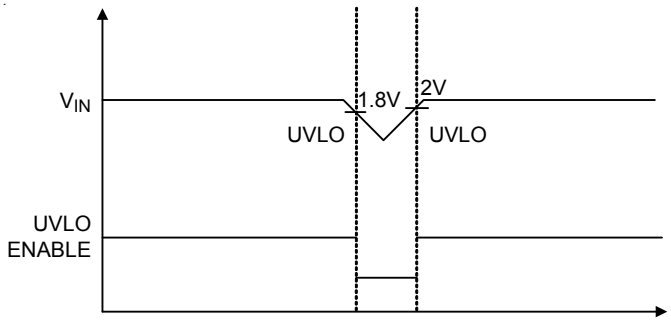
Over-Temperature Protection (OTP)

Over-Temperature Protection prevents the RT8935 from overheating due to excessive power dissipation. When the junction temperature exceeds T_J = 150°C, the OTP will be triggered and latche the device, which also shuts down all outputs. Cycle the VIN (below the UVLO falling threshold) will clear the fault latch and reactivate the device.

Protection \ Function	Level Shifter
OTP, T > 150°C	OFF (Hi-Z)

Under-Voltage Lockout (UVLO)

The UVLO circuit compares the input voltage at VIN with the UVLO threshold (2V rising, 1.8V falling, typ.) to ensure the input voltages is high enough for reliable operation. The 200mV (typ.) hysteresis prevents supply transients from causing a shutdown. Once the VIN exceeds the UVLO rising threshold, start-up begins. When VIN falls below the UVLO falling threshold, the controller turns off all of IC internal functions.



Protection \ Function	Level Shifter
UVLO (Falling), VIN High to Low, VGH > UVLOGH	V_{GH}

Level Shift Function

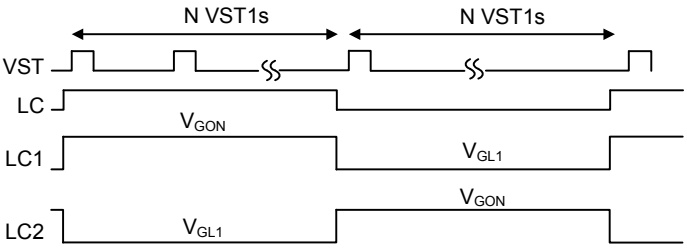
The RT8935 contains 12-channels level shifter. It is for GOA (Gate On Array) tech. There are 4 signals to generate STH1 to STH2, LC1 to LC2, and CKH1 to CKH8. V_{GL2} is the low voltage level for CKH1 to CKH8. V_{GL1} is the low voltage level for STH1 to STH2 and LC1 to LC2. Settings of level shifter output are listed bellow.

Terminate

Terminate signal is used to pull low the gate pulses which no more VCE edges can terminate in blanking. Terminate will be high right after the last VCE falling edge. If Terminate is pull to GND, the gate pulses will be pull low as the next VST rising edge. This pin will to GND with an internal 400kΩ resistor.

LC

For GOA circuit, two low frequency and complementary signals are needed. LC1 will follow LC and have transients between V_{GON} and V_{GL1}. LC2 will be the inverting of LC1. LC has transients before VST rising in the blanking.

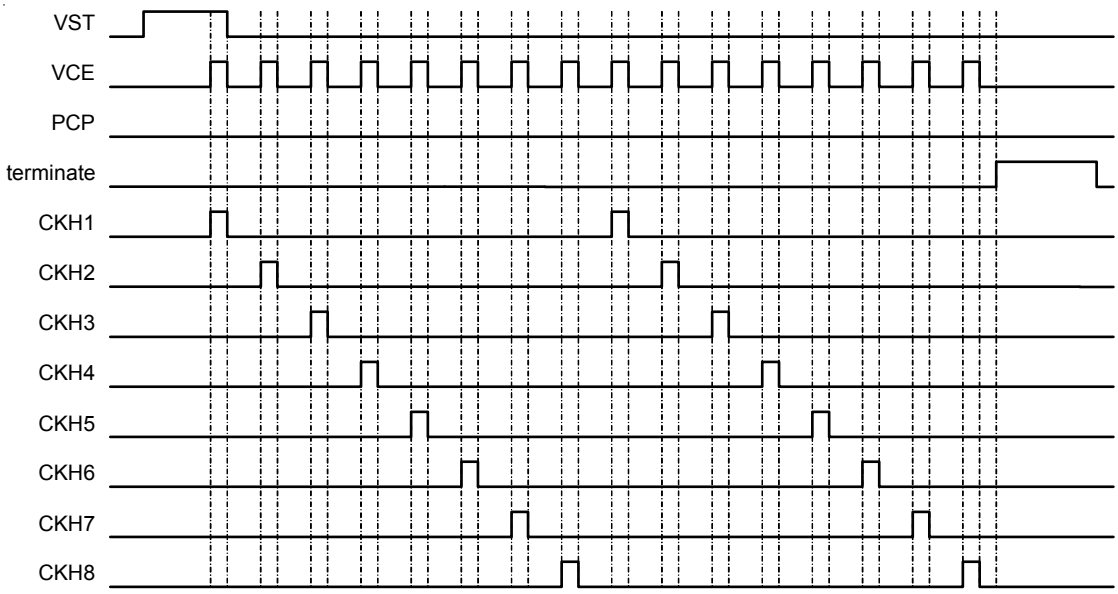


Setting

The SET1/2/3 mode1/mode2 will trigger and latch the function by each VST1 rising edge. The state can not be changed real time except noise interference.

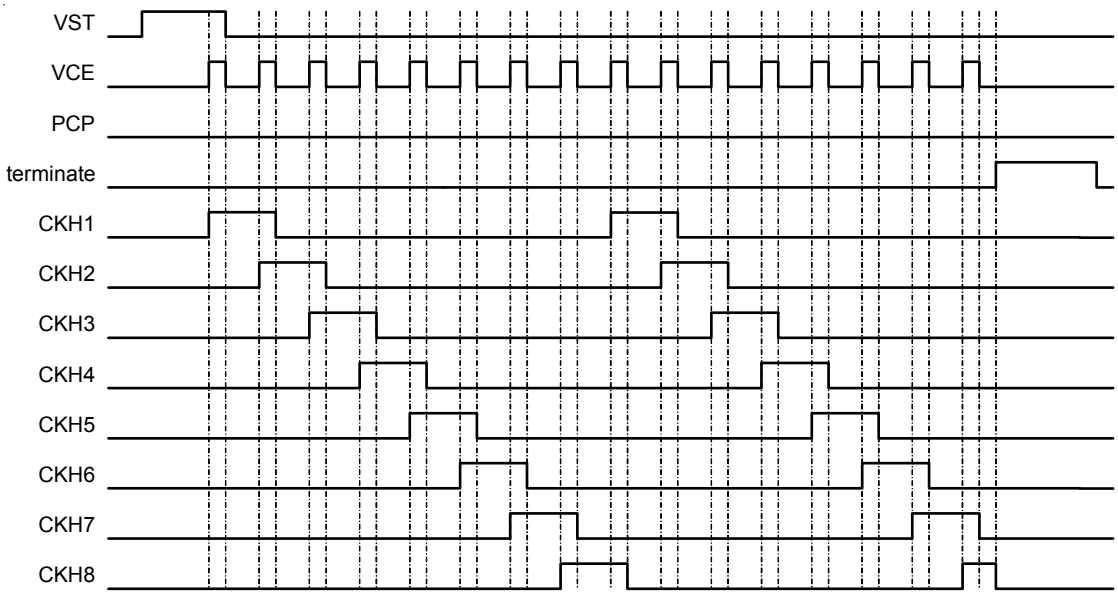
Mode1, Mode2

Mode1, Mode2 are the function of pre-charge type. The Mode1 pin will "don't care" at the 3-line pre-charge function. 8 phase for example, the no pre-charge is CKH1 to CKH8 as below.



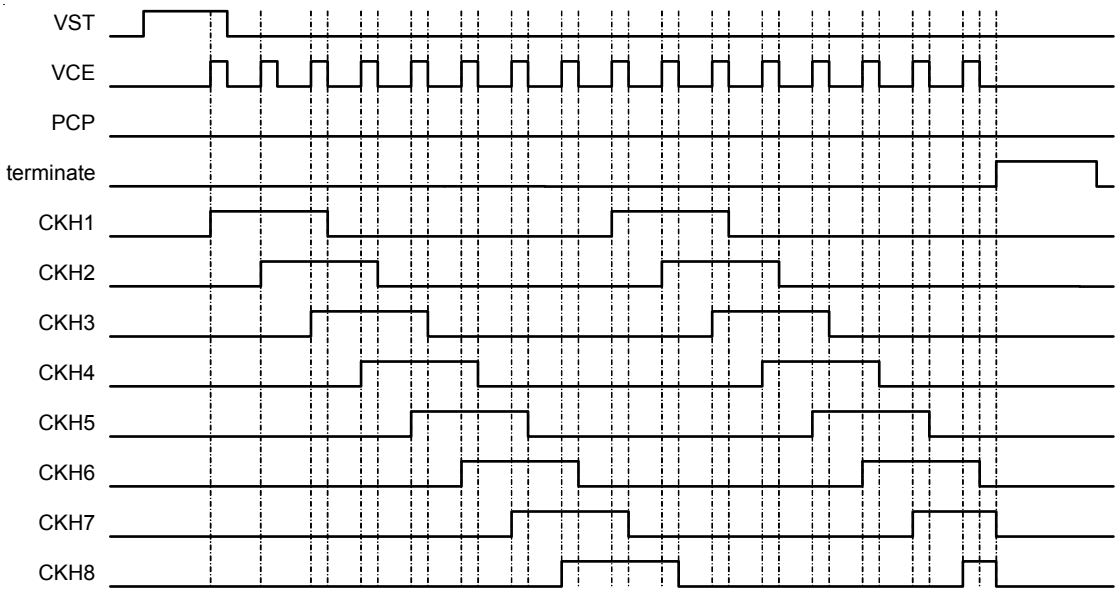
Disable charge sharing mode, No pre-charge

The 1-line pre-charge is CKH1 to CKH8 as below.



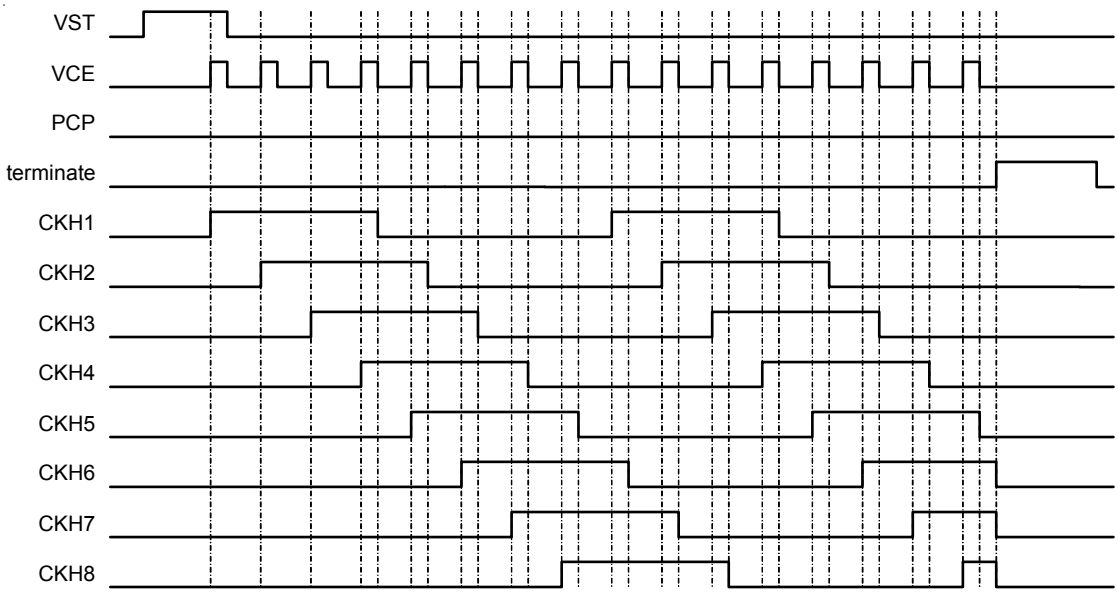
Disable charge sharing mode, 1-line pre-charge

The 2-line pre-charge is CKH1 to CKH8 as below.



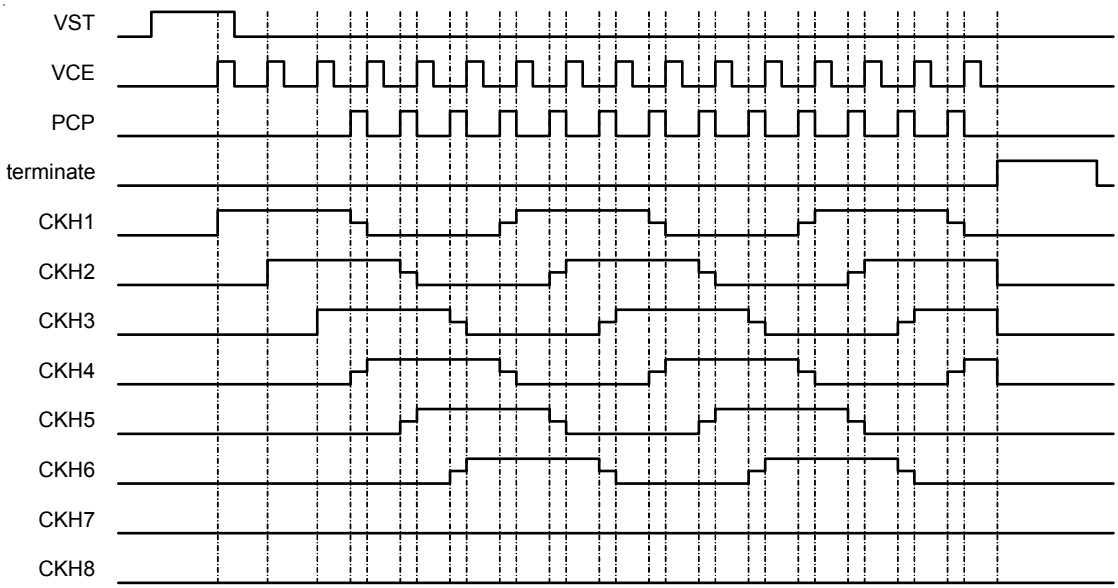
Disable charge sharing mode, 2-line pre-charge

The 3-line pre-charge is CKH1 to CKH8 as below.



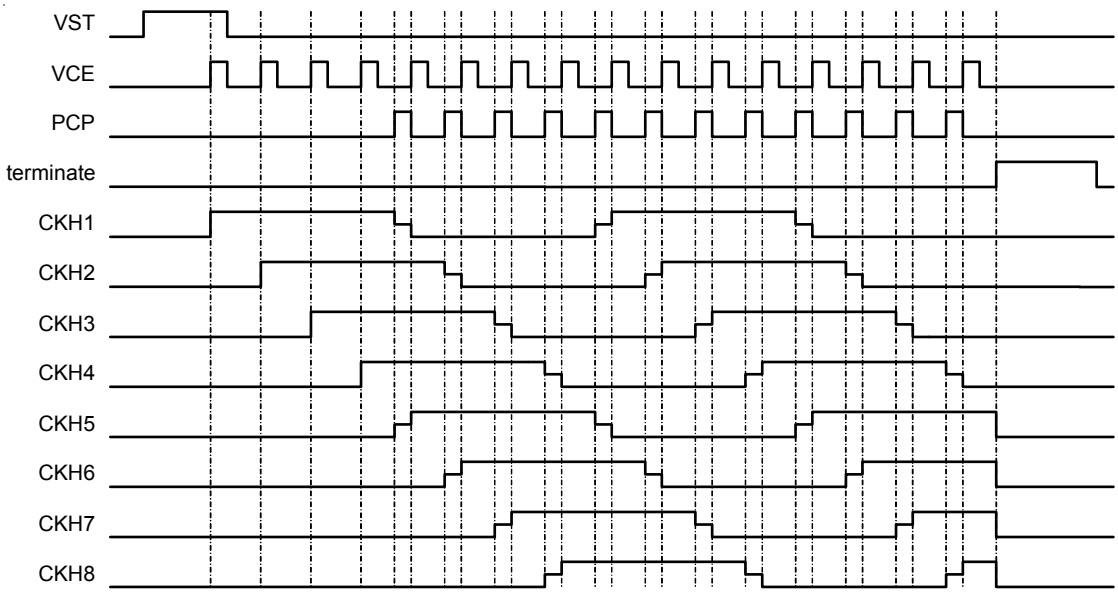
Disable charge sharing mode, 3-line pre-charge

Set3 is the function of charge sharing mode type. The Set2 pin will "don't care" at the charge sharing mode. For example, the waveform [Set1, Set2, Set3, Mode1, Mode2] = [Low, Don't care, High, Don't care, Don't care] is as below.



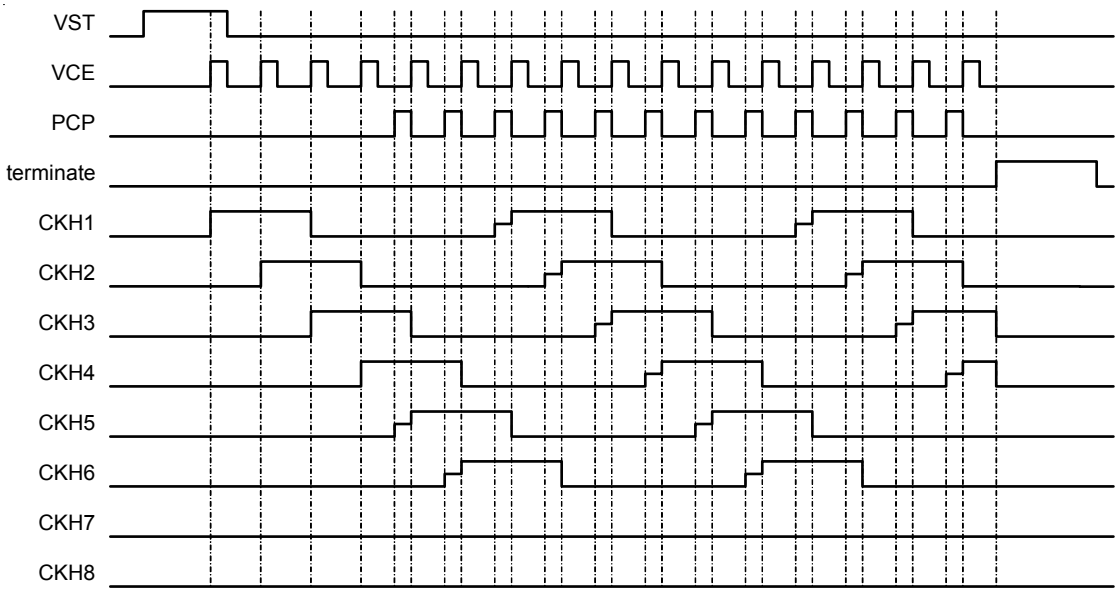
6 phase charge sharing mode 1

The waveform [Set1, Set2, Set3, Mode1, Mode2] = [High, Don't care, High, Don't care, Don't care] is as below.



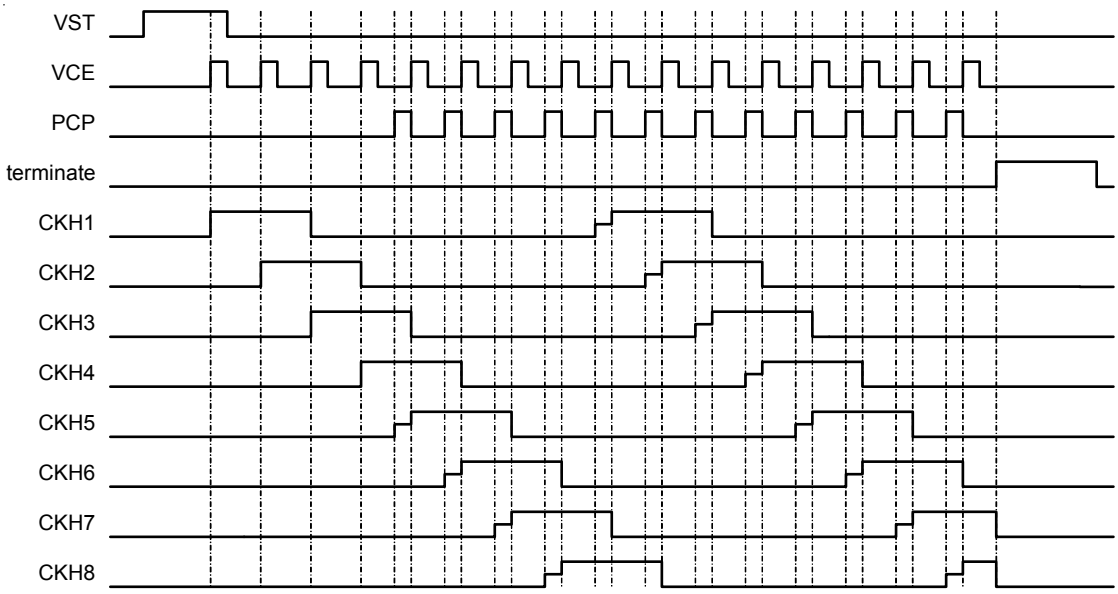
8 phase charge sharing mode 1

The waveform [Set1, Set2, Set3, Mode1, Mode2] = [Low, Don't care, Low, High, Low] is as below.



6 phase 1-line pre-charge charge sharing mode 2

The waveform [Set1, Set2, Set3, Mode1, Mode2] = [High, Don't care, Low, High, Low] is as below.



8 phase 1-line pre-charge charge sharing mode 2

Table 4. The Setting and Mode Table

Pin	Status	Level Shifter Output
SET1	VIN	8 phases. CKH1 to CKH 8 output.
	GND	6 phases. CKH1 to CKH 6 output. CkH7 and 8 keep in VGL2.
	Floating	4 phases. CKH1 to CKH 4 output. CkH5 to 8 keep in VGL2.
SET2	VIN	There is no time interval between CKHs.
	GND/Floating	There is some time interval between CKHs. The time interval can be adjusted by Tcon.
SET3	VIN	Enable charge sharing mode 1.
	GND	Enable charge sharing mode 2.
	Floating	Disable charge sharing mode.
MODE1	Logic signal high	1-line pre-charge.
	Logic signal low	No pre-charge.
	Floating	2-line pre-charge.
MODE2	Logic signal high	3-line pre-charge.
	Logic signal low/Floating	Keep MODE1 Setting.

There are two waveforms to show some settings listed above. The settings in the first waveform are in the first waveform is [Set1, Set2, Set3, Mode1, Mode2] = [Low, Low, Floating, Floating, Low].

The settings in the second waveform are in the second waveform is [Set1, Set2, Set3, Mode1, Mode2] = [Floating, High, Floating, Floating, Low].

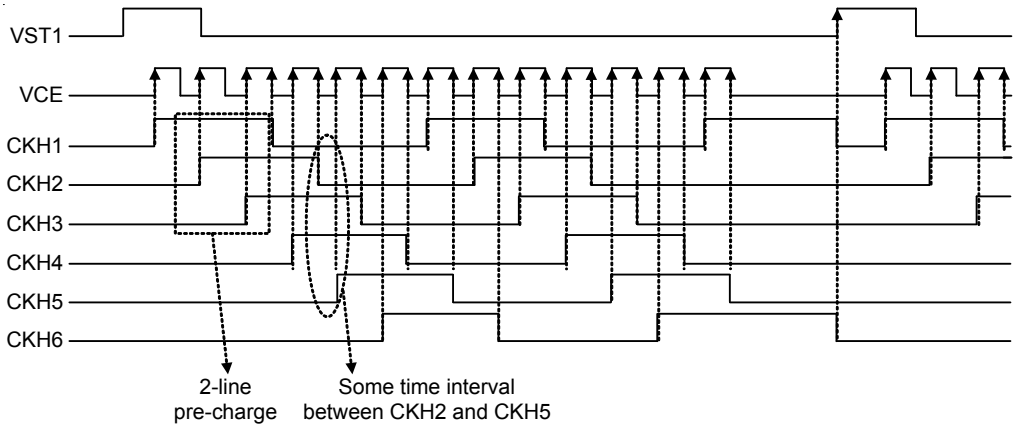


Figure 3. The First Waveform

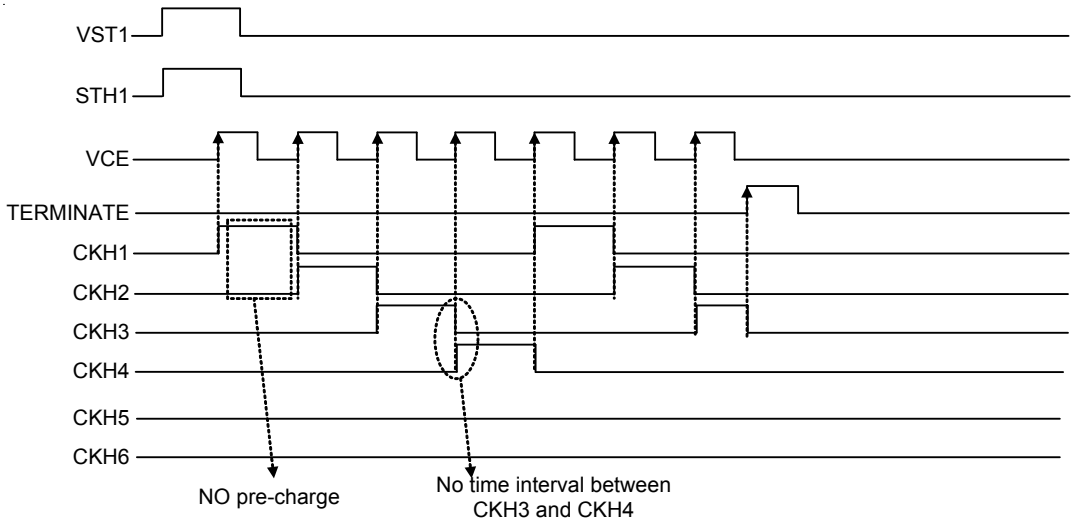


Figure 4. The Second Waveform

XON Function

The RT8935 defines a special output timing of the level-shifter output : Once VIN drops below UVLO falling threshold, all the output (include XON, STH1 to STH2, LC1 to LC2, and CKH1 to CKH8) must be pulled high immediately and simultaneously.

When VIN is abnormal as following diagram, XON function will reset (XON is pulled to V_{GL3}, CKH1 to CKH8 are pulled to V_{GL2}, and STH1 to STH2 and LC1 to LC2 are pulled to V_{GL1}) no mater what voltage level VIN falls to. If VIN falls below UVLO falling in the constraint region, XON function can still be active. That is, XON, CKH1 to CKH8, STH1 to STH2, and LC1 to LC2 are pulled to VGH.

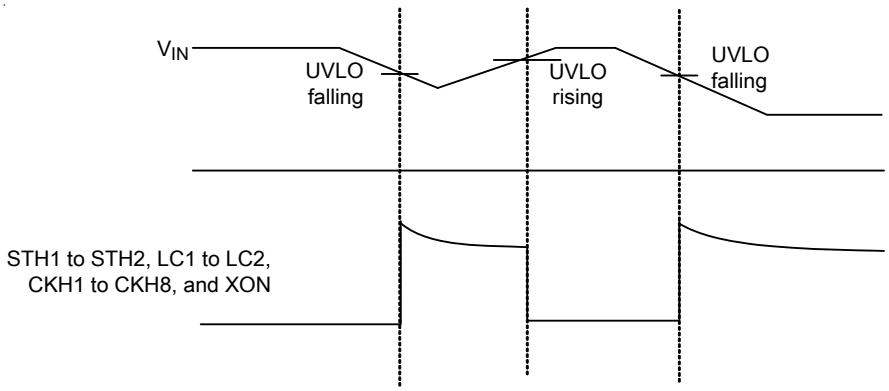


Figure 5. XON Function at Power Off

Timing Chart

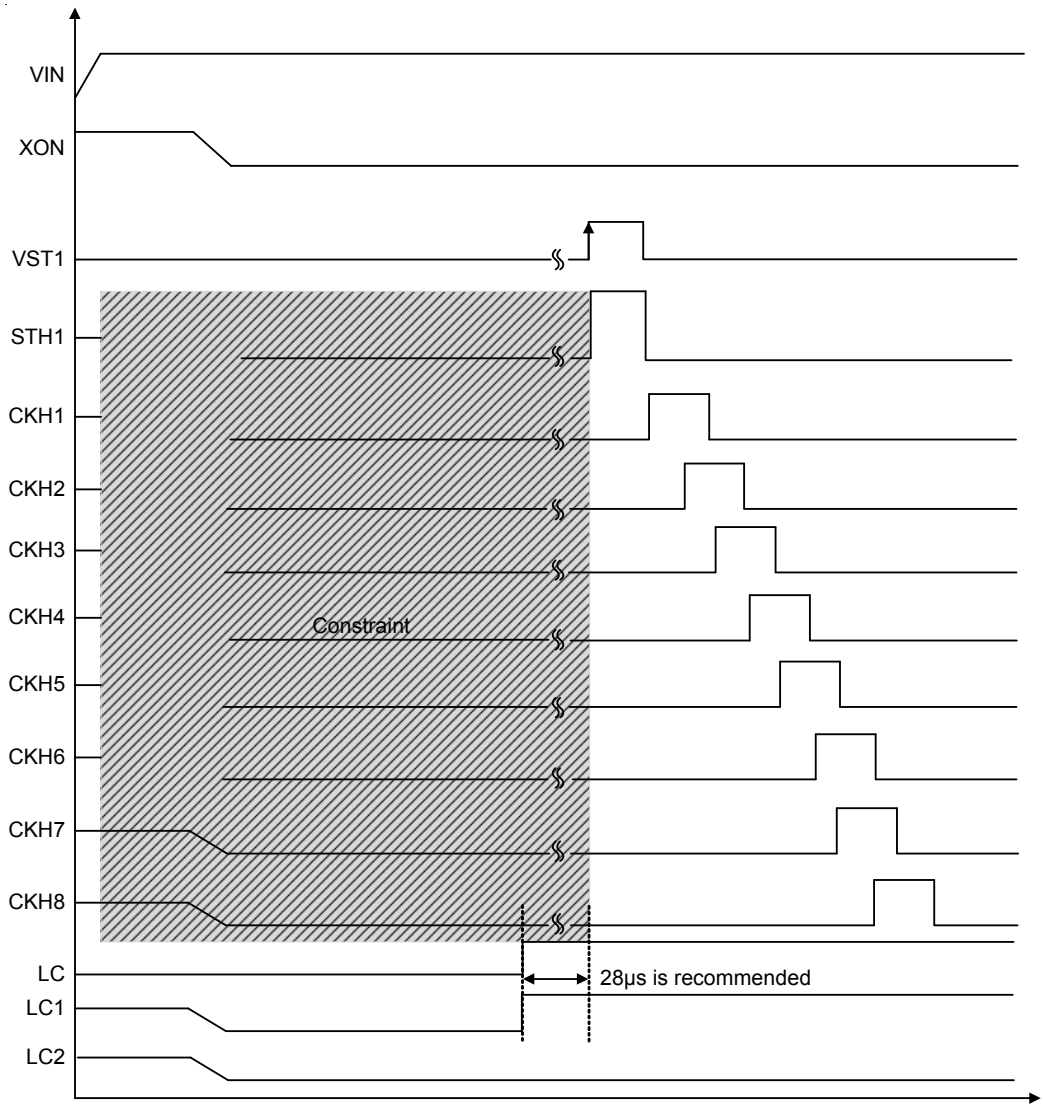


Figure 6. Nornal Operation at Power Off

In normal operation, CKH1 to CKH8 would be kept low within constraint till the 1st VST rising edge to be received. LC1 to LC2 would be kept low till the 1st LC rising edge or 1st VST rising edge to be received.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN 32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 27.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.8°C/W) = 3.59W for a WQFN 32L 4x4 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (27.5°C/W) = 3.64W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

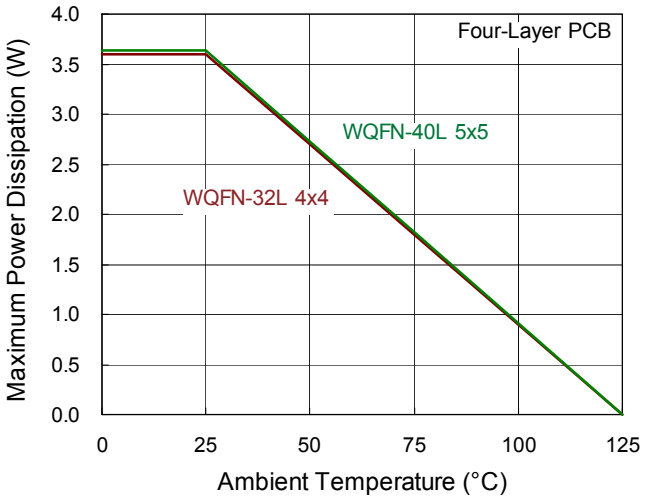
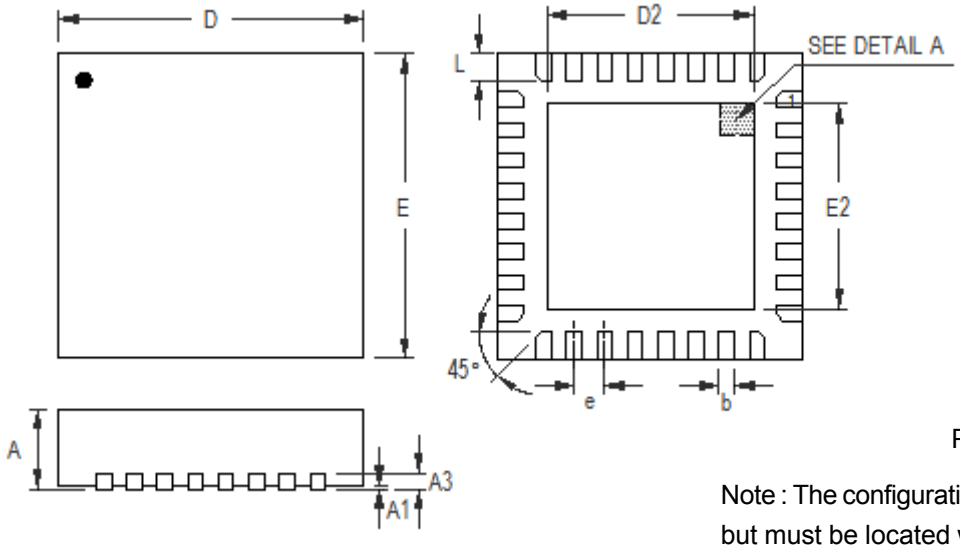


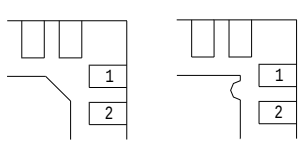
Figure 7. Derating Curve of Maximum Power Dissipation

Layout Consideration

- The VIN input capacitor should be closed the chip.
- The VGH input capacitor should be closed the chip.
- The VGL input capacitor should be closed the chip.
- The exposed pad of the chip should be connected to ground plane for thermal consideration.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016

W-Type 32L QFN 4x4 Package

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