



**MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/
V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S)**

CMOS F²MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller

The MB90540G/545G series with FULL-CAN and Flash ROM is specially designed for automotive and industrial applications. Its main features are on-board CAN Interfaces (MB90540G series: 2 channels, MB90545G series: 1 channel), which conform to CAN V2.0A and V2.0B specifications, supporting very flexible message buffer scheme and so offering more functions than a normal full CAN approach. The instruction set by F²MC-16LX CPU core inherits an AT architecture of the F²MC family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The micro controller has a 32-bit accumulator for processing long word data. The MB90540G/545G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interfaces, 8/16-bit timer, I/O timer (input capture (ICU), output compare (OCU)).

Features

- Clock
 - Embedded PLL clock multiplication circuit
 - Operating clock (PLL clock) can be selected from : divided-by-2 of oscillation or one to four times the oscillation
 - Minimum instruction execution time : 62.5 ns (operation at oscillation of 4 MHz, PLL four times multiplied : machine clock 16 MHz and at operating V_{CC} = 5.0 V)
- Subsystem Clock : 32 kHz
- Instruction set to optimize controller applications
 - Rich data types (bit, byte, word, long word)
 - Rich addressing mode (23 types)
 - Enhanced signed multiplication/division instruction and RETI instruction functions
 - Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
 - Adoption of system stack pointer
 - Enhanced pointer indirect instructions
 - Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed : 4-byte Instruction queue
- Enhanced interrupt function : 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
 - Extended intelligent I/O service function (EI²OS)
- Embedded ROM size and types
 - MASK ROM : 256 Kbytes / 64 Kbytes / 128 Kbytes
 - Flash ROM : 128 Kbytes/256 Kbytes
 - Embedded RAM size : 2 Kbytes/4 Kbytes/6 Kbytes/8 Kbytes (evaluation chip)
- Flash ROM
 - Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands
 - A flag indicating completion of the algorithm
 - Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory
- Erase can be performed on each block
- Block protection with external programming voltage
- Low-power consumption (stand-by) mode
 - Sleep mode (mode in which CPU operating clock is stopped)
 - Stop mode (mode in which oscillation is stopped)
 - CPU intermittent operation mode
 - Watch mode
 - Hardware stand-by mode
- Process
 - 0.5 μm CMOS technology
- I/O port
 - General-purpose I/O ports : 81 ports
- Timer
 - Watchdog timer : 1 channel
 - 8/16-bit PPG timer : 8/16-bit × 4 channels
 - 16-bit reload timer : 2 channels
- 16-bit I/O timer
 - 16-bit free-run timer : 1 channel
 - Input capture : 8 channels
 - Output compare : 4 channels
- Extended I/O serial interface : 1 channel
- UART0
 - With full-duplex double buffer (8-bit length)
 - Clock asynchronous or clock synchronized (with start/stop bit) transmission can be selectively used.
- UART 1 (SCI)
 - With full-duplex double buffer (8-bit length)
 - Clock asynchronous or clock synchronized serial (extended I/O serial) can be used.
- External interrupt circuit (8 channels)
 - A module for starting an extended intelligent I/O service (EI²OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module
 - Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
 - 8/10-bit resolution can be selectively used.

Starting by an external trigger input.
Conversion time : 26.3 μ s

■ FULL-CAN interfaces

MB90540G series : 2 channels

MB90545G series : 1 channel

Conforming to Version 2.0 Part A and Part B

Flexible message buffering (mailbox and FIFO buffering can be mixed)

■ External bus interface : Maximum address space 16 Mbytes

■ Package: QFP-100, LQFP-100

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1. Product Lineup

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, 1/2 when PLL stop) Minimum instruction execution time : 62.5 ns (machine clock 16MHz, 4MHz osc. four times multiplied by PLL)		
ROM	Flash memory MB90F543G(S)/F548G(S) / F548GL(S) : 128 Kbytes MB90F549G(S)/F546G(S) : 256 Kbytes	MASK ROM : MB90547G(S): 64 Kbytes MB90543G(S)/548G(S): 128 Kbytes MB90549G(S): 256 Kbytes	External
RAM	MB90F548G(S)/F548GL(S): 4 Kbytes MB90F543G (S) /F549G(S) : 6 Kbytes MB90F546G(S) : 8 Kbytes	MB90547G(S): 2 Kbytes MB90548G(S): 4 Kbytes MB90543G(S)/549G(S): 6 Kbytes	8 Kbytes
Clocks	MB90F543G/F548G/F549G/F546G/ F548GL : Two clocks system MB90F543GS/F548GS/F549GS/ F546GS/F548GLS : One clock system	MB90543G/547G/548G/549G : Two clocks system MB90543GS/547GS/548GS/ 549GS : One clock system	Two clocks system*1
Operating voltage range	*3		
Temperature range	-40 °C to 105 °C		
Package	QFP100, LQFP100		PGA-256
Emulator-specify power supply ²	—		None
UART0	Full duplex double buffer Support asynchronous/synchronous (with start/stop bit) transfer Baud rate : 4808/5208/9615/10417/19230/38460/62500/500000 bps (asynchronous) 500 K/1 M/2 Mbps (synchronous) at System clock = 16 MHz		
UART1 (SCI)	Full duplex double buffer Asynchronous (start-stop synchronized) and CLK-synchronous communication Baud rate : 1202/2404/4808/9615/19230/31250/38460/62500 bps (asynchronous) 62.5 K/125 K/250 K/500 K/1 M/2 Mbps (synchronous) at 6, 8, 10, 12, 16 MHz		
Serial I/O	Transfer can be started from MSB or LSB Supports internal clock synchronized transfer and external clock synchronized transfer Supports positive-edge and negative-edge clock synchronization Baud rate : 31.25 K/62.5 K/125 K/500 K/1 Mbps at System clock = 16 MHz		
A/D Converter	10-bit or 8-bit resolution 8 input channels Conversion time : 26.3 μs (per one channel)		

(Continued)

Features	MB90F543G (S) /F548G (S) MB90F549G (S) /F546G (S) MB90F548GL(S)	MB90543G (S) MB90547G (S) MB90548G (S) MB90549G (S)	MB90V540G
16-bit Reload Timer (2 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = System clock frequency) Supports External Event Count function Signals an interrupt when overflow		
16-bit Free-run Timer	Supports Timer Clear when a match with Output Compare (Channel 0) Operation clock freq. : $f_{sys}/2^2$, $f_{sys}/2^4$, $f_{sys}/2^6$, $f_{sys}/2^8$ (f_{sys} = System clock freq.)		
16-bit Output Compare (4 channels)	Signals an interrupt when a match with 16-bit Free-run Timer Four 16-bit compare registers A pair of compare registers can be used to generate an output signal		
16-bit Input Capture (8 channels)	Rising edge, falling edge or rising & falling edge sensitive Four 16-bit Capture registers Signals an interrupt upon external event		
8/16-bit Programmable Pulse Generator (4 channels)	Supports 8-bit and 16-bit operation modes Eight 8-bit reload counters Eight 8-bit reload registers for L pulse width Eight 8-bit reload registers for H pulse width A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter 4 output pins Operation clock freq. : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = System clock frequency, f_{osc} = Oscillation clock frequency)		
CAN Interface MB90540G series : 2 channels MB90545G series : 1 channel	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		
32 kHz Sub-clock	Sub-clock for low power operation		
External Interrupt (8 channels)	Can be programmed edge sensitive or level sensitive		
External bus interface	External access using the selectable 8-bit or 16-bit bus is enabled (external bus mode.)		
I/O Ports	Virtually all external pins can be used as general purpose I/O All push-pull outputs and schmitt trigger inputs Bit-wise programmable as input/output or peripheral signal Sub-clock for 32 kHz Sub clock low power operation		
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Erase-Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block Block protection by externally programmed voltage		

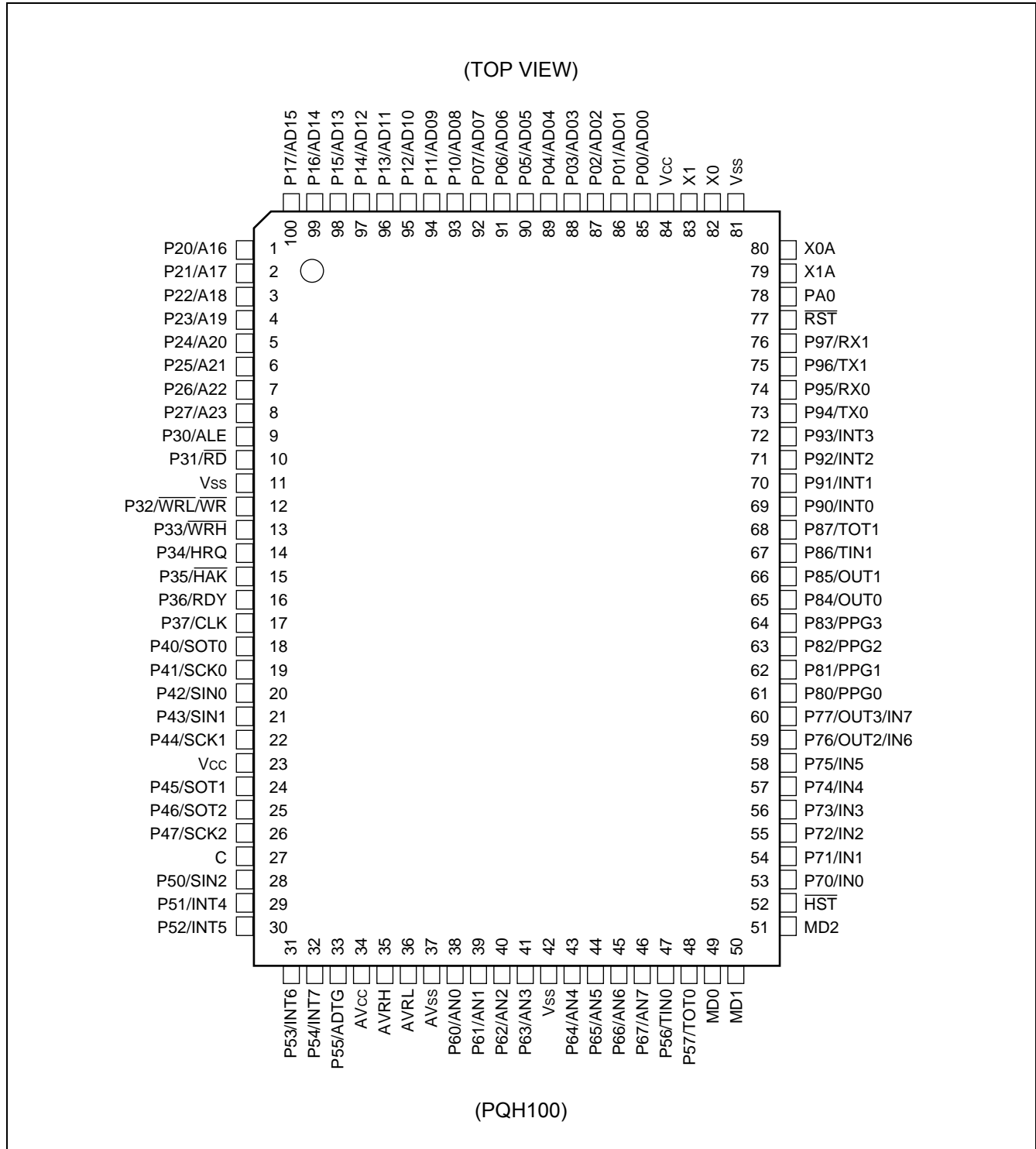
*1 : If the one clock system is used, equip X0A and X1A with clocks from the tool side.

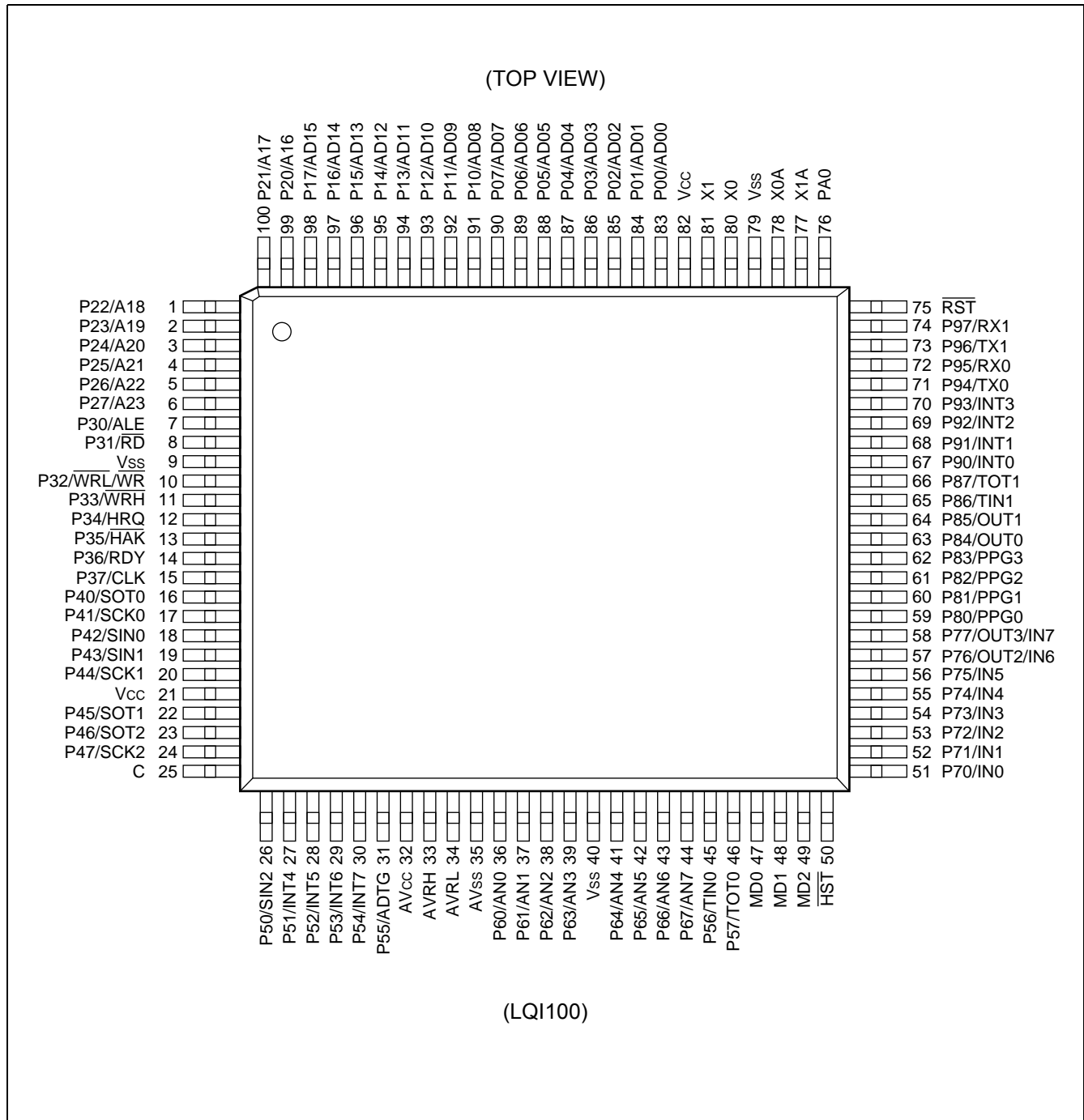
*2 : It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used. Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*3 : Operating Voltage Range

Products	Operation guarantee range
MB90F543G(S)/F546G(S)/F548G(S)/ MB90549G(S)/F549G(S)/V540/V540G	4.5 V to 5.5 V
MB90F548GL(S)/543G(S)/547G(S)/548G(S)	3.5 V to 5.5 V

2. Pin Assignment





3. Pin Description

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
80 81	82 83	X0 X1	A (Oscillation)	High speed crystal oscillator input pins
78	80	X0A	A (Oscillation)	Low speed crystal oscillator input pins. For the one clock system parts, perform external pull-down processing.
77	79	X1A		Low speed crystal oscillator input pins. For the one clock system parts, leave it open.
75	77	$\overline{\text{RST}}$	B	External reset request input pin
50	52	$\overline{\text{HST}}$	C	Hardware standby input pin
83 to 90	85 to 92	P00 to P07	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
91 to 98	93 to 100	P10 to P17	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		AD08 to AD15		I/O pins for 8 higher bits of the external address/data bus. This function is enabled when the external bus is enabled.
99 to 6	1 to 8	P20 to P27	I	General I/O port with programmable pullup. In external bus mode, this function is valid when the corresponding bits in the external address output control register (HACR) are set to "1".
		A16 to A23		8-bit I/O pins for A16 to A23 at the external address/data bus. In external bus mode, this function is valid when the corresponding bits in the external address output control register (HACR) are set to "0".
7	9	P30	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
8	10	P31	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode.
		$\overline{\text{RD}}$		Read strobe output pin for the data bus. This function is enabled when the external bus is enabled.
10	12	P32	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output is disabled.
		$\overline{\text{WRL}}$		Write strobe output pin for the data bus. This function is enabled when both the external bus and the $\overline{\text{WR}}/\overline{\text{WRL}}$ pin output are enabled. $\overline{\text{WRL}}$ is write-strobe output pin for the lower 8 bits of the data bus in 16-bit access.
		$\overline{\text{WR}}$		$\overline{\text{WR}}$ is write-strobe output pin for the 8 bits of the data bus in 8-bit access.

(Continued)

Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
11	13	P33	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode, external bus 8-bit mode or when WRH pin output is disabled.
		$\overline{\text{WRH}}$		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.
12	14	P34	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold functions are enabled.
13	15	P35	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold functions are enabled.
14	16	P36	I	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready functions are enabled.
15	17	P37	H	General I/O port with programmable pullup. This function is enabled in the single-chip mode or when the CLK output is disabled.
		CLK		CLK output pin. This function is enabled when both the external bus and CLK outputs are enabled.
16	18	P40	G	General I/O port. This function is enabled when UART0 disables the serial data output.
		SOT0		Serial data output pin for UART0. This function is enabled when UART0 enables the serial data output.
17	19	P41	G	General I/O port. This function is enabled when UART0 disables serial clock output.
		SCK0		Serial clock I/O pin for UART0. This function is enabled when UART0 enables the serial clock output.
18	20	P42	G	General I/O port. This function is always enabled.
		SIN0		Serial data input pin for UART0. Set the corresponding Port Direction Register to input if this function is used.
19	21	P43	G	General I/O port. This function is always enabled.
		SIN1		Serial data input pin for UART1. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
20	22	P44	G	General I/O port. This function is enabled when UART1 disables the clock output.
		SCK1		Serial clock pulse I/O pin for UART1. This function is enabled when UART1 enables the serial clock output.
22	24	P45	G	General I/O port. This function is enabled when UART1 disables the serial data output.
		SOT1		Serial data output pin for UART1. This function is enabled when UART1 enables the serial data output.
23	25	P46	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the serial data output.
		SOT2		Serial data output pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the serial data output.
24	26	P47	G	General I/O port. This function is enabled when the Extended I/O serial interface disables the clock output.
		SCK2		Serial clock pulse I/O pin for the Extended I/O serial interface. This function is enabled when the Extended I/O serial interface enables the Serial clock output.
26	28	P50	D	General I/O port. This function is always enabled.
		SIN2		Serial data input pin for the Extended I/O serial interface. Set the corresponding Port Direction Register to input if this function is used.
27 to 30	29 to 32	P51 to P54	D	General I/O port. This function is always enabled.
		INT4 to INT7		External interrupt request input pins for INT4 to INT7. Set the corresponding Port Direction Register to input if this function is used.
31	33	P55	D	General I/O port. This function is always enabled.
		ADTG		Trigger input pin for the A/D converter. Set the corresponding Port Direction Register to input if this function is used.
36 to 39	38 to 41	P60 to P63	E	General I/O port. This function is enabled when the analog input enable register specifies a port.
		AN0 to AN3		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
41 to 44	43 to 46	P64 to P67	E	General I/O port. The function is enabled when the analog input enable register specifies a port.
		AN4 to AN7		Analog input pins for the 8/10-bit A/D converter. This function is enabled when the analog input enable register specifies A/D.
45	47	P56	D	General I/O port. This function is always enabled.
		TIN0		Event input pin for the 16-bit reload timers 0. Set the corresponding Port Direction Register to input if this function is used.

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Pin No.		Pin name	Circuit type	Function
LQFP ²	QFP ¹			
46	48	P57	D	General I/O port. This function is enabled when the 16-bit reload timers 0 disables the output.
		TOT0		Output pin for the 16-bit reload timers 0. This function is enabled when the 16-bit reload timers 0 enables the output.
51 to 56	53 to 58	P70 to P75	D	General I/O ports. This function is always enabled.
		IN0 to IN5		Trigger input pins for input captures ICU0 to ICU5. Set the corresponding Port Direction Register to input if this function is used.
57 , 58	59 , 60	P76 , P77	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT2 , OUT3		Event output pins for output compares OCU2 and OCU3. This function is enabled when the OCU enables the waveform output.
		IN6 , IN7		Trigger input pins for input captures ICU6 and ICU7. Set the corresponding Port Direction Register to input and disable the OCU waveform output if this function is used.
59 to 62	61 to 64	P80 to P83	D	General I/O ports. This function is enabled when 8/16-bit PPG disables the waveform output.
		PPG0 to PPG3		Output pins for 8/16-bit PPGs. This function is enabled when 8/16-bit PPG enables the waveform output.
63 , 64	65 , 66	P84 , P85	D	General I/O ports. This function is enabled when the OCU disables the waveform output.
		OUT0 , OUT1		Waveform output pins for output compares OCU0 and OCU1. This function is enabled when the OCU enables the waveform output.
65	67	P86	D	General I/O port. This function is always enabled.
		TIN1		Input pin for the 16-bit reload timers 1. Set the corresponding Port Direction Register to input if this function is used.
66	68	P87	D	General I/O port. This function is enabled when the 16-bit reload timers 1 disables the output.
		TOT1		Output pin for the 16-bit reload timers 1. This function is enabled when the 16-bit reload timers 1 enables the output.
67 to 70	69 to 72	P90 to P93	D	General I/O port. This function is always enabled.
		INT0 to INT3		External interrupt request input pins for INT0 to INT3. Set the corresponding Port Direction Register to input if this function is used.
71	73	P94	D	General I/O port. This function is enabled when CAN0 disables the output.
		TX0		TX output pin for CAN0. This function is enabled when CAN0 enables the output.

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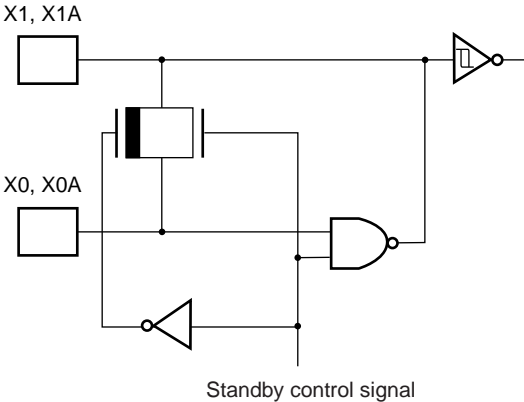
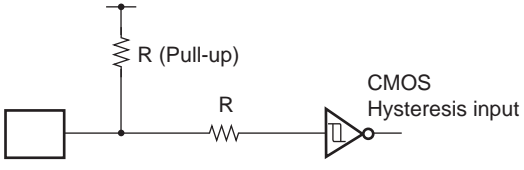

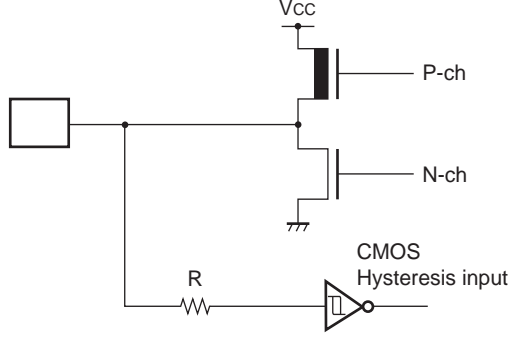
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Pin No.		Pin name	Circuit type	Function
LQFP ^{*2}	QFP ^{*1}			
72	74	P95	D	General I/O port. This function is always enabled.
		RX0		RX input pin for CAN0 Interface. When the CAN function is used, output from the other functions must be stopped.
73	75	P96	D	General I/O port. This function is enabled when CAN1 disables the output.
		TX1		TX output pin for CAN1. This function is enabled when CAN1 enables the output (only MB90540G series) .
74	76	P97	D	General I/O port. This function is always enabled.
		RX1		RX input pin for CAN1 Interface. When the CAN function is used, output from the other functions must be stopped (only MB90540G series) .
76	78	PA0	D	General I/O port. This function is always enabled.
32	34	AV _{CC}	Power supply	Power supply pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AV _{CC} is applied to V _{CC} .
35	37	AV _{SS}	Power supply	Power supply pin for the A/D Converter.
33	35	AVRH	Power supply	External reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	36	AVRL	Power supply	External reference voltage input pin for the A/D Converter.
47, 48	49, 50	MD0, MD1	C	Input pins for specifying the operating mode. The pins must be directly connected to V _{CC} or V _{SS} .
49	51	MD2	F	Input pin for specifying the operating mode. The pin must be directly connected to V _{CC} or V _{SS} .
25	27	C	—	Power supply stabilization capacitor pin. It should be connected externally to an 0.1 μF ceramic capacitor.
21, 82	23, 84	V _{CC}	Power supply	Input pin for power supply (5.0 V) .
9, 40, 79	11, 42, 81	V _{SS}	Power supply	Input pin for power supply (0.0 V) .

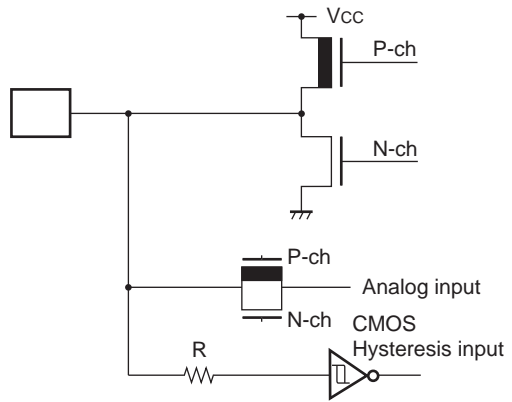
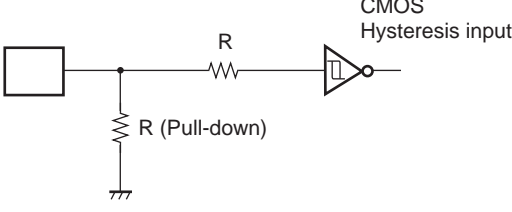
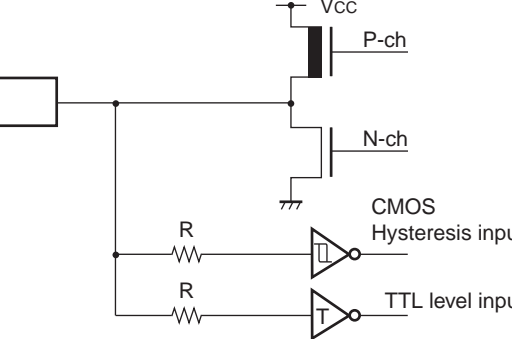
*1 : PQH100

*2 : LQI100

4. I/O Circuit Type

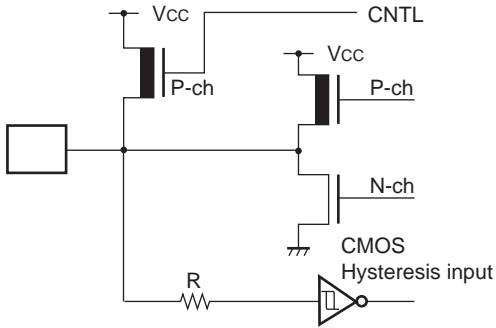
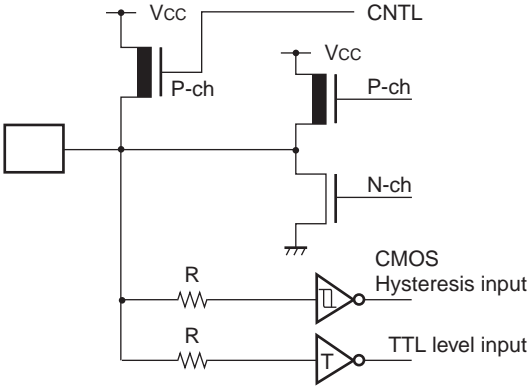
Circuit type	Diagram	Remarks
A		<ul style="list-style-type: none"> ■ High-speed oscillation feedback resistor : 1 MΩ approx. ■ Low-speed oscillation feedback resistor: 10 MΩ approx.
B		<ul style="list-style-type: none"> ■ CMOS Hysteresis input ■ Pull-up resistor : 50 kΩ approx.
C		<ul style="list-style-type: none"> ■ CMOS Hysteresis input
D		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input

(Continued)

Circuit type	Diagram	Remarks
E		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ Analog input
F		<ul style="list-style-type: none"> ■ CMOS Hysteresis input ■ Pull-down Resistor : 50 kΩ approx. (except Flash devices)
G		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only)

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Circuit type	Diagram	Remarks
H		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ Programmable pull-up resistor : 50 kΩ approx.
I		<ul style="list-style-type: none"> ■ CMOS level output ■ CMOS Hysteresis input ■ TTL level input (Flash devices in Flash writer mode only) ■ Programmable pullup resistor : 50 kΩ approx.

5. Handling Devices

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} .
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (AV_{CC} , $AVRH$) to exceed the digital power-supply voltage.

(2) Handling unused pins

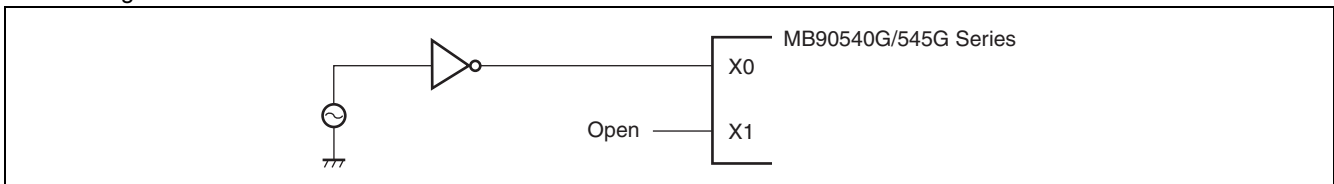
Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than $2\text{ k}\Omega$.

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

(3) Using external clock

To use external clock, drive X0 pin only and leave X1 pin unconnected.

Below is a diagram of how to use external clock.



(4) Use of the sub-clock

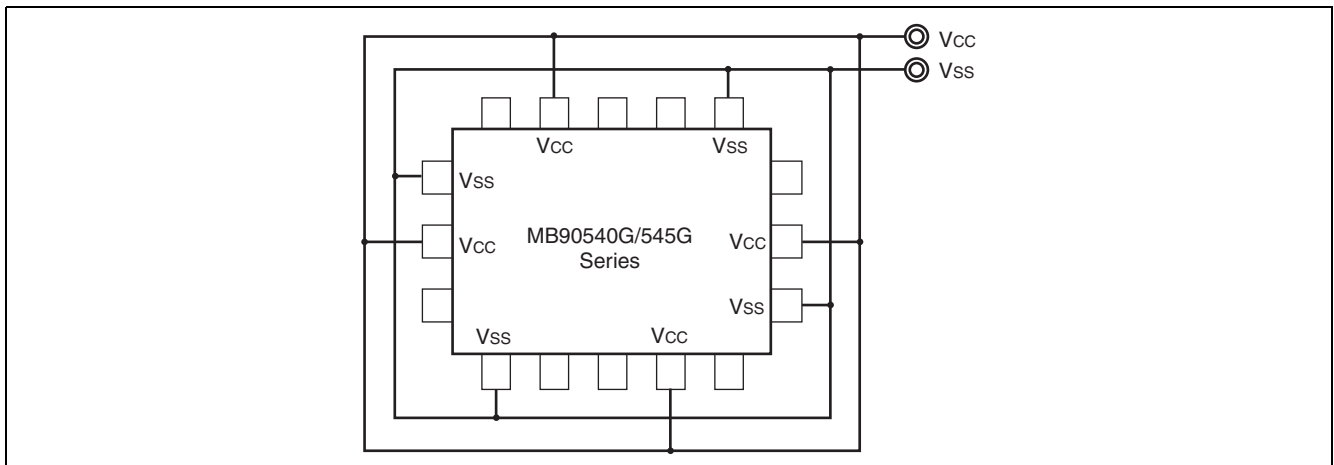
Use one clock system parts when the sub-clock is not used. In that case, pull-down the pin X0A and leave the pin X1A open. When using two clock system parts, a 32 kHz oscillator has to be connected to the X0A and X1A pins.

(5) Power supply pins (V_{CC}/V_{SS})

In products with multiple V_{CC} or V_{SS} pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electromagnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect V_{CC} and V_{SS} pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around $0.1\ \mu\text{F}$ between V_{CC} and V_{SS} pins near the device.



(6) Pull-up/down resistors

The MB90540G/545G Series does not support internal pull-up/down resistors (except Port0 – Port3 : pull-up resistors) . Use external components where needed.

(7) Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via the shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuits do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

(8) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , AV_{RH} , AV_{RL}) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}) .

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AV_{RH} or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable) .

(9) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AV_{RH} = V_{SS}$.

(10) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(11) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V) .

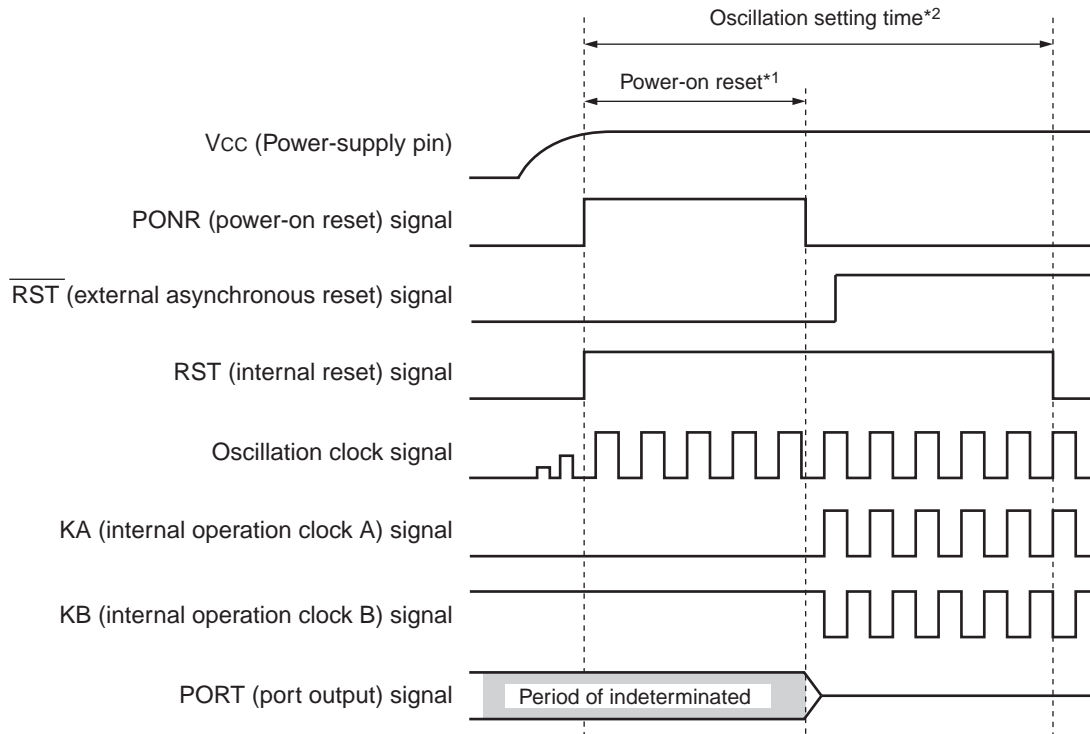
(12) Indeterminate outputs from ports 0 and 1 (MB90V540G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{\text{RST}}$ pin is "H", the outputs become indeterminate.
- If $\overline{\text{RST}}$ pin is "L", the outputs become high-impedance.

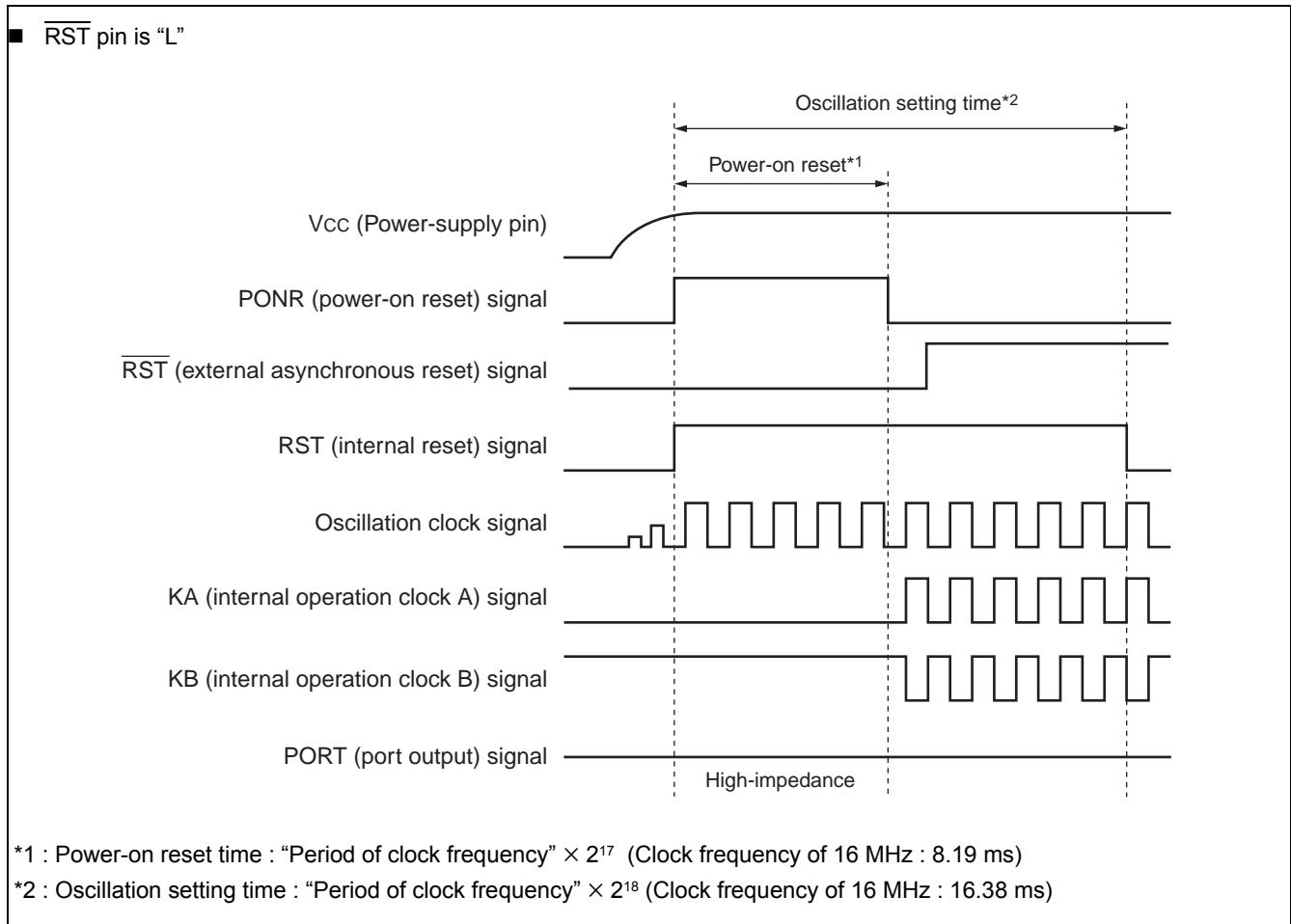
Pay attention to the port output timing shown as follow.

■ $\overline{\text{RST}}$ pin is "H"



*1 : Power-on reset time : "Period of clock frequency" \times 2^{17} (Clock frequency of 16 MHz : 8.19 ms)

*2 : Oscillation setting time : "Period of clock frequency" \times 2^{18} (Clock frequency of 16 MHz : 16.38 ms)



(13) Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(14) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the Signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank registers (DTB, ADB, USB, SSB) are set to other than "00H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

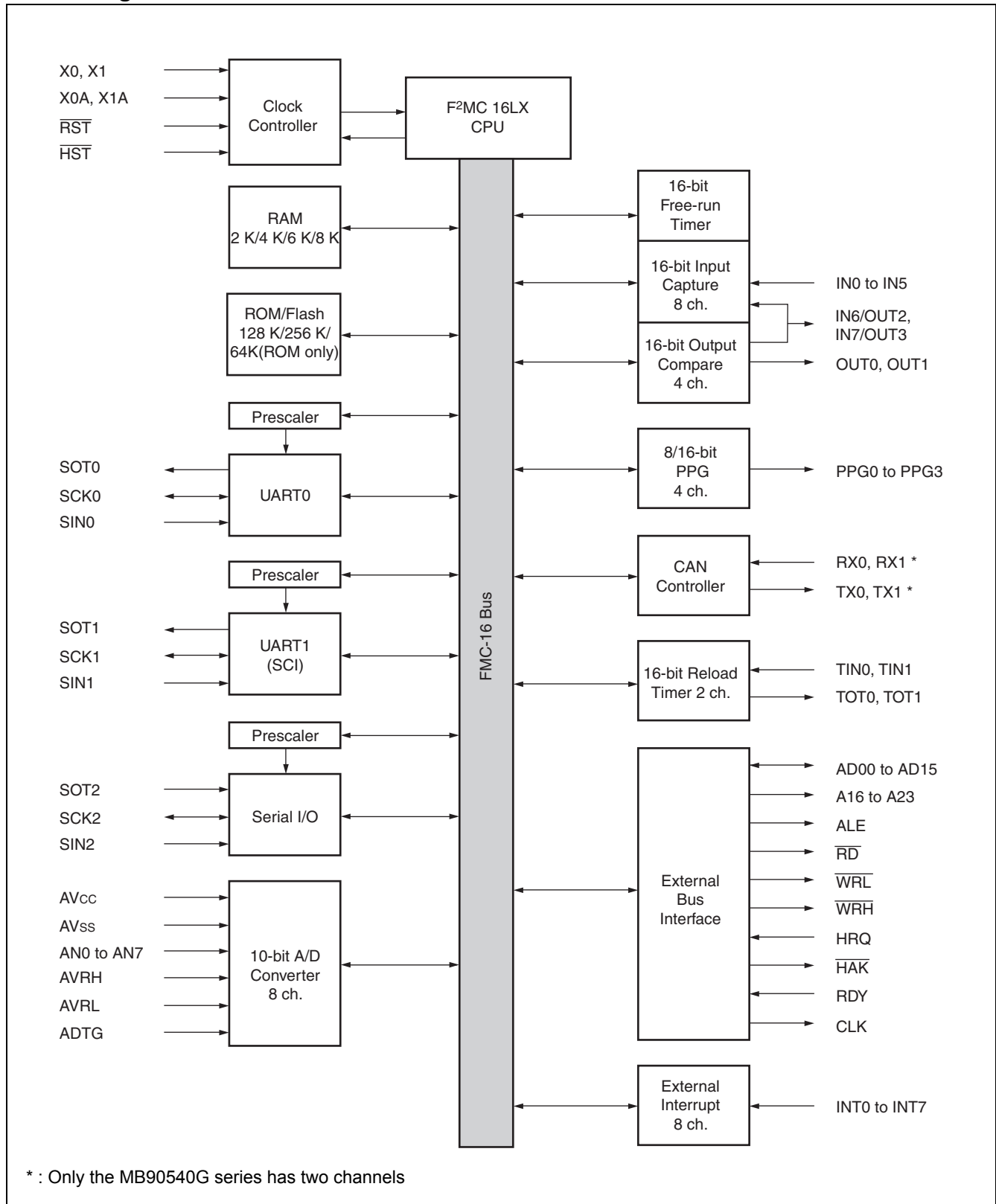
(15) Using REALOS

The use of EI²OS is not possible with the REALOS real time operating system.

(16) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. Block Diagram



7. Memory Map

The memory space of the MB90540G/545G Series is shown below.

MB90V540G/ F546G (S)		MB90543G(S) F543G(S)		MB90548G(S) MB90F548GL(S) MB90F548G (S)		MB90549G (S) / F549G (S)		MB90547G (S)	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)
FF0000H		FF0000H		FF0000H		FF0000H		FF0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)		
FE0000H		FE0000H		FE0000H		FE0000H			
FDFFFFH	ROM (FD bank)		External		External	FDFFFFH	ROM (FD bank)		External
FD0000H						FD0000H			
FCFFFFH	ROM (FC bank)					FCFFFFH	ROM (FC bank)		
FC0000H	External					FC0000H	External		
00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)	00FFFFH	ROM (Image of FF bank)
004000H		004000H		004000H		004000H		004000H	
003FFFH	Peripheral	003FFFH	Peripheral	003FFFH	Peripheral	003FFFH	Peripheral	003FFFH	Peripheral
003900H		003900H		003900H		003900H		003900H	
	External		External		External		External		External
0020FFH		002000H		002000H		002100H		002000H	
001FF5H	ROM correction	0018FFH				0018FFH			
001FF0H			RAM 6 K	0010FFH			RAM 6 K		
	RAM 8 K			000100H		000100H		0008FFH	RAM 2 K
000100H	External	000100H	External	000100H	External	000100H	External	000100H	External
0000BFH	Peripheral	0000BFH	Peripheral	0000BFH	Peripheral	0000BFH	Peripheral	0000BFH	Peripheral
000000H		000000H		000000H		000000H		000000H	

Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits address are the same, the table in ROM can be referenced without using the "far" specification in the pointer declaration. For example, an attempt to access 00C000H accesses the value at FFC000H in ROM. The ROM area in bank FF exceeds 48 Kbytes, and its entire image cannot be shown in bank 00. The image between FF4000H and FFFFFFFH is visible in bank 00, while the image between FF0000H and FF3FFFH is visible only in bank FF.

8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00 _H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 data register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 data register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 data register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 data register	PDR9	R/W	Port 9	XXXXXXXX _B
0A _H	Port A data register	PDRA	R/W	Port A	_____X _B
0B _H to 0F _H	Reserved				
10 _H	Port 0 direction register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
11 _H	Port 1 direction register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
12 _H	Port 2 direction register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
13 _H	Port 3 direction register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
14 _H	Port 4 direction register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 _B
15 _H	Port 5 direction register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 _B
16 _H	Port 6 direction register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 _B
17 _H	Port 7 direction register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 _B
18 _H	Port 8 direction register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 _B
19 _H	Port 9 direction register	DDR9	R/W	Port 9	0 0 0 0 0 0 0 0 _B
1A _H	Port A direction register	DDRA	R/W	Port A	_____0 _B
1B _H	Analog Input Enable register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 _B
1C _H	Port 0 Pullup control register	PUCR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
1D _H	Port 1 Pullup control register	PUCR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
1E _H	Port 2 Pullup control register	PUCR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
1F _H	Port 3 Pullup control register	PUCR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
20 _H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0 _B
21 _H	Serial Status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 _B
22 _H	Serial input data register 0/ Serial output data register 0	UIDR0/UODR0	R/W		XXXXXXXX _B
23 _H	Rate and data register 0	URD0	R/W		0 0 0 0 0 0 0 X _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
24 _H	Serial mode register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial control register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial input data register 1/ Serial output data register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial status register 1	SSR1	R/W		0 0 0 0 1_0 0 _B
28 _H	UART1 prescaler control register	CDCR	R/W		0__1 1 1 1 _B
29 _H	Serial Edge select register	SES1	R/W		_____0 _B
2A _H	Prohibited				
2B _H	Serial I/O prescaler	SCDCR	R/W	Extended I/O Serial Interface	0__1 1 1 1 _B
2C _H	Serial mode control register	SMCS	R/W		____0 0 0 0 _B
2D _H	Serial mode control register	SMCS	R/W		0 0 0 0 0 1 0 _B
2E _H	Serial data register	SDR	R/W		XXXXXXXX _B
2F _H	Serial Edge select register	SES2	R/W		_____0 _B
30 _H	External interrupt enable register	ENIR	R/W		External Interrupt
31 _H	External interrupt request register	EIRR	R/W	XXXXXXXX _B	
32 _H	External interrupt level register	ELVR	R/W	0 0 0 0 0 0 0 0 _B	
33 _H	External interrupt level register	ELVR	R/W	0 0 0 0 0 0 0 0 _B	
34 _H	A/D control status register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0 _B
35 _H	A/D control status register 1	ADCS1	R/W		0 0 0 0 0 0 0 0 _B
36 _H	A/D data register 0	ADCR0	R		XXXXXXXX _B
37 _H	A/D data register 1	ADCR1	R/W		0 0 0 0 1_XX _B
38 _H	PPG0 operation mode control register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0_0 0 0__1 _B
39 _H	PPG1 operation mode control register	PPGC1	R/W		0_0 0 0 0 0 1 _B
3A _H	PPG0/1 clock selection register	PPG01	R/W		0 0 0 0 0__ _B
3B _H	Prohibited				
3C _H	PPG2 operation mode control register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0_0 0 0__1 _B
3D _H	PPG3 operation mode control register	PPGC3	R/W		0_0 0 0 0 0 1 _B
3E _H	PPG2/3 Clock Selection Register	PPG23	R/W		0 0 0 0 0__ _B
3F _H	Prohibited				
40 _H	PPG4 operation mode control register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0_0 0 0__1 _B
41 _H	PPG5 operation mode control register	PPGC5	R/W		0_0 0 0 0 0 1 _B
42 _H	PPG4/5 clock selection register	PPG45	R/W		0 0 0 0 0__ _B
43 _H	Prohibited				
44 _H	PPG6 operation mode control register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0_0 0 0__1 _B
45 _H	PPG7 operation mode control register	PPGC7	R/W		0_0 0 0 0 0 1 _B
46 _H	PPG6/7 clock selection register	PPG67	R/W		0 0 0 0 0__ _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
47 _H to 4B _H	Prohibited				
4C _H	Input capture control status register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 _B
4D _H	Input capture control status register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 _B
4E _H	Input capture control status register 4/5	ICS45	R/W	Input Capture 4/5	0 0 0 0 0 0 0 0 _B
4F _H	Input capture control status register 6/7	ICS67	R/W	Input Capture 6/7	0 0 0 0 0 0 0 0 _B
50 _H	Timer control status register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0 _B
51 _H	Timer control status register 0	TMCSR0	R/W		___ _ _ 0 0 0 0 _B
52 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
53 _H	Timer register 0/reload register 0	TMR0/TMRLR0	R/W		XXXXXXXX _B
54 _H	Timer control status register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0 _B
55 _H	Timer control status register 1	TMCSR1	R/W		___ _ _ 0 0 0 0 _B
56 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
57 _H	Timer register 1/reload register 1	TMR1/TMRLR1	R/W		XXXXXXXX _B
58 _H	Output compare control status register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0 _B
59 _H	Output compare control status register 1	OCS1	R/W		_ _ _ 0 0 0 0 0 0 _B
5A _H	Output compare control status register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0 _B
5B _H	Output compare control status register 3	OCS3	R/W		_ _ _ 0 0 0 0 0 0 _B
5C _H to 6B _H	Prohibited				
6C _H	Timer Data register	TCDT	R/W	I/O Timer	0 0 0 0 0 0 0 0 _B
6D _H	Timer Data register	TCDT	R/W		0 0 0 0 0 0 0 0 _B
6E _H	Timer Control register	TCCS	R/W		0 0 0 0 0 0 0 0 _B
6F _H	ROM mirror function selection register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1 _B
70 _H to 7F _H	Reserved for CAN 0 Interface.				
80 _H to 8F _H	Reserved for CAN 1 Interface.				
90 _H to 9D _H	Prohibited				
9E _H	Program address detection control status register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0 _B
9F _H	Delayed interrupt/release register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0 _B
A0 _H	Low-power mode control register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0 _B
A1 _H	Clock selection register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
A2 _H to A4 _H	Prohibited				
A5 _H	Automatic ready function select register	ARSR	W	External Memory Access	0 0 1 1 _ _ 0 0 _B
A6 _H	External address output control register	HACR	W		0 0 0 0 0 0 0 0 _B
A7 _H	Bus control signal selection register	ECSR	W		0 0 0 0 0 0 0 _ _B
A8 _H	Watchdog Timer control register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control register	TBTC	R/W	Time Base Timer	1 - - 0 0 1 0 0 _B
AA _H	Watch timer control register	WTC	R/W	Watch Timer	1 X 0 0 0 0 0 0 _B
AB _H to AD _H	Prohibited				
AE _H	Flash memory control status register (Flash only, otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0 _B
AF _H	Prohibited				
B0 _H	Interrupt control register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt control register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt control register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt control register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt control register 04	ICR04	R/W		0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt control register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt control register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt control register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt control register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt control register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt control register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt control register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt control register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt control register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt control register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt control register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	External				

Address	Register	Abbreviation	Access	Resource name	Initial value
1FF0 _H	Program address detection register 0	PADR0	R/W	Address Match Detection Function	XXXXXXXX _B
1FF1 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF2 _H	Program address detection register 0	PADR0	R/W		XXXXXXXX _B
1FF3 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF4 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B
1FF5 _H	Program address detection register 1	PADR1	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3900 _H	Reload L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
3901 _H	Reload H	PRLH0	R/W		XXXXXXXX _B
3902 _H	Reload L	PRL1	R/W		XXXXXXXX _B
3903 _H	Reload H	PRLH1	R/W		XXXXXXXX _B
3904 _H	Reload L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
3905 _H	Reload H	PRLH2	R/W		XXXXXXXX _B
3906 _H	Reload L	PRL3	R/W		XXXXXXXX _B
3907 _H	Reload H	PRLH3	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
3908 _H	Reload L	PRL4	R/W		XXXXXXXX _B
3909 _H	Reload H	PRLH4	R/W		XXXXXXXX _B
390A _H	Reload L	PRL5	R/W		XXXXXXXX _B
390B _H	Reload H	PRLH5	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
390C _H	Reload L	PRL6	R/W		XXXXXXXX _B
390D _H	Reload H	PRLH6	R/W		XXXXXXXX _B
390E _H	Reload L	PRL7	R/W		XXXXXXXX _B
390F _H	Reload H	PRLH7	R/W	XXXXXXXX _B	
3910 _H to 3917 _H	Reserved				
3918 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
3919 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
391A _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391B _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
391C _H	Input Capture Register 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
391D _H	Input Capture Register 2	IPCP2	R		XXXXXXXX _B
391E _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
391F _H	Input Capture Register 3	IPCP3	R		XXXXXXXX _B
3920 _H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
3921 _H	Input Capture Register 4	IPCP4	R		XXXXXXXX _B
3922 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3923 _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
3924 _H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
3925 _H	Input Capture Register 6	IPCP6	R		XXXXXXXX _B
3926 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
3927 _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
3928 _H	Output Compare Register 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
3929 _H	Output Compare Register 0	OCCP0	R/W		XXXXXXXX _B
392A _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392B _H	Output Compare Register 1	OCCP1	R/W		XXXXXXXX _B
392C _H	Output Compare Register 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
392D _H	Output Compare Register 2	OCCP2	R/W		XXXXXXXX _B
392E _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
392F _H	Output Compare Register 3	OCCP3	R/W		XXXXXXXX _B
3930 _H to 39FF _H	Reserved				
3A00 _H to 3AFF _H	Reserved for CAN 0 Interface.				
3B00 _H to 3BFF _H	Reserved for CAN 0 Interface.				
3C00 _H to 3CFF _H	Reserved for CAN 1 Interface.				
3D00 _H to 3DFF _H	Reserved for CAN 1 Interface.				
3E00 _H to 3FFF _H	Reserved				

■ Read/write notation

- R/W : Reading and writing permitted
- R : Read-only
- W : Write-only

■ Initial value notation

- 0 : Initial value is "0".
- 1 : Initial value is "1".
- X : Initial value is undefined.
- : Initial value is unused.

Note: Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

9. CAN Controller

The MB90540G series contains two CAN controllers (CAN0 and CAN1) , the MB90545G series contains only one (CAN0) . The Evaluation Chip MB90V540G also has two CAN controllers.

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 1 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message buffer valid register	BVALR	R/W	00000000 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit request register	TREQR	R/W	00000000 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit cancel register	TCANR	W	00000000 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmit complete register	TCR	R/W	00000000 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive complete register	RCR	R/W	00000000 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote request receiving register	RRTRR	R/W	00000000 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive overrun register	ROVRR	R/W	00000000 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Receive interrupt enable register	RIER	R/W	00000000 00000000 _B
00007F _H	00008F _H				

(Continued)

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003B00 _H	003D00 _H	Control status register	CSR	R/W, R	00---000 0----0-1 _B
003B01 _H	003D01 _H				
003B02 _H	003D02 _H	Last event indicator register	LEIR	R/W	----- 000-0000 _B
003B03 _H	003D03 _H				
003B04 _H	003D04 _H	Receive/transmit error counter register	RTEC	R	00000000 00000000 _B
003B05 _H	003D05 _H				
003B06 _H	003D06 _H	Bit timing register	BTR	R/W	-1111111 11111111 _B
003B07 _H	003D07 _H				
003B08 _H	003D08 _H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXX _B
003B09 _H	003D09 _H				
003B0A _H	003D0A _H	Transmit RTR register	TRTRR	R/W	00000000 00000000 _B
003B0B _H	003D0B _H				
003B0C _H	003D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXX _B
003B0D _H	003D0D _H				
003B0E _H	003D0E _H	Transmit request enable register	TIER	R/W	00000000 00000000 _B
003B0F _H	003D0F _H				
003B10 _H	003D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXX _B
003B11 _H	003D11 _H				XXXXXXXX XXXXXXXX _B
003B12 _H	003D12 _H				XXXXXXXX XXXXXXXX _B
003B13 _H	003D13 _H				XXXXXXXX XXXXXXXX _B
003B14 _H	003D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXX _B
003B15 _H	003D15 _H				XXXXXXXX XXXXXXXX _B
003B16 _H	003D16 _H				XXXXX--- XXXXXXXX _B
003B17 _H	003D17 _H				XXXXX--- XXXXXXXX _B
003B18 _H	003D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXX _B
003B19 _H	003D19 _H				XXXXXXXX XXXXXXXX _B
003B1A _H	003D1A _H				XXXXX--- XXXXXXXX _B
003B1B _H	003D1B _H				XXXXX--- XXXXXXXX _B

List of Message Buffers (ID Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A00 _H to 003A1F _H	003C00 _H to 003C1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
003A20 _H	003C20 _H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXX _B
003A21 _H	003C21 _H				XXXXXXXX XXXXXXXX _B
003A22 _H	003C22 _H				XXXXX--- XXXXXXXX _B
003A23 _H	003C23 _H				XXXXX--- XXXXXXXX _B

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A24 _H	003C24 _H	ID register 1	IDR1	R/W	XXXXXXXXXXXXXXXX _B
003A25 _H	003C25 _H				XXXXX---XXXXXXXX _B
003A26 _H	003C26 _H				
003A27 _H	003C27 _H				
003A28 _H	003C28 _H	ID register 2	IDR2	R/W	XXXXXXXXXXXXXXXX _B
003A29 _H	003C29 _H				XXXXX---XXXXXXXX _B
003A2A _H	003C2A _H				
003A2B _H	003C2B _H				
003A2C _H	003C2C _H	ID register 3	IDR3	R/W	XXXXXXXXXXXXXXXX _B
003A2D _H	003C2D _H				XXXXX---XXXXXXXX _B
003A2E _H	003C2E _H				
003A2F _H	003C2F _H				
003A30 _H	003C30 _H	ID register 4	IDR4	R/W	XXXXXXXXXXXXXXXX _B
003A31 _H	003C31 _H				XXXXX---XXXXXXXX _B
003A32 _H	003C32 _H				
003A33 _H	003C33 _H				
003A34 _H	003C34 _H	ID register 5	IDR5	R/W	XXXXXXXXXXXXXXXX _B
003A35 _H	003C35 _H				XXXXX---XXXXXXXX _B
003A36 _H	003C36 _H				
003A37 _H	003C37 _H				
003A38 _H	003C38 _H	ID register 6	IDR6	R/W	XXXXXXXXXXXXXXXX _B
003A39 _H	003C39 _H				XXXXX---XXXXXXXX _B
003A3A _H	003C3A _H				
003A3B _H	003C3B _H				

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A3C _H	003C3C _H	ID register 7	IDR7	R/W	XXXXXXXXXXXXXXXX _B
003A3D _H	003C3D _H				XXXXX---XXXXXXXX _B
003A3E _H	003C3E _H				
003A3F _H	003C3F _H				
003A40 _H	003C40 _H	ID register 8	IDR8	R/W	XXXXXXXXXXXXXXXX _B
003A41 _H	003C41 _H				XXXXX---XXXXXXXX _B
003A42 _H	003C42 _H				
003A43 _H	003C43 _H				
003A44 _H	003C44 _H	ID register 9	IDR9	R/W	XXXXXXXXXXXXXXXX _B
003A45 _H	003C45 _H				XXXXX---XXXXXXXX _B
003A46 _H	003C46 _H				
003A47 _H	003C47 _H				
003A48 _H	003C48 _H	ID register 10	IDR10	R/W	XXXXXXXXXXXXXXXX _B
003A49 _H	003C49 _H				XXXXX---XXXXXXXX _B
003A4A _H	003C4A _H				
003A4B _H	003C4B _H				
003A4C _H	003C4C _H	ID register 11	IDR11	R/W	XXXXXXXXXXXXXXXX _B
003A4D _H	003C4D _H				XXXXX---XXXXXXXX _B
003A4E _H	003C4E _H				
003A4F _H	003C4F _H				
003A50 _H	003C50 _H	ID register 12	IDR12	R/W	XXXXXXXXXXXXXXXX _B
003A51 _H	003C51 _H				XXXXX---XXXXXXXX _B
003A52 _H	003C52 _H				
003A53 _H	003C53 _H				
003A54 _H	003C54 _H	ID register 13	IDR13	R/W	XXXXXXXXXXXXXXXX _B
003A55 _H	003C55 _H				XXXXX---XXXXXXXX _B
003A56 _H	003C56 _H				
003A57 _H	003C57 _H				
003A58 _H	003C58 _H	ID register 14	IDR14	R/W	XXXXXXXXXXXXXXXX _B
003A59 _H	003C59 _H				XXXXX---XXXXXXXX _B
003A5A _H	003C5A _H				
003A5B _H	003C5B _H				
003A5C _H	003C5C _H	ID register 15	IDR15	R/W	XXXXXXXXXXXXXXXX _B
003A5D _H	003C5D _H				XXXXX---XXXXXXXX _B
003A5E _H	003C5E _H				
003A5F _H	003C5F _H				

List of Message Buffers (DLC Registers and Data Registers)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A60 _H	003C60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
003A61 _H	003C61 _H				
003A62 _H	003C62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
003A63 _H	003C63 _H				
003A64 _H	003C64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
003A65 _H	003C65 _H				
003A66 _H	003C66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
003A67 _H	003C67 _H				
003A68 _H	003C68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
003A69 _H	003C69 _H				
003A6A _H	003C6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
003A6B _H	003C6B _H				
003A6C _H	003C6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
003A6D _H	003C6D _H				
003A6E _H	003C6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
003A6F _H	003C6F _H				
003A70 _H	003C70 _H	DLC register 8	DLCR8	R/W	----XXXX
003A71 _H	003C71 _H				
003A72 _H	003C72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
003A73 _H	003C73 _H				
003A74 _H	003C74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
003A75 _H	003C75 _H				
003A76 _H	003C76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
003A77 _H	003C77 _H				
003A78 _H	003C78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
003A79 _H	003C79 _H				
003A7A _H	003C7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
003A7B _H	003C7B _H				
003A7C _H	003C7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
003A7D _H	003C7D _H				
003A7E _H	003C7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
003A7F _H	003C7F _H				
003A80 _H to 003A87 _H	003C80 _H to 003C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

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Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
003A88 _H to 003A8F _H	003C88 _H to 003C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
003A90 _H to 003A97 _H	003C90 _H to 003C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
003A98 _H to 003A9F _H	003C98 _H to 003C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA0 _H to 003AA7 _H	003CA0 _H to 003CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
003AA8 _H to 003AAF _H	003CA8 _H to 003CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB0 _H to 003AB7 _H	003CB0 _H to 003CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
003AB8 _H to 003ABF _H	003CB8 _H to 003CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC0 _H to 003AC7 _H	003CC0 _H to 003CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
003AC8 _H to 003ACF _H	003CC8 _H to 003CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD0 _H to 003AD7 _H	003CD0 _H to 003CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
003AD8 _H to 003ADF _H	003CD8 _H to 003CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE0 _H to 003AE7 _H	003CE0 _H to 003CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
003AE8 _H to 003AEF _H	003CE8 _H to 003CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF0 _H to 003AF7 _H	003CF0 _H to 003CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
003AF8 _H to 003AFF _H	003CF8 _H to 003CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Map

Interrupt cause	E ² OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	#08	FFFFDC _H	—	—
INT9 instruction	N/A	#09	FFFFD8 _H	—	—
Exception	N/A	#10	FFFFD4 _H	—	—
CAN 0 RX	N/A	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N/A	#12	FFFFCC _H		
CAN 1 RX	N/A	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS	N/A	#14	FFFFC4 _H		
External Interrupt INT0/INT1	*1	#15	FFFFC0 _H	ICR02	0000B2 _H
Time Base Timer	N/A	#16	FFFFBC _H		
16-bit Reload Timer 0	*1	#17	FFFFB8 _H	ICR03	0000B3 _H
8/10-bit A/D Converter	*1	#18	FFFFB4 _H		
16-bit Free-run Timer	N/A	#19	FFFFB0 _H	ICR04	0000B4 _H
External Interrupt INT2/INT3	*1	#20	FFFFAC _H		
Serial I/O	*1	#21	FFFFA8 _H	ICR05	0000B5 _H
8/16-bit PPG 0/1	N/A	#22	FFFFA4 _H		
Input Capture 0	*1	#23	FFFFA0 _H	ICR06	0000B6 _H
External Interrupt INT4/INT5	*1	#24	FFFF9C _H		
Input Capture 1	*1	#25	FFFF98 _H	ICR07	0000B7 _H
8/16-bit PPG 2/3	N/A	#26	FFFF94 _H		
External Interrupt INT6/INT7	*1	#27	FFFF90 _H	ICR08	0000B8 _H
Watch Timer	N/A	#28	FFFF8C _H		
8/16-bit PPG 4/5	N/A	#29	FFFF88 _H	ICR09	0000B9 _H
Input Capture 2/3	*1	#30	FFFF84 _H		
8/16-bit PPG 6/7	N/A	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0	*1	#32	FFFF7C _H		
Output Compare 1	*1	#33	FFFF78 _H	ICR11	0000BB _H
Input Capture 4/5	*1	#34	FFFF74 _H		
Output Compare 2/3 - Input Capture 6/7	*1	#35	FFFF70 _H	ICR12	0000BC _H
16-bit Reload Timer 1	*1	#36	FFFF6C _H		
UART 0 RX	*2	#37	FFFF68 _H	ICR13	0000BD _H
UART 0 TX	*1	#38	FFFF64 _H		
UART 1 RX	*2	#39	FFFF60 _H	ICR14	0000BE _H
UART 1 TX	*1	#40	FFFF5C _H		
Flash Memory	N/A	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N/A	#42	FFFF54 _H		

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*1 : The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2 : The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

Notes :

- N/A : The interrupt request flag is not cleared by the EI²OS interrupt clear signal.
- For a peripheral module with two interrupt causes for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by a hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Units	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *1
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH/AVRL, AVRH \geq AVRL$ *1
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*2
Maximum clamp current	I_{CLAMP}	-2.0	+2.0	mA	*6
Total maximum clamp current	$\sum I_{CLAMP} $	—	20	mA	*6
"L" level max output current	I_{OL}	—	15	mA	*3
"L" level avg. output current	I_{OLAV}	—	4	mA	*4
"L" level max overall output current	$\sum I_{OL}$	—	100	mA	
"L" level avg. overall output current	$\sum I_{OLAV}$	—	50	mA	*5
"H" level max output current	I_{OH}	—	-15	mA	*3
"H" level avg. output current	I_{OHAV}	—	-4	mA	*4
"H" level max overall output current	$\sum I_{OH}$	—	-100	mA	
"H" level avg. overall output current	$\sum I_{OHAV}$	—	-50	mA	*5
Power consumption	P_D	—	500	mW	Flash device
		—	400	mW	MASK ROM
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1 : $AV_{CC}, AVRH, AVRL$ should not exceed V_{CC} . Also, $AVRH, AVRL$ should not exceed AV_{CC} , and $AVRL$ does not exceed $AVRH$.

*2 : V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

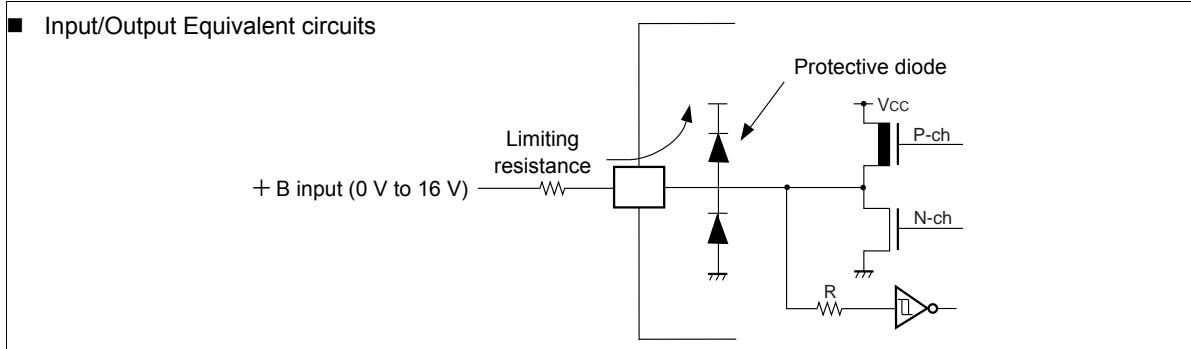
*3 : The maximum output current is a peak value for a corresponding pin.

*4 : Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5 : Total average current is an average current value observed for a 100 ms period for all corresponding pins.

- *6 :
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0
 - Use within recommended operating conditions.
 - Use at DC voltage (current) .
 - The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
 - Care must be taken not to leave the + B input pin open.

- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
- Sample recommended circuits :



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

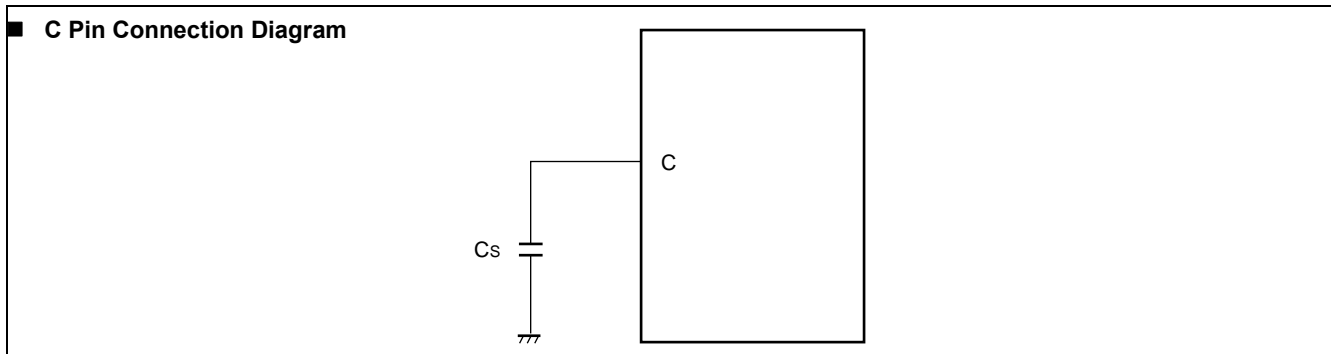
11.2 Recommended Conditions

 (V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value			Units	Remarks	
		Min	Typ	Max			
Power supply voltage	V _{CC} , AV _{CC}	4.5	5.0	5.5	V	Under normal operation : Other than MB90F548GL(S)/543G(S)/547G(S)/548G(S)	
							Under normal operation when A/D converter is used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)
		3.5	5.0	5.5	V	Under normal operation when A/D converter is not used : MB90F548GL(S)/543G(S)/547G(S)/548G(S)	
		3.0	—	5.5	V	Maintain RAM data in stop mode	
Smooth capacitor	C _S	0.022	0.1	1.0	μF	*	
Operating temperature	T _A	−40	—	+105	°C		

*: Use a ceramic capacitor or a capacitor of better 4. AC characteristics. The bypass capacitor should be greater than this capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



11.3 DC Characteristics

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IH}	TTL input pin	—	2.0	—	—	V	
	V_{IHM}	MD input pin	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	$V_{CC} - 0.3$	—	$0.2 V_{CC}$	V	
	V_{IL}	TTL input pin	—	—	—	0.8	V	
	V_{ILM}	MD input pin	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH}	All output pins	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	All output pins	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash devices

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(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Units	Remarks
				Min	Typ	Max		
Power supply current*	I _{CC}	V _{CC}	Internal frequency : 16 MHz, At normal operating	—	40	55	mA	
			Internal frequency : 16 MHz, At Flash programming/erasing	—	50	70	mA	Flash device
	I _{CCS}		Internal frequency : 16 MHz, At sleep mode	—	12	20	mA	
	I _{CTS}		$V_{CC} = 5.0\text{ V} \pm 10\%$, Internal frequency : 2 MHz, At pseudo timer mode	—	300	600	μA	
				—	600	1100	μA	MB90F548GL (S) only
	I _{CCCL}		Internal frequency : 8 kHz, At sub operation, $T_A = 25\text{ }^\circ\text{C}$	—	200	400	μA	MB90543G(S)/547G(S)/548(S) only
				—	400	750	μA	MB90F548GL only
				—	50	100	μA	MASK ROM
	I _{CCLS}		Internal frequency : 8 kHz, At sub sleep, $T_A = 25\text{ }^\circ\text{C}$	—	15	40	μA	
	I _{CCT}		Internal frequency : 8 kHz, At timer mode, $T_A = 25\text{ }^\circ\text{C}$	—	7	25	μA	
I _{CCH1}	At stop, $T_A = 25\text{ }^\circ\text{C}$	—	5	20	μA			
I _{CCH2}	At hardware standby mode, $T_A = 25\text{ }^\circ\text{C}$	—	50	100	μA			
Input capacity	C _{IN}	Other than AV _{CC} , AV _{SS} , AVRH, AVRL, C, V _{CC} , V _{SS}	—	5	15	pF		

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics
11.4.1 Clock Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Oscillation frequency	f_c	X0, X1	3	—	16	MHz	No multiplier When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			8	—	16	MHz	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			4	—	8	MHz	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	5.33	MHz	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	4	MHz	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			3	—	5	MHz	When using an oscillator circuit $V_{CC} < 4.5\text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			3	—	16	MHz	No multiplier When using an external clock
			8	—	16	MHz	PLL multiplied by 1 When using an external clock
			4	—	8	MHz	PLL multiplied by 2 When using an external clock
			3	—	5.33	MHz	PLL multiplied by 3 When using an external clock
	3	—	4	MHz	PLL multiplied by 4 When using an external clock		
	f_{CL}	X0A, X1A	—	32.768	—	kHz	

(Continued)

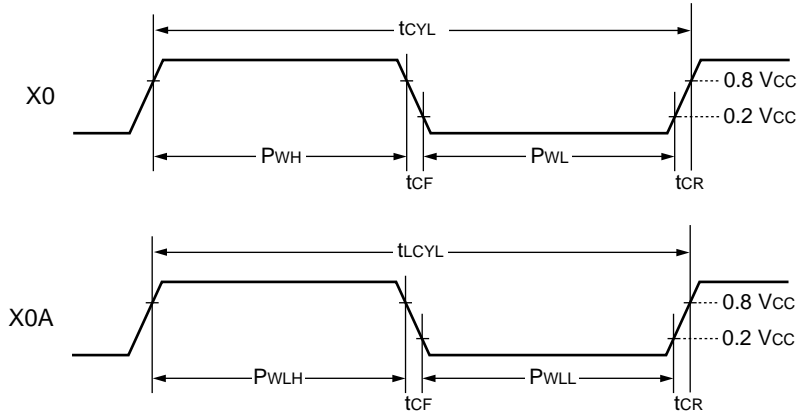
(Continued)

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

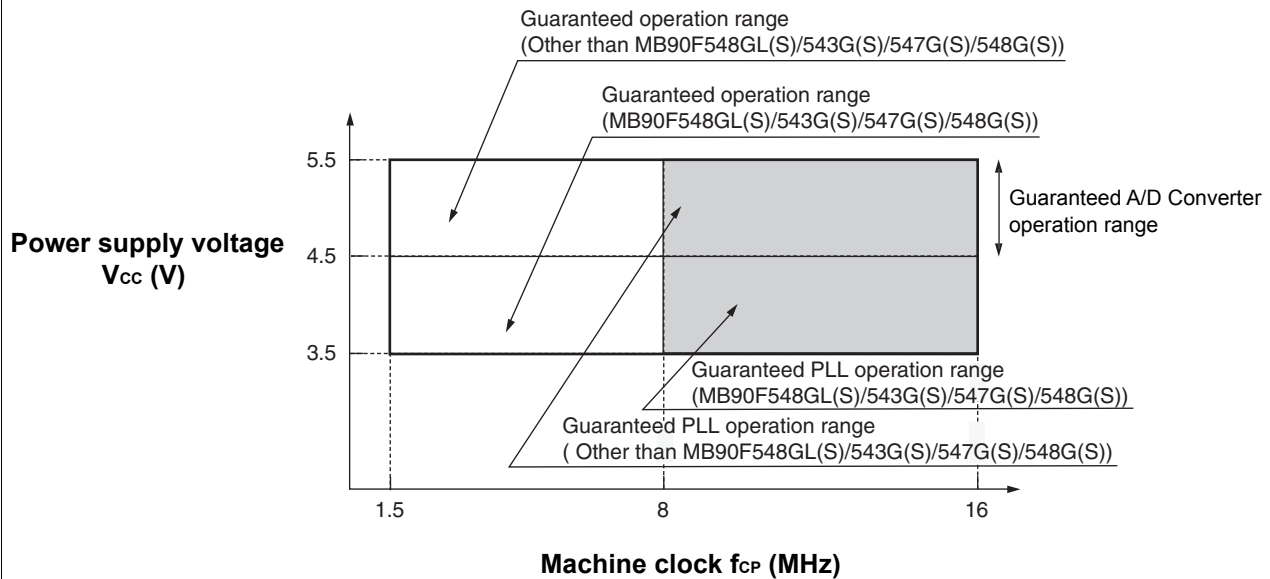
 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Clock cycle time	t _{CYL}	X0, X1	62.5	—	333	ns	No multiplier When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			62.5	—	125	ns	PLL multiplied by 1 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			125	—	250	ns	PLL multiplied by 2 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			187.5	—	333	ns	PLL multiplied by 3 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			250	—	333	ns	PLL multiplied by 4 When using an oscillator circuit $V_{CC} = 5.0\text{ V} \pm 10\%$
			200	—	333	ns	When using an oscillator circuit $V_{CC} < 4.5\text{ V}$ (MB90F548GL(S)/543G(S)/ 547G(S)/548G(S))
			62.5	—	333	ns	No multiplier When using an external clock
			62.5	—	125	ns	PLL multiplied by 1 When using an external clock
			125	—	250	ns	PLL multiplied by 2 When using an external clock
			187.5	—	333	ns	PLL multiplied by 3 When using an external clock
	250	—	333	ns	PLL multiplied by 4 When using an external clock		
	t _{LCYL}	X0A, X1A	—	30.5	—	μs	
Input clock pulse width	P _{WH} , P _{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P _{WLH} , P _{WLL}	X0A	—	15.2	—	μs	
Input clock rise and fall time	t _{CR} , t _{CF}	X0	—	—	5	ns	When using an external clock
Machine clock frequency	f _{CP}	—	1.5	—	16	MHz	When using main clock
	f _{LCP}	—	—	8.192	—	kHz	When using sub-clock
Machine clock cycle time	t _{CP}	—	62.5	—	666	ns	When using main clock
	t _{LCP}	—	—	122.1	—	μs	When using sub-clock

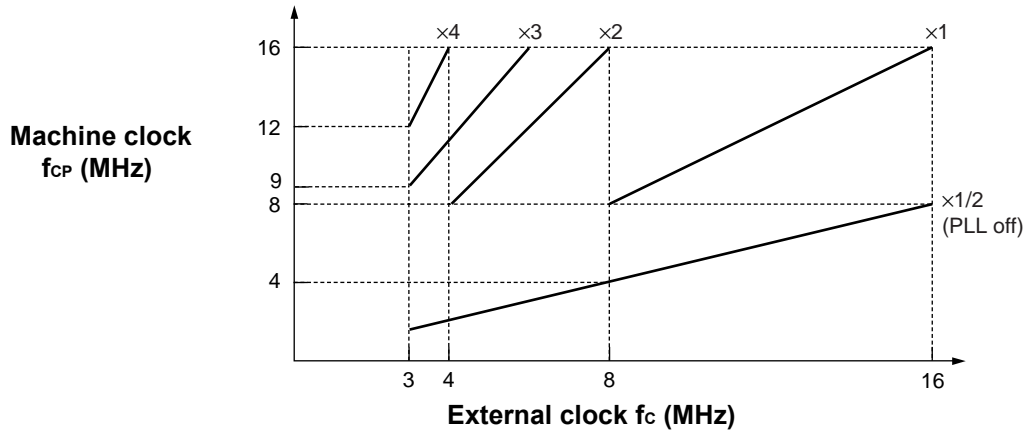
■ **Clock Timing**



■ **Guaranteed PLL operation range**



■ External clock frequency and Machine clock frequency



AC characteristics are set to the measured reference voltage values below.

■ Input signal waveform

Hysteresis Input Pin



TTL Input Pin



■ Output signal waveform

Output Pin

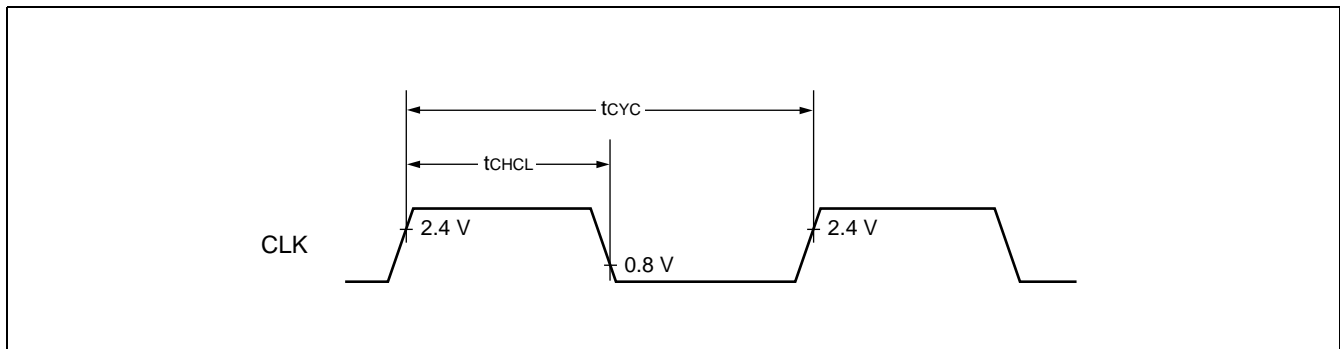


11.4.2 Clock Output Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	$V_{CC} = 5\text{ V} \pm 10\%$	62.5	—	ns	
CLK \uparrow → CLK \downarrow	t_{CHCL}			20	—	ns	


11.4.3 Reset and Hardware Standby Input Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

Parameter	Symbol	Pin name	Value		Units	Remarks
			Min	Max		
Reset input time	t_{RSTL}	\overline{RST}	$4 t_{CP}$	—	ns	Under normal operation
			Oscillation time of oscillator + $4 t_{CP}$	—	ms	In stop mode
			100	—	μs	In pseudo timer mode (MB90543G (S) /547G (S) /548G (S))
			$4 t_{CP}$	—	ns	In pseudo timer mode (Other than MB90543G (S) /547G (S) /548G (S))
			$2 t_{LCP}$	—	μs	In sub-clock mode, sub-sleep mode, timer mode
Hardware standby input time	t_{HSTL}	HST	$4 t_{CP}$	—	ns	Under normal operation

 Note : “ t_{cp} ” represents one cycle time of the machine clock.

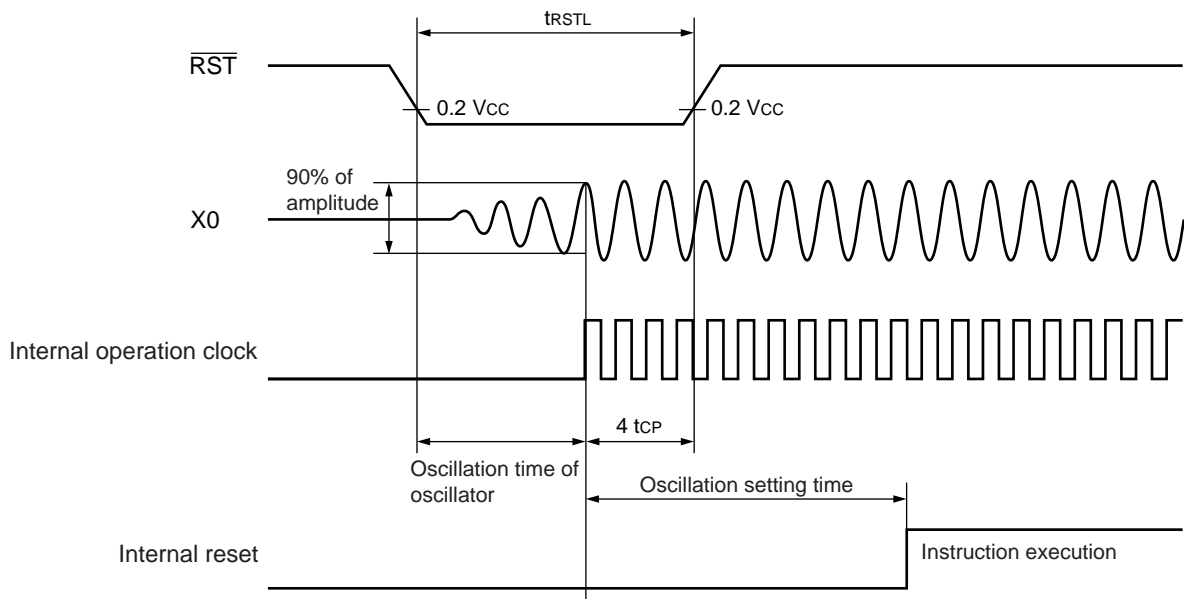
 Oscillation time of oscillator is time that amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ns.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

■ In under normal operation, pseudo timer mode, sub-clock mode, sub-sleep mode, timer mode



■ In stop mode



11.4.4 Power On Reset

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

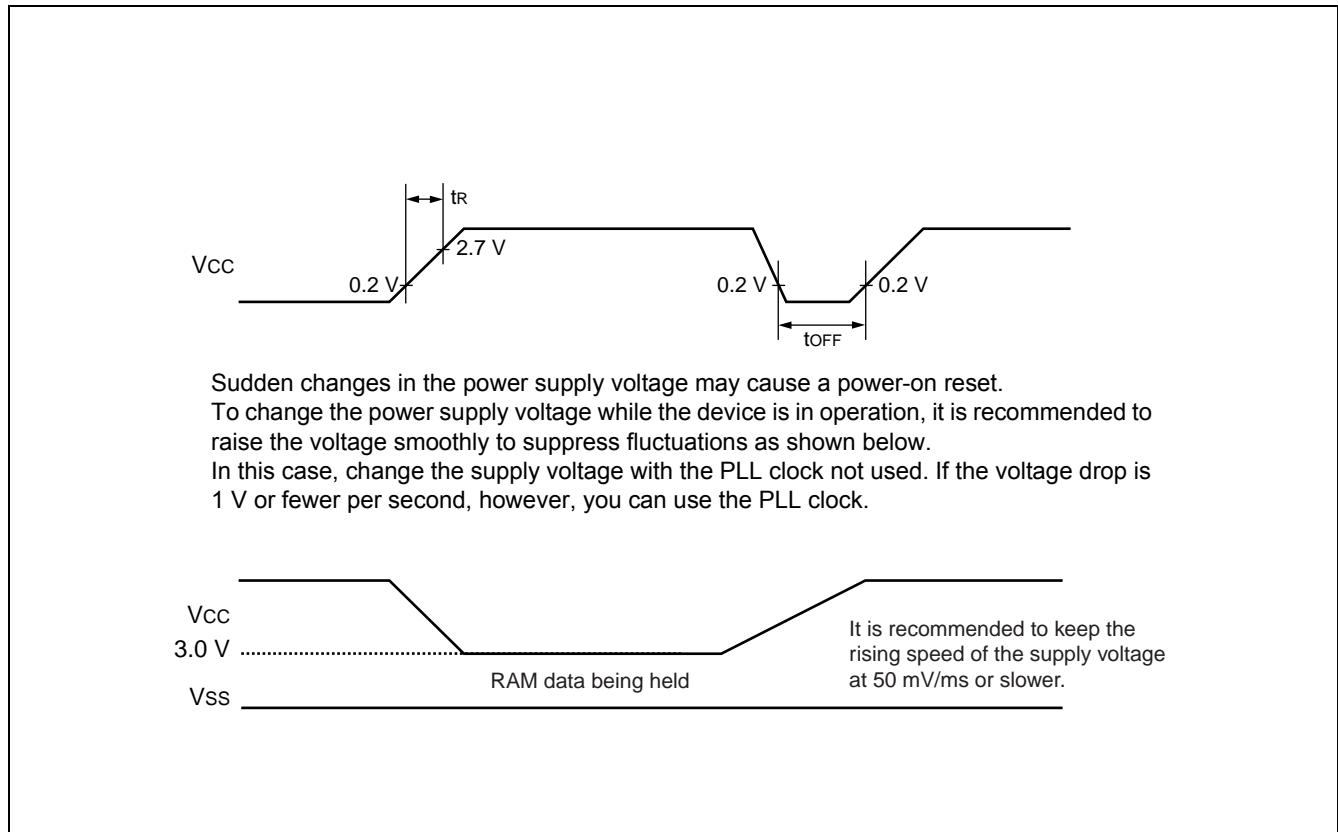
(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}	—	50	—	ms	Waiting time until power-on

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : ■ The above values are used for creating a power-on reset.

■ Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.

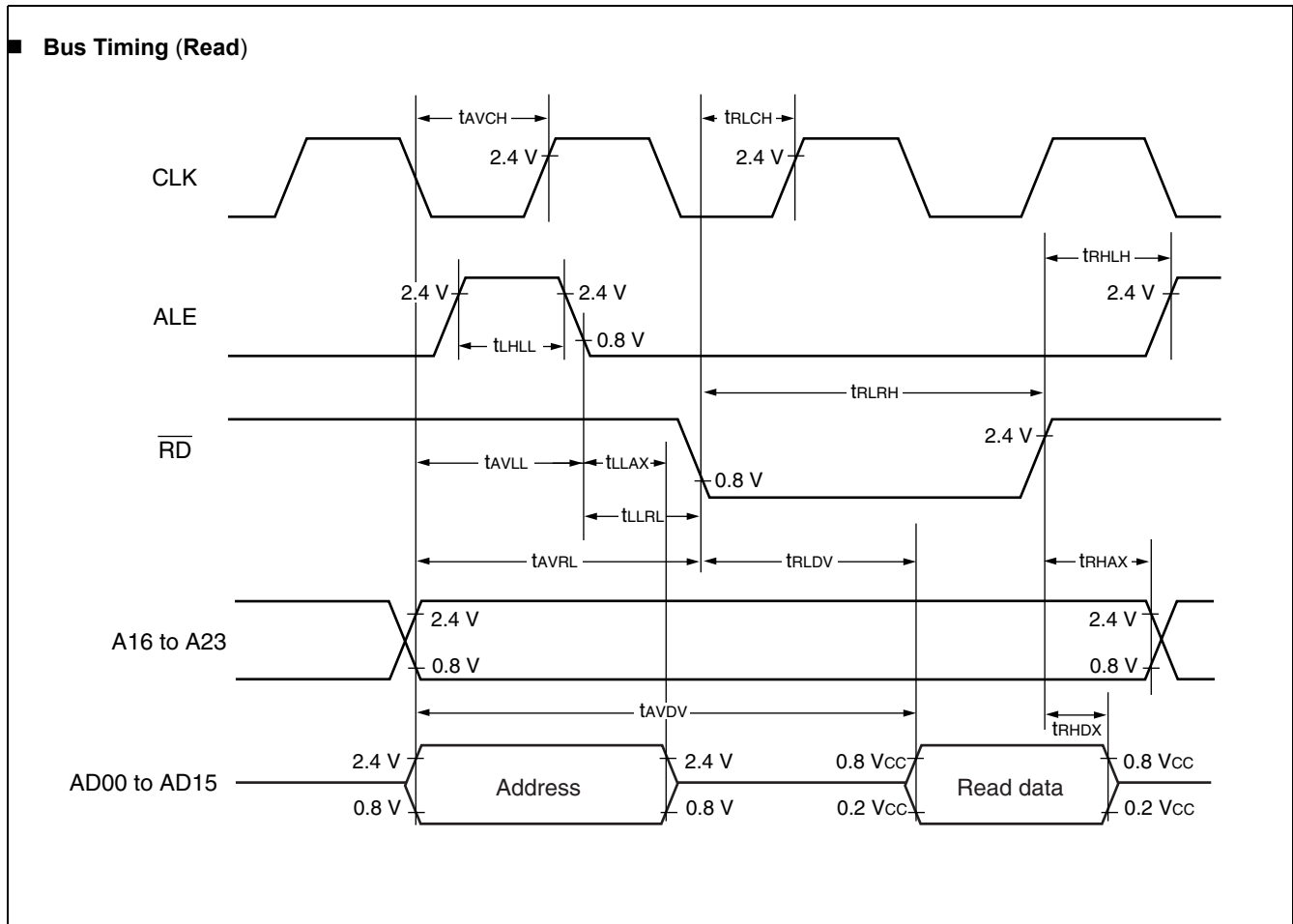


11.4.5 Bus Timing (Read)

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 20$	—	ns	
Valid address → ALE↓ time	t_{AVLL}	ALE, A16 to A23, AD00 to AD15		$t_{CP}/2 - 20$	—	ns	
ALE↓ → Address valid time	t_{LLAX}	ALE, AD00 to AD15		$t_{CP}/2 - 15$	—	ns	
Valid address → \overline{RD} ↓ time	t_{AVRL}	A16 to A23, AD00 to AD15, \overline{RD}		$t_{CP} - 15$	—	ns	
Valid address → Valid data input	t_{AVDV}	A16 to A23, AD00 to AD15		—	$5 t_{CP}/2 - 60$	ns	
\overline{RD} pulse width	t_{RLRH}	\overline{RD}		$3 t_{CP}/2 - 20$	—	ns	
\overline{RD} ↓ → Valid data input	t_{RLDV}	\overline{RD} , AD00 to AD15		—	$3 t_{CP}/2 - 60$	ns	
\overline{RD} ↑ → Data hold time	t_{RHDX}	\overline{RD} , AD00 to AD15		0	—	ns	
\overline{RD} ↑ → ALE↑ time	t_{RHLH}	\overline{RD} , ALE		$t_{CP}/2 - 15$	—	ns	
\overline{RD} ↑ → Address valid time	t_{RHAX}	\overline{RD} , A16 to A23		$t_{CP}/2 - 10$	—	ns	
Valid address → CLK↑ time	t_{AVCH}	A16 to A23, AD00 to AD15, CLK		$t_{CP}/2 - 20$	—	ns	
\overline{RD} ↓ → CLK↑ time	t_{RLCH}	\overline{RD} , CLK		$t_{CP}/2 - 20$	—	ns	
ALE↓ → \overline{RD} ↓ time	t_{LLRL}	ALE, \overline{RD}	$t_{CP}/2 - 15$	—	ns		

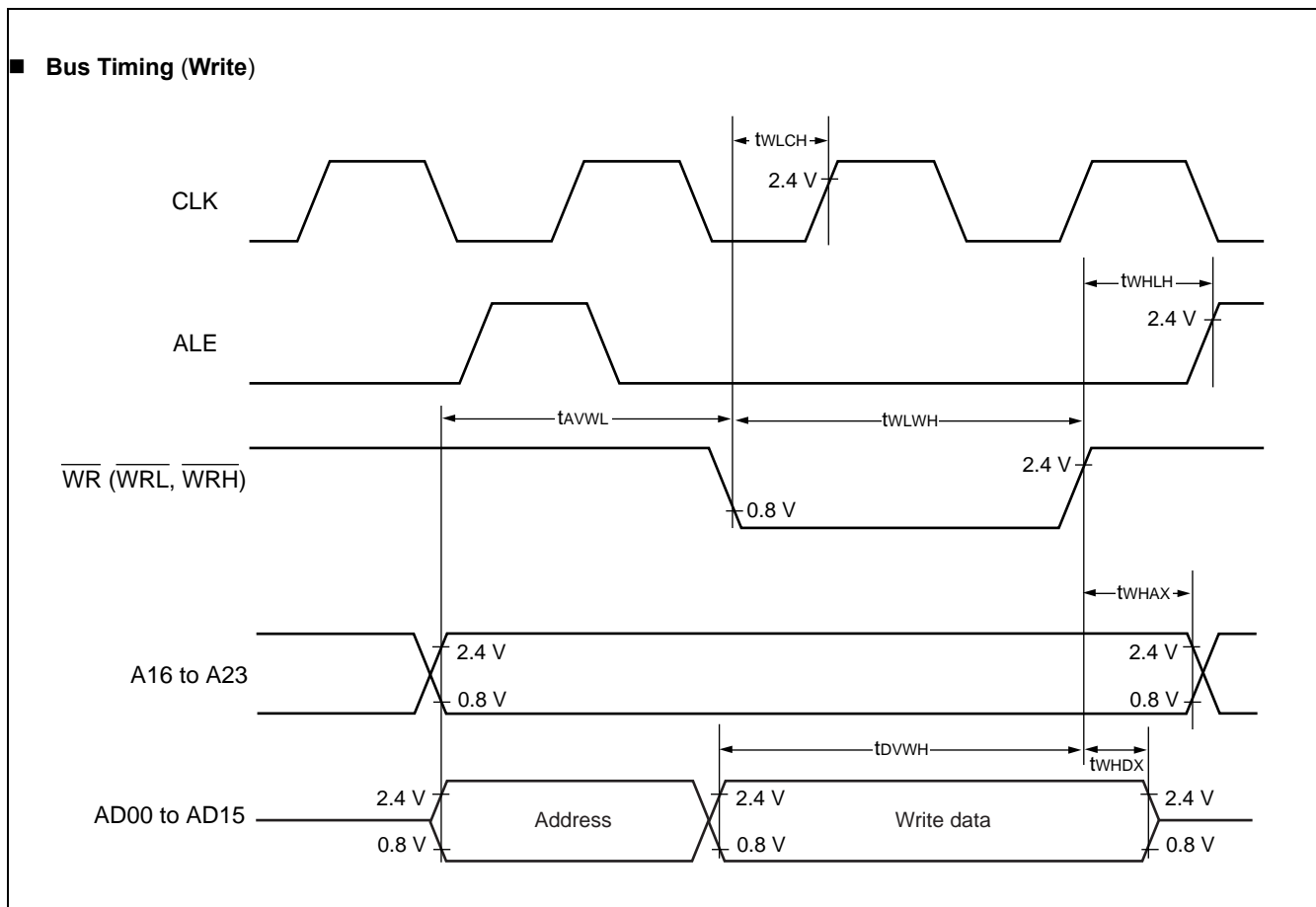


11.4.6 Bus Timing (Write)

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR}\downarrow$ time	t_{AVWL}	A16 to A23 AD00 to AD15, \overline{WR}	—	$t_{CP} - 15$	—	ns	
\overline{WR} pulse width	t_{WLWH}	WR		$3 t_{CP}/2 - 20$	—	ns	
Valid data output $\rightarrow \overline{WR}\uparrow$ time	t_{DVWH}	AD00 to AD15, \overline{WR}		$3 t_{CP}/2 - 20$	—	ns	
$\overline{WR}\uparrow \rightarrow$ Data hold time	t_{WHDX}	AD00 to AD15, \overline{WR}		20	—	ns	
$\overline{WR}\uparrow \rightarrow$ Address valid time	t_{WHAX}	A16 to A23, \overline{WR}		$t_{CP}/2 - 10$	—	ns	
$\overline{WR}\uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	\overline{WR} , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR}\uparrow \rightarrow$ CLK \uparrow time	t_{WLCH}	\overline{WR} , CLK		$t_{CP}/2 - 20$	—	ns	



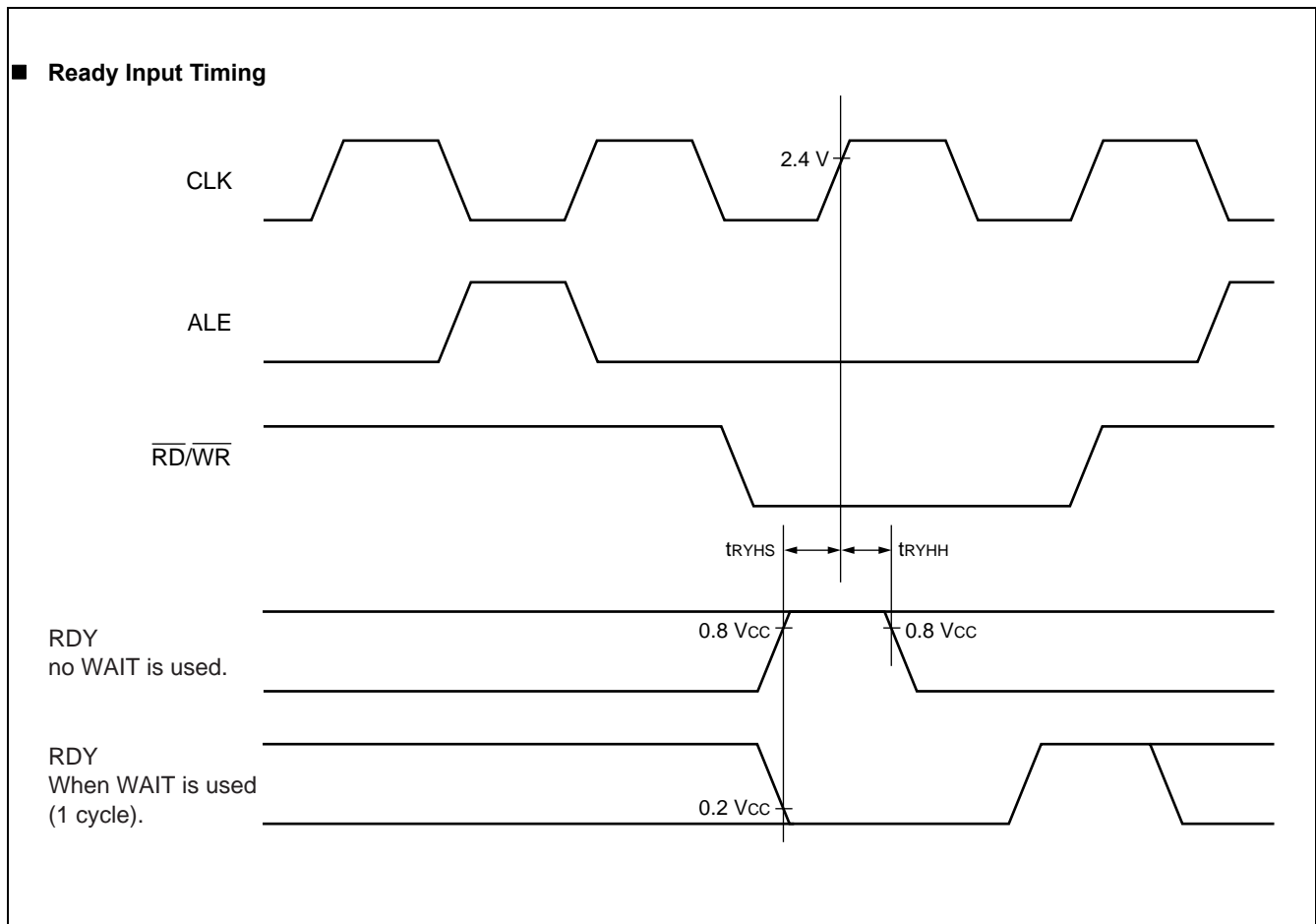
11.4.7 Ready Input Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

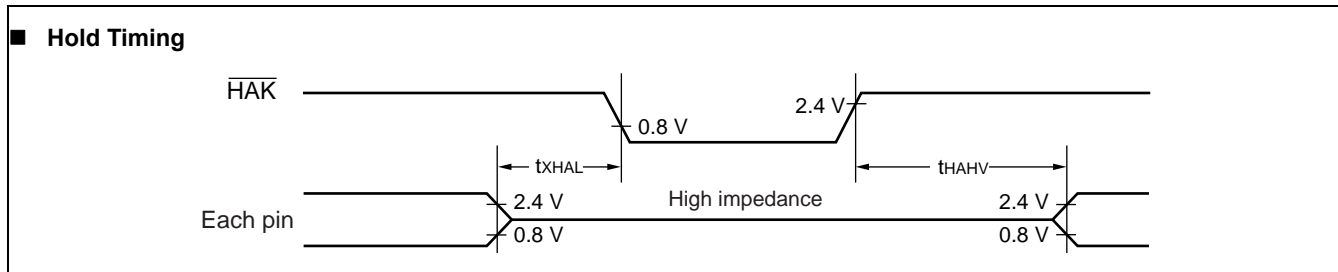


11.4.8 Hold Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \rightarrow $\overline{\text{HAK}}\downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns	
$\overline{\text{HAK}}\uparrow$ time \rightarrow Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	t_{CP}	$2 t_{\text{CP}}$	ns	

 Note : There is more than 1 cycle from the time HRQ is read to the time the $\overline{\text{HAK}}$ is changed.

11.4.9 UART0/1, Serial I/O Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

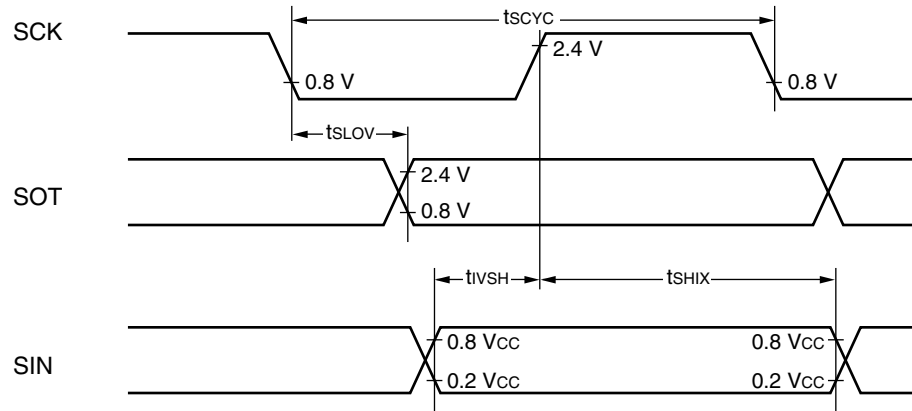
 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$8 t_{\text{CP}}$	—	ns	
SCK \downarrow \rightarrow SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		— 80	80	ns	
Valid SIN \rightarrow SCK \uparrow	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK \uparrow \rightarrow Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$4 t_{\text{CP}}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK2		$4 t_{\text{CP}}$	—	ns	
SCK \downarrow \rightarrow SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN \rightarrow SCK \uparrow	t_{VSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK \uparrow \rightarrow Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2	60	—	ns		

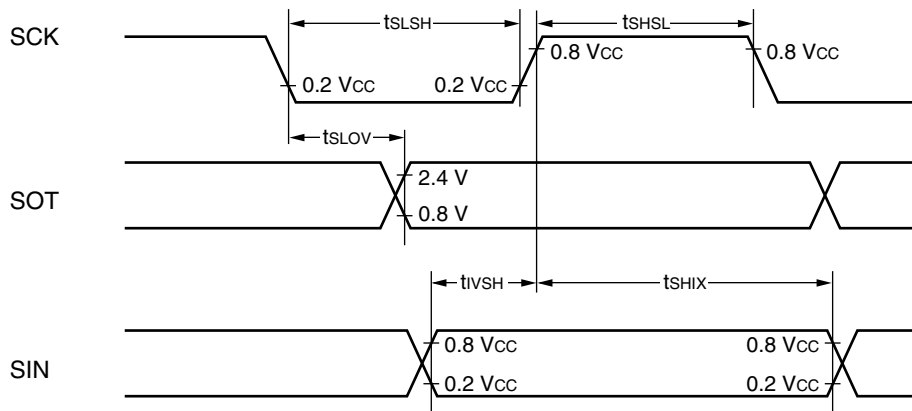
Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- For t_{CP} (Machine clock cycle time), refer to "(1) Clock Timing".

■ Internal Shift Clock Mode



■ External Shift Clock Mode

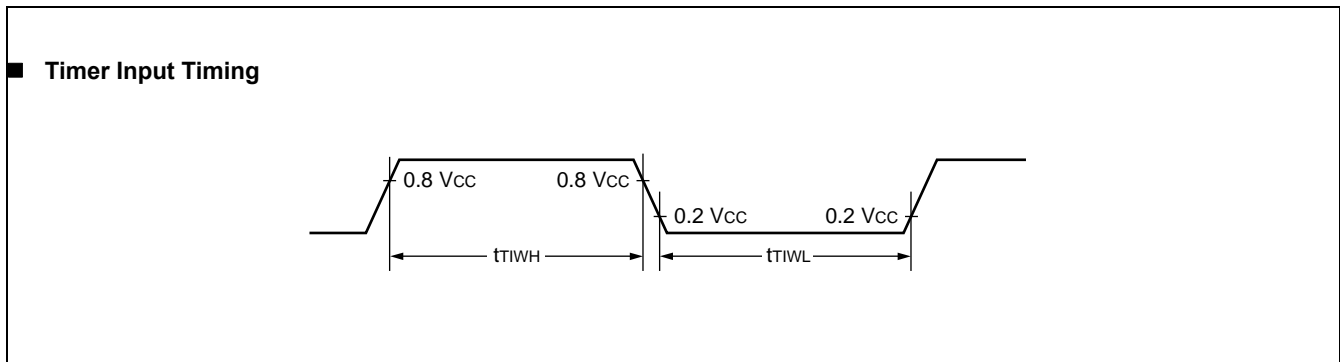


11.4.10 Timer Input Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

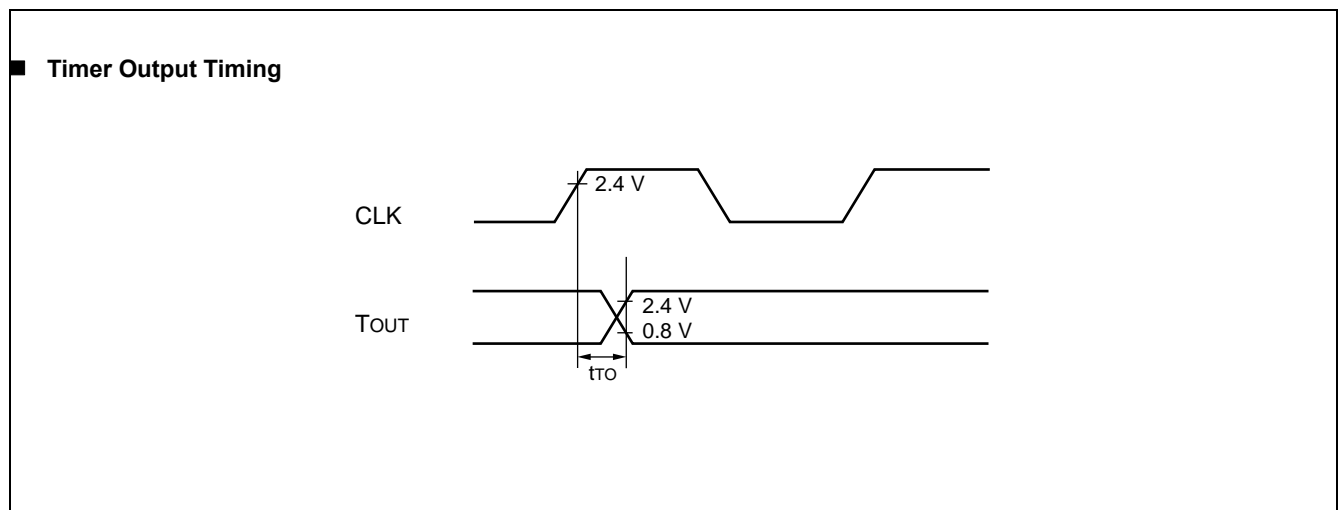
Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN7					


11.4.11 Timer Output Timing

 (MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

 (Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
CLK \uparrow → T _{OUT} change time	t_{TO}	TOT0, TOT1, PPG0 to PPG3	—	30	—	ns	

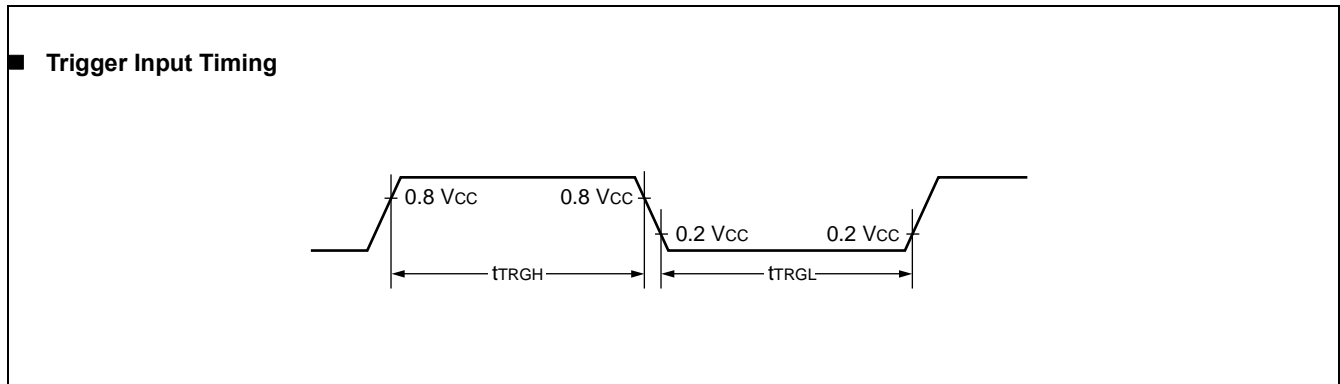


11.4.12 Trigger Input Timing

(MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 3.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

(Other than MB90543G(S)/547G(S)/548G(S)/F548GL(S): $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Units	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under normal operation
	t_{TRGL}			1	—	μs	In stop mode



11.5 A/D Converter

11.5.1 Electrical Characteristics

($V_{CC} = AV_{CC} = 5.0 V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 V$, $3.0 V \leq AVRH - AVRL$, $T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$)

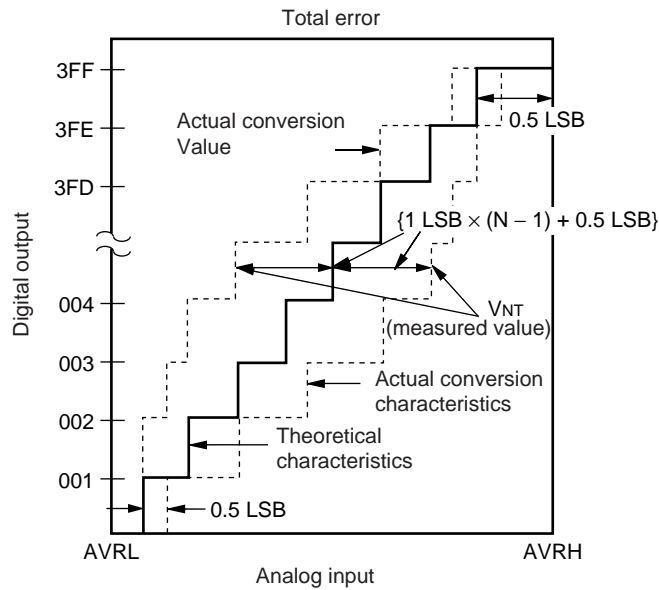
Parameter	Symbol	Pin name	Value			Units	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AVRL - 3.5$ LSB	$AVRL + 0.5$ LSB	$AVRL + 4.5$ LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 6.5$ LSB	$AVRH - 1.5$ LSB	$AVRH + 1.5$ LSB	V	
Compare time	—	—	$352 t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Sampling time	—	—	$64 t_{CP}$	—	—	ns	Internal frequency : 16 MHz
Analog port input current	I_{AIN}	AN0 to AN7	-1	—	1	μA	$V_{CC} = AV_{CC} = 5.0 V \pm 1\%$
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$AVRL + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$AVRH - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage supply current	I_R	AVRH	—	400	600	μA	Flash device
			—	140	260	μA	MASK ROM
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not using an A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0 V$) when the CPU is stopped.

Note: The functionality of the A/D converter is only guaranteed for $V_{CC} = 5.0 V \pm 10\%$ (also for MB90543G(S)/547G(S)/548G(S)/F548G(S)/F548GL(S)).

11.5.2 A/D Converter Glossary

- Resolution : Analog changes that are identifiable with the A/D converter
- Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics
- Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$V_{OT} (\text{Theoretical value}) = \text{AVRL} + 0.5 \text{ LSB [V]}$$

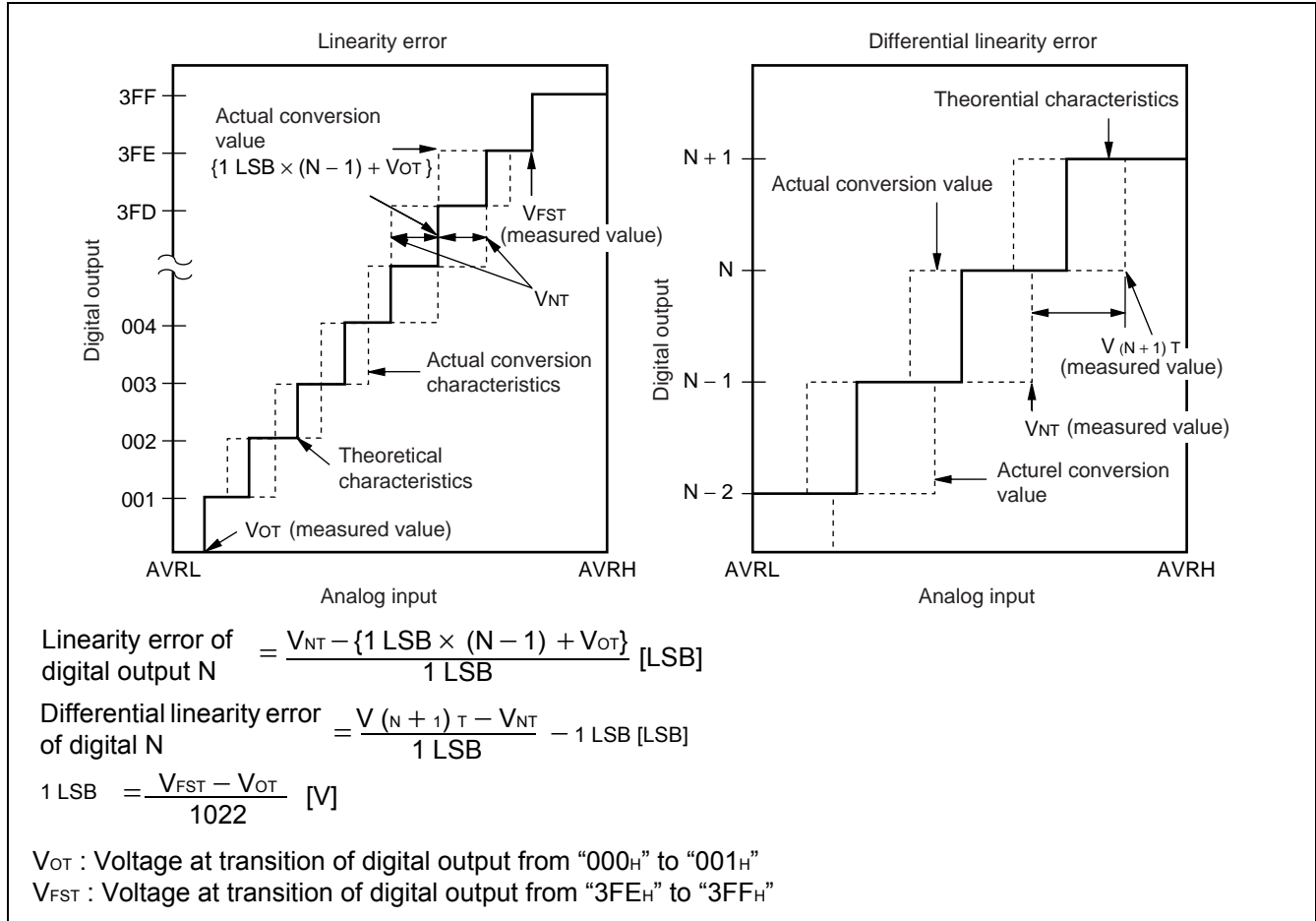
$$V_{FST} (\text{Theoretical value}) = \text{AVRH} - 1.5 \text{ LSB [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

(Continued)

(Continued)

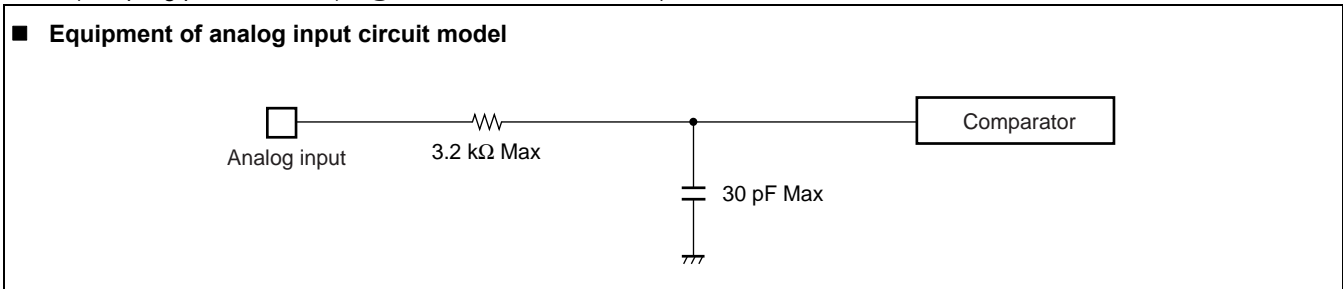


11.5.3 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

Note : When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz) .



11.5.4 Error

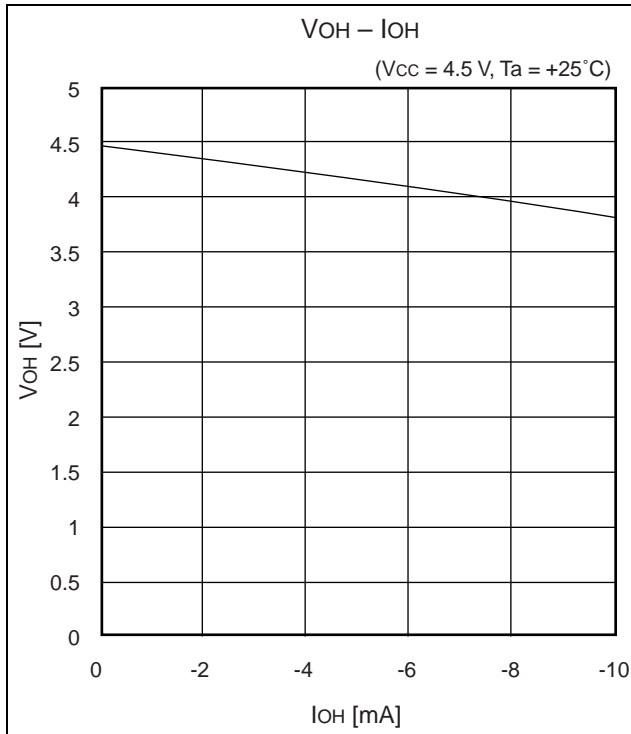
The smaller the | AVRH – AVRL |, the greater the error would become relatively.

11.6 Flash Memory Program/Erase Characteristics

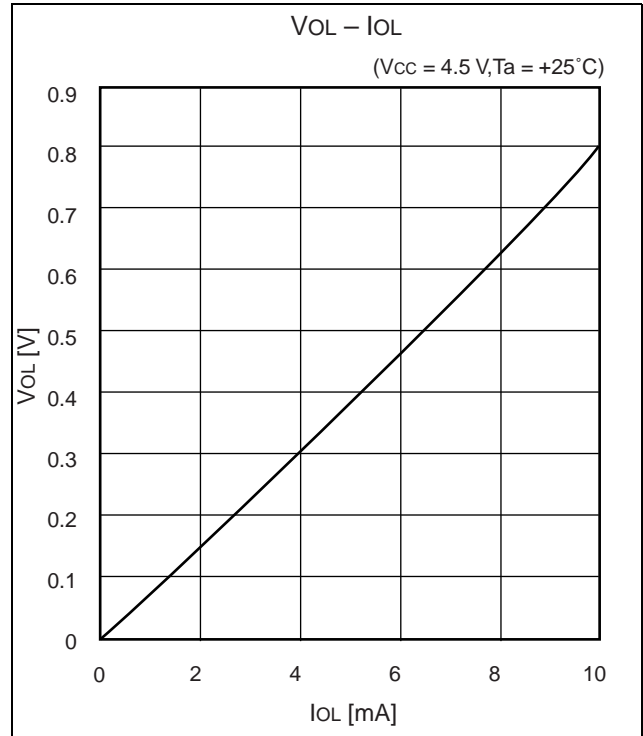
Parameter	Condition	Value			Units	Remarks	
		Min	Typ	Max			
Sector erase time	T _A = + 25 °C V _{CC} = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure	
Chip erase time		—	5	—	s	MB90F543G (S) /F548G (S) /F548GL (S)	Excludes 00H programming prior erasure
		—	7	—	s	MB90F549G (S) /F546G (S)	
Word (16 bit width) programming time		—	16	3,600	μs	Excludes system-level overhead	
Erase/Program cycle	—	10,000	—	—	cycle		

12. Example Characteristics

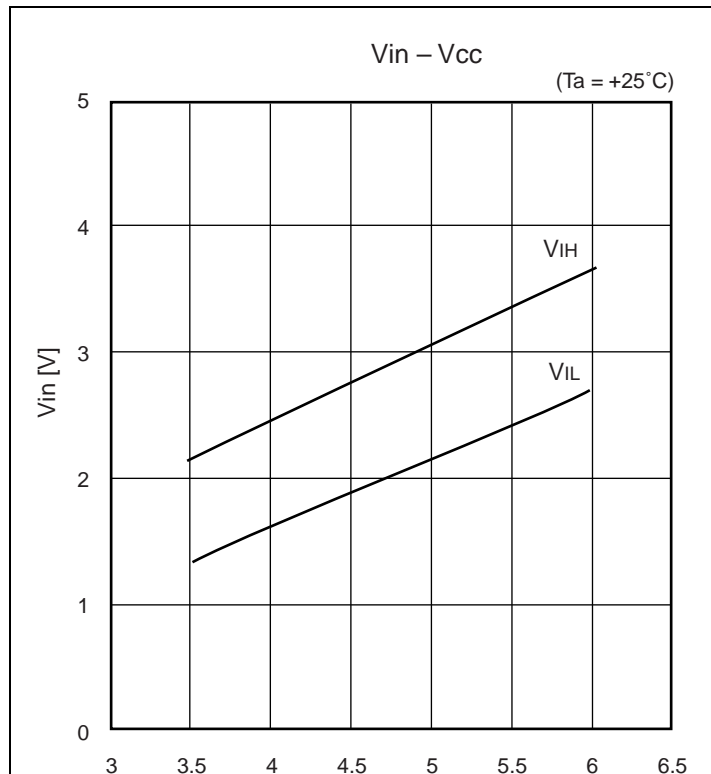
- "H" level output voltage



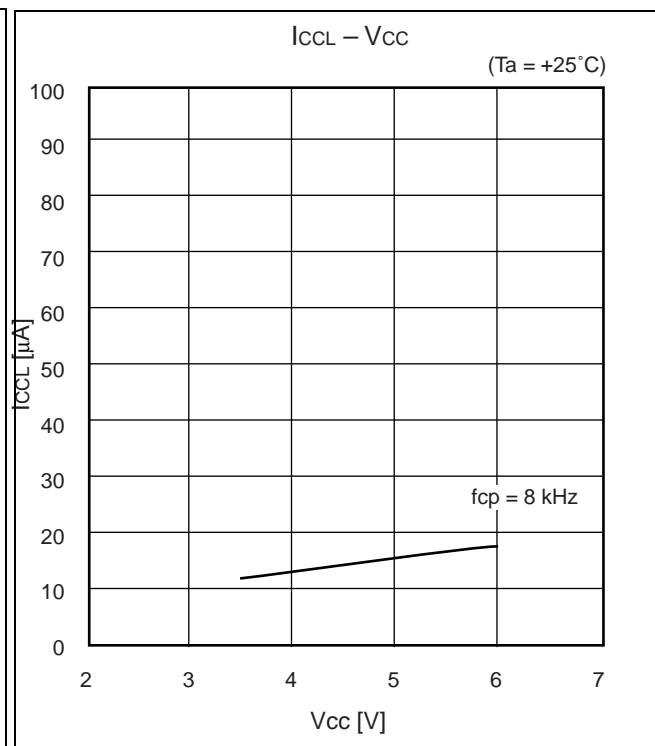
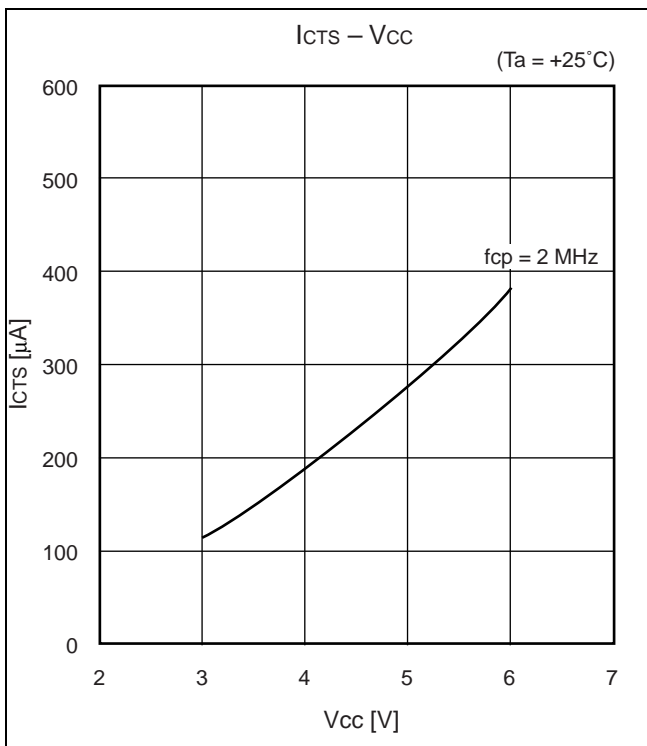
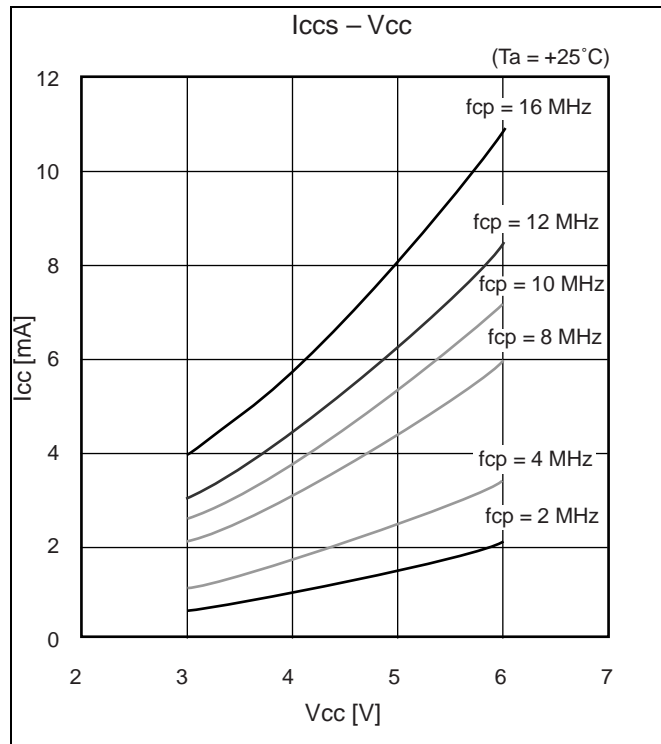
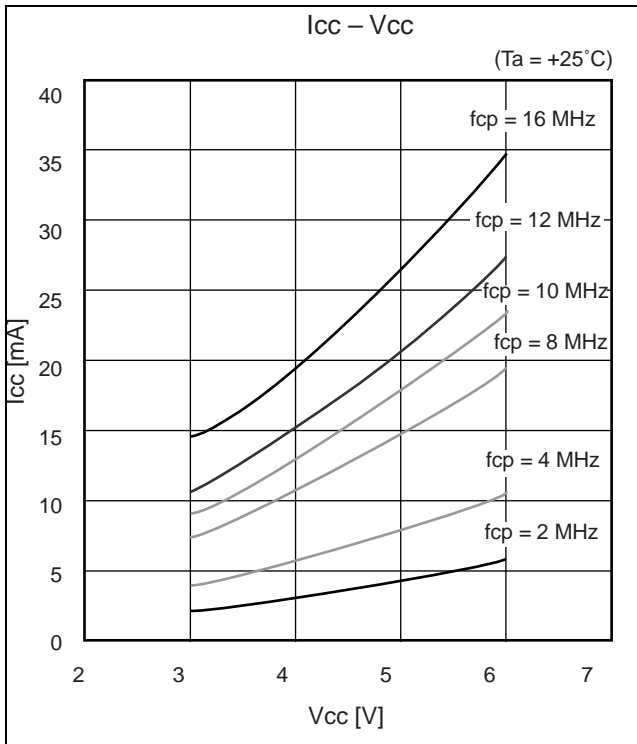
- "L" level output voltage

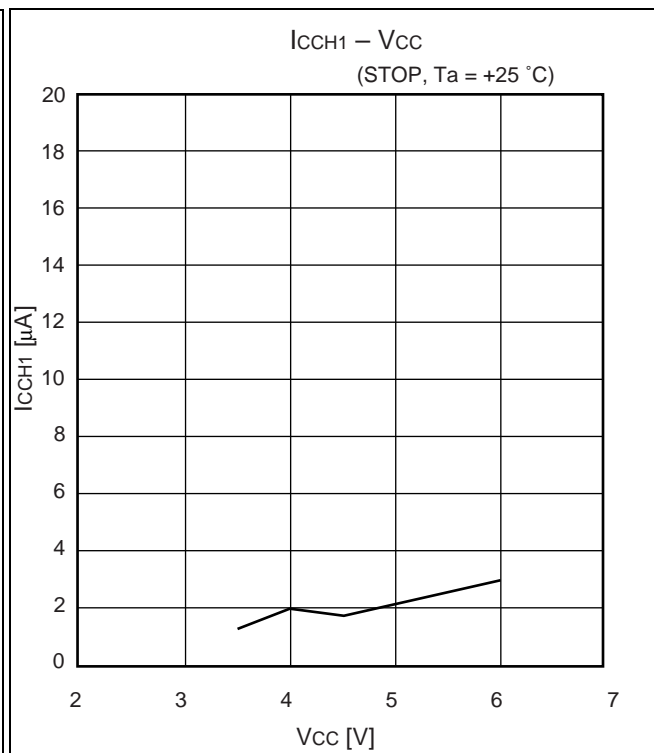
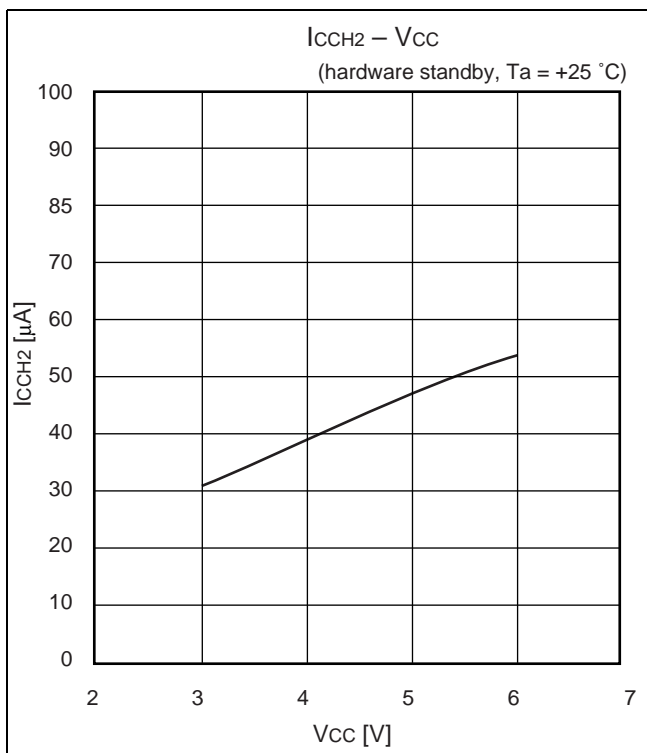
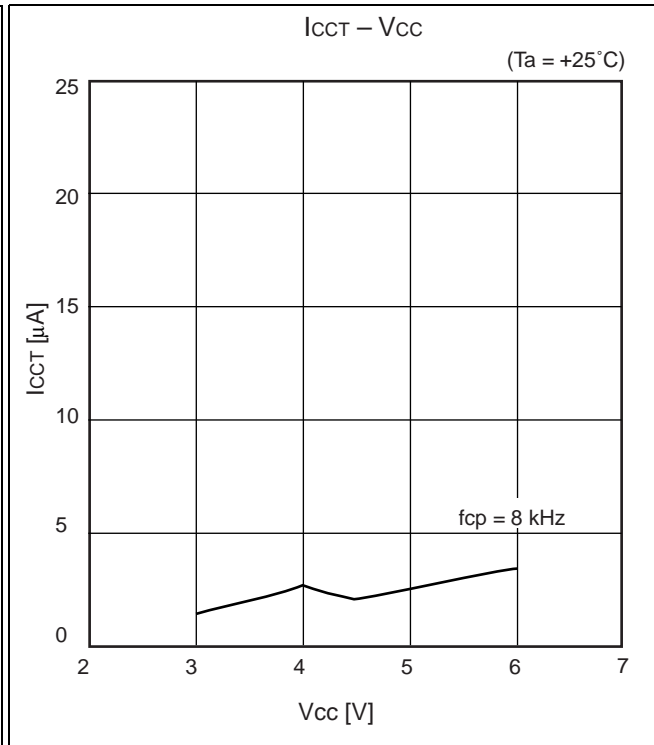
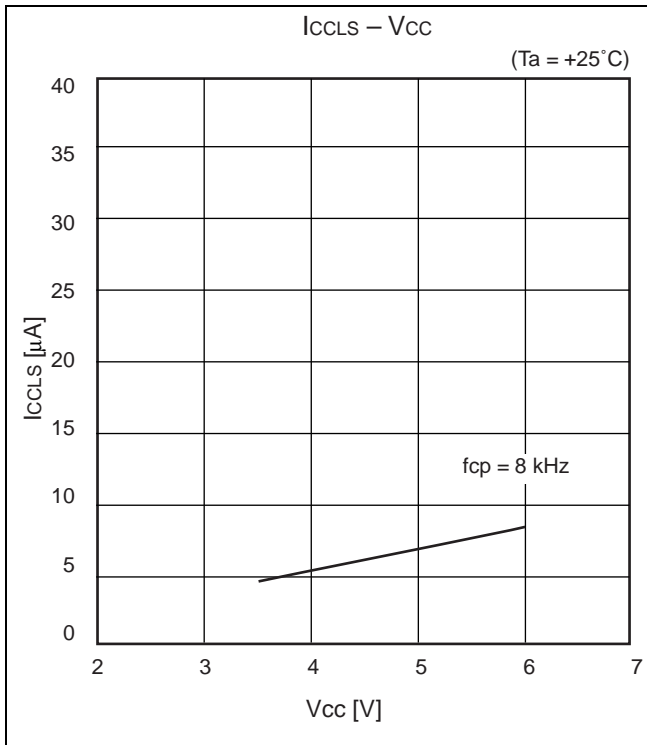


- "H" level input voltage/ "L" level input voltage
(Hysteresis input)

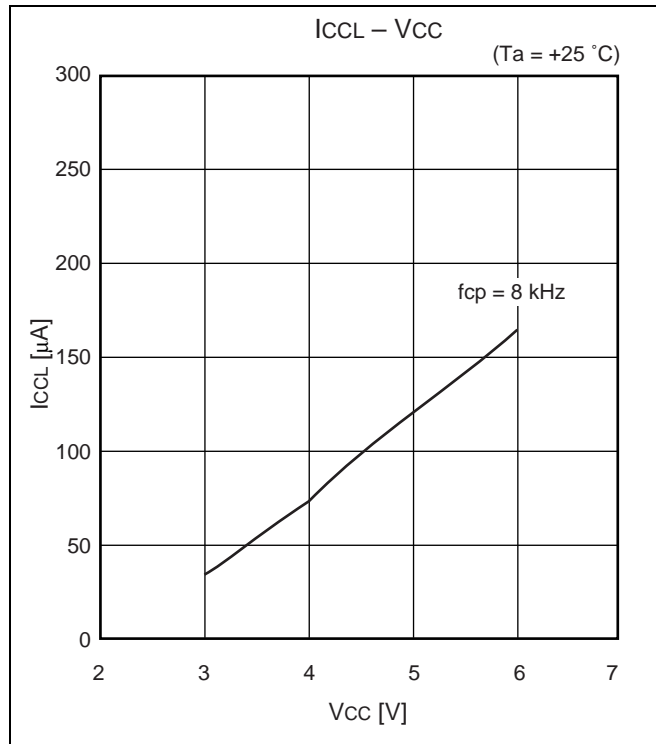
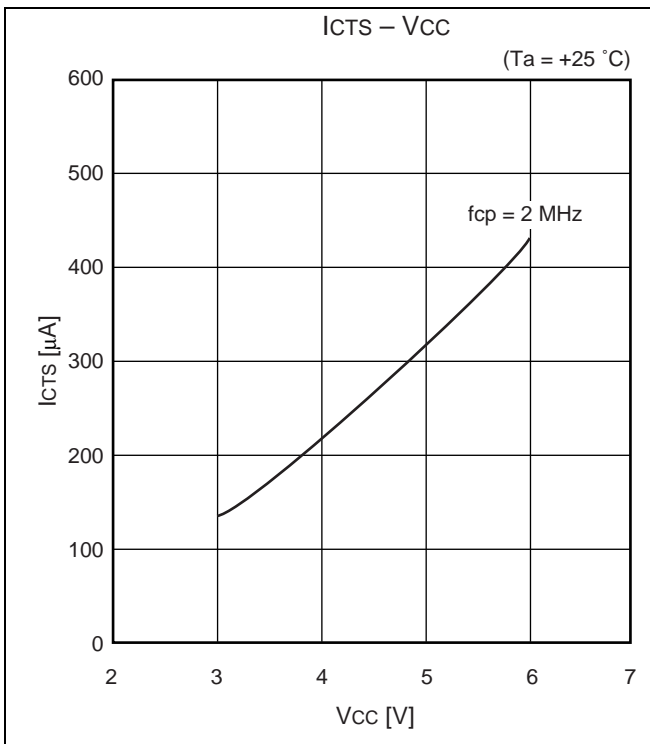
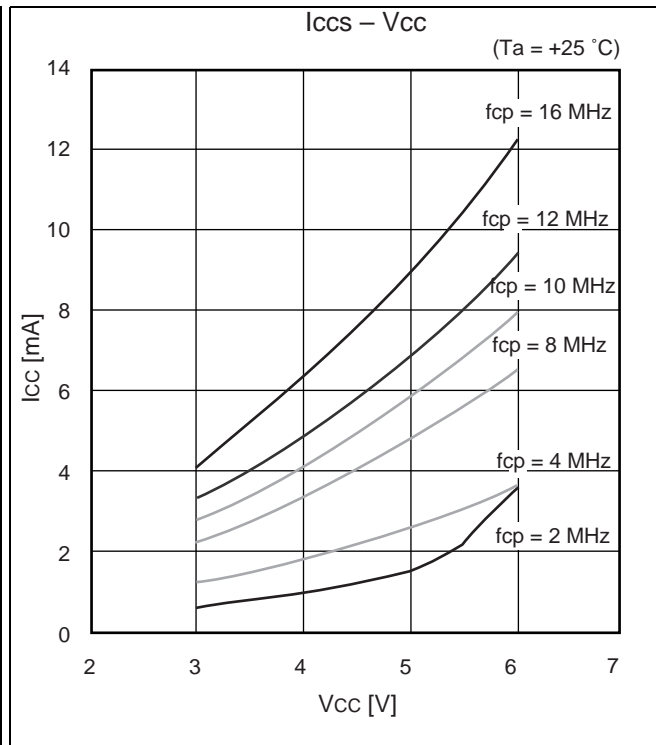
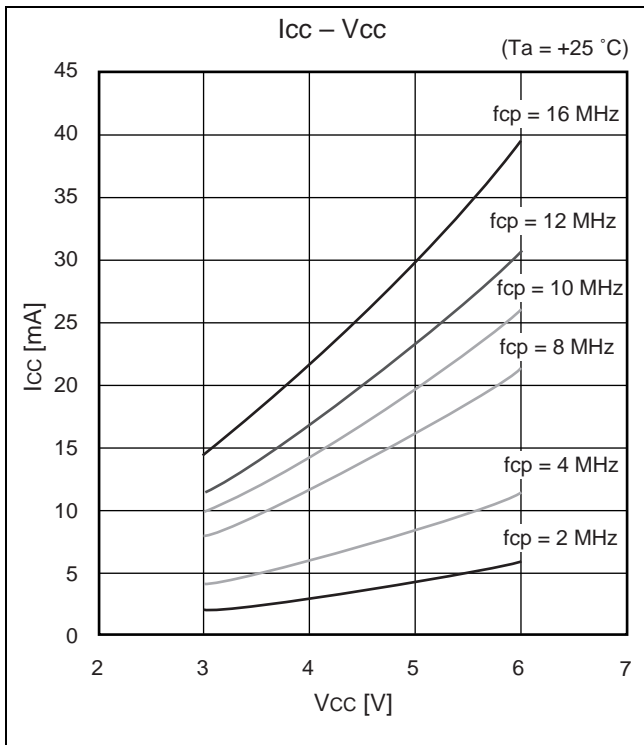


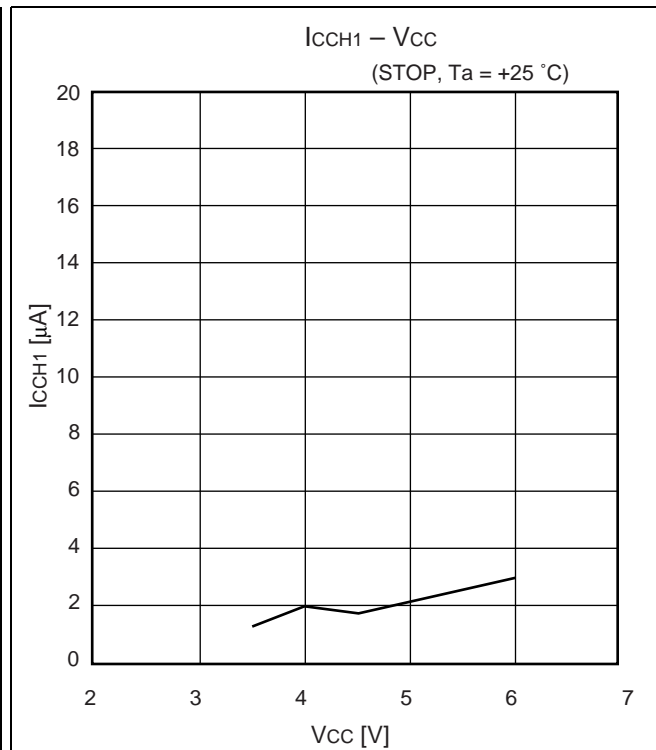
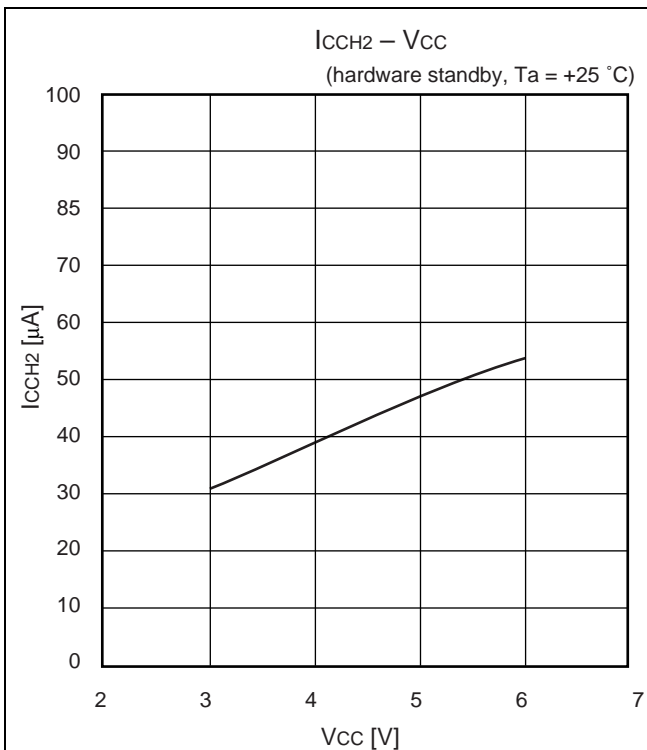
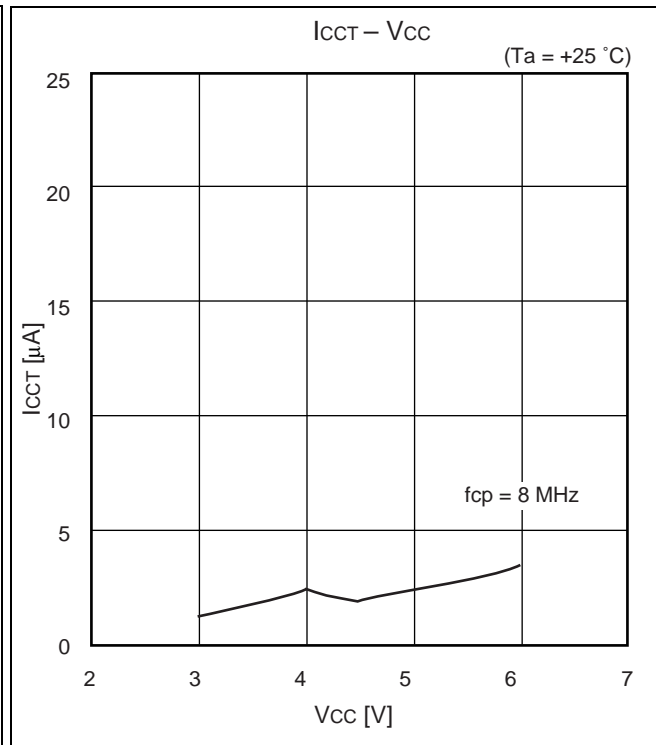
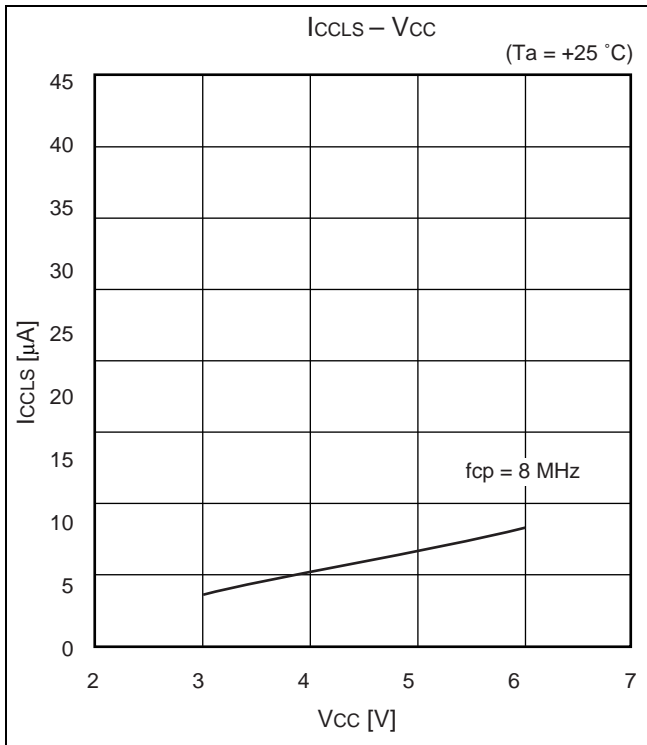
■ Power supply current (MB90549G)





■ Power supply current (MB90F549G)



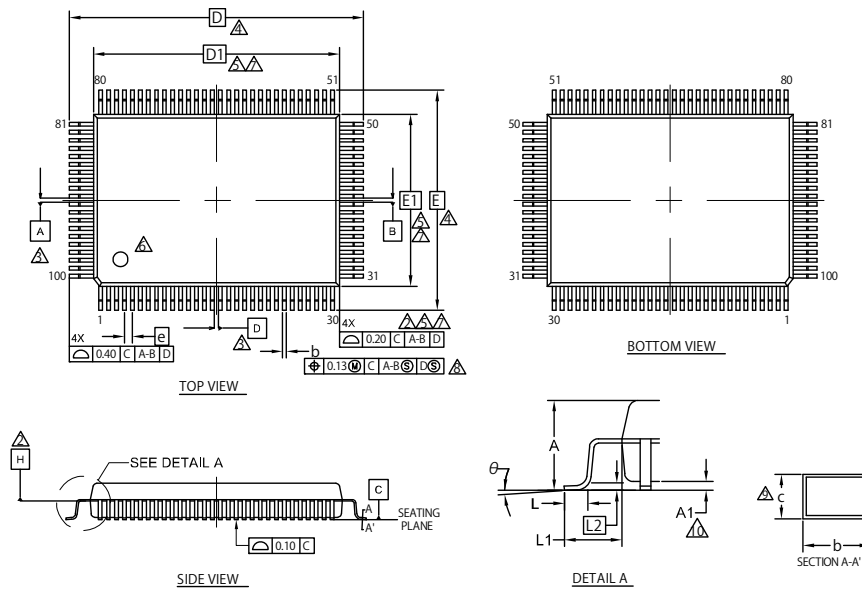


13. Ordering Information

Part number	Package	Remarks
MB90F543GPF MB90F543GSPF MB90F546GPF MB90F546GSPF MB90F548GPF MB90F548GSPF MB90F548GLPF MB90F548GLSPF MB90F549GPF MB90F549GSPF MB90543GPF MB90543GSPF MB90547GPF MB90547GSPF MB90548GPF MB90548GSPF MB90549GPF MB90549GSPF	100-pin Plastic QFP (PQH100)	
MB90F543GPMC MB90F543GSPMC MB90F546GPMC MB90F546GSPMC MB90F548GPMC MB90F548GSPMC MB90F548GLPMC MB90F548GLSPMC MB90F549GPMC MB90F549GSPMC MB90543GPMC MB90543GSPMC MB90547GPMC MB90547GSPMC MB90548GPMC MB90548GSPMC MB90549GPMC MB90549GSPMC	100-pin Plastic LQFP (LQI100)	

14. Package Dimensions

Package Type	Package Code
QFP 100	PQH100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

NOTES

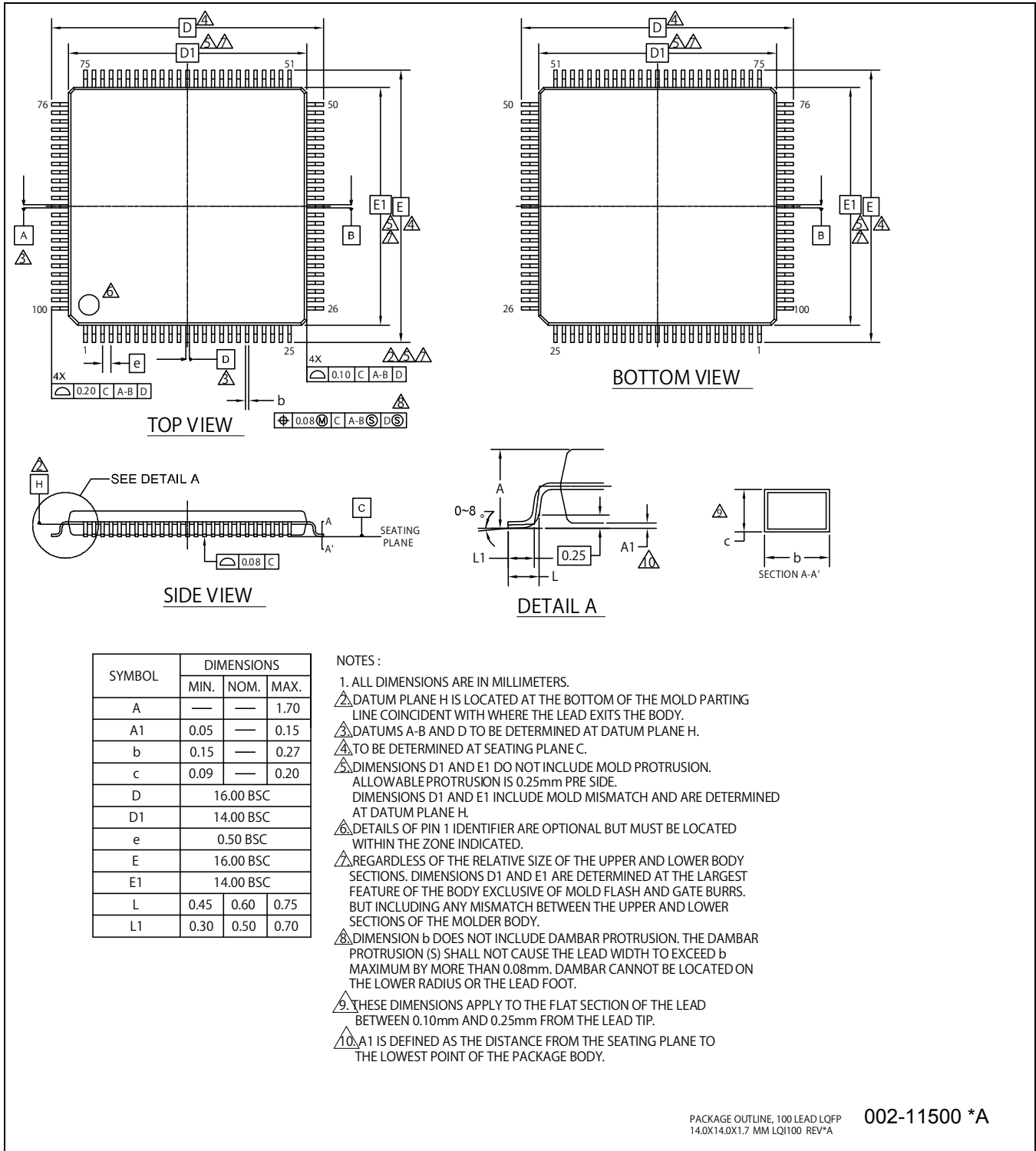
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15156 **

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

(Continued)

Package Type	Package Code
LQFP 100	LQ1100



15. Major Changes

Spansion Publication Number: DS07-13703-7E

Section	Change Results
■ PRODUCT LINEUP	Changed the name in peripheral resource. 16-bit I/O Timer → 16-bit Free-run Timer
■ I/O CIRCUIT TYPE	Changed the name of input typ. Hysteresis → CMOS Hysteresis HYS → CMOS Hysteresis
■ BLOCK DIAGRAM	Changed the arrow direction of SOT1 signal at UART1(SCI). “← →” (input/output) → “←” (output)
■ I/O MAP	Changed the text of “Note”.
■ INTERRUPT MAP	Changed the name of peripheral resource of the pin number: #19. I/O Timer → 16-bit Free-run Timer
■ ELECTRICAL CHARACTERISTICS 2. Recommended Conditions	Changed the remarks of “parameter: Power supply voltage”.
3. DC Characteristics	Changed the maximum value of symbol : VILM of parameter: Input voltage. $V_{CC} + 0.3 \rightarrow V_{SS} + 0.3$
	Added the following remarks for parameter : Pull-down resistance. Except Flash device
4. AC Characteristics (1) Clock Timing	Added the value when using an external clock in Oscillation frequency and Clock cycle time on (1) Clock Timing for parameter.
	Added the item of A/D converter operation range in figure of “■ Guaranteed PLL operation range”
(3) Reset and Hardware Standby Input Timing	Changed the following item. (3) Reset and Hardware Standby Input Timing Remarks: In sub-clock mode, sub-sleep mode, timer mode $2t_{CP} \rightarrow 2t_{LCP}$
(4) Power On Reset	Changed as follows; Due to repetitive operation → Waiting time until power-on
5. A/D Converter	Changed the unit of Zero transition voltage and Full scale transition voltage. mV → V
■ ORDERING INFORMATION	Added the MB90F548GLPMC in Part Numbers.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90F543G(S)/546G(S)/548G(S)/549G(S)/549G(S)/V540G/MB90543G(S)/547G(S)/548G(S)/F548GL(S) CMOS F2MC-16LX MB90540G/545G Series 16-bit Proprietary Microcontroller Document Number: 002-07696				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	11/13/2008	Migrated to Cypress and assigned document number 002-07696. No change to document contents or format.
*A	5537115	AKIH	11/30/2016	Updated to Cypress template
*B	6040590	YSAT	02/05/2018	Adapted new Cypress logo Updated following package code FPT-100P-M06 → PQH100 FPT-100P-M20 → LQI100

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