TF Semiconductor Solutions

Advanced Information

TF1388M

3-Phase Half-Bridge Gate Driver

Features

- **Three floating high-side drivers in bootstrap operation to 250V**
- **420mA source / 750mA sink output current capability**
- **Logic input 3.3V capability**
- **Internal deadtime of 315ns to protect MOSFETs**
- **Matched prop delay time maximum of 50ns**
- **Outputs in phase with inputs**
- **Schmitt triggered logic inputs**
- **Cross conduction prevention logic**
- **Undervoltage lockout for all channels**
- **Extended temperature range: -40°C to +125°C**
- **Space saving SOIC-20 package**

Applications

- 3-Phase Motor Inverter Driver
- White Goods - Air Conditioner, Washing Machine, Refrigerator
- Industrial Motor Inverter - Power Tools, Robotics
- General Purpose 3-Phase Inverter

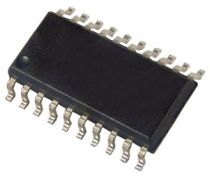
Description

The TF1388M is a three-phase gate driver IC designed for high voltage three-phase applications, driving N-channel MOSFETs and IGBTs in a half-bridge configuration. TF Semiconductor's high voltage process enables the TF1388M high sides to switch to 250V in a bootstrap operation.

The TF1388M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices and are enabled low to better function in high noise environments. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF1388M offers numerous protection functions. A shoot-through protection logic prevents both outputs being high with both inputs high (fault state), an undervoltage lockout for V_{CC} shuts down all drivers through an internal fault control, and a UVLO for V_{BS} shuts down the respective high side output. The TF1388M is offered in SOIC 20 package and operates over an extended -40 °C to +125 °C temperature range.

SOIC-20

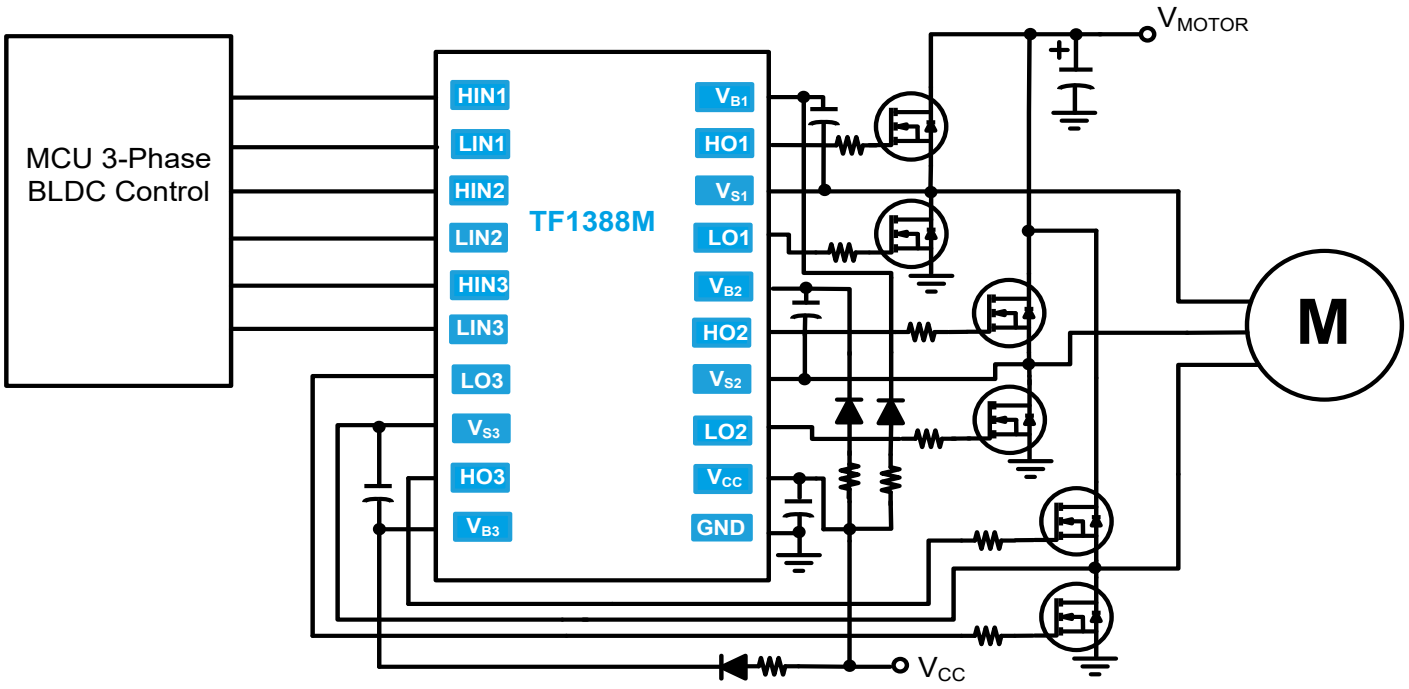


Ordering Information

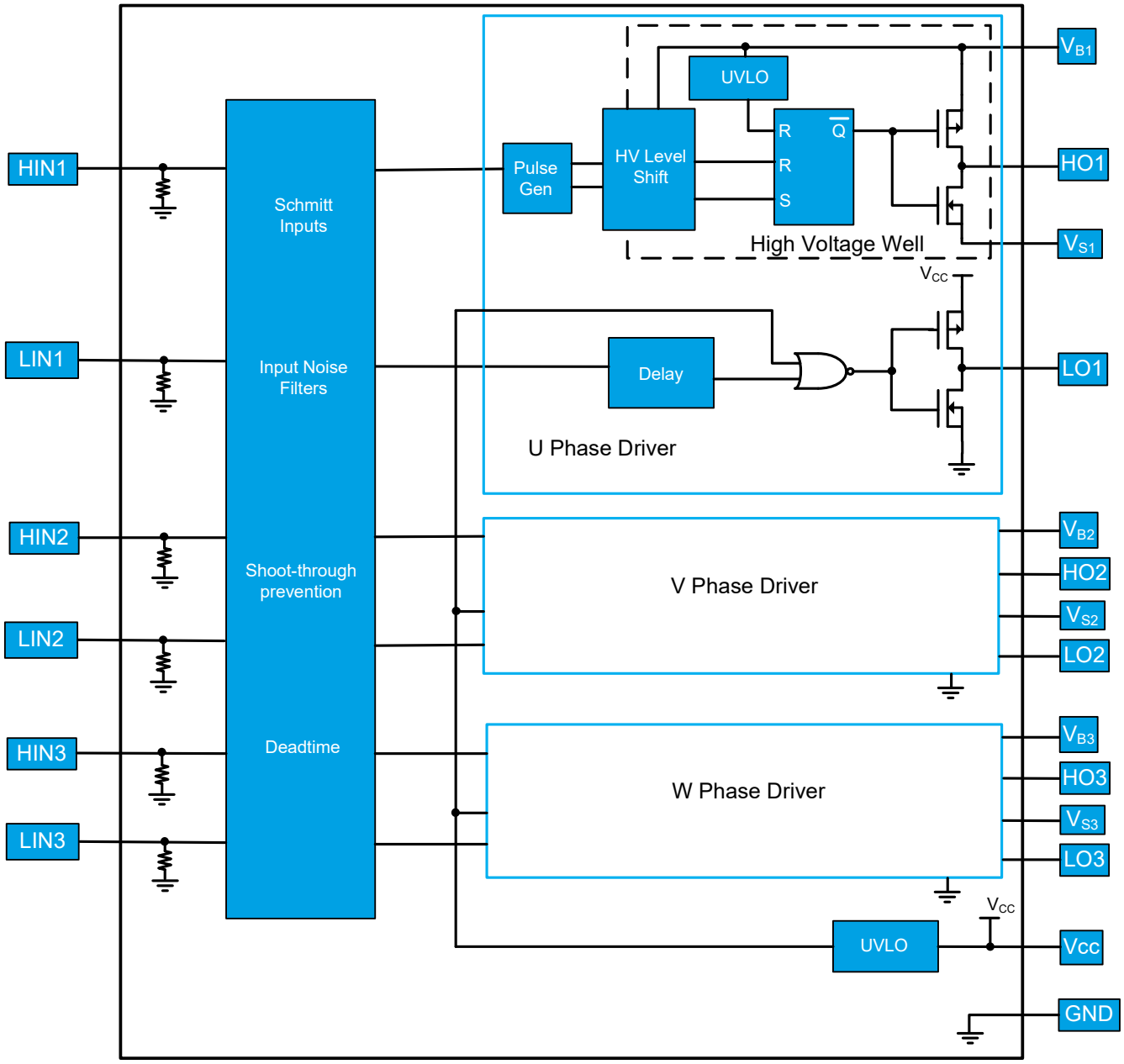
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF1388M-TGU	SOIC-20	Tube / 35	YYWW TF2388M Lot ID
TF1388M-TGH	SOIC-20	T&R / 1500	

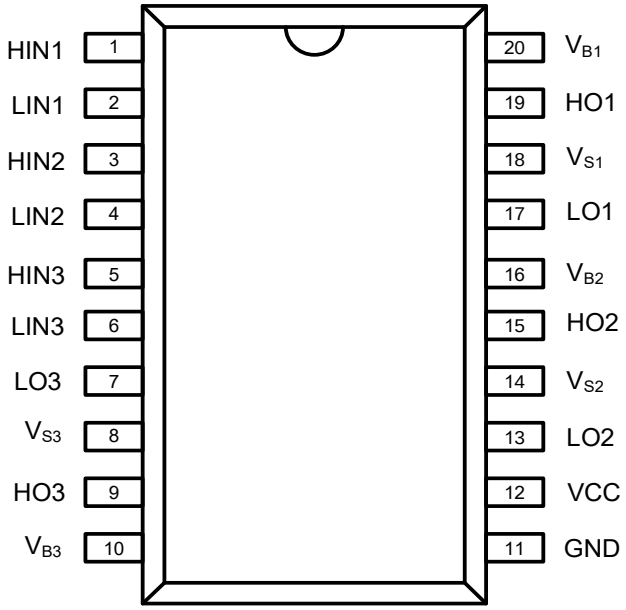
Typical Application



Functional Block Diagram



Pin Diagram



Top View: SOIC-20

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
HIN1, HIN2, HIN3	1, 3, 5	Logic input for high-side gate driver output, in phase with HO.
LIN1, LIN2, LIN3	2, 4, 6	Logic input for low-side gate driver output, in phase with LO.
LO3, LO2, LO1	7, 13, 17	Low-side gate driver output
V_{S3},V_{S2},V_{S1}	8, 14, 18	High-side floating supply return
HO3, HO2, HO1	9, 15, 19	High-side gate driver output
V_{B3},V_{B2},V_{B1}	10, 16, 20	High-side floating supply
GND	11	Low-side driver and logic return
VCC	12	Low-side and logic fixed supply

Absolute Maximum Ratings *(NOTE1)*

V_B - High-side floating supply voltage.....-0.3V to +274V
V_S - High-side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High-side floating output voltage.....V_S-0.3V to V_B+0.3V
V_{LO} - Low-side output voltage.....-0.3V to V_{CC}+0.3V
dV_S/dt - Offset supply voltage transient.....50 V/ns
V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
V_{IN} - Logic input voltage (HIN and LIN).....-0.3V to 5.5V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at T_A=25°C
SOIC-20.....1.88W

SOIC-20 Thermal Resistance ***(NOTE2)***
θ_{JA}.....66.6°C/W

T_J - Junction operating temperature.....+150 °C
T_L - Lead Temperature (soldering, 10 seconds).....+300 °C
T_{stg} - Storage temerature .....-55 to 150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	250	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	COM	V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +250V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "0" input voltage	*NOTE5*	2.4			V
V_{IL}	Logic "1" input voltage				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.2	0.5	
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.07	0.2	
I_{LK}	Offset supply leakage current	VB = VS = 250V			10	μA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		50	80	
I_{BSO}	Operating V_{BS} supply current	fs = 20khz		400		
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		230	330	
I_{CCO}	Operating V_{CC} supply current	fs = 20khz		500		
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		25	80	
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			2	
R_{IN}	Input pull-down resistance			200		kΩ
V_{BSUV+} V_{CCUV+}	V_{BS} and V_{CC} supply under-voltage positive going threshold		7.1	8.5	9.9	V
V_{BSUV-} V_{CCUV-}	V_{BS} and V_{CC} supply under-voltage negative going threshold		6.7	8.1	9.5	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 μs	270	420		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 μs	600	750		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HIN1,2,3 and LIN1,2,3). The V_O and I_O parameters are applicable to the outputs (HO1,2,3 and LO1,2,3 and are referenced to COM.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HINx and LINx) should have an amplitude of 2.4V minimum with a pulse width of 600ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V	70	120	170	ns
t_{off}	Turn-off propogation delay	V_S = 0V	70	120	170	
t_r	Turn-on rise time	V_S = 0V		45	75	
t_f	Turn-off fall time			25	40	
t_{DM}	Delay matching				50	ns
t_{DT}	Deadtime		200	315	430	ns
t_{DTM}	Deadtime matching				50	ns

Timing Waveforms

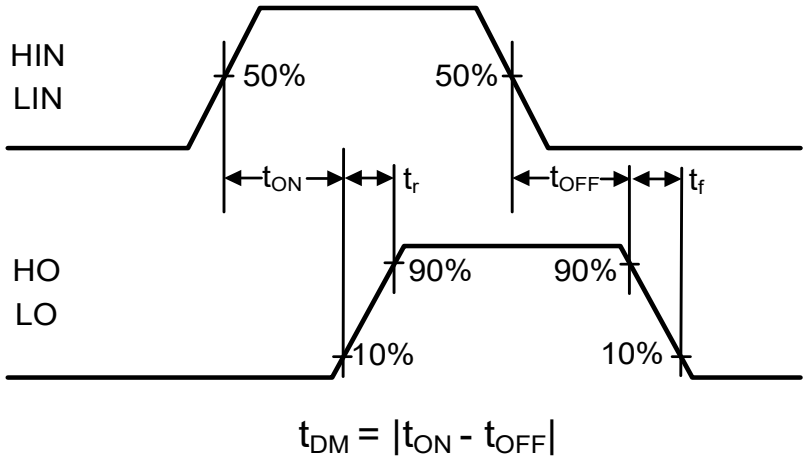


Figure 1. Switching Time Waveform Definitions

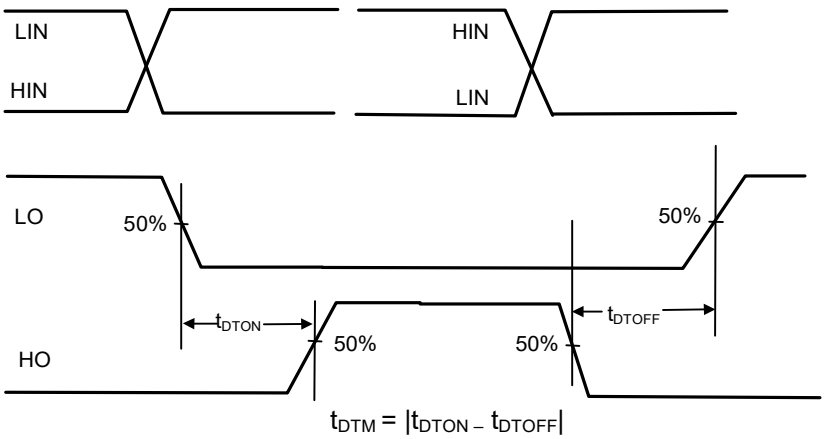
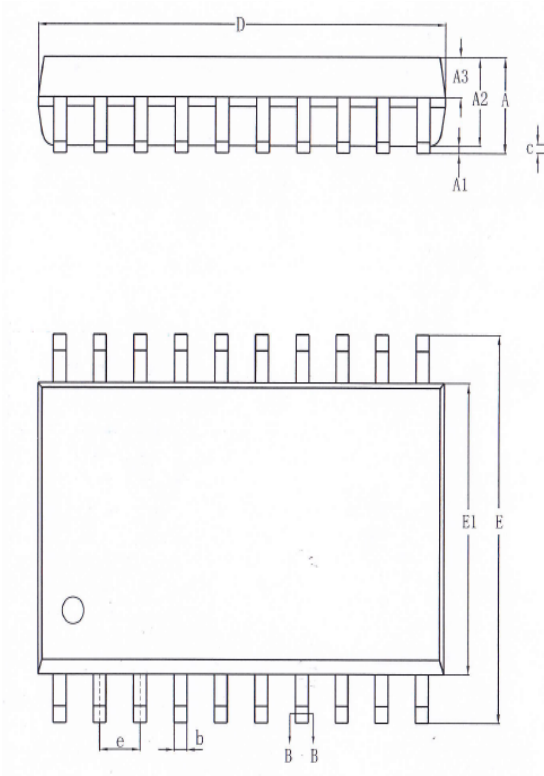
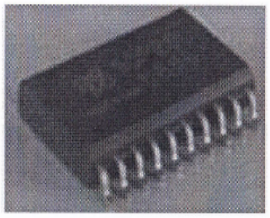


Figure 2. Deadtime Waveform Definitions

Package Dimensions (SOIC-20)





	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
	A	—	—	2.65
	A1	0.10	—	0.30
	A2	2.25	2.30	2.35
	A3	0.97	1.02	1.07
⚠	b	0.35	—	0.43
⚠	b1	0.34	0.37	0.40
⚠	c	0.25	—	0.29
	c1	0.24	0.25	0.26
⚠	D	12.70	12.80	12.90
	E	10.10	10.30	10.50
⚠	E1	7.40	7.50	7.60
	e	1.27BSC		
	L	0.70	—	1.00
	L1	1.40REF		
	θ	0	—	8°

Revision History

Rev.	Change	Owner	Date
1.0	First release, advanced information datasheet	Duke Walton	10/20/2022

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