Data Sheet

# QCFJ-3439T

## Automotive 17A Peak Gate Drive Optocoupler with Integrated Desaturation Sensing, Active Miller Clamping, FAULT, GATE, and UVLO Status Feedback and Negative Bias

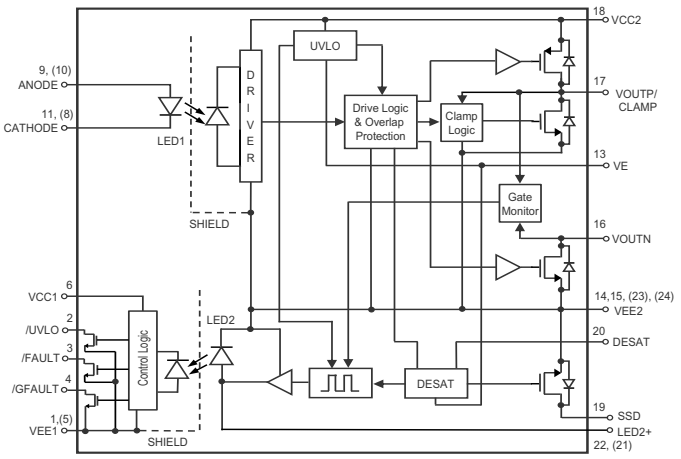
## Description

The Broadcom® QCFJ-3439T is a 17A peak smart gate drive optocoupler. The high peak output current and wide operating voltage range make it ideal for driving IGBT or MOSFET directly in motor-control and inverter applications.

The device features fast propagation delay with excellent timing skew performance. It provides IGBT/MOSFET with desaturation protection and functional safety reporting. This full-featured and easy-to-implement gate drive optocoupler comes in a compact, surface-mountable SO-24 package with 0.8-mm pitch for space-savings, so it is suitable for HEV and EV applications.

Broadcom R$^2$Coupler™ isolation products provide reinforced insulation and reliability that deliver safe signal isolation critical in automotive and high-temperature industrial applications.

**Figure 1: QCFJ-3439T Functional Diagram**




## Features

- Qualified to AEC-Q100 Grade 1 test guidelines[1]
- Automotive temperature range: –40°C to +125°C
- Minimum peak output current: ±10A
- Minimum Miller clamp sinking current: 1A
- Maximum propagation delay: 140 ns
- Integrated fail-safe IGBT/MOSFET protection
  - IGBT/MOSFET desaturation sensing with configurable “Soft” turn-off and feedback
  - Under Voltage Lock-out (UVLO) protection with feedback
- Functional safety reporting
  - IGBT/MOSFET desaturation fault feedback
  - IGBT/MOSFET gate status feedback
  - UVLO status feedback
- High noise immunity
  - Common-mode Rejection (CMR): 100 kV/µs at $V_{CM}$ = 1000V
  - Miller current clamping
  - Direct LED input with low input impedance and low noise sensitivity
  - Negative gate bias
- SO-24 package with 8-mm creepage and clearance
- Regulatory approvals:
  - UL1577, CSA
  - IEC 60747-5-5

## Applications

IGBT/SiC MOSFET gate driver for traction inverter, charger, and HVAC.

1. Refer to ESD immunity.

# Ordering Information

| Part Number | Option (RoHS Compliant) | Package | Surface Mount | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity |
|---|---|---|---|---|---|---|
| QCFJ-3439T | -500UE | SO-24 | X | X | X | 850 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

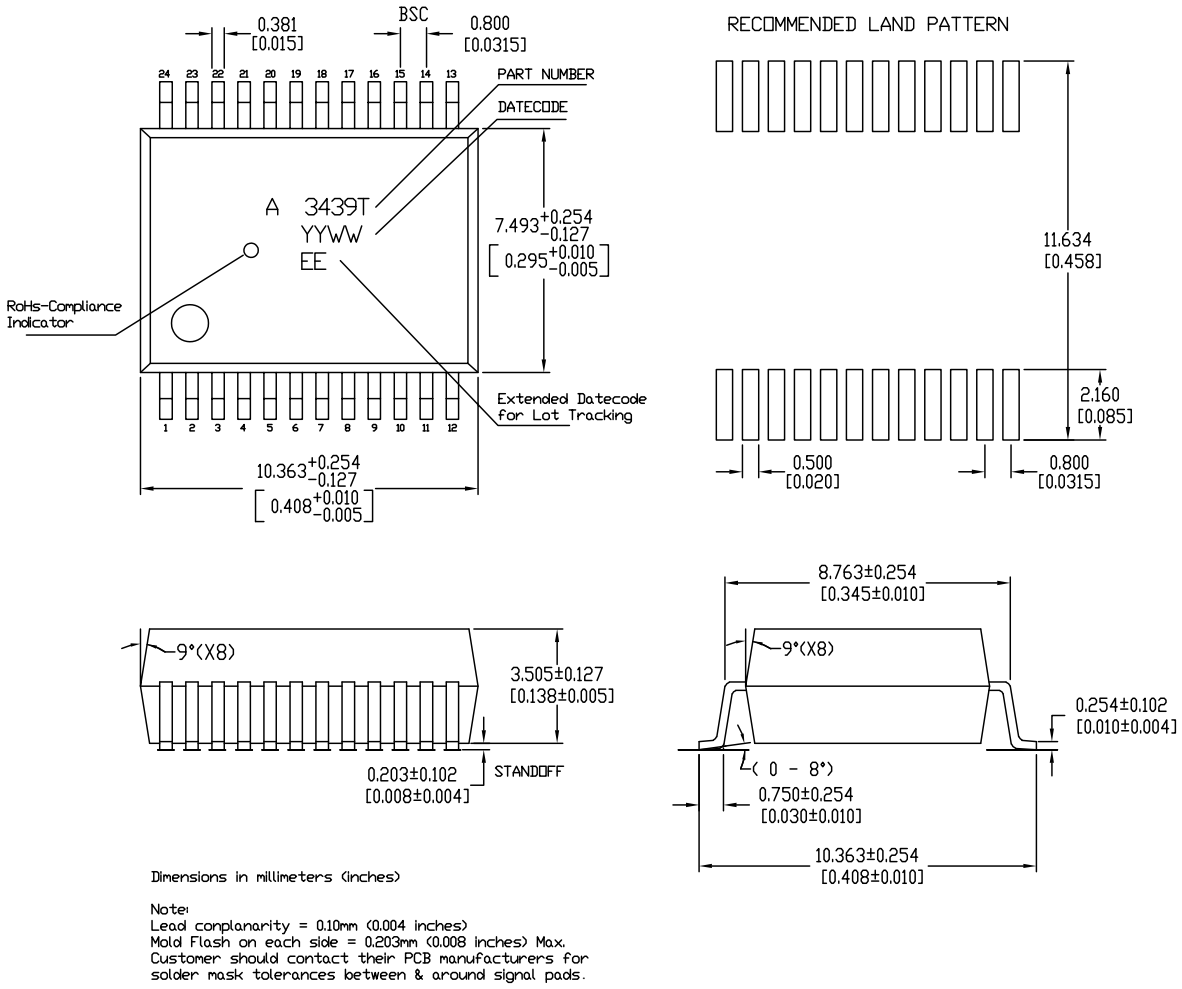
Example 1:

QCFJ-3439T-500UE to order product of SO-24 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

# Package Outline Drawing

**Figure 2: Package Outline Drawing (24-Lead Surface Mount)**



# Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest version).

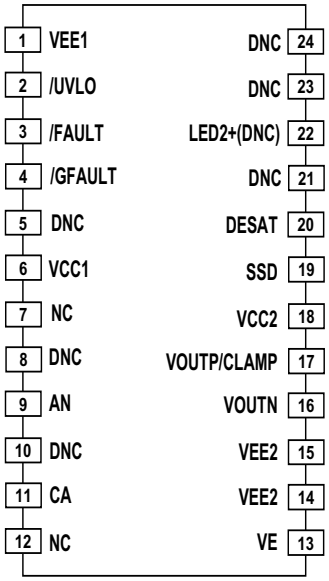
**NOTE:** Non-halide flux should be used.

# Product Overview Description

The QCFJ-3439T (shown in Figure 1) is a highly integrated power control device that incorporates all the necessary components for an isolated IGBT/MOSFET gate drive circuit. It is primarily designed with high peak driving current capability to ensure optimum performance for direct driving IGBT/MOSFET in various applications. Besides high peak output current, it incorporates fail-safe IGBT/MOSFET desaturation sensing with soft gate turn-off and feedback, active Miller current clamping, and functional safety feedbacks of supply UVLO and gate status, in a compact SO-24 package. Direct LED input allows flexible logic configuration and differential current mode driving with low input impedance, greatly increasing its noise immunity.

# Package Pin Out

**Figure 3: QCFJ-3439T Pin Configuration**




# Pin Description

**Table 1: Pin Description**

| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | VEE1 | Input ground |
| 2 | /UVLO | VCC1 under voltage feedback and VCC2 under voltage lock-out feedback |
| 3 | /FAULT | Desaturation fault feedback |
| 4 | /GFAULT | IGBT/MOSFET gate status feedback |
| 5 | DNC | Do not connect (Internally this pin is connected to VEE1 lead frame.) |
| 6 | VCC1 | Input positive power supply |
| 7 | NC | No connection |
| 8 | DNC | Do not connect (Internally connected to input LED cathode lead frame.) |
| 9 | AN | Input LED anode |
| 10 | DNC | Do not connect (Internally connected to input LED anode lead frame.) |
| 11 | CA | Input LED cathode |
| 12 | NC | No connection |
| 13 | VE | IGBT emitter/ MOSFET source reference |
| 14 | VEE2 | Output negative power supply |
| 15 | VEE2 | Output negative power supply |
| 16 | VOUTN | Output driver to turn-off IGBT/MOSFET gate |
| 17 | VOUTP/CLAMP | Output driver to turn-on IGBT/MOSFET gate/ Miller current clamping output |
| 18 | VCC2 | Output positive power supply |
| 19 | SSD | Soft shutdown output driver |

**Table 1: Pin Description (Continued)**

| Pin No. | Pin Name | Function |
|---|---|---|
| 20 | DESAT | Desaturation protection sensing |
| 21 | DNC | Do not connect (Internally connected to LED2+ lead frame.) |
| 22 | LED2+(DNC) | Do not connect, for testing only |
| 23 | DNC | Do not connect (Internally connected to VEE2 lead frame.) |
| 24 | DNC | Do not connect (Internally connected to VEE2 lead frame.) |

# Organization Approval

The QCFJ-3439T is approved by the following organizations.

| | |
|---|---|
| **UL** | Approved under UL 1577, component recognition program up to $V_{ISO}$ = 5000 $V_{RMS}$ |
| **CAN/CSA** | Approved under CAN/CSA-C22.2 No.62368-1 |
| **IEC/EN/DIN EN 60747-5-5** | Approved under: IEC 60747-5-5, EN 60747-5-5, DIN EN 60747-5-5 |

# IEC/EN/DIN EN60747-5-5 Insulation Characteristics[2]

| Description | Symbol | Characteristic | Units |
|---|---|---|---|
| Insulation Classification per DIN VDE 0110/1.89, Table 1 | | | |
| For rated mains voltage ≤ 150 Vrms | | I-IV | |
| For rated mains voltage ≤ 300 Vrms | | I-IV | |
| For rated mains voltage ≤ 600 Vrms | | I-IV | |
| Climatic Classification | | 40/125/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | 1230 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method b[a]<br>$V_{IORM} \times 1.875 = V_{PR}$, 100% production test with tm = 1s, partial discharge < 5 pC | $V_{PR}$ | 2306 | $V_{PEAK}$ |
| Input to Output Test Voltage, Method a[a]<br>$V_{IORM} \times 1.6 = V_{PR}$, type and sample test, tm = 10s, partial discharge < 5 pC | $V_{PR}$ | 1968 | $V_{PEAK}$ |
| Highest Allowable Overvoltage (transient overvoltage $t_{ini}$ = 60s) | $V_{IOTM}$ | 8000 | $V_{PEAK}$ |
| Safety-limiting values – maximum values allowed in the event of a failure | | | |
| Case Temperature | $T_S$ | 175 | °C |
| Input Current | $I_{S,INPUT}$ | 400 | mA |
| Output Power | $P_{S,OUTPUT}$ | 1200 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500V | $R_S$ | $> 10^9$ | Ω |

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog,* under Product Safety Regulation section IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.

# Insulation and Safety-Related Specifications

| Parameter | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Minimum External Air Gap (Clearance) | L(101) | 8.3 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 8.3 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.3 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and the detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1. |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110). |

2. Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by the protective circuits in the application. The surface mount classification is class A in accordance with CECCOO802.

# Absolute Maximum Ratings

Unless otherwise specified, all voltages at input IC reference to $V_{EE1}$, all voltages at output IC reference to $V_{EE2}$.

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | –55 | 150 | °C | |
| Operating Temperature | $T_A$ | –40 | 125 | °C | |
| IC Junction Temperature | $T_J$ | — | 150 | °C | |
| Average LED Input Current | $I_{F(AVG)}$ | — | 20 | mA | |
| Peak Transient LED Input Current (<1-µs pulse width, 300 pps) | $I_{F(TRAN)}$ | — | 1 | A | |
| LED Reverse Input Voltage ($V_R$) | $V_{CA} – V_{AN}$ | — | 6 | V | |
| Input Supply Voltage | $V_{CC1}$ | –0.5 | 6 | V | a |
| /UVLO Pin Voltage | $V_{/UVLO}$ | –0.5 | 6 | V | a |
| /FAULT Pin Voltage | $V_{/FAULT}$ | –0.5 | 6 | V | a |
| /GFAULT Pin Voltage | $V_{/GFAULT}$ | –0.5 | 6 | V | a |
| /UVLO Output Sinking Current | $I_{/UVLO}$ | — | 5 | mA | |
| /FAULT Output Sinking Current | $I_{/FAULT}$ | — | 5 | mA | |
| /GFAULT Output Sinking Current | $I_{/GFAULT}$ | — | 5 | mA | |
| Total Output Supply Voltage | $V_{CC2}$ | –0.5 | 30 | V | b |
| Positive Output Supply Voltage | $V_{CC2} – V_E$ | –0.5 | $30 – (V_E – V_{EE2})$ | V | |
| Negative Output Supply Voltage | $V_{EE2} – V_E$ | –15 | 0.5 | V | |
| DESAT Pin Voltage | $V_{DESAT} – V_E$ | –0.5 | $V_{CC2}$ + 0.5 | V | |
| Gate Driver Output Voltage, SSD | $V_{SSD}$ | –0.5 | $V_{CC2}$ + 0.5 | V | b |
| Gate Driver Output Voltage, $V_{OUTP}$/CLAMP | $V_{OUTP/CLAMP}$ | –0.5 | $V_{CC2}$ + 0.5 | V | b |
| Gate Driver Output Voltage, $V_{OUTN}$ | $V_{OUTN}$ | –0.5 | $V_{CC2}$ + 0.5 | V | b |
| Peak Output Current for $V_{OUTP}$ and $V_{OUTN}$ | $\|I_{OUT(PEAK)}\|$ | — | 10 | A | c |
| Peak Miller Clamp Sinking Current | $I_{CLAMP(PEAK)}$ | — | 5 | A | d |
| Desat Discharge Current (Continuous) | $I_{DSCHG}$ | — | 12 | mA | |
| Output IC Power Dissipation | $P_O$ | — | 800 | mW | e |
| Input IC Power Dissipation | $P_I$ | — | 150 | mW | f |
| ESD Immunity | $\|V_{ESD}\|$ | — | 2 | kV | g |
| | | — | 1.5 | kV | h |
| | | — | 750 | V | i |
| | | — | 500 | V | j |

a. Reference to $V_{EE1}$.

b. Reference to $V_{EE2}$.

c. Maximum pulse width=5 µs, maximum duty cycle=1%. The peak output current is limited to ±10A by external resistors. See Printed Circuit Board Layout Recommendation in the applications notes section to take care of high current loops during gate switching. All operating conditions should not exceed maximum junction temperature rating.

d. Maximum pulse width=5 µs, maximum duty cycle=1%.

e. Output IC power dissipation is derated linearly above 105°C from 800 mW to 550 mW at 125°C for a high effective thermal conductivity board. For a low effective thermal conductivity board, output IC power dissipation is derated linearly above 105°C from 700 mW to 350 mW at 125°C. PCB thermal resistance characteristic must be considered so as not to exceed the absolute maximum rating. See Figure 4 for details.

f. Input IC power dissipation is derated linearly above 105°C from 150 mW to 125 mW at 125°C for high effective thermal conductivity board. For low effective thermal conductivity board, input IC power dissipation is derated linearly above 105°C from 120 mW to 100 mW at 125°C. See Figure 4 for details.

g. Human Body Model (HBM) per AEC Q100-002, all pins expect LED2 (pins 21, 22).

h. Human Body Model (HBM) per AEC Q100-002, pins 21, 22.

i. Charge Device Model (CDM) per AEC Q100-011, all corner pins.

j. Charge Device Model (CDM) per AEC Q100-011, all pins.

# Recommended Operating Conditions

Unless otherwise specified, all voltages at input IC reference to $V_{EE1}$, all voltages at output IC reference to $V_{EE2}$.

| Parameter | Symbol | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | –40 | 125 | °C | |
| Input IC Supply Voltage | $V_{CC1}$ | 4.5 | 5.5 | V | |
| Total Output IC Supply Voltage | $V_{CC2} – V_{EE2}$ | 15 | 25 | V | a |
| Positive Output IC Supply Voltage | $V_{CC2} – V_E$ | 15 | 20 | V | |
| Negative Output IC Supply Voltage | $V_{EE2} – V_E$ | –10 | 0 | V | b |
| Input LED Turn-on Current | $I_{F(ON)}$ | 11 | 16 | mA | |
| Input LED Turn-off Voltage ($V_{AN} – V_{CA}$) | $V_{F(OFF)}$ | –5.5 | 0.8 | V | |
| Input LED Turn On Pulse Width | $T_{on(LED)}$ | 100 | — | ns | c |

a. Should not exceed absolute maximum rating of total output supply voltage.

b. Negative output IC supply is optional. Connect $V_E$ to $V_{EE2}$ if negative gate bias is not required by the application.

c. Minimum input pulse width for a guaranteed output pulse under no load condition.

# Electrical and Switching Specifications

Unless otherwise specified, all minimum/maximum specifications are at recommended operating conditions; all voltages at input IC reference to $V_{EE1}$, all voltages at output IC reference to $V_{EE2}$. All typical values at $T_A$ = 25°C, $V_{CC1}$ = 5V, $V_{CC2} – V_E$ = 15V, $V_{EE2} – V_E$ = –10V.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| **IC Supply Current** | | | | | | | | |
| Input Supply Current | $I_{CC1}$ | 1 | 1.6 | 2.5 | mA | | 7 | |
| Output High Supply Current | $I_{CC2H}$ | 4.5 | 6.6 | 8.6 | mA | $I_F$ = 11 mA, No load | 8 | |
| Output Low Supply Current | $I_{CC2L}$ | 3.5 | 5.6 | 7.5 | mA | $I_F$ = 0 mA, No load | 8 | |
| Output High $V_E$ Supply Current | $I_{EH}$ | –0.4 | –0.7 | –1.2 | mA | $I_F$ = 11 mA, No load | 9 | |
| Output Low $V_E$ Supply Current | $I_{EL}$ | –0.4 | –0.7 | –1.2 | mA | $I_F$ = 0 mA, No load | 9 | |
| **$V_{CC1}$ Under Voltage Protection** | | | | | | | | |
| $V_{CC1}$ Under Voltage Turn On Threshold | $V_{UV1\_TH+}$ | 3.9 | 4.2 | 4.4 | V | | | |
| $V_{CC1}$ Under Voltage Turn Off Threshold | $V_{UV1\_TH–}$ | 3.6 | 3.9 | 4.1 | V | | | |
| **Logic Input and Output** | | | | | | | | |
| $V_{CC1}$ MOS Threshold | $V_{CC1\_MOS\_TH}$ | 0.5 | 1.4 | 1.7 | V | I/UVLO = 0.5 mA | | |
| LED Forward Voltage ($V_{AN} – V_{CA}$) | $V_F$ | 1.25 | 1.55 | 1.85 | V | $I_F$ = 11 mA | 10 | |
| LED Reverse Breakdown Voltage ($V_{CA} – V_{AN}$) | $V_{BR}$ | 6 | — | — | V | $I_F$ = –10 µA | | |
| LED Input Capacitance | $C_{IN}$ | — | 35 | — | pF | f = 1 MHz, $V_F$ = 0V | | |
| LED Turn On Current Threshold, Low to High | $I_{TH+}$ | — | 2.4 | 7.5 | mA | | 11 | |
| LED Turn On Current Threshold, High to Low | $I_{TH–}$ | 0.3 | 2.1 | — | mA | | 11 | |
| LED Turn On Current Hysteresis | $I_{TH\_HYS}$ | — | 0.3 | — | mA | | | |
| /UVLO Logic Low Output Voltage | $V_{/UVLO\_L}$ | — | — | 0.4 | V | $I_{/UVLO}$ = 4 mA | | |
| /UVLO Logic High Output Current | $I_{/UVLO\_H}$ | — | 0.02 | 2 | µA | $V_{/UVLO}$ = 5V | | |
| /FAULT Logic Low Output Voltage | $V_{/FAULT\_L}$ | — | — | 0.4 | V | $I_{/FAULT}$ = 4 mA | | |
| /FAULT Logic High Output Current | $I_{/FAULT\_H}$ | — | 0.02 | 2 | µA | $V_{/FAULT}$ = 5V | | |
| /GFAULT Logic Low Output Voltage | $V_{/GFAULT\_L}$ | — | — | 0.4 | V | $I_{/GFAULT}$ = 4 mA | | |

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| /GFAULT Logic High Output Current | $I_{/GFAULT\_H}$ | — | 0.02 | 2 | µA | $V_{/GFAULT}$ = 5V | | |
| **Gate Driver** | | | | | | | | |
| VOUTP High Level Voltage | $V_{OUTP\_H}$ | $V_{CC2}$ – 0.15 | $V_{CC2}$ – 0.05 | $V_{CC2}$ – 0.01 | V | $I_O$ = –100 mA | | |
| VOUTN Low Level Voltage | $V_{OUTN\_L}$ | 0.01 | 0.03 | 0.1 | V | $I_O$ = 100 mA | | |
| VOUTP High Level Peak Sourcing Current | $I_{OUTP(PEAK)}$ | – | –16 | –10 | A | $V_{OUTP}$ = $V_{CC2}$ – 15V | 12 | a |
| VOUTN Low Level Peak Sinking Current | $I_{OUTN(PEAK)}$ | 10 | 17 | — | A | $V_{OUTN}$ = $V_{EE2}$ + 15V | 13 | a |
| VOUTP Output PMOS $R_{DS(ON)}$ | $R_{OUTP}$ | 0.1 | 0.5 | 1.5 | Ω | $I_O$ = –100 mA | | |
| VOUTN Output NMOS $R_{DS(ON)}$ | $R_{OUTN}$ | 0.1 | 0.3 | 1.0 | Ω | $I_O$ = 100 mA | | |
| Low Level SSD Voltage | $V_{SSD}$ | 0.01 | 0.04 | 0.5 | V | $I_{SSD}$ = 40 mA | | |
| Low Level SSD Current | $I_{SSD}$ | 1 | — | — | A | $V_{SSD}$ = 10V | 14 | |
| $V_{IN}$ to High Level VOUTP Propagation Delay Time | $t_{PLH}$ | — | 98 | 140 | ns | $V_{IN}$ = 5V, $R_{LED}$ = 260Ω, Rg_on = 2.2Ω, Rg_off = 2.2Ω Cload = 2.2 nF, f = 10 kHz, Duty cycle = 50% | 15, 20 | b |
| $V_{IN}$ to Low Level VOUTN Propagation Delay Time | $t_{PHL}$ | — | 95 | 140 | ns | | 15, 20 | c |
| Pulse Width Distortion | PWD | –60 | — | 60 | ns | | | d |
| Dead Time Distortion ($t_{PLH}$ – $t_{PHL}$) | DTD | –60 | — | 60 | ns | | | e |
| VOUTP 10% to 90% Rise Time | $t_R$ | — | 23 | — | ns | | 20 | |
| VOUTN 90% to 10% Fall Time | $t_F$ | — | 19 | — | ns | | 20 | |
| Output High Level Common Mode Transient Immunity | $\|CM_H\|$ | 100 | — | — | kV/µs | $T_A$ = 25°C $V_{CM}$ = 1000V | | f |
| Output Low Level Common Mode Transient Immunity | $\|CM_L\|$ | 100 | — | — | kV/µs | $T_A$ = 25°C $V_{CM}$ = 1000V | | g |
| **Active Miller Clamp** | | | | | | | | |
| Clamp Threshold Voltage | $V_{MC\_TH}$ | 1.5 | 2 | 2.5 | V | | | |
| Clamp Low Level Sinking Current | $I_{CLAMP}$ | 1 | 2.5 | — | A | $V_{CLAMP}$ = $V_{EE2}$ + 2.5V | 16 | |
| Clamp Low Level Peak Sinking Current | $I_{CLAMP(PEAK)}$ | 2.5 | 4 | — | A | $V_{CLAMP}$ = $V_{EE2}$ + 10V | 16 | |
| **$V_{CC2}$ UVLO Protection (UVLO Voltage $V_{UVLO}$ Reference to $V_E$)** | | | | | | | | |
| $V_{CC2}$ UVLO Threshold Low to High | $V_{UVLO2\_TH+}$ | 11.25 | 12.9 | 13.75 | V | $V_{OUTP}$ – $V_E$ > 5V | | h, i |
| $V_{CC2}$ UVLO Threshold High to Low | $V_{UVLO2\_TH–}$ | 10.35 | 11.8 | 12.65 | V | $V_{OUTP}$ – $V_E$ < 5V | | h, j |
| $V_{CC2}$ UVLO Hysteresis | $V_{UVLO2\_HYS}$ | 0.9 | 1.1 | 1.3 | V | | | |
| $V_{CC2}$ to /UVLO High Delay | $t_{PLH\_UVLO2}$ | — | 10 | 25 | µs | | | k |
| $V_{CC2}$ to /UVLO Low Delay | $t_{PHL\_UVLO2}$ | — | 8.8 | 20 | µs | | | l |

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| $V_{CC2}$ UVLO to $V_{OUTP}$ High Delay | $t_{UVLO2\_ON}$ | — | 3 | 6 | µs | | | m |
| $V_{CC2}$ UVLO to $V_{OUTN}$ Low Delay | $t_{UVLO2\_OFF}$ | — | 0.8 | 4 | µs | | | n |
| **Gate Status** | | | | | | | | |
| $V_{GATE}$ Status Check Blanking Time | $t_{GFAULT(BLANKING)}$ | 2.2 | 3.3 | 6 | µs | | | o |
| $V_{GATE}$ Status Check to /GFAULT Signal Low Delay | $t_{PHL\_GFAULT}$ | 2.5 | 3.3 | 6 | µs | | | p |
| $V_{GATE}$ Status Check to /GFAULT Signal High Delay | $t_{PLH\_GFAULT}$ | 7 | 10 | 18 | µs | | | q |
| **Desaturation/Short-Circuit Protection (Reference to $V_E$)** | | | | | | | | |
| DESAT Sensing Threshold | $V_{DESAT\_TH} - V_E$ | 7.0 | 7.5 | 8.0 | V | | 17 | r |
| DESAT DC Charging Current | $I_{CHG}$ | 0.95 | 1.0 | 1.05 | mA | $V_{DESAT}$ = 2V | 18 | |
| DESAT Peak Discharging Current | $I_{DSCHG}$ | 19 | 60 | — | mA | $V_{DESAT}$ = 9V | 19 | |
| DESAT Blanking Time | $t_{DESAT(BLANKING)}$ | 0.5 | 0.8 | 1.1 | µs | | | s |
| DESAT Sense to 90% $V_{GATE}$ Delay | $t_{DESAT(90\%)}$ | 0.05 | 0.13 | 0.3 | µs | $R_{SSD}$ = 15Ω Cload = 2.2 nF | | t |
| DESAT Sense to $V_{GATE}$ = ($V_{EE2}$ + 2V) Delay | $t_{DESAT(2V)}$ | 0.1 | 0.17 | 0.5 | µs | | | u |
| DESAT Sense to /FAULT Low Signal Delay | $t_{DESAT(/FAULT)}$ | 0.6 | 1.6 | 3.2 | µs | | | v |
| Output Mute Time due to DESAT Sense | $t_{DESAT(MUTE)}$ | 0.13 | 0.2 | 0.4 | ms | | | w |
| Time Input Kept Low Before / FAULT Reset to High | $t_{DESAT(RESET)}$ | 0.13 | 0.2 | 0.4 | ms | | | x |

a. Maximum pulse width = 10µs, maximum duty cycle = 1%. All operating conditions should not exceed absolute maximum ratings. Junction temperature rating, $T_J$ should not exceed 150°C.

b. $t_{PLH}$ is defined as propagation delay from 50% of input voltage, $V_{IN}$ to 50% of $V_{OUTP}$ high level output.

c. $t_{PHL}$ is defined as propagation delay from 50% of input voltage, $V_{IN}$ to 50% of $V_{OUTN}$ Low level output.

d. Pulse Width Distortion (PWD) is defined as ($t_{PHL} - t_{PLH}$) of any given unit.

e. Dead Time Distortion (DTD) is defined as ($t_{PLH} - t_{PHL}$) between any two parts under the same test conditions.

f. Common-mode transient immunity (CMTI) in the high state is the maximum tolerable $dV_{CM}/d_t$ of the common-mode pulse, $V_{CM}$, to ensure that the output will remain in the high state (that is, $V_{CC2} - V_{OUTP} < 1.0V$ or $V_{/FAULT} > 2V$). A 330-pF and a 10-kΩ pull-up resistor are connected to input logic feedback pins.

g. Common-mode transient immunity (CMTI) in the low state is the maximum tolerable $dV_{CM}/d_t$ of the common-mode pulse, $V_{CM}$, to ensure that the output will remain in a low state (that is, $V_{OUTN} - V_{EE2} < 1.0V$ or $V_{/FAULT} < 2V$). A 330-pF and a 10-kΩ pull-up resistor are connected to input logic feedback pins.

h. When $V_O$ of the QCFJ-3439T is allowed to go high ($V_{CC2} - V_E > V_{UVLO2\_TH+}$), the DESAT detection feature of the QCFJ-3439T will be the primary source of IGBT protection. $V_{CC2}$ must be greater than $V_{UVLO2\_TH+}$ threshold to ensure DESAT is functional. The DESAT detection feature will remain functional until $V_{CC2}$ is below $V_{UVLO2\_TH-}$ threshold. Thus, the DESAT detection and UVLO features of the QCFJ-3439T work in conjunction to ensure constant IGBT protection.

i. This is the “increasing” (that is, turn-on or “positive going” direction) of $V_{CC2} - V_E$.

j. This is the “decreasing” (that is, turn-off or “negative going” direction) of $V_{CC2} - V_E$.

k. The delay time when $V_{CC2}$ exceeded $V_{UVLO2\_TH+}$ threshold to 50% of /UVLO positive going edge.

l. The delay time when $V_{CC2}$ exceeded $V_{UVLO2\_TH-}$ threshold to 50% of /UVLO negative going edge.

m. The delay time when $V_{CC2}$ exceeded $V_{UVLO2\_TH+}$ threshold to 50% of $V_{OUTP}$ positive going edge (that is, $V_{OUTP}$ turn-on).

n. The delay time when $V_{CC2}$ exceeded $V_{UVLO2\_TH-}$ threshold to 50% of $V_{OUTN}$ negative going edge (that is, $V_{OUTN}$ turn-off).

o. The internal delay time for QCFJ-3439T to start sensing voltage at the $V_{OUTP}$/CLAMP or $V_{OUTN}$ pin when the driver output changes states (that is, $V_{OUTP}$ turn-on or $V_{OUTN}$ turn-off).

p. The delay time from when gate sense detects voltage at $V_{OUTP}$/CLAMP or $V_{OUTN}$ pin does not correspond to LED input logic to 50% of /GFAULT negative-going edge.

q. The delay time from when gate sense detects voltage at $V_{OUTP}$/CLAMP or $V_{OUTN}$ pin correspond to LED input logic or LED input state change reset to 50% of /GFAULT positive-going edge.

r. See the description of operation During a Desaturation (or Short Circuit) Condition section of this data sheet for further details.

s. When the $V_{OUTP}$ is turned on, there is an internal delay time for QCFJ-3439T to start sensing voltage at the DESAT pin. This delay time is called the $t_{DESAT(BLANKING)}$.

t. The amount of time from when DESAT threshold is exceeded to 90% of $V_{GATE}$ negative going edge as mentioned test conditions.

u. The amount of time from when DESAT threshold is exceeded to 10% of $V_{GATE}$ negative going edge as mentioned test conditions.

v. The amount of time from when DESAT threshold is exceeded to 50% of /FAULT negative going edge.

w. The amount of time when DESAT threshold is exceeded, driver output ($V_{OUTP}$) is mute to LED input.

x. The amount of time when DESAT Mute time ($t_{DESAT(MUTE)}$) is expired, LED input must be kept Low for /FAULT status to return to High.

# Package Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Input-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 | — | — | $V_{RMS}$ | RH < 50%, t = 1 minute, $T_A$ = 25°C | a, b, c |
| Resistance (Input – Output) | $R_{I-O}$ | — | $10^{14}$ | — | Ω | $V_{I-O}$ = 500Vdc | c |
| Capacitance (Input – Output) | $C_{I-O}$ | — | 1.3 | — | pF | f = 1 MHz | |

a. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 VRMS for 1 second.

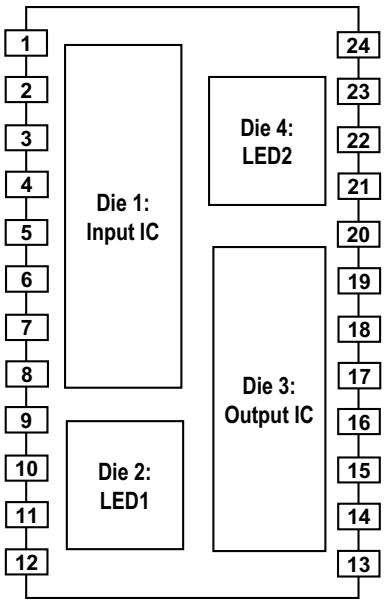
b. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table.

c. The device is considered as a two-terminal device: pins 1 to 12 are shorted together and pins 13 to 24 are shorted together.

# Thermal Resistance Model for QCFJ-3439T

The diagram for measurement is shown in Figure 4. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first, and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated, and all the dice temperatures are recorded and so on until the fourth die is heated. With the known ambient temperature, the die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for this case of four heat sources.

**Figure 4: Diagram of QCFJ-3439T for Thermal Resistance Model**




$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \cdot \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

### Definitions

$R_{11}$: Thermal Resistance of Die1 due to heating of Die1 (°C/W)
$R_{12}$: Thermal Resistance of Die1 due to heating of Die2 (°C/W)
$R_{13}$: Thermal Resistance of Die1 due to heating of Die3 (°C/W)
$R_{14}$: Thermal Resistance of Die1 due to heating of Die4 (°C/W)

$R_{21}$: Thermal Resistance of Die2 due to heating of Die1 (°C/W)
$R_{22}$: Thermal Resistance of Die2 due to heating of Die2 (°C/W)
$R_{23}$: Thermal Resistance of Die2 due to heating of Die3 (°C/W)
$R_{24}$: Thermal Resistance of Die2 due to heating of Die4 (°C/W)

$R_{31}$: Thermal Resistance of Die3 due to heating of Die1 (°C/W)
$R_{32}$: Thermal Resistance of Die3 due to heating of Die2 (°C/W)
$R_{33}$: Thermal Resistance of Die3 due to heating of Die3 (°C/W)
$R_{34}$: Thermal Resistance of Die3 due to heating of Die4 (°C/W)

$R_{41}$: Thermal Resistance of Die4 due to heating of Die1 (°C/W)
$R_{42}$: Thermal Resistance of Die4 due to heating of Die2 (°C/W)
$R_{43}$: Thermal Resistance of Die4 due to heating of Die3 (°C/W)
$R_{44}$: Thermal Resistance of Die4 due to heating of Die4 (°C/W)

$P_1$: Power dissipation of Die1 (W)
$P_2$: Power dissipation of Die2 (W)
$P_3$: Power dissipation of Die3 (W)
$P_4$: Power dissipation of Die4 (W)

$T_1$: Junction temperature of Die1 due to heat from all dice (°C)
$T_2$: Junction temperature of Die2 due to heat from all dice (°C)
$T_3$: Junction temperature of Die3 due to heat from all dice (°C)
$T_4$: Junction temperature of Die4 due to heat from all dice (°C)

$T_a$: Ambient temperature (°C)

$\Delta T_1$: Temperature difference between Die1 junction and ambient (°C)
$\Delta T_2$: Temperature deference between Die2 junction and ambient (°C)
$\Delta T_3$: Temperature difference between Die3 junction and ambient (°C)
$\Delta T_4$: Temperature deference between Die4 junction and ambient (°C)

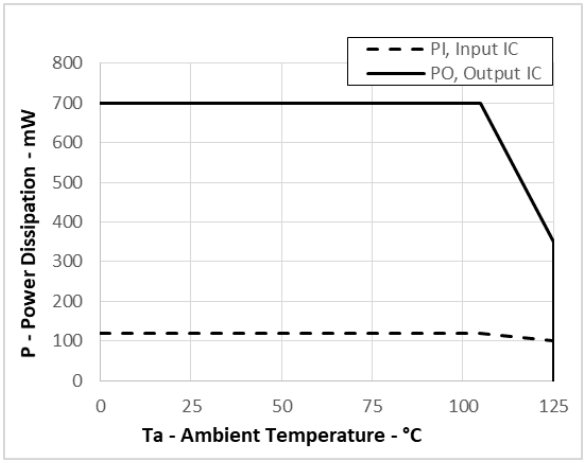
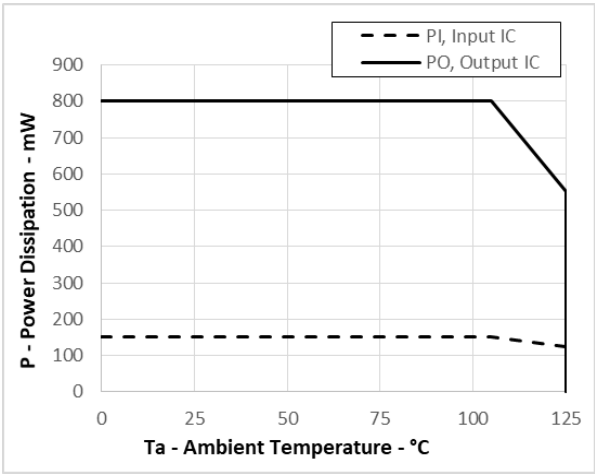
$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a \quad \text{---------- (1)}$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a \quad \text{---------- (2)}$$

$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a \quad \text{---------- (3)}$$

$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P3 + R_{44} \times P_4) + T_a \quad \text{---------- (4)}$$

Measurement is done on both low effective thermal conductivity test board (according to JESD51-3) and on high effective thermal conductivity test board (according to JESD51-7).

| Test Board Type | Test Board Conditions | Thermal Resistance | Power Dissipation Derating Chart |
|---|---|---|---|
| Low effective thermal conductivity board | ■ Single layer board for signal.<br>■ Outer layer copper thickness: 2 oz.<br>■ Board size: 76.2 mm × 76.2 mm | $R_{11}$: 68.1°C/W<br>$R_{12}$: 37.6°C/W<br>$R_{13}$: 23.3°C/W<br>$R_{14}$: 46.8°C/W<br>$R_{21}$: 26.8°C/W<br>$R_{22}$: 250.1°C/W<br>$R_{23}$: 31.1°C/W<br>$R_{24}$: 43.0°C/W<br>$R_{31}$: 27.3°C/W<br>$R_{32}$: 53.2°C/W<br>$R_{33}$: 59.0°C/W<br>$R_{34}$: 65.3°C/W<br>$R_{41}$: 31.3°C/W<br>$R_{42}$: 41.1°C/W<br>$R_{43}$: 39.1°C/W<br>$R_{44}$: 227.7°C/W | **Figure 5: Power Dissipation Derating Chart using Low Effective Thermal Conductivity Board**<br>  <br>**NOTE:**<br>■ Input IC power dissipation is derated linearly above 105°C from 120 mW to 100 mW at 125°C.<br>■ Output IC power dissipation is derated linearly above 105°C from 700 mW to 350 mW at 125°C. |
| High effective thermal conductivity board | ■ Four-layer board that embodies two signal layers, a power plane, and a ground plane.<br>■ Outer layer copper thickness: 2 oz.<br>■ Inner layers copper thickness: 1 oz.<br>■ Board size: 76.2 mm × 76.2 mm | $R_{11}$: 42.6°C/W<br>$R_{12}$: 17.8°C/W<br>$R_{13}$: 10.9°C/W<br>$R_{14}$: 23.8°C/W<br>$R_{21}$: 11.8°C/W<br>$R_{22}$: 213.6°C/W<br>$R_{23}$: 16.7°C/W<br>$R_{24}$: 21.0°C/W<br>$R_{31}$: 11.7°C/W<br>$R_{32}$: 26.8°C/W<br>$R_{33}$: 37.6°C/W<br>$R_{34}$: 35.2°C/W<br>$R_{41}$: 15.2°C/W<br>$R_{42}$: 22.4°C/W<br>$R_{43}$: 23.0°C/W<br>$R_{44}$: 195.0°C/W | **Figure 6: Power Dissipation Derating Chart using High Effective Thermal Conductivity Board**<br>  <br>**NOTE:**<br>■ Input IC power dissipation is derating linearly above 105°C from 150 mW to 125 mW at 125°C.<br>■ Output IC power dissipation is derated linearly above 105°C from 800 mW to 550 mW at 125°C. |

The application and environmental design for the QCFJ-3439T must ensure that the junction temperature of the internal ICs and LED within the gate driver optocoupler do not exceed 150°C. The following examples are based on a typical circuit shown in Figure 23 for estimation of maximum power dissipation and corresponding effect on junction temperatures. This thermal calculation can only be used as a reference for thermal comparison between actual application board layout and PCB board according to JESD51-7. The actual power dissipation achievable will depend on the application environment (PCB layout, air flow, part placement, and so on).

**Calculation of Input IC Power Dissipation, P1**

Input IC Power Dissipation, $P_1 = I_{CC1}$ (Max.) × $V_{CC1}$ (Recommended Max.)
= 2.5 mA × 5.5V
= 13.75mW

**Calculation of Input LED Power Dissipation, $P_2$**

LED1 Power Dissipation, P2 = $I_{F(LED)}$ (Recommended Max.) × $V_{F(LED)}$ (125°C) × Duty Cycle
= 16 mA × 1.25V * 50%
= 10 mW

**Calculation of Output IC Power Dissipation, $P_3$**

Output IC Power Dissipation, $P_3 = I_{CC2}$ (Max.) × $V_{CC2}$ (Applications Max.) + $P_{HS}$ + $P_{LS}$ + $P_{MC}$

$P_{HS}$ – High Side PMOS Switching Power Dissipation = $(V_{CC2} \times Qg \times f_{PWM}) \times R_{OUTP} / (R_{OUTP} + R_{GH}) / 2$
= 20V × 4 µC × 10 kHz × (1.5Ω / (1.5Ω + 2.2Ω) / 2)
= 162 mW

$P_{LS}$ – Low Side NMOS Switching Power Dissipation = $(V_{CC2} \times Qg \times f_{PWM}) \times R_{OUTN} / (R_{OUTN} + R_{GL}) / 2$
= 20V × 4 µC × 10 kHz × (1Ω / (1Ω + 2.2Ω) / 2)
= 125 mW

$P_{MC}$ – Miller Clamp NMOS Switching Power Dissipation = $(V_{THCLAMP}(MAX) \times Qg_{\_2.5V} \times f_{PWM}) \times R_{DS\_MC}/(R_{DS\_MC} + R_{MC})/2$
= 2.5V × 0.5 µC × 10 kHz × (2.5Ω / (2.5Ω + 1Ω) / 2)
=4.5 mW

Output IC Power Dissipation, $P_3$ = (7.5 mA × 20V) + 162 mW + 125 mW + 4.5 mW
= 441.5 mW ($P_3 < P_{o(MAX)}$)

**Calculation of LED2 Power Dissipation, $P_4$**

LED2 Power Dissipation, $P_4 = I_{F(LED2)}$ (Design Max.) × $V_{F(LED2)}$ (125°C) × Duty Cycle
= 10 mA × 1.25V × 50%
= 6.25 mW

Input IC Junction Temperature, $T_1 = (42.6°C/W \times P_1 + 17.8°C/W \times P_2 + 10.9°C/W \times P_3 + 23.8°C/W \times P_4) + T_a$

LED1 Junction Temperature = $T_2 = (11.8°C/W \times P_1 + 213.6°C/W \times P_2 + 16.7°C/W \times P_3 + 21°C/W \times P_4) + T_a$

Output IC Junction Temperature = $T_3 = (11.7°C/W \times P_1 + 26.8°C/W \times P_2 + 37.6°C/W \times P_3 + 35.2°C/W \times P_4) + T_a$

LED2 Junction Temperature = $T_4 = (15.2°C/W \times P_1 + 22.4°C/W \times P_2 + 23°C/W \times P_3 + 195°C/W \times P_4) + T_a$

**Junction temperatures of the internal ICs and LEDs must not exceed 150°C.**

# Typical Performance Plots

**Figure 7: $I_{CC1}$ vs. Temperature**

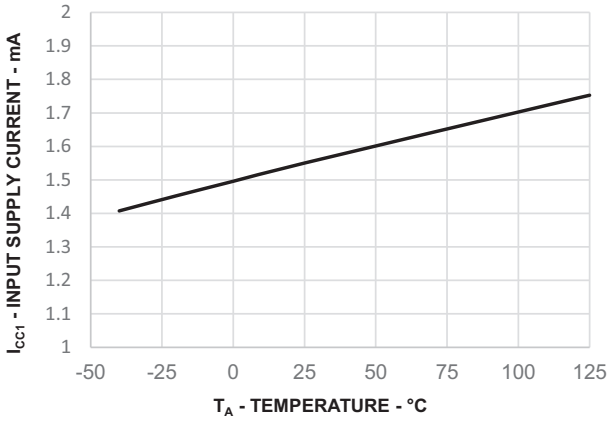



**Figure 8: $I_{CC2}$ vs. Temperature**

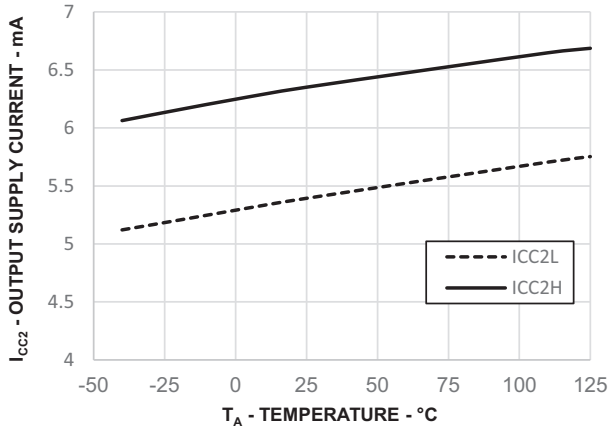



**Figure 9: $I_E$ vs. Temperature**

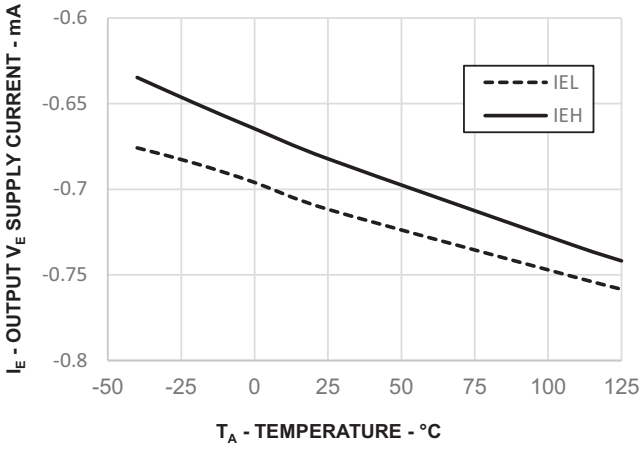



**Figure 10: $I_F$ vs. $V_F$**

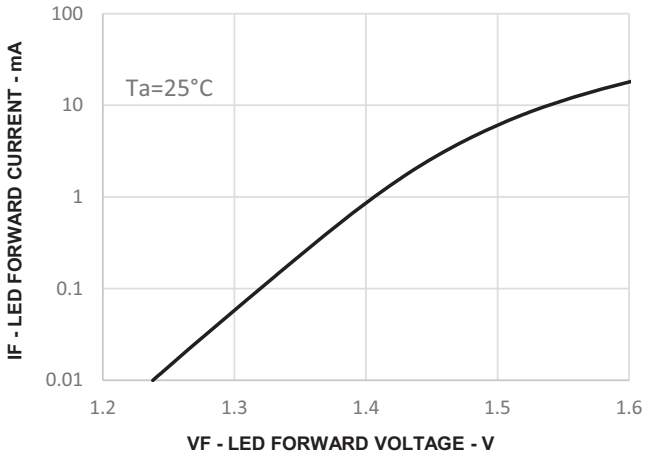



**Figure 11: $I_{TH}$ vs. Temperature**

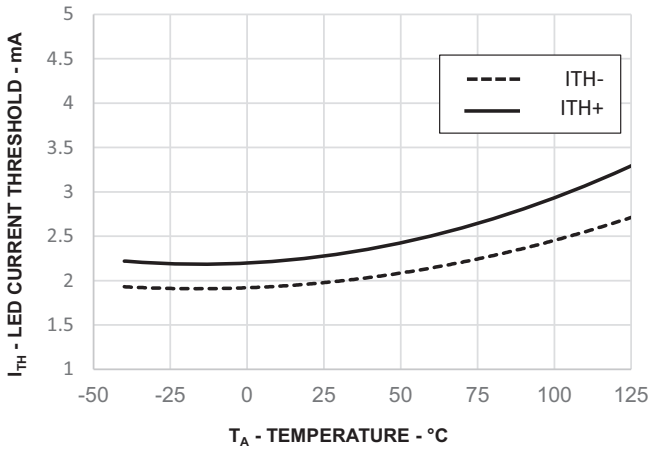



**Figure 12: $I_{OUTP}$ vs. $V_{OUTP}$**

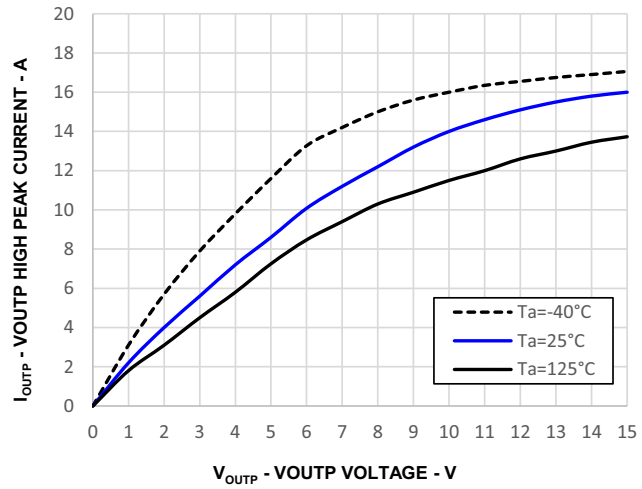


**Figure 13: $I_{OUTN}$ vs. $V_{OUTN}$**

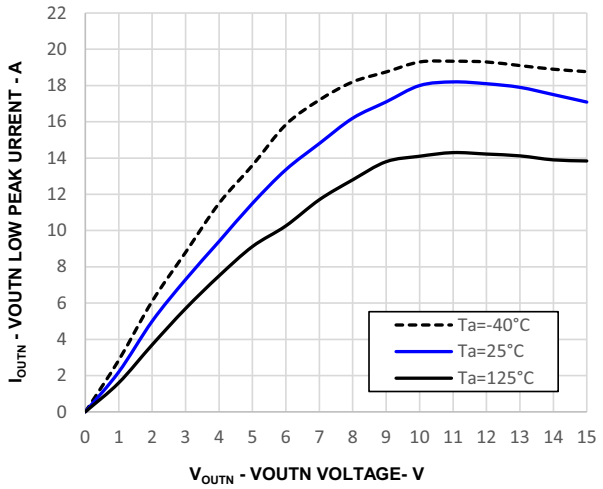



**Figure 14: $I_{SSD}$ vs. $V_{SSD}$**

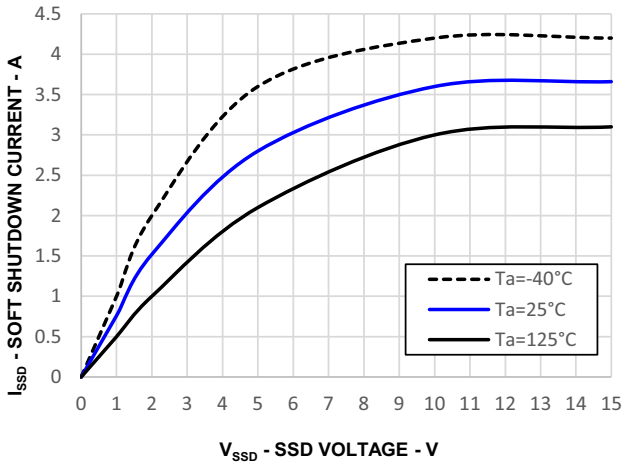



**Figure 15: $T_P$ vs. Temperature**

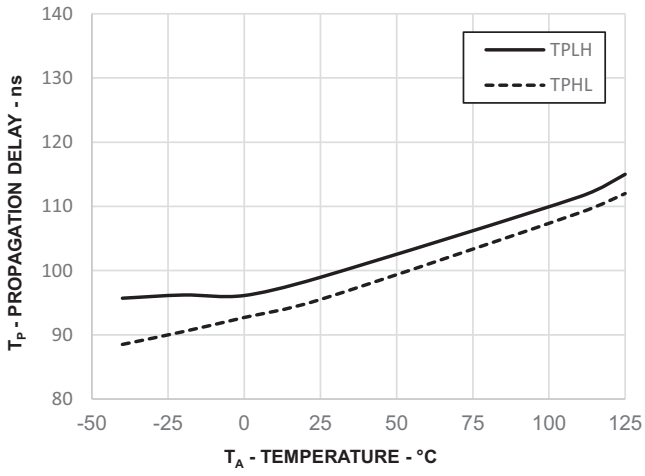



**Figure 16: $I_{CLAMP}$ vs. $V_{CLAMP}$**

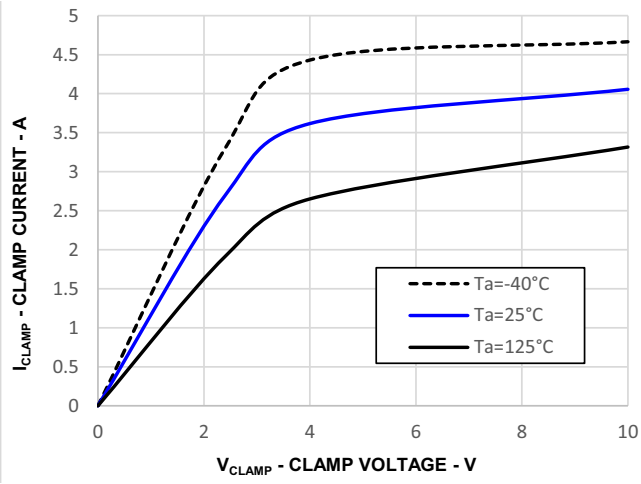



**Figure 17: $V_{DESAT}$ vs. Temperature**

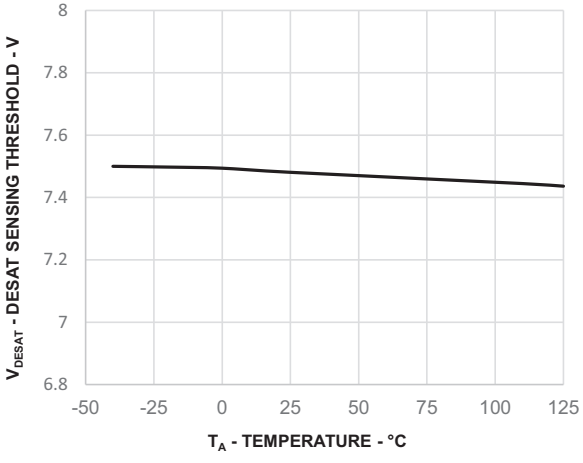



**Figure 18: $I_{CHG}$ vs. Temperature**

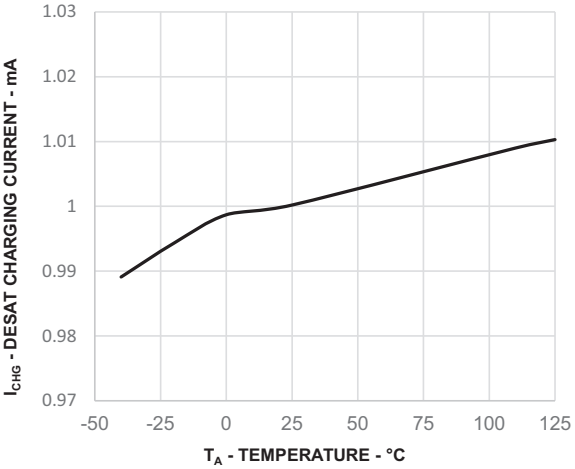


**Figure 19: $I_{DSCHG}$ vs. Temperature**

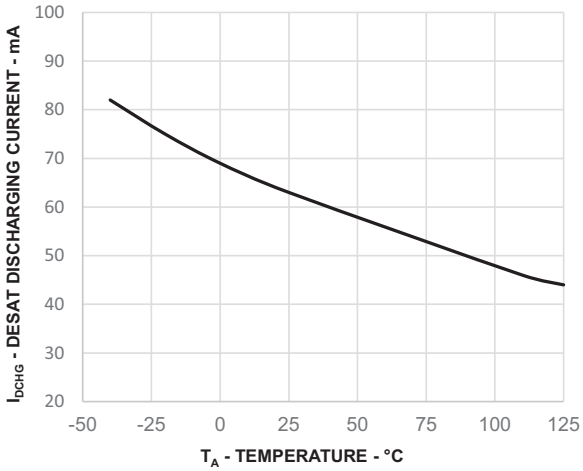



**Figure 20: Propagation Delay Test Circuit**

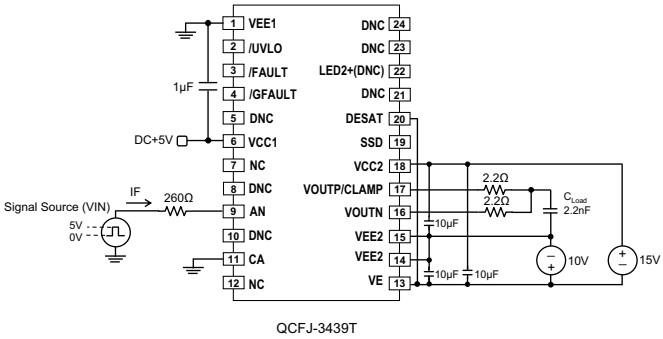



**Figure 21: CMR Output High Test Circuit**

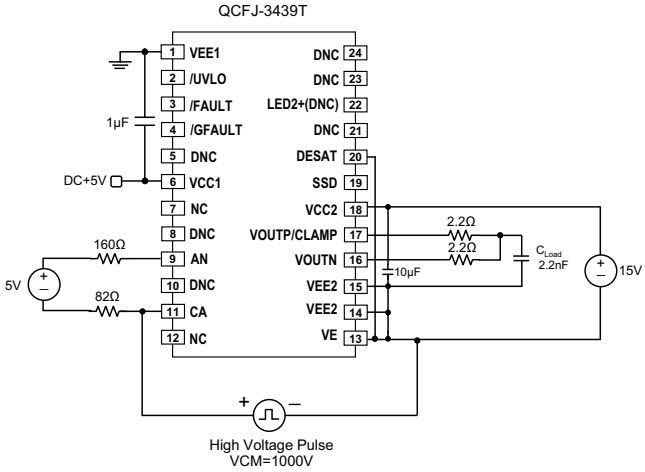



**Figure 22: CMR Output Low Test Circuit**

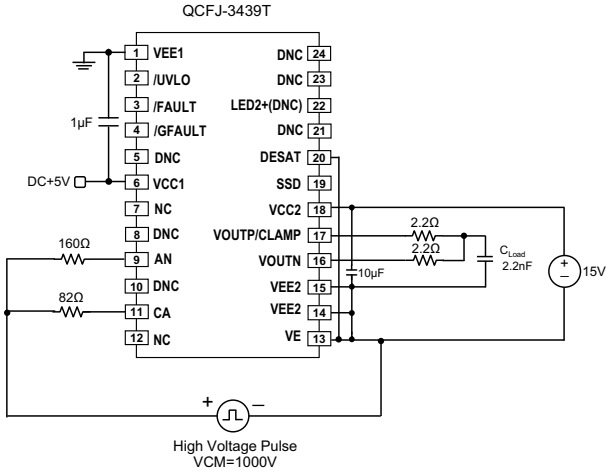
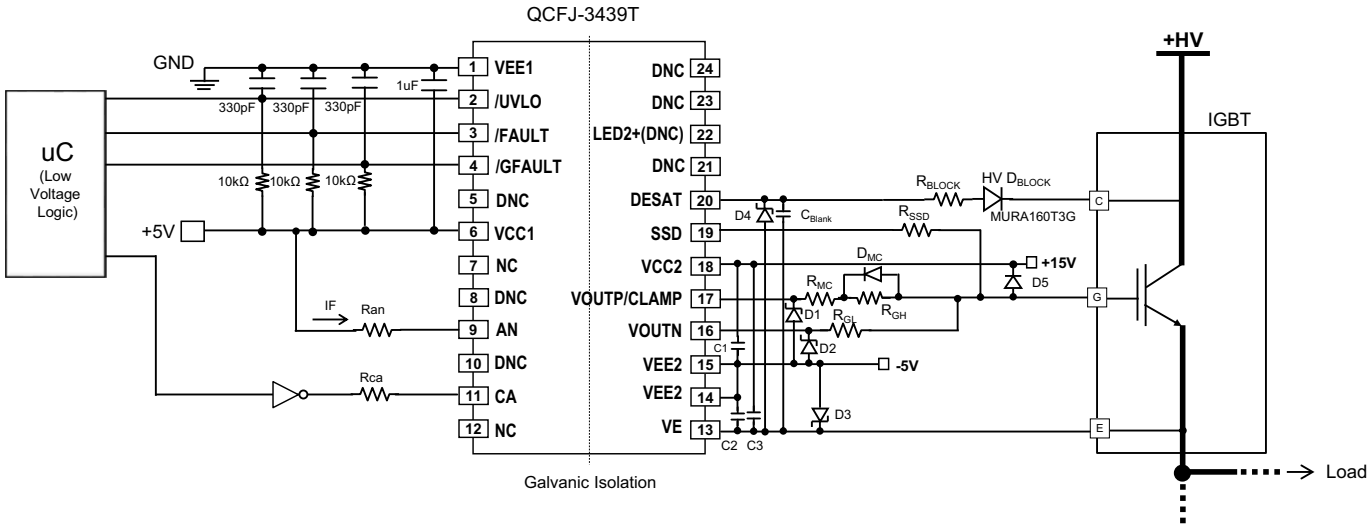


**Figure 23: QCFJ-3439T Typical Gate Driver Circuit with IGBT Desaturation/Short-Circuit Sensing**




**NOTE:** The values of the components are subjected to change with varying application requirements.

The QCFJ-3439T has a LED input control input and three fault reporting mechanisms: namely $V_{CC1}$ under voltage and $V_{CC2}$ under voltage lockout (/UVLO), IGBT/MOSFET desaturation fault (/FAULT) and IGBT/MOSFET gate status (/GFAULT). These open drain /UVLO, /FAULT, and /GFAULT outputs are connected to 10-kΩ pull-up resistors and 330-pF filtering capacitors and are suitable for wired OR applications. /UVLO has the highest fault priority and follows by /FAULT and /GFAULT.

QCFJ-3439T is designed with high peak driving/sinking current capability for direct driving IGBT/MOSFET. Depending on the load gate charge and the requirement of ripple voltage during load switching, minimum capacitance for C1, C2, and C3 can be calculated. These capacitors serve as supplies decoupling capacitors as well as local charge reservoir that provide large transient charge necessary during load switching transition. Use minimum of 1 µF for C1, C2, and C3.

The two resistors ($R_{an}$ and $R_{ca}$) that connected to input LED's anode and cathode are recommended to be in the ratio of 2:1. The right resistor ratio helps to balance the common mode impedances at the LED's anode and cathode. This then helps to equalize the common mode voltage changes at the anode and cathode to give high CMR performance. For example, use 160Ω and 82Ω for $R_{an}$ and $R_{ca}$, respectively, on a 5V LED driving circuit.

The HV blocking diode ($D_{BLOCK}$), resistor ($R_{BLOCK}$), Schottky diode ($D_4$) and blanking capacitor, $C_{Blank}$ are used to protect the DESAT pin and prevent false fault detection. During over current fault condition, the IGBT/MOSFET is soft shut down through the SSD pin and the rate of shutdown can be adjusted by $R_{SSD}$.

The gate resistors ($R_{GH}$ and $R_{GL}$) are used to limit the gate current, control the IGBT/MOSFET rise/fall times and dissipate gate driver output power. Because pin 17 is shared by VOUTP and CLAMP function, a Schottky diode, $D_{MC}$, and $R_{MC}$ are used to provide a separate active Miller clamp sinking path to shunt parasitic IGBT/MOSFET Miller current during the off cycle. Use an $R_{MC}$ value in the range of 0.5Ω to less than 1Ω for optimum Miller clamp function.

Schottky diodes (D1, D2, and D3) are used to prevent VOUTP, VOUTN, and VE from going below VEE2 due to negative transient caused by parasitic inductance. These Schottky diodes can be omitted if the driver high current path is well taken care of by proper layout design.

# Description of Operations and Functions

## Output Controls and Status Flags

The secondary output state (VOUTP/CLAMP, VOUTN, and SSD) is controlled by the combination of $V_{CC2}$, LED current ($I_F$) and desaturation (DESAT) conditions. The status flags (/UVLO, /FAULT, and /GFAULT) at the primary side reflect the state of the circuit operation. Note that VCC1 provides power supply to the device's fault reporting mechanisms. If VCC1 is under voltage, all status flags are pulled to low state. The secondary output drivers and protection functions (VOUTN, VOUTP, CLAMP, DESAT, and SSD) remains operational even when there is no VCC1 supply. The following table shows the logic truth table for these outputs. The logic level is defined by the respective threshold of each function pin.

**Table 2: Output Controls and Status Flags**

| Condition | Inputs | | | | Secondary Outputs | | | Status Flag | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | VCC1 | VCC2 | IF | DESAT sense | VOUTP/CLAMP | VOUTN | SSD | /UVLO | /FAULT | /GFAULT |
| VCC1 UVLO | Low | High | Low | Not Active | Low(CLAMP) | Low | High-Z | Low | Low | Low |
| | Low | High | High | Active (DESAT is not triggered) | High(VOUTP) | High-Z | High-Z | Low | Low | Low |
| VCC2 UVLO | High | Low | X[a] | Not active | Low(CLAMP) | Low | High-Z | Low | High | High |
| Desaturation Fault | High | High | Low | Not active | Low(CLAMP) | Low | High-Z | High | High | High |
| | High | High | High | Active (DESAT is triggered) | Low(CLAMP) | High-Z | Low | High | Low | High |
| Gate Fault | High | High | Low | Not active | High-Z(VOUTP)[b] | High[b] | High-Z | High | High | Low |
| | High | High | High | Active (DESAT is not triggered) | Low(VOUTP)[c] | High-Z[c] | High-Z | High | High | Low |
| Normal Switching | High | High | Low | Not Active | Low(CLAMP) | Low | High-Z | High | High | High |
| | High | High | High | Active DESAT is not triggered) | High(VOUTP) | High-Z | High-Z | High | High | High |

a. "X" means don't care.

b. When LED input goes low, the status of gate is checked via VOUTP/CLAMP pin after the internal delay time, $t_{GFAULT(BLANKING)}$. If VOUTP/CLAMP voltage level is higher than $V_{EE2}$ + 2V after the $t_{GFAULT(BLANKING)}$ time, /GFAULT is pulled to low.

c. When LED input goes high, the status of gate is checked via VOUTN pin after the internal delay time, $t_{GFAULT(BLANKING)}$. If VOUTN voltage level is lower than $V_{CC2}$ – 2V after the $t_{GFAULT(BLANKING)}$ time, /GFAULT is pulled to low.

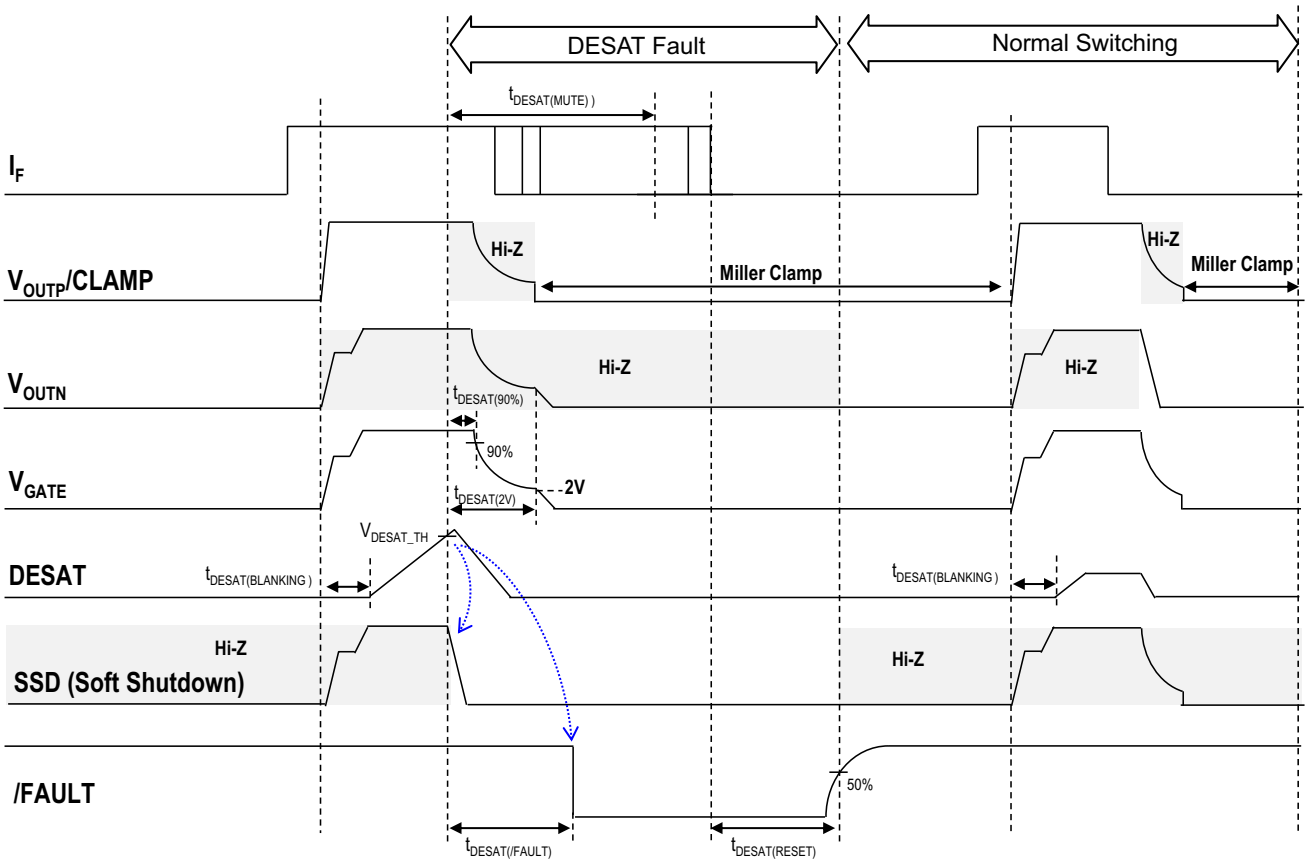
## Description of DESAT Sense and Protection

The QCFJ-3439T DESAT pin monitors the drain-source voltage of the MOSFET or the collector-emitter voltage of the IGBT. When the MOSFET/IGBT goes into desaturation and these voltages exceed the predetermined threshold, $V_{DESAT\_TH}$, QCFJ-3439T triggers a local fault shutdown sequence through the SSD pin and slowly reduces the high over current to prevent damaging voltage spikes appear across MOSFET's drain-source or IGBT's collector-emitter. The desaturation fault is reported to microcontroller through the isolated feedback channel (/FAULT pin) of the QCFJ-3439T. During the off state (no LED input) of the IGBT, the fault detect circuitry is disabled to prevent false "fault' signals.

## During a Desaturation (or Short Circuit) Condition

1. DESAT terminal monitors IGBT's $V_{CE}$ or MOSFET's $V_{DS}$ voltage.
2. When the voltage on the DESAT terminal exceeds 7.5V, the output drivers ($V_{OUTP}$ and $V_{OUTN}$) go to Hi-Z state and the SSD goes to low state. SSD pulls down the VGATE at a slow rate adjustable through resistor $R_{SSD}$.
3. Output driver VOUTP and VOUTN ignores all PWM commands during mute time ($t_{DESAT(MUTE)}$).
4. /FAULT output goes low, notifying the microcontroller of the desaturation fault condition.
5. Microcontroller takes appropriate action.
6. When $t_{DESAT(MUTE)}$ expires, LED input must be kept at low for a period of $t_{DESAT(RESET)}$ time before fault condition can be cleared. /FAULT status will return to high and SSD output will return to Hi-Z state.
7. In the event of LED input goes high during $t_{DESAT(RESET)}$ time, the $t_{DESAT(RESET)}$ timing will be reset and the LED input will need to be kept low for another $t_{DESAT(RESET)}$ time before fault condition can be cleared.
8. Output drivers (VOUTP and VOUTN) start to respond to LED input after fault condition is cleared.

**Figure 24: Circuit Behaviors during Desaturation (or Short Circuit) Event**



## Desaturation Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the total DESAT blanking time, is controlled by both the internal DESAT blanking time $t_{DESAT(BLANKING)}$ and external blanking time. The external blanking time is determined by internal charge current ($I_{CHG}$), the DESAT voltage threshold ($V_{DESAT\_TH}$), and the external blanking capacitor ($C_{BLANK}$).

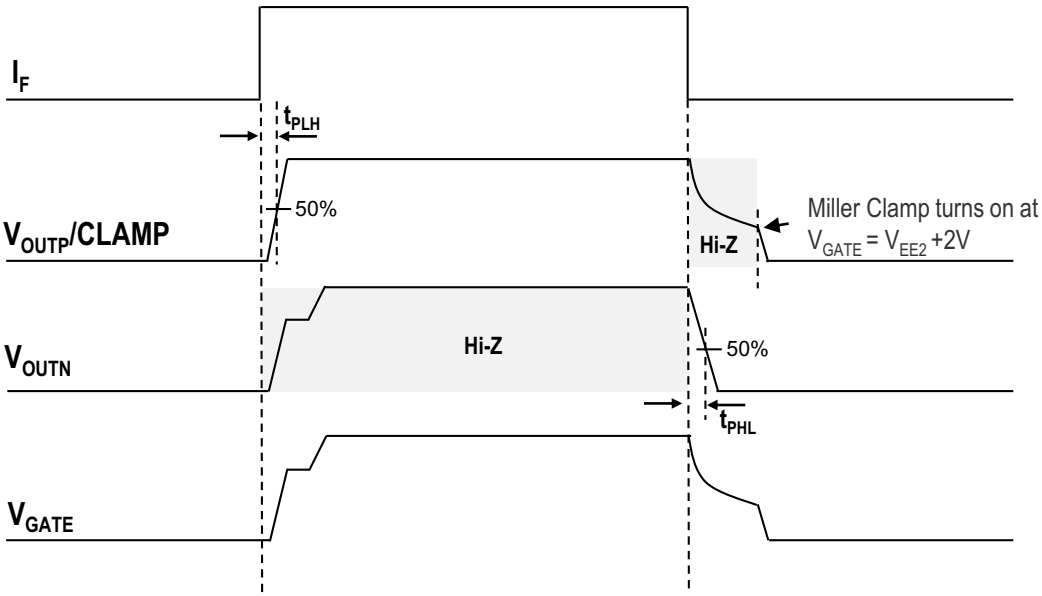
The total blanking time is calculated as follow:

$$t_{BLANK} = t_{DESAT(BLANKING)} + [C_{BLANK} \times V_{DESAT\_TH} / I_{CHG}]$$

## Description of Gate Driver and Miller Clamping

The gate driver is directly controlled by the LED current. When LED current is driven high the output of the QCFJ-3439T is capable of delivering minimum 10A peak sourcing current to drive the IGBT's/MOSFET's gate. While LED is switched off the gate driver is able to sink a minimum of 10A peak current to switch the gate off fast. Additional Miller clamping pull-down transistor is activated when output voltage reaches about 2V with respect to VEE2 to provide low impedance path to miller current as shown in the following figure.

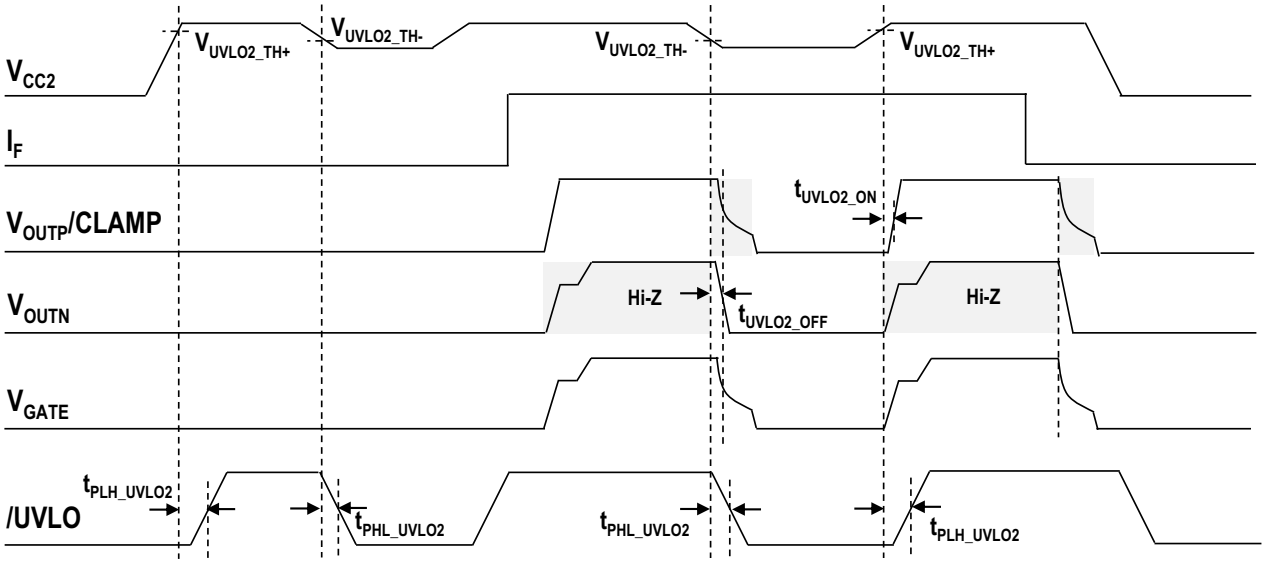
**Figure 25: Gate Drive Switching Behavior under Normal Conditions**



# Description of Under Voltage Lock Out

Insufficient gate voltage to IGBT/MOSFET can increase turn-on resistance of IGBT/MOSFET, resulting a large power loss and IGBT/MOSFET damage due to high heat dissipation. The QCFJ-3439T monitors the output power supply, VCC2 constantly. When output power supply is lower than under voltage lockout (UVLO) threshold gate driver output will shut off to protect IGBT/MOSFET from low voltage bias. During power up, the UVLO feature locks the gate driver output low to prevent unwanted turn on at lower supply voltage.

**Figure 26: Circuit Behaviors at Power-Up, Power-Down, and UVLO**



# Description of Gate Status Monitoring

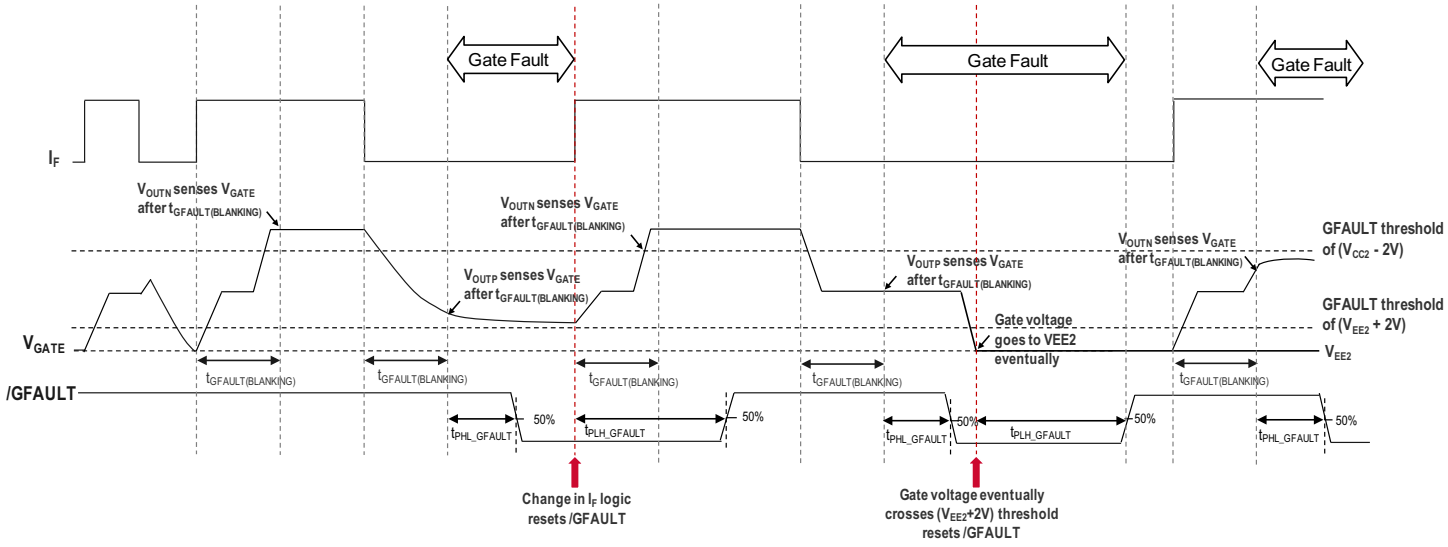
The status of IGBT/MOSFET gate voltage is monitored by output pins $V_{OUTP}$/CLAMP and $V_{OUTN}$. The /GFAULT output goes low when the gate voltage does not correspond to the LED input logic. The status of the gate is checked after a GFAULT sense blanking time ($t_{GFAULT(BLANKING)}$) to allow sufficient time for the gate to charge or discharge to its final level. $T_{GFAULT(BLANKING)}$ is internally fixed by the IC. There is no gate status check during the blanking time. If the switching of gate voltage is slow with large external gate resistances and the gate rise or fall time exceeds the GFAULT sense blanking time ($t_{GFAULT(BLANKING)}$), a delay in reading the GFAULT status flag must be added in the MCU by users to prevent false GFAULT reporting.

When the LED input logic goes high, gate voltage is sensed through the $V_{OUTN}$ pin after the GFAULT sense blanking time ($t_{GFAULT(BLANKING)}$) expires. /GFAULT output goes low if gate voltage is lower than $V_{CC2}$ – 2V. On the other hand, when the LED input logic is low, gate voltage is sensed through the $V_{OUTP}$/CLAMP pin after the GFAULT sense blanking time ($t_{GFAULT(BLANKING)}$) expires. /GFAULT output goes low if gate voltage is higher than $V_{EE2}$ + 2V. Note that $V_{OUTP}$ and CLAMP functions share the same pin. The gate voltage is continuously monitored by the $V_{OUTP}$ whether it is in Hi-Z or CLAMP state when the LED input logic is low.

/GFAULT flag status will be cleared under two conditions stated as follow:

1. The LED input logic state changes, such as from low to high or from high to low.
2. The gate voltage follows LED input logic eventually, whereby gate voltage manages to cross the threshold of $V_{CC2}$ – 2V or $V_{EE2}$ + 2V.

**Figure 27: Circuit Behaviors during Gate Status Monitoring**



# Printed Circuit Board Layout Recommendations

Take care when designing the layout of printed circuit board (PCB) for optimum performance.

Maintain adequate spacing between the high-voltage isolated circuitry and any input-referenced circuitry. Maintain the same minimum spacing between two adjacent high-side isolated regions of the printed circuit board as well. Insufficient spacing reduces the effective isolation and increases parasitic coupling that will affect CMR performance.

The QCFJ-3439T is used for direct driving the power module. Due to high peak current source and sink capability and fast switching transient, the placement and routing of supply bypass capacitors, the gate charging and discharging paths require special attention. Use planes for supply and ground, such as VCC2 and VEE2 planes. In addition, connect IC power pins, such as VCC2 (pin 18) and VEE2 (pins 14 and 15) directly to these planes using multiple via holes locally. Nevertheless, put effort into maintaining short, clean charging and discharging paths to minimize oscillation (noise) due to parasitic inductance in the high current loop.

As for input side circuitry, use planes for supply and ground. Connect IC power supply VCC1 (pin 6), input side ground VEE1 (pin 1) and the bypass capacitor locally to these planes through multiple via holes.

For thermal dissipation purposes, it is recommended to place large copper area for top layer VEE2 (pins 14 and 15) and connect the copper area with multiple via holes to VEE2 plane at the bottom layer of PCB as illustrated in the following figure.

**Figure 28: Example of Recommended Layout**