合力为科技
HLW TECHNOLOGY®

HLW3070 Datasheet

REV 1.0

Contents

1 FUNCTION DESCRIPTION

HLW3070 is a high precision sigma delta Analog-to-Digital converter chip with low power consumption , single differential input channel . Hlw30370 has temperature sensor and oscillator inside.

The PGA of HLW3070 :1,2,64,128(default).

Out data rate of HLW3070:10Hz(default)、40Hz、640Hz、1.28kHz.

MCU can communicate with HLW3070 through two wires ,SCLK and $\overline{DRDY}$ / $DOUT$.

The configuration can be modified, such as channel selection, PGA selection, output rate selection, etc.

1.1 MAIN FUNCTION

- Built in crystal oscillator and integrated temperature sensor
- With power down function
- 2-wire SPI interface, the fastest rate is 1.1MHz
- VDD: 2.6V~5.5V

1.2 ADC CHARACTER

- The PGA can choose 1、2、64 or 128.
- 24 bits no missing code
- The ENOB is 20bit When PGA is set to 128 and VDD = 5V , the ENOB is 19.5bit When PGA is set to 128 and VDD = 3.3V
- P-P noise: PGA=128、10Hz：180nV；INL<0.0015%
- Out data rate of HLW3070:10Hz、40Hz、640Hz、1.28kHz.
- short of Input channel

1.3 APPLICATIONS

- Industrial process control

- Weight scales
- Liquid/gas chemical analysis
- Blood analysis
- Smart transmitters
- Portable instrumentation

1.4 BASIC STRUCTURE FUNCTION DESCRIPTION

HLW3070 is a high precision sigma delta Analog-to-Digital converter chip with low power consumption, single differential input channel. There is a differential input channel and a temperature sensor in HLW3070.

The PGA of HLW3070 has 1,2,64,and 128. When PGA = 128, the ENOB can reach 20 bits (working at 5V).

HLW3070 has an RC oscillator inside and does not need an external crystal oscillator.

Hlw3070 can be configured in various functional modes, such as temperature detection, PGA selection, ADC data output rate selection, etc.

HLW3070 has power down mode.

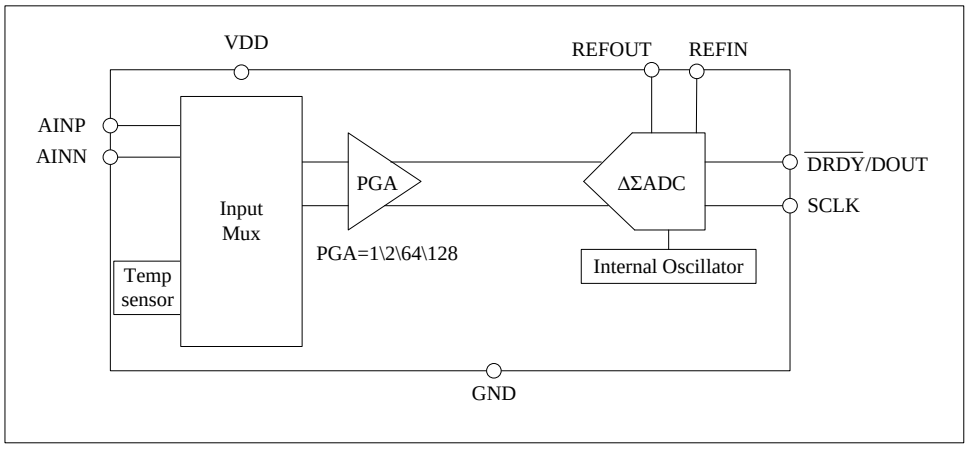


figure 1 Principle Block Diagram

1.5 PINS

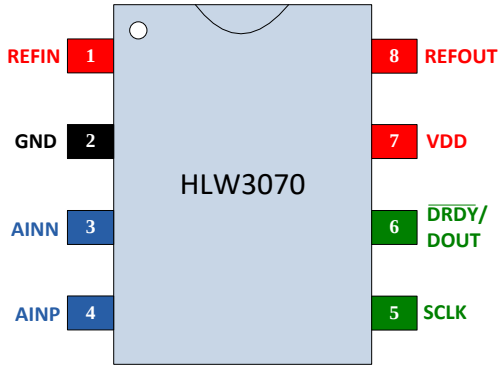


figure 2 Pin Diagram

Table1 Pin Description

PIN NUMBER	SYMBOL	INPUT/OUTPUT	DESCRIPTION
1	REFIN	AI	Input of Reference voltage
2	GND	P	Analog ground
3	AINN	AI	Negative input
4	AINP	AI	Positive input
5	SCLK	DI	Serial clock input.
6	$\overline{DRDY}$ / *DOUT*	DI/DO	Serial data input/output
7	VDD	P	Power
8	REFOUT	AO	Output of Reference voltage

2 CHARACTER DESCRIPTION

2.1 ABSOLUTE MAXIMUM LIMIT VALUES

PARAMETER	SYMBOL	MIN	MAX	UNIT
Power voltage	VDD	-0.3	6	V
Current Of Power Momentary			100	mA
Current Of Power Continuous			10	mA
Digital Input Voltage		-0.3	DVDD+0.3	V
Digital Output Voltage		-0.3	DVDD+0.3	V
Junction Temperature			150	℃
Operating Temperature		-40	85	℃
Storage Temperature		-60	150	℃
Pin Soldering Temperature			240	℃

2.2 DIGITAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
VIH	0.7×DVDD		DVDD+0.1	V	
VIL	DGND		0.3×DVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2×DVDD	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	-10			μA	VI=DGND
Frequency of sclk clock			1.1	MHz	

2.3 ELECTRICAL CHARACTERISTICS

All parameters are tested under the conditions of ambient temperature - 40 ~ 85 ℃ and internal reference voltage

- **ANALOG CHARACTERISTICS**

PARAMETER	CONDITION	MIN	TYPE	MAX	UNIT
Analog input					
Full-scale input range (AINP-AINN)			±0.5VREF/PGA		V
Analog input range	PGA=1，2	AGND-0.1		AVDD+0.1	V
	PGA=64，128	AGND+0.75		AVDD-0.75	V

Differential input impedance	PGA=1、2		190		MΩ
	PGA=64、128		28		MΩ
System performance					
Resolution	No missing codes		24		Bits
Output data rate			10	1280	Hz
P-P noise	PGA=128、10Hz		180		nv
Effective Resolution	PGA=128、10Hz		20（5V） 19.5（3.3V）		Bit
Integral nonlinearity	PGA=128		±15		ppm
Offset error	PGA=128		±1.4		μV
Offset error drift	PGA=128		20		nv/℃
Gain error	PGA=128		±0.5		%
Gain error drift	PGA=128		8		ppm/℃
Voltage reference input					
Internal reference source	REFIN	2.0	VDD	VDD+0.1	V
Voltage reference output					
external reference source	REFOUT		VDD		V
CLOCK					
fosc			5.2		MHz
Clock temperature drift			250		ppm/℃
Temperature sensor					
Temperature	TempError		±3		℃

- **Power character**

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
Power	VDD			5	5.5	V
Current	Normal mode	PGA=1、2		1.57		mA
		PGA=64、128		2.34		mA
	Power down			0.1	0.1	μA

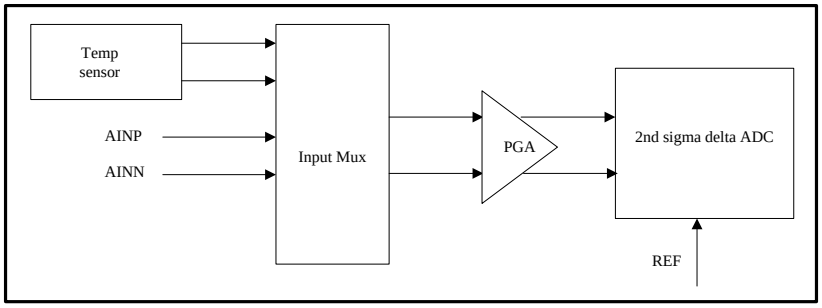
- **（VDD=3.3V）Power character**

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
Power	VDD		2.6	3.3		V
Current	Normal mode	PGA=1、2		1.26		mA
		PGA=64、128		2.11		mA
	Power down			0.1		μA

3 FUNCTION MODULE DESCRIPTION

3.1 ANALOG INPUT

HLW3070 has one ADC integrated with single differential input channel. The signal input can be the differential input signals AINP and AINN, or the output signal of the temperature sensor. The switching of the input signal is controlled by the register (CH_SEL [1:0]), and its basic structure is shown as follows:



The PGA of HLW3070 can be configured with: 1, 2, 64, 128, controlled by register (PGA_SEL [1:0]);

The reference voltage can be external input but also internal output, to use the external reference voltage, to turn off the internal reference, internal reference control by the register (REFO_OFF) control.

3.2 TEMPERATURE SENSOR

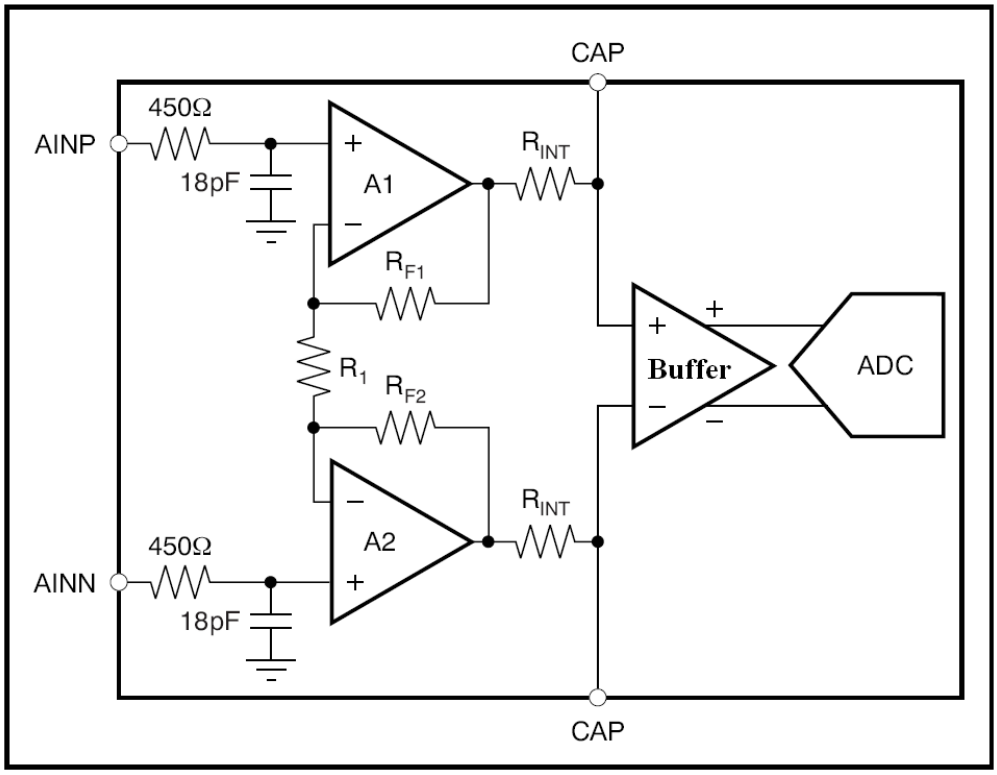
Temperature measurement function is provided inside the chip

- When CH_SEL [1:0]=2 'b10, ADC analog signal input is connected to the internal temperature sensor, and other analog input signals are invalid. The ADC derives the actual temperature value by measuring the voltage difference between the output of the internal temperature sensor.
- When CH_sel [1:0]=2 'b10, ADC only supports PGA=1. Temperature sensors need single point correction.
- Calibration method: At A certain temperature point A, temperature sensor is used to measure and get code value Ya. So the temperature at other temperature points B = Yb*(273.15+A)/ ya-273.15

A Temperature is in degrees Celsius. Ya is the temperature code at point A. Yb is the temperature code at point B.

3.3 Low noise PGA amplifier

HLW3070 provides a low noise, low drift PGA amplifier and bridge sensor differential output connection. its basic structure is shown in the figure below, Front anti-EMI filter circuit R=450Ω, C=18pF to achieve 20M high frequency filtering. Low noise PGA amplifiers achieve 64 times amplification through RF1, R1, RF2, and constitute 64 and 128 PGA amplifiers with the rear switch capacitor PGA. Pga_sel [1:0] is used to configure PGA 1, 2, 64, 128, etc. When using PGA= 1,2, the 64-x low-noise PGA amplifier is turned off to save power. When using low noise PGA amplifiers, the input range is between GND+0.75V and VDD-0.75V, beyond which actual performance degrades. A built-in 45pF capacitor is connected at the CAP port, and a built-in 2K resistor RINT forms a low-pass filter, which is used as the high-frequency filter of the output signal of the low-noise PGA amplifier. At the same time, the low-pass filter can also be used as the anti-aliasing filter of ADC.



HLW3070 has built-in Buffer. When PGA= 1,2, HLW3070 uses Buffer to reduce problems caused by low ADC differential input impedance, such as insufficient establishment time, large gain error, etc. When PGA= 64,128, HLW3070 also uses Buffer to reduce the establishment error, gain error and internal code drift caused by low noise PGA after low pass filtering with RINT=2K and CINT=0.1μF.

3.4 CLOCK SYSTEM

HLW3070 uses internal crystal oscillator to provide the clock frequency required by the system, with a typical value of 5.2MHz.

3.5 POR&POWER DOWN

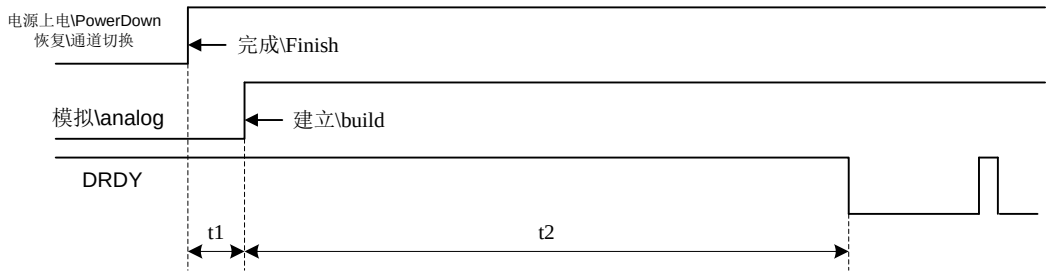
- When the chip is powered on, the built-in power-on reset circuit will generate reset signal to reset the chip automatically
- When SCLK changes from low level to high level and stays at high level over 100μs, HLW3070 enters PowerDwon mode and the power consumption is less than 0.1μA. When SCLK returns to low power level, the chip will return to normal working state.

3.6 SERIAL PERIPHERAL INTERFACE

HLW3070 uses 2-wire SPI serial communication, and data reception and function configuration can be realized through SCLK and $\overline{DRDY}$ / $DOUT$.

（1）The establishment time of ADC sampling signal

When the ADC data output rate is 10Hz or 40Hz, the digital part needs three data conversion cycles to meet the establishment time requirements of analog input signal and filter; When the ADC data output rate is 640Hz or 1280Hz, the digital part needs four data conversion cycles to meet the establishment time requirements of analog input signal and filter. The whole establishment process of HLW3070 is shown in the figure below:



PARAMETER	DESCRIPTION		MIN	TYPE	MAX	UNIT
t1	Power on/PowerDown Recovery / The establishment time after channel switchover			2		ms
t3	PGA switch \ Rate switch after The setup time required for the simulation			0.8		μs
t2	Set up the time ($\overline{DRDY}$ / $DOUT$ Keep the level high)	10\40Hz		300\75		ms
		640\1280Hz		6.25\3.125		ms

（2）ADC data output rate

The HLW3070 data output rate can be configured through the register speed_sel[1:0].

SPEED_SEL[1:0]	**Data output rate** (Hz)
00	10
01	40
10	640
11	1280

（3）DATA FORMAT

The output data of HLW3070 is 24-bit binary complement, and the highest bit (MSB) is output first. The minimum significant bit (LSB) is (0.5vref /Gain)/(2^23-1). Positive FSR output code is 7FFFFFH, negative FSR output code is 800000H. The following table shows the ideal output codes corresponding to different analog input signals. ,

V_{IN} （AINP-AINN）	Output Data
≥+0.5V_{REF}/Gain	7FFFFFH
(+0.5V_{REF}/Gain)/(2^{23}-1)	000001H
0	000000H
(-0.5V_{REF}/Gain)/(2^{23}-1)	FFFFFFH

$\leqslant +0.5V_{REF}/Gain$	800000H

The effects of noise, INL, offset error and gain error are not considered

（4）DATA READY/DATA INPUT AND OUTPUT

The $\overline{DRDY}$ / $DOUT$ pin has four uses. First, when the output is low, it indicates that the new data has been converted.

Second, as the data output pin, when the data is ready, after the rising edge of the first SCLK, $\overline{DRDY}$ / $DOUT$ outputs the highest bit (MSB) of the converted data. On the rising edge of each SCLK, the data automatically shifts by 1 bit. After 24 SCLKS, all 24 bits of data will be read out. If the sending of SCLK is suspended at this time, the last bit of data will be kept until the next data is ready. After that, when it is pulled down again, it means that the new data has been converted and the next data can be read.

Third, at the 25th and 26th SCLK, the output register status update flag;

Fourth, as the pin of register data writing or reading, SPI needs to send 46 SCLK when it needs to configure register or read register value. According to the input command word, it can determine whether register writing or reading operation is performed.

（5）SERIAL CLOCK INPUT

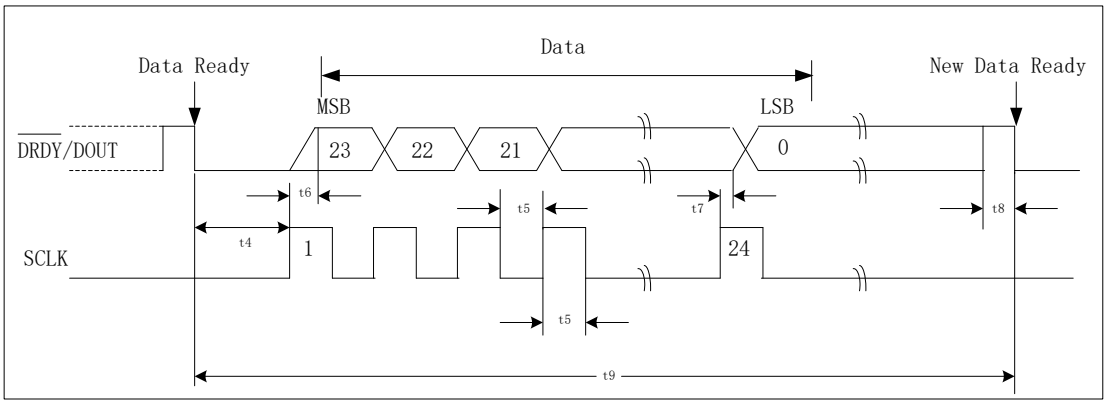
The SCLK is a digital pin for serial clock input.This signal should be a clean signal, Burrs or slow rising edges can lead to incorrect data reading or error states. Therefore, the rise and fall time of SCLK should be less than 50ns.

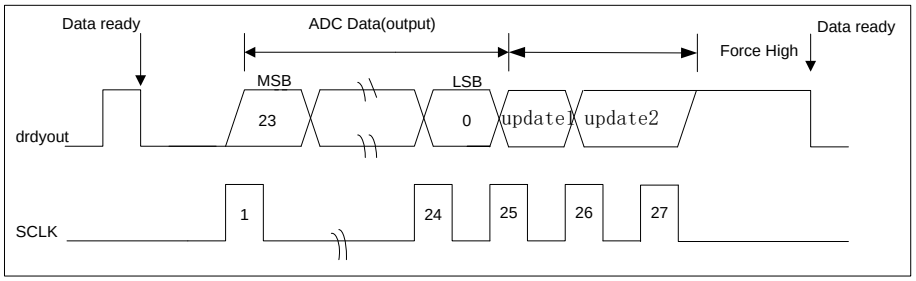
（6）DATA OUTPUT

HLW3070 can continuously convert analog input signals. When $\overline{DRDY}$ / $DOUT$ is pulled down, it indicates that data is ready for reception. The highest bit of output can be read out when the first SCLK is input, and all 24 bits of data can be read out after 24 SCLKS. Until it is pulled to a high level.

Is there a write operation flag in the 25th and 26th SCLK output configuration registers? When the corresponding value of the 25th SCLK is 1, it indicates that the Config register has been written a new value. The corresponding bit of the 26th SCLK is reserved for chip expansion. Indicates that the new

data is ready for the next data conversion. The timing sequence is shown as follows:



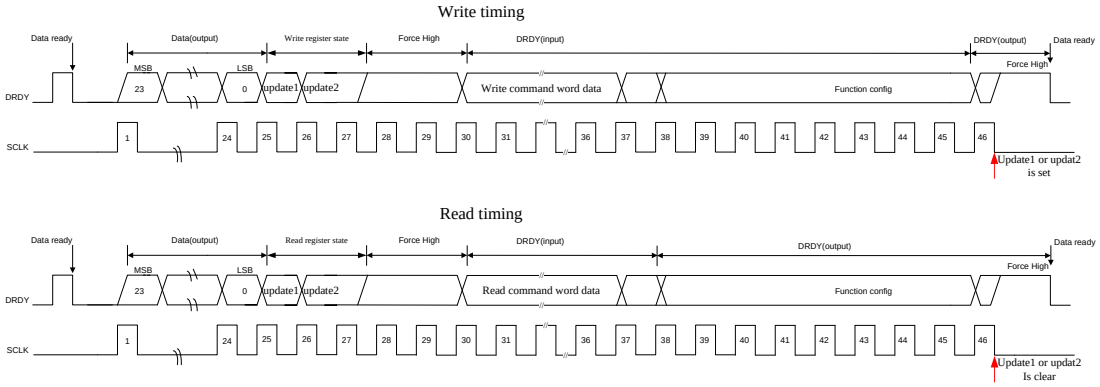


SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t4	$\overline{DRDY}$ / $DOUT$ The interval time between $\overline{DRDY}$ / $DOUT$ setting low and the first SCLK.		0			ns
t5	width of SCLK pulse.		455			ns
t6	SCLK edge to SDO new output data		455			ns
t7	SDO data hold time		227.5		455	ns
t8	Data update, not allowed to read the previous data			26.13		μs
t9	Conversion time (1/data rate)	10Hz		100		ms
		40Hz		25		ms
		640Hz		1.5625		ms
		1280Hz		0.78125		ms

（7）Functional configuration

HLW3070 can be configured with different functions through SCLK and $\overline{DRDY}$ / $DOUT$. The

sequence diagram of function configuration is shown as follows:



Description of the function configuration process, after $\overline{DRDY}/DOUT$ going from high to low:

- SCLK 1 through 24 read ADC data. If you do not need to configure or read registers, you can omit the following steps.
- From SCLK 25 to SCLK 26, reads register write operation status.
- The 27th SCLK, pull up the $\overline{DRDY}/DOUT$ output.
- From SCLK 28 to SCLK 29, switch $\overline{DRDY}/DOUT$ to input.
- For SCLK 30 to 36, register write or read command word data (high first).
- The 37th SCLK switches the direction of $\overline{DRDY}/DOUT$ (if a register is written, $\overline{DRDY}/DOUT$ is the input; If you are reading a register, $\overline{DRDY}/DOUT$ is the output).
- The 38th through 45th SCLK, input register configuration data or output register configuration data (high first input/output).
- The 46th SCLK switches $\overline{DRDY}/DOUT$ to output and raises $\overline{DRDY}/DOUT$. Update1 / update2 is set or cleared.

（8）SPI command word

HLW3070 has two command words with a length of 7bits. The command words are described as follows:

COMMAND NAME	Command byte	DESCRIPTION
Write configuration register	0x65	Write :Config REG
read configuration register	0x56	Read:Config REG

HLW3070 has a set of registers:Config REG.

- Config Register

REG	R/W	DESCRIPTION	Reset Value
DESCRIPTION	Reserved	Configuration register	0x0C

Configure Bits	B7	B6	B5	B4
DESCRIPTION	Reserved	REF output switch	Rate selection for ADC output	
Configure Bits	B3	B2	B1	B0
DESCRIPTION	PGA Selection		Channel selection	

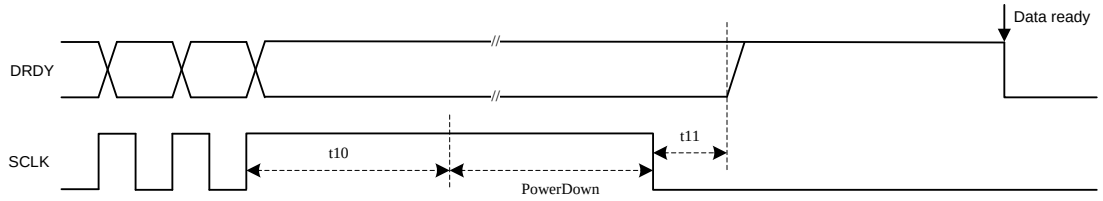
The table of Config Register

Bits	DESCRIPTION	
[7]	-	Reserved。Default:0，Write 0 instead of 1
[6]	REFO_OFF	REF output switch：REF output is turned on by default 1= Close REF output。 0= Open REF output。
[5:4]	SPEED_SEL	ADC output rate selection: the default value is 10Hz SPEED_SEL[1:0] / DESCRIPTION 00 / 10Hz 01 / 40Hz 10 / 640Hz 11 / 1280Hz
[3:2]	PGA_SEL	PGA selection: The default PGA is 128. In temperature measurement mode, PGA_SEL is 00 PGA_SEL[1:0] / DESCRIPTION 00 / 1 01 / 2 10 / 64 11 / 128
[1:0]	CH_SEL[1:0]	Channel selection: The default channel is channel A CH_SEL[1:0] / DESCRIPTIO

			N	
			00	Channel A
			01	Reserved
			10	temperature
			11	Short

（9）Power down Model

When SCLK changes from low level to high level and stays at high level over 100μs, HLW3070 enters Powerdown mode, at which time all circuits of the chip will be turned off, and the power consumption approaches 0. When SCLK returns to low power level, the chip will return to normal working state.

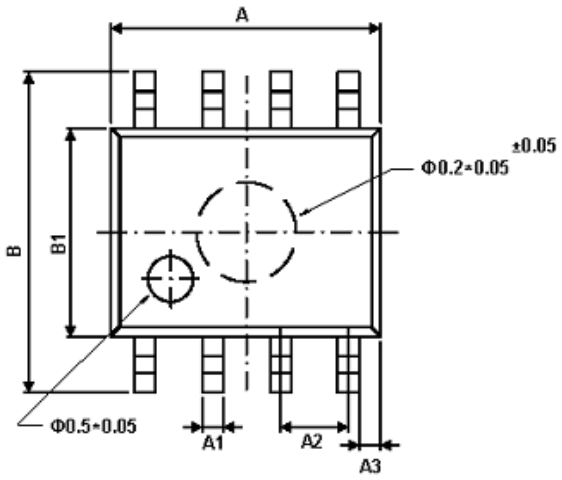


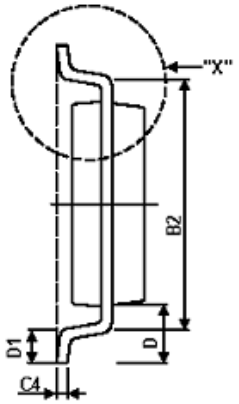
Schematic of HLW3070 PowerDown mode

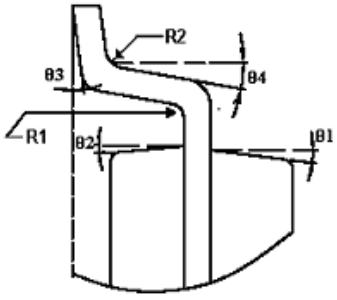
symbol	DESCRIPTION	MIN	TYP	MAX
t10	SCLK high level holding time	100μs		
t11	Low level retention time after SCLK drops	10μs		

4 HLW3070 PACKAGE

尺寸 / 标注	最小 （mm）	最大 （mm）	尺寸 / 标注	最小 （mm）	最大 （mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	







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